

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### General Description

The MAX4751/MAX4752/MAX4753 are low on-resistance, low-voltage, quad, single-pole/single-throw (SPST) analog switches that operate from a single +1.6V to +3.6V supply. These devices have fast switching speeds ( $t_{ON} = 30\text{ns}$ ,  $t_{OFF} = 25\text{ns}$ ), handle rail-to-rail analog signals, and consume less than  $1\mu\text{W}$  of quiescent power. The MAX4753 has break-before-make switching.

When powered from a +3V supply, the MAX4751/MAX4752/MAX4753 feature low  $0.9\Omega$  (max) on-resistance ( $R_{ON}$ ), with  $0.12\Omega$  (max)  $R_{ON}$  matching and  $0.1\Omega$  (max)  $R_{ON}$  flatness. The digital input is 1.8V CMOS compatible when using a single +3V supply.

The MAX4751 has four normally open (NO) switches, the MAX4752 has four normally closed (NC) switches, and the MAX4753 has two NO and two NC switches. The MAX4751/MAX4752/MAX4753 are available in  $3\text{mm} \times 3\text{mm}$ , 16-pin QFN and 14-pin TSSOP packages.

### Applications

Power Routing  
 Battery-Powered Systems  
 Audio and Video Signal Routing  
 Low-Voltage Data-Acquisition Systems  
 Communications Circuits  
 PCMCIA Cards  
 Cellular Phones  
 Modems  
 Hard Drives

### Features

- ◆ **Low  $R_{ON}$**   
 $0.9\Omega$  max (+3V Supply)  
 $2.5\Omega$  max (+1.8V Supply)
- ◆ **On-Resistance Flatness:  $0.1\Omega$  max (+3V)**
- ◆  **$R_{ON}$  Matching**  
 $0.12\Omega$  max (+3V Supply)  
 $0.25\Omega$  max (+1.8V Supply)
- ◆ **+1.6V to +3.6V Single-Supply Operation**
- ◆ **Available in 16-Pin QFN and  $3\text{mm} \times 3\text{mm}$  Packages**
- ◆ **1.8V CMOS Logic Compatible (+3V Supply)**
- ◆ **High Current-Handling Capacity (100mA Continuous)**
- ◆ **Fast Switching:  $t_{ON} = 30\text{ns}$ ,  $t_{OFF} = 25\text{ns}$**

### Ordering Information

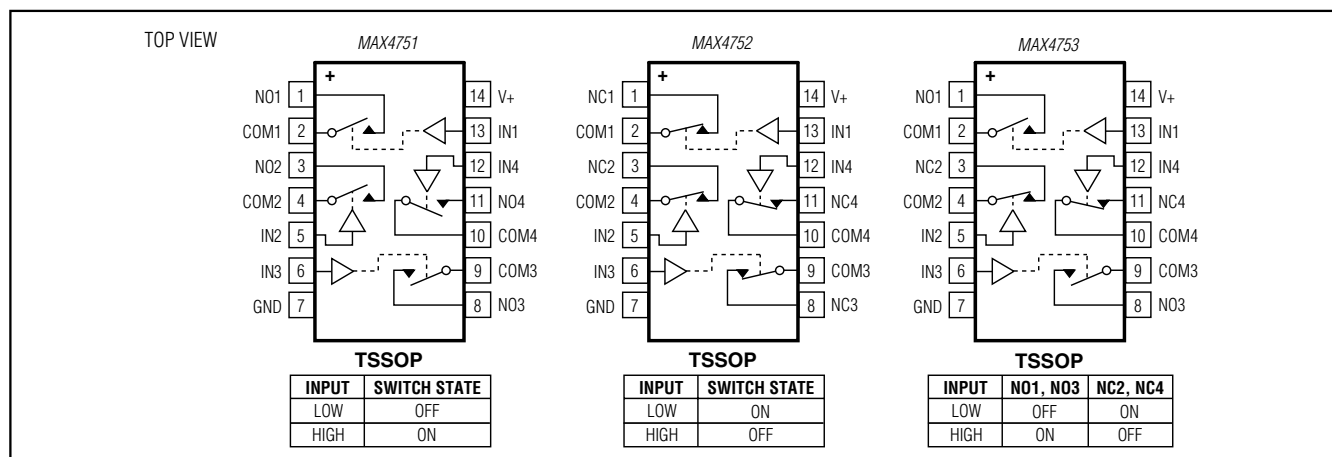
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4751EUD+T	-40°C to +85°C	14 TSSOP	—
MAX4751EGE+T	-40°C to +85°C	16 QFN-EP* ( $3\text{mm} \times 3\text{mm}$ )	AAC
MAX4752EUD+T	-40°C to +85°C	14 TSSOP	—
MAX4752EGE+T	-40°C to +85°C	16 QFN-EP* ( $3\text{mm} \times 3\text{mm}$ )	AAD
MAX4753EUD+T	-40°C to +85°C	14 TSSOP	—
MAX4753EGE+T	-40°C to +85°C	16 QFN-EP* ( $3\text{mm} \times 3\text{mm}$ )	AAE

\*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

### Pin Configurations/Functional Diagrams/Truth Tables



Pin Configurations/Functional Diagrams/Truth Tables continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V+, IN_	-0.3V to +4V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (COM_, NO_, NC_)	±100mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms 10% duty cycle)	±200mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
TSSOP (derate 9.1W/°C above +70°C)	727mW
QFN (derate 16.9W/°C above +70°C)	1349mW

Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

**Note 1:** Signals on COM\_, NO\_, or NC\_ exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V<sub>IH</sub> = +1.4V, V<sub>IL</sub> = +0.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +3.0V, T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub>			0		V+	V
On-Resistance (Note 4)	R <sub>ON</sub>	V+ = 2.7V, I <sub>COM_</sub> = 100mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 1.5V	+25°C	0.6	0.9		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR <sub>ON</sub>	V+ = 2.7V, I <sub>COM_</sub> = 100mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 1.5V	+25°C	0.03	0.12		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			0.15	
On-Resistance Flatness (Note 6)	R <sub>FLAT(ON)</sub>	V+ = 2.7V, I <sub>COM_</sub> = 100mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 1V, 1.5V, 2V	+25°C	0.04	0.1		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			0.12	
NO_ or NC_ Off-Leakage Current (Note 7)	I <sub>NO_(OFF)</sub> , I <sub>NC_(OFF)</sub>	V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.6V, V <sub>NO_</sub> or V <sub>NC_</sub> = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-5		+5	
COM_ Off-Leakage Current (Note 7)	I <sub>COM_(OFF)</sub>	V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.6V, V <sub>NO_</sub> or V <sub>NC_</sub> = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-5		+5	
COM_ On-Leakage Current (Note 7)	I <sub>COM_(ON)</sub>	V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.6V, V <sub>NO_</sub> or V <sub>NC_</sub> = 0.3V, 3.6V, or unconnected	+25°C	-2.5	0.002	+2.5	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-5		+5	

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V<sub>IH</sub> = +1.4V, V<sub>IL</sub> = +0.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +3.0V, T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>SWITCH DYNAMIC CHARACTERISTICS</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF, Figure 1	+25°C	6	30	ns	
			T <sub>MIN</sub> to T <sub>MAX</sub>		30		
Turn-Off Time	t <sub>OFF</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF, Figure 1	+25°C	10	25	ns	
			T <sub>MIN</sub> to T <sub>MAX</sub>		25		
Break-Before-Make (Note 8) (MAX4753 Only)	t <sub>BBM</sub>	V <sub>NO</sub> and V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF, Figure 1	+25°C	7	ns		
			T <sub>MIN</sub> to T <sub>MAX</sub>	2			
Charge Injection	Q	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1.0nF, Figure 2	+25°C	21	pC		
NO <sub>-</sub> or NC <sub>-</sub> Off-Capacitance	C <sub>OFF</sub>	f = 1MHz, Figure 3	+25°C	31	pF		
COM <sub>-</sub> Off-Capacitance	C <sub>COM(OFF)</sub>	f = 1MHz, Figure 3	+25°C	30	pF		
COM <sub>-</sub> On-Capacitance	C <sub>COM(ON)</sub>	f = 1MHz, Figure 3	+25°C	75	pF		
Off-Isolation (Note 9)	V <sub>ISO</sub>	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 4	f = 10MHz	+25°C	-51	dB	
			f = 1MHz	+25°C	-65		
Crosstalk		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 4	f = 10MHz	+25°C	-70	dB	
			f = 1MHz	+25°C	-80		
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V <sub>COM</sub> = 2V <sub>P-P</sub> , R <sub>L</sub> = 32Ω	+25°C	0.031	%		
<b>DIGITAL I/O</b>							
Input Logic High	V <sub>IH</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>	1.4		V	
Input Logic Low	V <sub>IL</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>		0.5	V	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 or V+	T <sub>MIN</sub> to T <sub>MAX</sub>	-1	0.0005	+1	μA
<b>POWER SUPPLY</b>							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	V+ = 3.6V, V <sub>IN</sub> = 0 or V+				1	μA

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### ELECTRICAL CHARACTERISTICS—Single +1.8V Supply

(V+ = +1.8V, V<sub>IH</sub> = +1V, V<sub>IL</sub> = +0.4V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub>			0		V+	V
On-Resistance (Note 4)	R <sub>ON</sub>	V+ = 1.8V, I <sub>COM_</sub> = 10mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 0.9V	+25°C		1.4	2.5	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			3	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR <sub>ON</sub>	V+ = 1.8V, I <sub>COM_</sub> = 10mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 0.9V	+25°C		0.05	0.25	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			0.25	
<b>SWITCH DYNAMIC CHARACTERISTICS</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = 1.0V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF, Figure 1	+25°C		25	35	ns
			T <sub>MIN</sub> to T <sub>MAX</sub>			35	
Turn-Off Time	t <sub>OFF</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = 1.0V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF, Figure 1	+25°C		20	25	ns
			T <sub>MIN</sub> to T <sub>MAX</sub>			30	
Charge Injection	Q	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1.0nF, Figure 2	+25°C		8		pC
<b>DIGITAL I/O</b>							
Input Logic High	V <sub>IH_</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>	1.0			V
Input Logic Low	V <sub>IL_</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>			0.4	V
Input Leakage Current	I <sub>IN_</sub>	V <sub>IN_</sub> = 0 or V+	T <sub>MIN</sub> to T <sub>MAX</sub>	-1	0.0005	+1	μA
<b>POWER SUPPLY</b>							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	V <sub>IN_</sub> = 0 or V+				1	μA

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 3:** Parts are tested at +85°C and guaranteed by design and correlation over the full temperature range.

**Note 4:** R<sub>ON</sub> and ΔR<sub>ON</sub> matching specifications for QFN-packaged parts are guaranteed by design.

**Note 5:** ΔR<sub>ON</sub> = R<sub>ON(MAX)</sub> - R<sub>ON(MIN)</sub>

**Note 6:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

**Note 7:** Leakage parameters are 100% tested at the maximum-rated hot operating temperature and guaranteed by correlation at T<sub>A</sub> = +25°C.

**Note 8:** Guaranteed by design, not production tested.

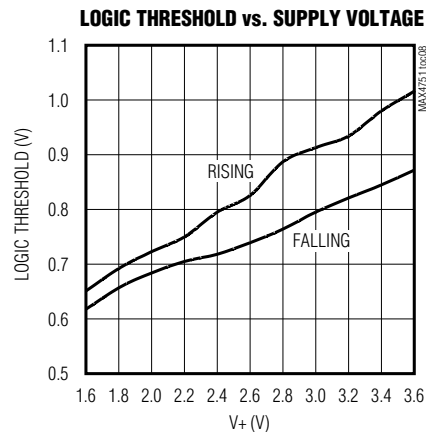
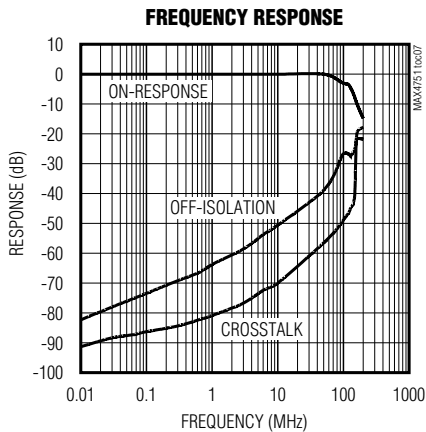
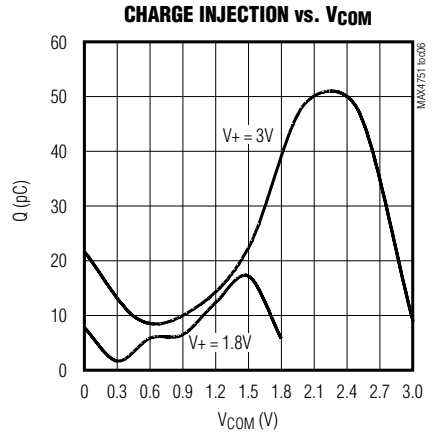
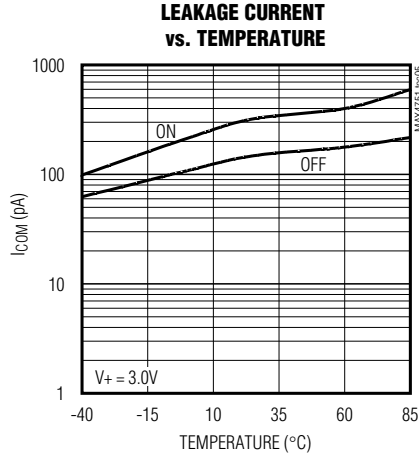
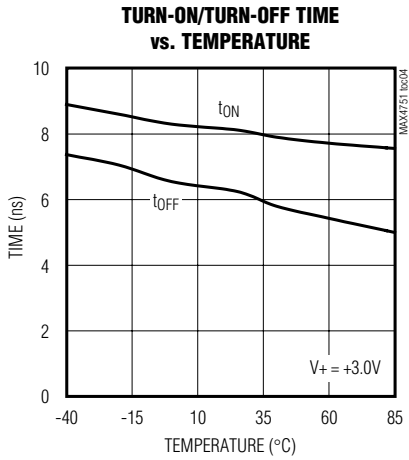
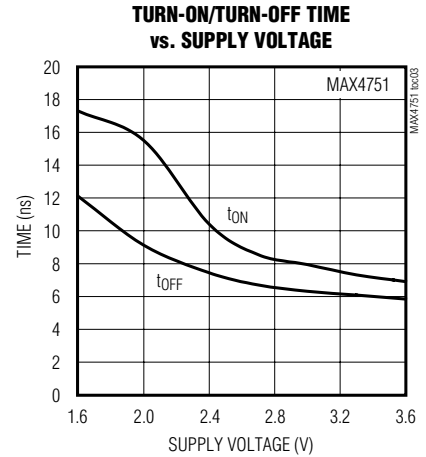
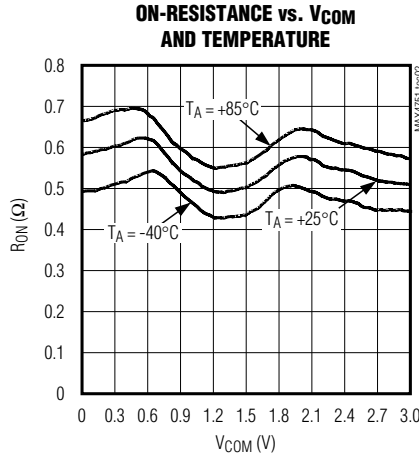
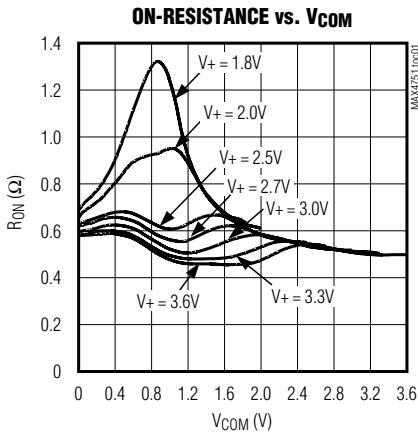
**Note 9:** Off-Isolation = 20log<sub>10</sub>[V<sub>COM</sub> / (V<sub>NC</sub> or V<sub>NO</sub>)], V<sub>COM</sub> = output, V<sub>NC</sub> or V<sub>NO</sub> = input to off switch.

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Typical Operating Characteristics

(V+ = +3V and TA = +25°C, unless otherwise noted.)

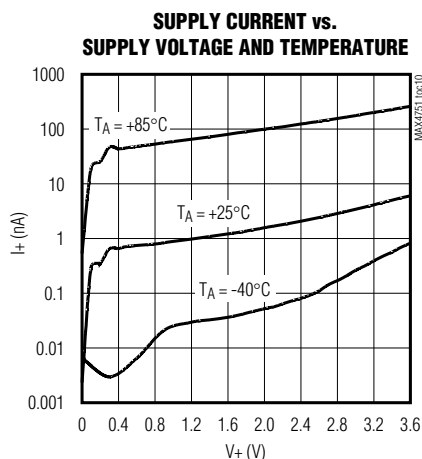
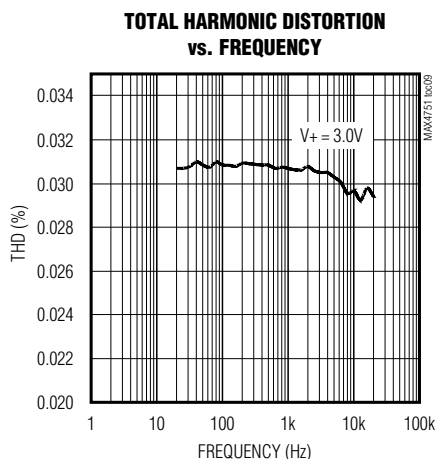


# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Typical Operating Characteristics (continued)

(V+ = +3V and T<sub>A</sub> = +25°C, unless otherwise noted.)



### Pin Description

PIN						NAME	FUNCTION
MAX4751		MAX4752		MAX4753			
TSSOP	QFN-EP	TSSOP	QFN-EP	TSSOP	QFN-EP		
1, 3, 8, 11	15, 1, 7, 11	—	—	—	—	NO1, NO2, NO3, NO4	Switch Normally Open Terminals
—	—	1, 3, 8, 11	15, 1, 7, 11	—	—	NC1, NC2, NC3, NC4	Switch Normally Closed Terminals
—	—	—	—	3, 11	1, 11	NC2, NC4	Switch Normally Closed Terminals
—	—	—	—	1, 8	15, 7	NO1, NO3	Switch Normally Open Terminals
2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	COM1, COM2, COM3, COM4	Switch Common Terminals
7	6	7	6	7	6	GND	Ground
13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	IN1, IN2, IN3, IN4	Logic Control Inputs
14	14	14	14	14	14	V+	Positive Supply Voltage
—	3, 10	—	3, 10	—	3, 10	N.C.	No Connection. Not internally connected.
—	—	—	—	—	—	EP	Exposed Pad (QFN Only). Connect EP to GND.

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Test Circuits/Timing Diagrams

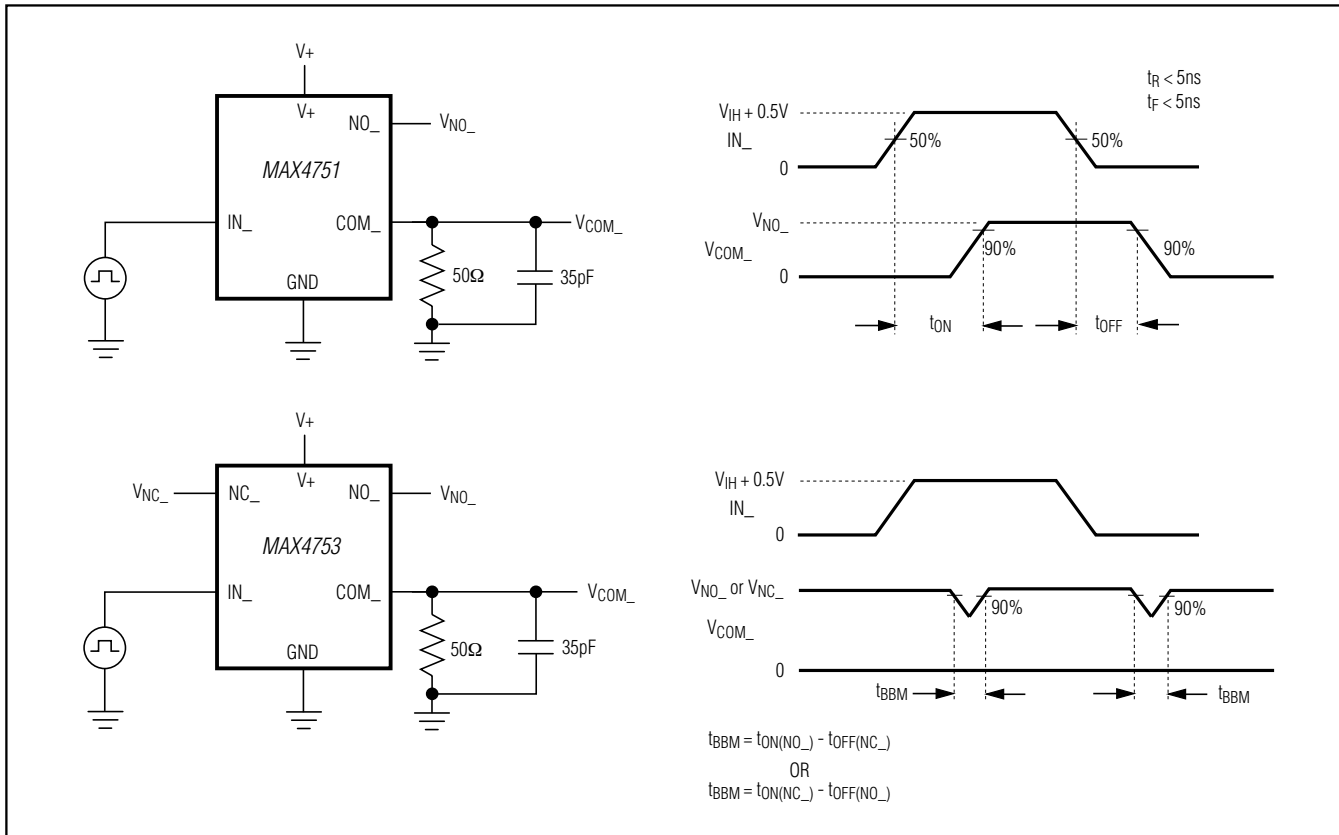


Figure1. Switching Times

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Test Circuits/Timing Diagrams (continued)

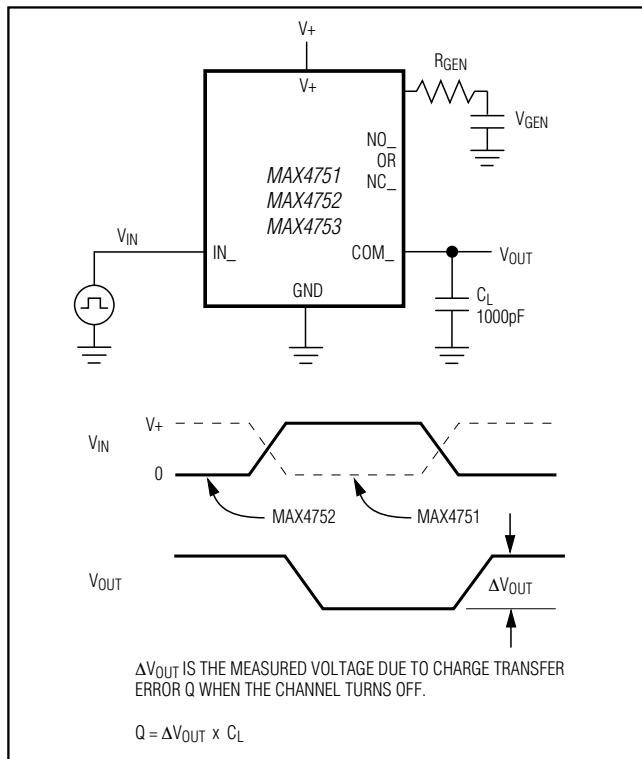


Figure 2. Charge Injection

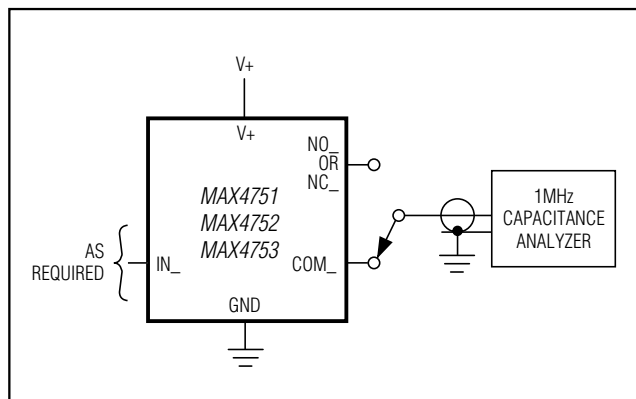


Figure 3. NO\_, NC\_, and COM\_ Capacitance

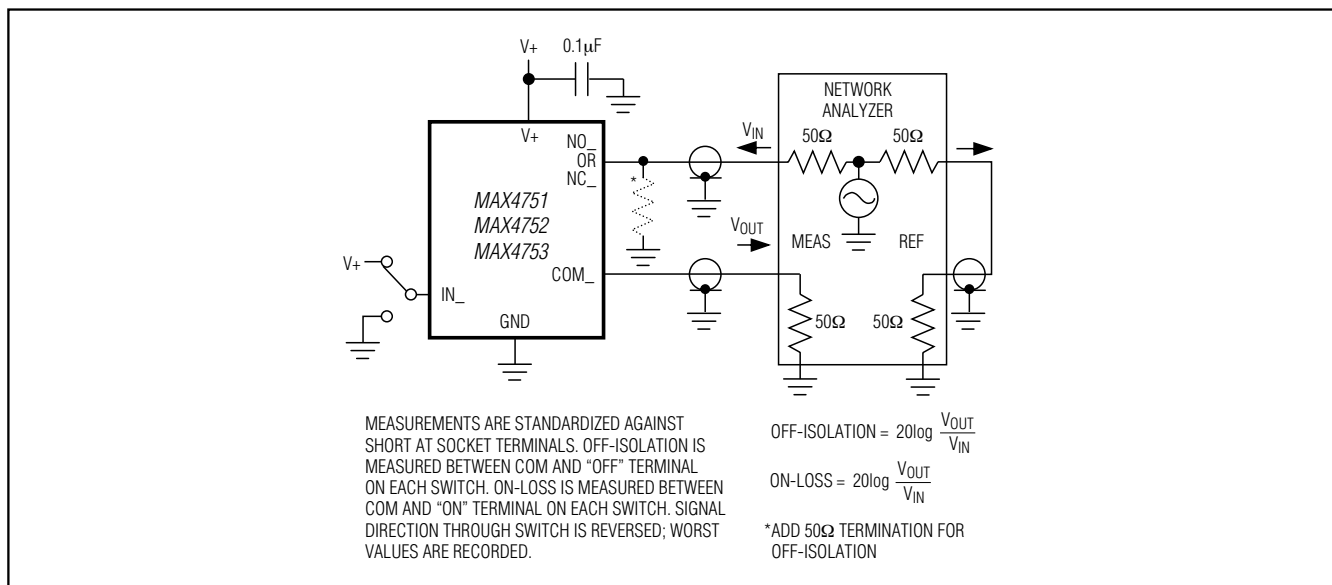


Figure 4. Off-Isolation, On-Loss, and Crosstalk



# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Detailed Description

The MAX4751/MAX4752/MAX4753 are low 0.9Ω max (at  $V_+ = 3V$ ) on-resistance, low-voltage quad analog switches that operate from a +1.6V to +3.6V single supply. CMOS construction allows switching analog signals that are within the supply voltage range (GND to  $V_+$ ).

When powered from a +3V supply, the 0.9Ω (max)  $R_{ON}$  allows high continuous currents to be switched in a variety of applications.

### Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence  $V_+$  on first, followed by  $NO_+$ ,  $NC_+$ , or  $COM_+$ . If power-supply sequencing is not possible, add two small-signal diodes ( $D1$ ,  $D2$ ) in series with the supply pins for overvoltage protection (Figure 5). Adding these diodes reduces the analog signal by one diode drop below  $V_+$  and one diode drop above GND, but does not affect the low switch resistance and low leakage characteristics of the device. Device operation is unchanged, and the difference between  $V_+$  and GND should not exceed 4V.

Power-supply bypassing is needed to improve noise margin and to prevent switching noise propagation from the  $V_+$  supply to other components. A 0.1μF capacitor, connected from  $V_+$  to GND, is adequate for most applications.

### Logic Inputs

The MAX4751/MAX4752/MAX4753 logic inputs can be driven up to +3.6V regardless of the supply voltage. For example, with a +1.8V supply,  $IN_+$  may be driven low to GND and high to +3.6V. Driving  $IN_+$  rail-to-rail minimizes power consumption.

### Analog Signal Levels

Analog signals that range over the entire supply voltage ( $V_+$  to GND) can be passed with very little change in on-

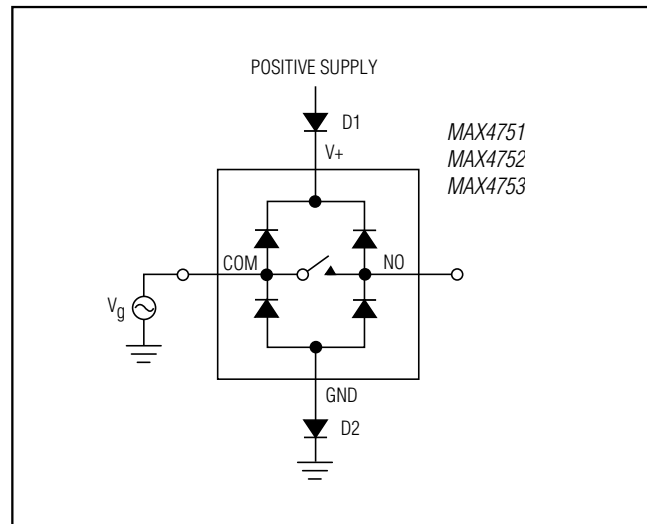


Figure 5. Overvoltage Protection Using Two External Blocking Diodes

resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the  $NO_+$ ,  $NC_+$ , and  $COM_+$  pins can be used as either inputs or outputs.

### Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

### Chip Information

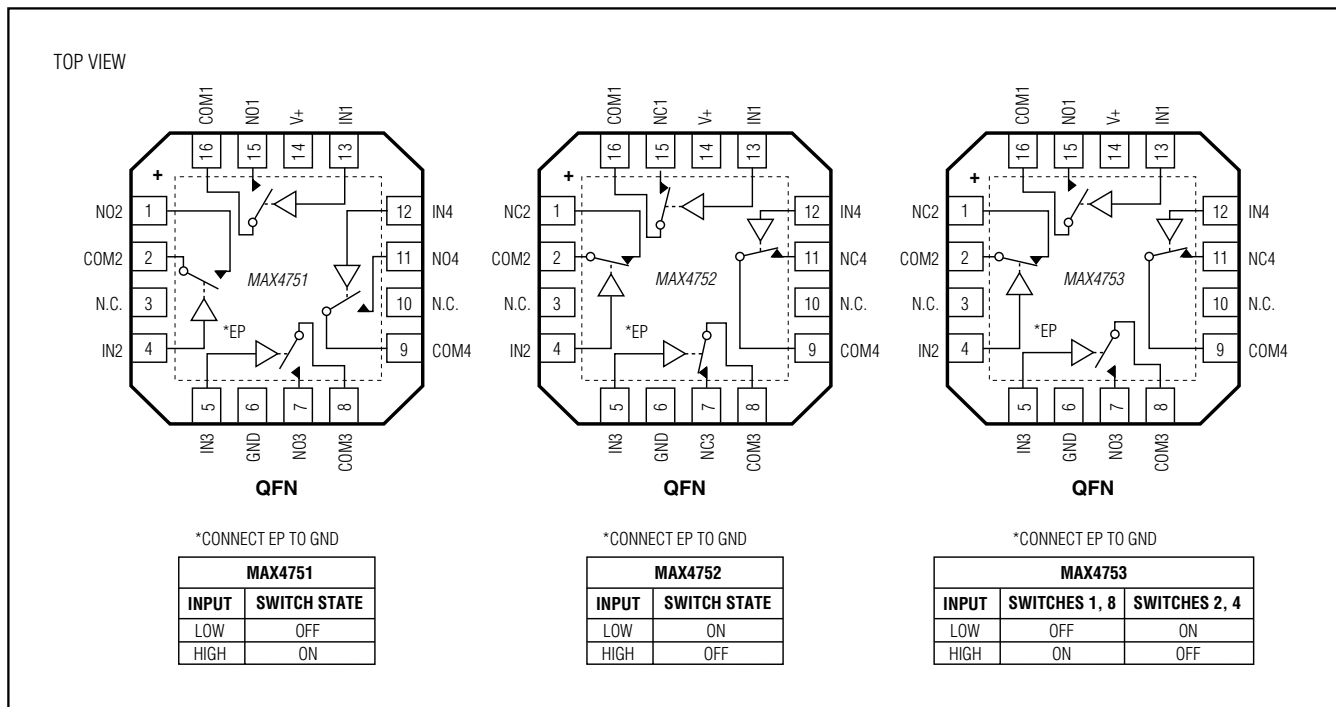
TRANSISTOR COUNT: 228

PROCESS: CMOS

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Pin Configurations/Functional Diagrams/Truth Tables (continued)



### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	<a href="#">21-0066</a>	<a href="#">90-0113</a>
16 QFN	G1633+2	<a href="#">21-0102</a>	<a href="#">90-0215</a>

# MAX4751/MAX4752/MAX4753

## 0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/13	Corrected packaging information	1, 2, 6, 10–13



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