19-5022; Rev 0; 10/09

EVALUATION KIT AVAILABLE

High-Bandwidth, VGA 2:1 Switch with ±15kV ESD Protection

MAX4885AE

General Description

The MAX4885AE integrates high-bandwidth analog switches, level-translating buffers, and level-translating FET switches to implement a complete 2:1 multiplexer for VGA signals. The device provides three very high-frequency 900MHz (typ) SPDT switches for RGB signals, two low-frequency clamping switches for the DDC signals, a pair of level-translating buffers for the H_ and V_ signals, and integrated extended ESD protection.

Horizontal and vertical synchronization (H_/V_) inputs feature level-shifting buffers to support low-voltage controllers and standard 5V-TTL-compatible monitors, meeting the VESA requirement. Display Data Channel (DDC), consisting of SDA_ and SCL_, are FET switches that protect the low-voltage VGA source from potential damage from high-voltage presence on the monitor while reducing capacitive load.

All seven output terminals of the MAX4885AE feature high-ESD protection to ±15kV Human Body Model (HBM) (see the *Pin Description*). All other pins are protected to ±2kV Human Body Model (HBM).

The MAX4885AE is specified over the extended -40°C to +85°C temperature range, and is available in a space-saving, 28-pin, 4mm x 4mm TQFN package.

Applications

Notebook Computer—MXM/Switchable Graphics

KVM for Servers

Features

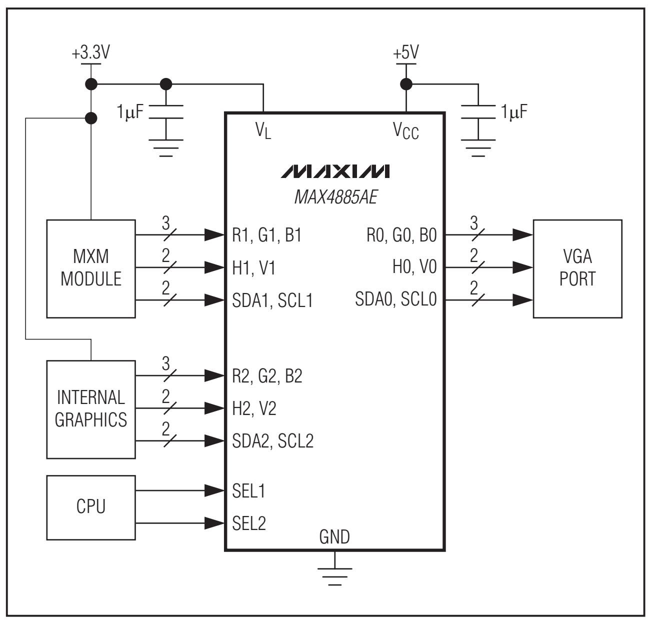
- ♦ Low 5Ω (typ) On-Resistance (R_, G_, B_ Signals)
- ♦ Low 5.5pF (typ) On-Capacitance (R_, G_, B_ Signals)
- ♦ Independent, Selectable Logic Inputs for Switching
- ♦ Similar Pin Configuration to MAX4885
- ♦ Ultra-Small, 28-Pin (4mm x 4mm) TQFN Package
- ♦ ±15kV ESD HBM

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4885AEETI+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)
V_{CC} .... -0.3V to +6V
V_L .... -0.3V to (V_{CC} + 0.3V)
R_, G_, B_, H0, V0, SDA0, SCL0 .... -0.3V to (V_{CC} + 0.3V)
H1, H2, V1, V2, SDA1, SDA2, SCL1,
SCL2, SEL1, SEL2 .... -0.3V to (V_L + 0.3V)
Continuous Current through R_, G_, B_ Switches .... ±50mA
Continuous Current through SDA_, SCL_ Switches .... ±50mA
Continuous Current into SEL1, SEL2, H1, H2, V1, V2 .... ±20mA
Peak Current through all Switches
(pulsed at 1ms, 10% duty cycle) .... ±100mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 28.6mW/°C above +70°C) 2285.7mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
28-Pin TQFN .... 35°C/W
Junction-to-Ambient Thermal Resistance (θ_{JC}) (Note 1)
28-Pin TQFN .... 3°C/W
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **http://www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_L = +2.2V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		+4.5		+5.5	V
Logic Supply Voltage	V_L	$V_L \le V_{CC}$	+2.2		V_{CC}	V
V_{CC} Supply Current	I_{CC}	V_{CC} = +5.5V, V_L = +3.6V, SEL_ = H1 = H2 = V1 = V2 = GND		2	5	µA
V_L Supply Current	I_L	V_{CC} = +5.5V, V_L = +3.6V, SEL_ = H1 = H2 = V1 = V2 = GND			1	µA
ANALOG SWITCHES						
On-Resistance (R_, G_, B_)	$R_{\text{-HF-ON}}$	V_{IN} = +0.7V, I_{IN} = ±10mA		5	8	Ω
On-Resistance Match (R_, G_, B_)	ΔR_{ON}	$0 \le V_{IN} \le +0.7V$, I_{IN} = -10mA			1	Ω
On-Resistance Flatness (R_, G_, B_)	$R_{FLAT(ON)}$	$0 \le V_{IN} \le +0.7V$, I_{IN} = -10mA		0.5	1	Ω
Off Leakage Current (R_, G_, B_)	I_{OFF}	$V_{R\_}$, $V_{G\_}$, $V_{B\_}$ = 0V or V_{CC}	-1		+1	µA
On-Resistance (SDA_, SCL_)	$R_{\text{-DDC}ON}$	V_{IN} = +0.7V, I_{IN} = ±10mA		15		Ω
Off-Leakage Current (SDA_, SCL_)	I_{OFF}	$V_{SDA\_}$, $V_{SCL\_}$ = 0V or V_L, V_{CC} = V_L = +5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_L = +2.2V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

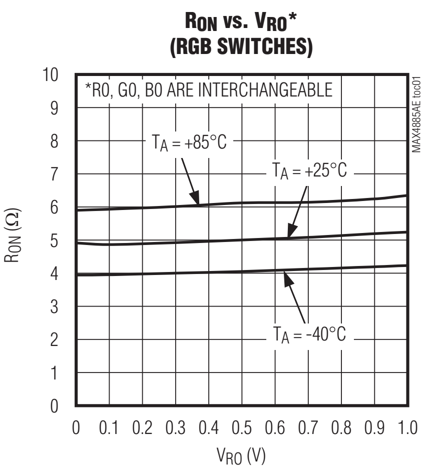
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SEL_, H1, H2, V1, V2)						
Input Threshold Low	V_{IL}		0.25 x V_L			V
Input Threshold High	V_{IH}				0.55 x V_L	V
Input Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_L		-1		+1	µA
SEL_ Enable/Disable Time	t_{ON}, t_{OFF}	R_L= 2.2kΩ, C_L = 10pF, Figure 1		300		ns
DIGITAL OUTPUTS (H0, V0)						
Output-Voltage Low	V_{OL}	I_{OUT} = 8mA, V_{CC} = +4.5V			0.8	V
Output-Voltage High	V_{OH}	I_{OUT} = -8mA, V_{CC} = +4.5V	2.4			V
Rise/Fall Time	t_R, t_F	R_L= 2.2kΩ, C_L = 10pF, Figure 2			8	ns
RGB AC PERFORMANCE						
Bandwidth	f_{MAX}	R_S = R_L = 50Ω		900		MHz
On-Loss	I_{LOSS}	f = 10MHz, R_S = R_L = 50Ω, 0 ≤ V ≤ +0.7V, Figure 3		0.4		dB
Crosstalk R_, G_, B_	V_{CT}	f = 50MHz, R_S = R_L = 50Ω, Figure 3		-40		dB
Off-Capacitance	C_{OFF}	f = 1MHz, R0 to R1/R2, G0 to G1/G2, B0 to B1/B2 (Note 2)		2.5		pF
On-Capacitance	C_{ON}	f = 1MHz, R0 to R1/R2, G0 to G1/G2, B0 to B1/B2 (Note 2)		5.5	8	pF
ESD PROTECTION						
R0, G0, B0, SDA0, SCL0, H0, V0	V_{ESD}	HBM (Notes 2, 3)		±15		kV
R0, G0, B0, SDA0, SCL0, H0, V0	V_{ESD}	IEC 61000-4-2 Contact (Notes 2, 3)		±8		kV
All Other Terminals	V_{ESD}	HBM (Note 2)		±2		kV

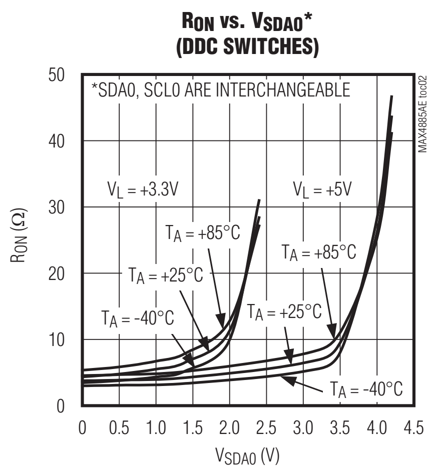
Note 2: Guaranteed by design. Not production tested.
Note 3: Tested terminal to GND, 1µF bypass capacitors on V_{CC} and V_L.

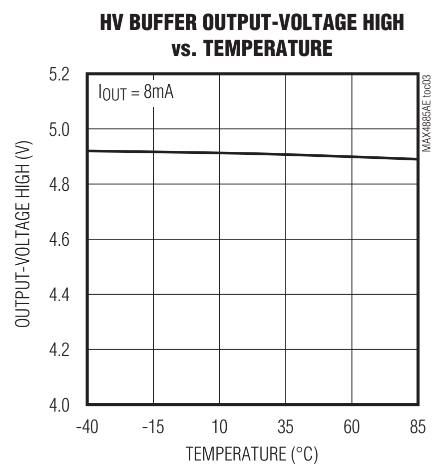
High-Bandwidth, VGA 2:1 Switch with ±15kV ESD Protection

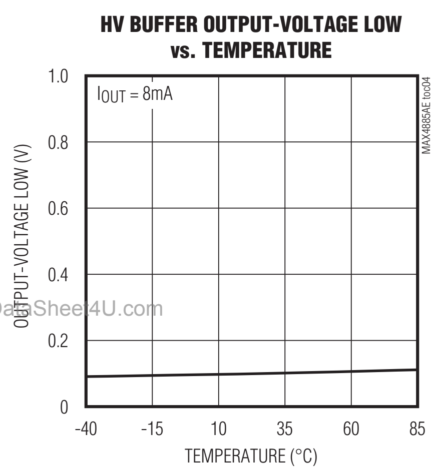
Typical Operating Characteristics

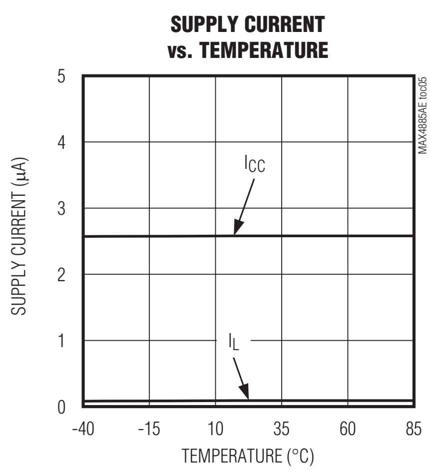
(V_{CC} = +5.0V, V_L = +3.3V, T_A = 25°C, unless otherwise noted.)

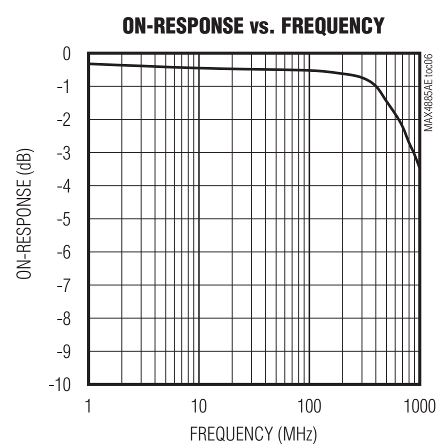


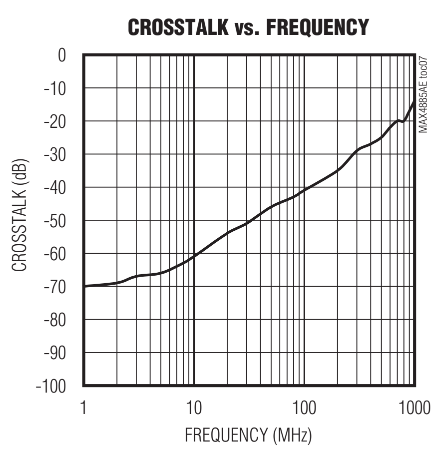












Test Circuits/Timing Diagrams

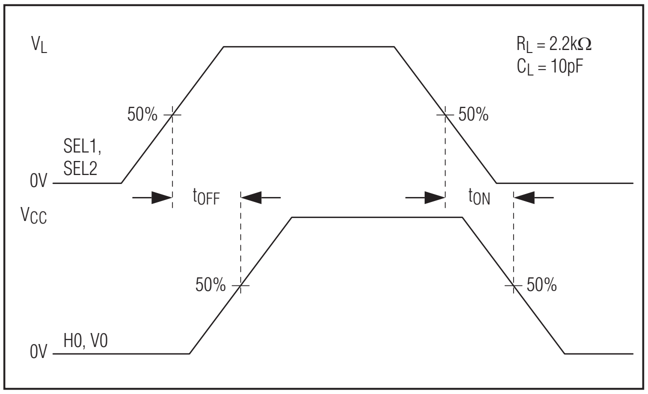


Figure 1. Enable/Disable Time

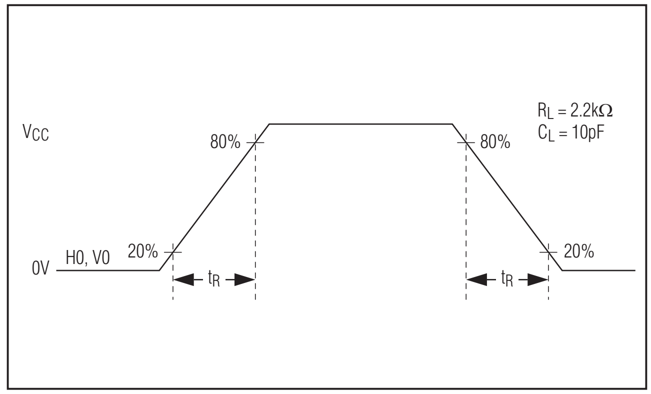


Figure 2. Rise/Fall Time

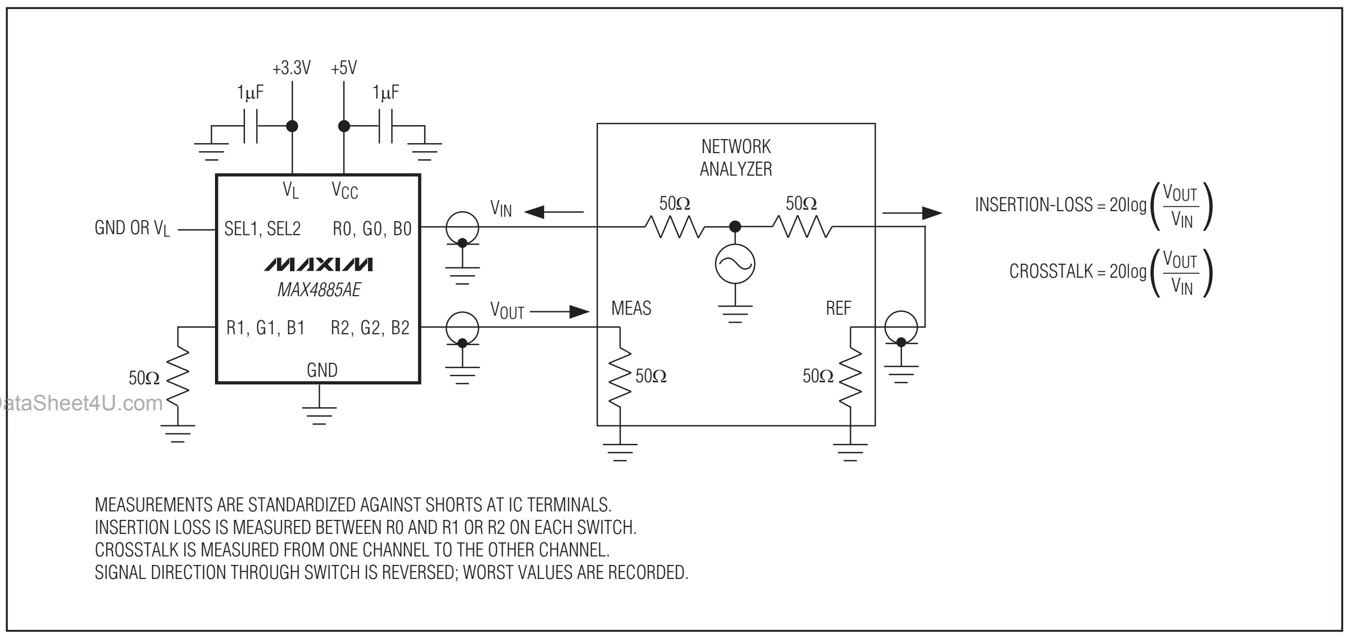
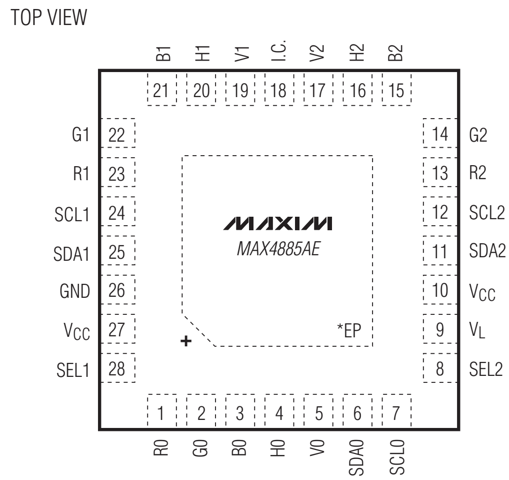


Figure 3. Insertion Loss and Crosstalk

High-Bandwidth, VGA 2:1 Switch with ±15kV ESD Protection

Pin Configuration



TQFN (4mm × 4mm)

*EXPOSED PAD. CONNECT TO GROUND OR LEAVE UNCONNECTED.

Pin Description

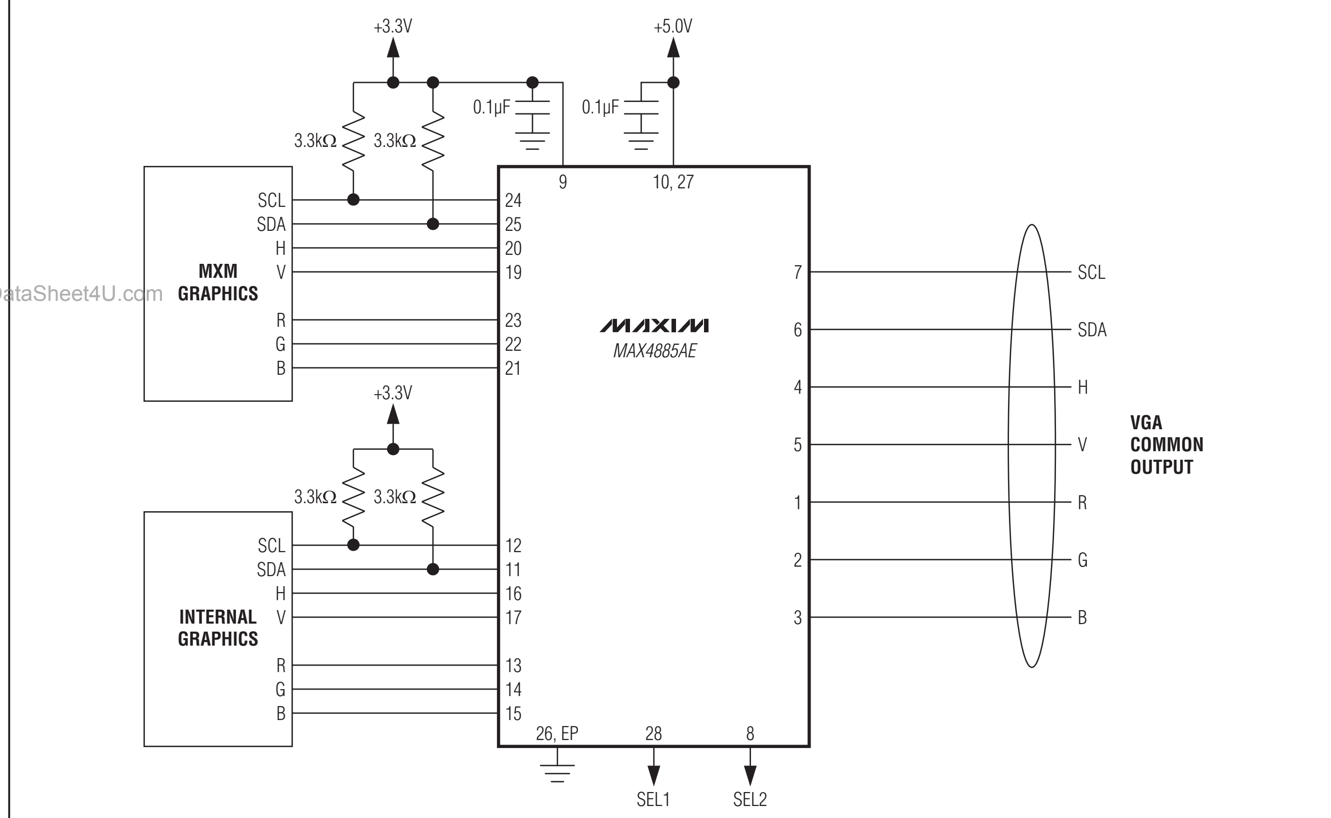
PIN	NAME	FUNCTION
1	R0	RGB Red Output (Note 4)
2	G0	RGB Green Output (Note 4)
3	B0	RGB Blue Output (Note 4)
4	H0	Horizontal Sync Output (Note 4)
5	V0	Vertical Sync Output (Note 4)
6	SDA0	I^2C Data Output (Note 4)
7	SCL0	I^2C Clock Output (Note 4)
8	SEL2	Select Input 2. Switches SDA_ and SCL_ signals.
9	V_L	Supply Voltage. $+2.2V \leq V_L \leq V_{CC}$. Bypass V_L to GND with a 1µF or larger ceramic capacitor.
10	V_{CC}	Supply Voltage. V_{CC} = +5.0V ±10%. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor.
11	SDA2	I^2C Input Data 2 (Note 5)
12	SCL2	I^2C Input Clock 2 (Note 5)
13	R2	RGB Red Input 2 (Note 6)
14	G2	RGB Green Input 2 (Note 6)
15	B2	RGB-Blue Input 2 (Note 6)
16	H2	Horizontal Sync Input 2 (Note 7)
17	V2	Vertical Sync Input 2 (Note 7)
18	I.C.	Internal Connection. Connect to ground or leave unconnected.
19	V1	Vertical Sync Input 1 (Note 7)
20	H1	Horizontal Sync Input 1 (Note 7)
21	B1	RGB Blue Input 1 (Note 6)

Pin Description (continued)

PIN	NAME	FUNCTION
22	G1	RGB Green Input 1 (Note 6)
23	R1	RGB Red Input 1 (Note 6)
24	SCL1	I2C Clock Input 1 (Note 5)
25	SDA1	I2C Data Input 1 (Note 5)
26	GND	Ground
27	V_{CC}	+5V Supply Pin
28	SEL1	Select Input 1. Switches R_, G_, B_, H_, and V_ signals.
—	EP	Exposed Pad. Connect exposed pad to ground or leave unconnected.

Note 4: Terminal with ±15kV HBM protection.
Note 5: SCL1, SCL2, SDA1, and SDA2 are identical and can be used interchangeably.
Note 6: R1, R2, G1, G2, B1, and B2 are identical and can be used interchangeably.
Note 7: H1, H2, V1, and V2 are identical and can be used interchangeably.

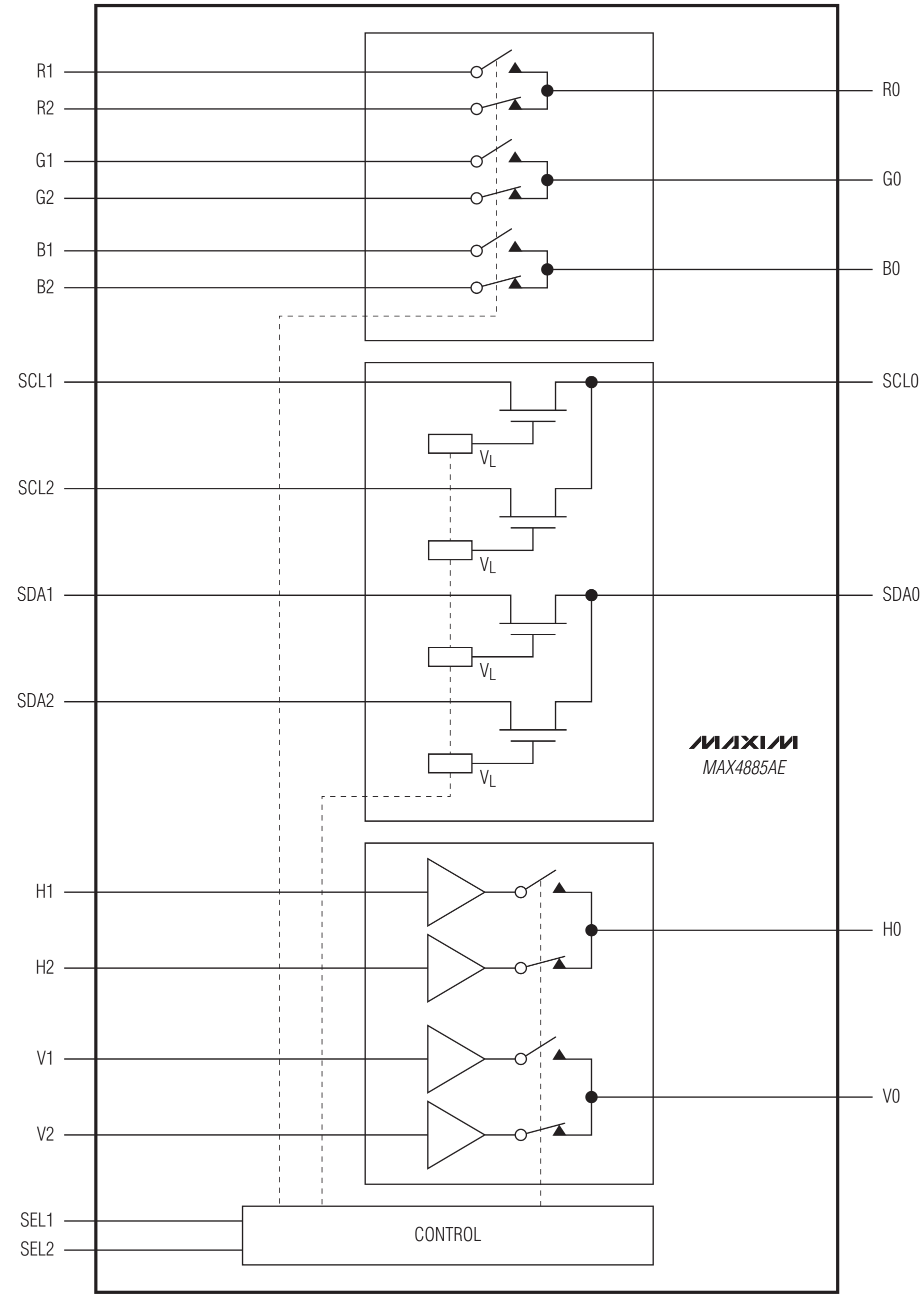
Typical Applications Circuit



NOTE: TWO VIDEO INPUT SOURCES BEING SWITCHED INTO ONE OUTPUT/SINK USING MAX4885AE.

High-Bandwidth, VGA 2:1 Switch with ±15kV ESD Protection

Functional Diagram



Detailed Description

The MAX4885AE integrates high-bandwidth analog switches and level-translating buffers to implement a complete 2:1 multiplexer for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, SDA, and SCL signals. These signals are required in notebook VGA switching applications.

The HSYNC and VSYNC inputs feature level-shifting buffers to support 5V-TTL output logic levels from low-voltage graphics controllers. These buffered switches can be driven from +2.0V up to +5.5V. RGB signals are routed with high-performance analog switches. SDA_ and SCL_ are I^2C signals with pullups to their respective voltages. The MAX4885AE protects the low-voltage side while effectively translating up to the high-voltage level.

Two select inputs are provided to individually select groups of switches.

RGB, HSYNC, and VSYNC signals are controlled by SEL1; and both SDA_ and SCL_ signals are controlled by SEL2.

Table 1. RGB/HV Truth Table

SEL1	FUNCTION	
0	R1 to R0 G1 to G0 B1 to B0	H1 to H0 V1 to V0
1	R2 to R0 G2 to G0 B2 to B0	H2 to H0 V2 to V0

Table 2. DDC Truth Table

SEL2	FUNCTION
0	SDA1 to SDA0 SCL1 to SCL0
1	SDA2 to SDA0 SCL2 to SCL0

RGB Switches

The MAX4885AE provides three SPDT high-bandwidth switches to route standard VGA R_, G_, and B_ signals (see Table 1). The R_, G_, and B_ analog switches are identical and any of the three switches can be used to route red, green, or blue video signals. The R0, G0, and B0 outputs are ESD protected to ±15kV (HBM).

Horizontal/Vertical Sync Level Shifter

H1, H2, V1, and V2 inputs are buffered to provide level-shifting and drive capability for horizontal/vertical sync signals that meet the VESA specification. The H_ and V_ level-shifters are identical, and each level-shifter can be used for either horizontal or vertical signals. The SDA0 and SCL0 outputs are ESD protected to ±15kV (HBM).

Display-Data Channel Multiplexer

The MAX4885AE provides two logic-level translating switches to route DDC signals (see Table 2). V_L is normally set to +3.3V to provide logic-shifting for VESA I^2C-compatible signals. The MAX4885AE protects the low-voltage graphics controller from +5V that could be present in VESA-compatible monitors. In some applications, such as KVM, where logic-level shifting is not required, then V_L can be connected to V_{CC}. The SDA_ and SCL_ switches are identical, and each switch can be used to route either SDA_ or SCL_ signals. The SDA0 and SCL0 outputs are ESD protected to ±15kV (HBM).

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the R0, G0, B0, H0, V0, SDA0, and SCL0 terminals of the MAX4885AE are designed for protection to the following limit: ±15kV using the HBM.

For optimum ESD performance, bypass V_{CC} and V_L pins to ground with 1µF or larger ceramic capacitors as close as possible to these supply pins.

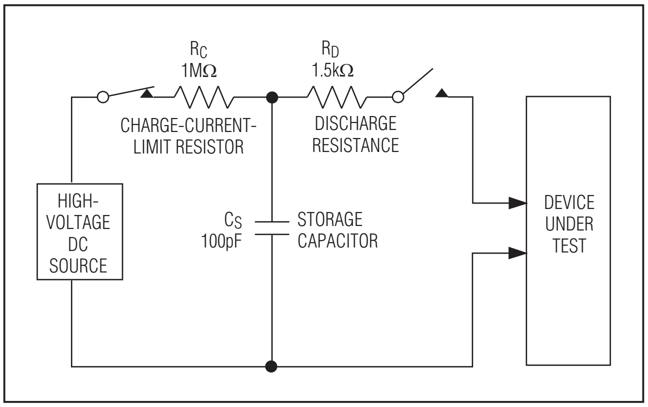


Figure 4. Human Body ESD Test Model

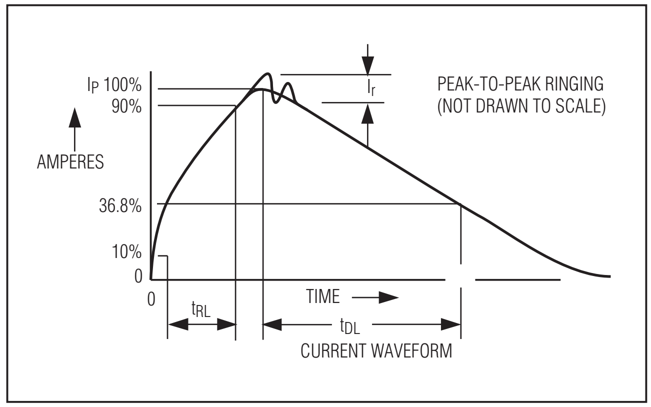


Figure 5. Human Body Model Current Waveform

Human Body Model

Figure 4 shows the HBM, and Figure 5 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report, test setup, methodology, and results.

Applications Information

The MAX4885AE provides the switching and level-shifting necessary to drive a standard VGA port from either an internal graphics controller or an add-in module (MXM or GPU—see *Typical Applications Circuit*). The R_, G_, and B_ signals are switched through the three low-capacitance SPDT switches. Internal buffers drive the HSYNC and VSYNC signals to VGA standard 5V-TTL levels. The DDC multiplexer provides level-shifting. Connect V_L to +3.3V for normal operation, or to V_{CC} to disable level-shifting for DDC signals as for KVM application.

Power-Supply Decoupling

Bypass each V_{CC} pin and V_L pin to ground with a 1µF or larger ceramic capacitor as close as possible to the device.

PCB Layout

High-speed switches such as the MAX4885AE requires proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to ground or leave unconnected.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2844+1	21-0139