19-4167; Rev 0; 6/08

EVALUATION KIT AVAILABLE

0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

MAX5961

General Description

The MAX5961 0 to 16V, quad, hot-swap controller provides complete protection for systems with up to four distinct supply voltages. The device allows the safe insertion and removal of circuit cards into live backplanes. The MAX5961 is an advanced hot-swap controller that monitors voltage and current with an internal 10-bit ADC. The device provides two levels of overcurrent circuit-breaker protection; a fast-trip threshold for a fast turn-off, and a lower slow-trip threshold for a delayed turn-off. The maximum overcurrent circuit-breaker threshold range is set independently for each channel with a trilevel input (ILIM_) or by programming though an I^{2}C interface.

The internal 10-bit ADC is multiplexed to monitor the output voltage and current of each hot-swap channel. The total time to cycle through all the eight measurements is 100µs (typ). Each 10-bit value is stored in an internal circular buffer so that 50 past samples of each signal can be read back through the I^{2}C interface at any time or after a fault condition.

The MAX5961 can be configured as four independent hot-swap controllers, hot-swap controllers operating in pairs, or as a group of four hot-swap controllers.

The device also includes five digital comparators per hot-swap channel to implement overcurrent warning, two levels of overvoltage detection, and two levels of undervoltage detection. The limits for overcurrent, overvoltage, and undervoltage are user-programmable. When any of the measured values violates the programmable limits, an external $\overline{\text{ALERT}}$ signal is asserted. In addition to the $\overline{\text{ALERT}}$ signal, depending on the selected operating mode, the MAX5961 can deassert a power-good signal and/or turn-off the external MOSFET.

The MAX5961 is available in a 48-pin thin QFN package and operates over the -40°C to +85°C extended temperature range.

Applications

PCI Express® Hot Plug

Servers

Disk Drives

Storage Systems

ASICs

PCI Express is a registered trademark of PCI-SIG Corp.

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Features

- **Four Independent Hot-Swap Controllers Protect from 0 to 16V (Provided IN ≥ 2.7V)**
- **10-Bit ADC Monitors Voltage and Current of Each Channel**
- **Circular Buffer Stores 5ms of Current and Voltage Measurements**
- **Four Independent Internal Charge Pumps Generate n-Channel MOSFET Gate Drives**
- **Internal 500mA Gate Pulldown Current for Fast Shutdown**
- **VariableSpeed/BiLevel™ Circuit-Breaker Protection**
- **Alert Output Indicates Undervoltage Warning, Undervoltage Critical, Overvoltage Warning, Overvoltage Critical, and Overcurrent Warning for Each Channel**
- **Independent Power-Good Outputs**
- **Autoretry or Latched Fault Management**
- **400kHz I^{2}C Interface**
- **7mm x 7mm 48-Pin TQFN Package**

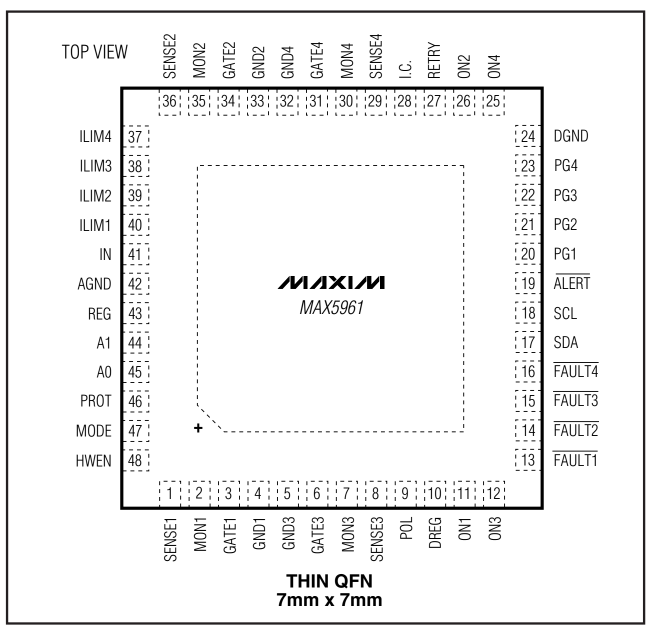
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5961ETM+	-40°C to +85°C	48 Thin QFN–EP*

+Denotes a lead-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

ABSOLUTE MAXIMUM RATINGS

IN, SENSE_, MON_, GATE_ to AGND....................-0.3V to +30V
PG_, ON_, FAULT_, SDA, SCL, ALERT,
REG, DREG, POL, RETRY, HWEN ....-0.3V to +6V
DREG to REG ....-0.3V to +0.3V
ILIM_, MODE, PROT, A0, A1 ....-0.3V to (V_{REG} + 0.3V)
GATE_ to MON_ (same channel) ....-0.3V to +6V
SENSE_ to MON_ (same channel) ....-0.3V to +6V
GND1, GND2, GND3, GND4, DGND to AGND.....-0.3V to +0.3V
SDA, ALERT Current ....-20mA to 50mA
GATE_, MON_, GND_ Current 500mA

Input/Output Current (all other pins)...................................20mA
Continuous Power Dissipation (T_A = +70°C)
For Single-Layer Board
48-Pin Thin QFN (derate 27.8mW/°C above +70°C)...2222.2mW
For Multilayer Board
48-Pin Thin QFN (derate 40mW/°C above +70°C) 3200mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{IN}		2.7		16	V
Hot-Swap Voltage Range	V_S		0		16	V
Undervoltage Lockout	V_{UVLO}	V_{IN} rising			2.7	V
Undervoltage Lockout Hysteresis	$V_{UVLO,HYST}$	V_{IN} falling		100		mV
Supply Current	I_{CC}	f_{SCL} = 400kHz, all 4 channels enabled		4	8	mA
Internal LDO Output Voltage	V_{REG}	2.7V < V_{IN} < 16V	2.49		2.9	V
ADC PERFORMANCE						
Resolution				10		Bits
Maximum Differential Nonlinearity	DNL			1		LSB
Maximum Integral Nonlinearity	INL			1		LSB
ADC Total Monitoring Cycle Time		Four voltage and four current–sense conversions	95	100	112	µs
MON_ LSB Voltage		16V range	15.25	15.43	15.60	mV
		8V range	7.655	7.735	7.805	
		4V range	3.835	3.870	3.905	
		2V range	1.915	1.935	1.955	
MON_ Code 000H to 001H Transition Voltage		16V range	13	28	41	mV
		8V range	7	16	22	
		4V range	5	9	13	
		2V range	2	5	9	
CURRENT MONITORING FUNCTION						
MON_, SENSE_ Input Range			0		16	V
SENSE_ Input Current		$V_{SENSE\_}$, $V_{MON\_}$ = 16V		32	75	µA
MON_ Input Current		$V_{SENSE\_}$, $V_{MON\_}$ = 16V		180	280	µA
Current Measurement Offset LSB Voltage		25mV range		24.34		mV
		50mV range		48.39		
		100mV range		96.77		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Measurement Error, 25mV Range		$V_{MON\_}$ = 0mV	$V_{SENSE\_}$ - $V_{MON\_}$ = 5mV	-6.8		+6.8	% Full Scale
			$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-7.6		+8	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 5mV	-8		+7.2	
			$V_{SENSE\_}$ - V_{MON} = 20mV	-7.6		+7.6	
Current Measurement Error, 50mV Range (Note 2)		$V_{MON\_}$ = 0mV	$V_{SENSE\_}$ - $V_{MON\_}$ = 10mV	-3.8		+4	% Full Scale
			$V_{SENSE\_}$ - $V_{MON\_}$ = 40mV	-5.5		+5.4	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 10mV	-4.2		+3.9	
			$V_{SENSE\_}$ - $V_{MON\_}$ = 40mV	-4		+4.3	
Current Measurement Error, 100mV Range (Note 2)		$V_{MON\_}$ = 0mV	$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-2.9		+2.6	% Full Scale
			$V_{SENSE\_}$ - $V_{MON\_}$ = 80mV	-5.1		+4.7	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-2.3		+2	
			$V_{SENSE\_}$ - $V_{MON\_}$ = 80mV	-2.7		+2.4	
Fast Current-Limit Threshold Error, 25mV Range		$V_{MON\_}$ = 0mV	Circuit-breaker DAC = 102	-2.3		+1.6	mV
			Circuit-breaker DAC = 255	-3		+1.9	
		$V_{MON\_}$ = 2.5V to 16V	Circuit-breaker DAC = 102	-2.5		+1.6	
			Circuit-breaker DAC = 255	-3		+1.8	
Fast Current-Limit Threshold Error, 50mV Range		$V_{MON\_}$ = 0mV	Circuit-breaker DAC = 102	-3.4		+2	mV
			Circuit-breaker DAC = 255	-5.3		+2.6	
		$V_{MON\_}$ = 2.5V to 16V	Circuit-breaker DAC = 102	-3.2		+1.5	
			Circuit-breaker DAC = 255	-4.5		+1.6	
Fast Current-Limit Threshold Error, 100mV Range		$V_{MON\_}$ = 0mV	Circuit-breaker DAC = 102	-6.3		+2.7	mV
			Circuit-breaker DAC = 255	-10.7		+4.7	
		$V_{MON\_}$ = 2.5V to 16V	Circuit-breaker DAC = 102	-4.9		+1.6	
			Circuit-breaker DAC = 255	-7.9		+1.5	
Slow Current-Limit Threshold Error, 25mV Range		$V_{MON\_}$ = 0mV, fast/slow 200%	Circuit-breaker DAC = 102	-1.2		+2.3	mV
			Circuit-breaker DAC = 255	-1.2		+2.7	
		$V_{MON\_}$ = 2.5V to 16V, fast/slow 200%	Circuit-breaker DAC = 102	-1.4		+2.4	
			Circuit-breaker DAC = 255	-1.2		+2.9	
Slow Current-Limit Threshold Error, 50mV Range		$V_{MON\_}$ = 0mV, fast/slow 200%	Circuit-breaker DAC = 102	-1.2		+3	mV
			Circuit-breaker DAC = 255	-1.4		+3.9	
		$V_{MON\_}$ = 2.5V to 16V, fast/slow 200%	Circuit-breaker DAC = 102	-1.2		+3.1	
			Circuit-breaker DAC = 255	-1.1		+3.8	
Slow Current-Limit Threshold Error, 100mV Range		$V_{MON\_}$ = 0mV, fast/slow 200%	Circuit-breaker DAC = 102	-1.5		+4.6	mV
			Circuit-breaker DAC = 255	-2.1		+6.6	
		$V_{MON\_}$ = 2.5V to 16V, fast/slow 200%	Circuit-breaker DAC = 102	-0.7		+4.5	
			Circuit-breaker DAC = 255	-0.9		+6	
Fast Circuit-Breaker Response Time	t_{FCD}	Overdrive = 10% of current-sense range			2		µs

0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slow Current-Limit Response Time	t_{SCD}	Overdrive = 4% of current-sense range		2.4		ms
		Overdrive = 8% of current-sense range		1.2		
		Overdrive = 16% of current-sense range		0.6		
THREE-STATE INPUTS						
A0, A1, ILIM_, MODE, PROT Low Current	$I_{IN,LOW}$	Input voltage = 0.4V	-40			µA
A0, A1, ILIM_, MODE, PROT High Current	$I_{IN,HIGH}$	Input voltage = V_{REG} - 0.2V			40	µA
A0, A1, ILIM_, MODE, PROT Unconnected Current	I_{FLOAT}	Maximum source/sink current for unconnected state	-4		+4	µA
A0, A1, ILIM_, MODE, PROT Low Voltage		Relative to GND_			0.4	V
A0, A1, ILIM_, MODE, PROT High Voltage		Relative to V_{REG}	-0.24			V
TWO-STATE INPUTS						
RETRY, HWEN, POL Input Logic Low Voltage					0.4	V
RETRY, HWEN, POL Input Logic High Voltage			V_{REG} - 0.4			V
RETRY, HWEN, POL Input Current			-1		+1	µA
ON_ Input Threshold		Rising	0.586	0.596	0.606	V
ON_ Input Hysteresis		Falling		4		%
ON_ Input Current			-100		+100	nA
TIMING						
MON_ to PG_ Delay		Register configurable (see Tables 31a and 31b)		50		ms
				100		
				200		
				400		
CHARGE PUMPS (GATE_)						
Charge-Pump Output Voltage		Relative to $V_{MON\_}$	4.5	5.3	5.5	V
Charge-Pump Output Source Current	$I_{G(UP)}$		4	5	6	µA
GATE_ Discharge Current	$I_{G(DN)}$	$V_{GATE\_}$ - $V_{MON\_}$ = 2V		500		mA
OUTPUTS ($\overline{\text{FAULT\_}}$, PG_, $\overline{\text{ALERT}}$)						
Output Voltage Low		I_{SINK} = 3.2mA			0.2	V
Output Leakage (Open-Drain)					1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 1)

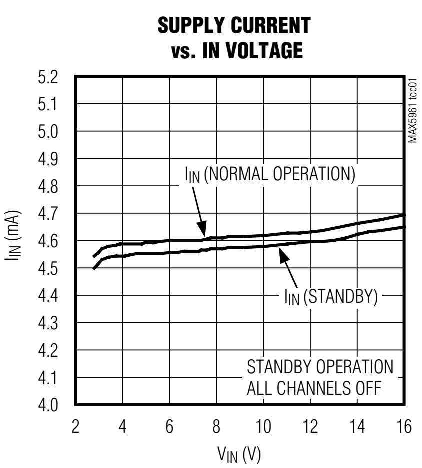
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C INTERFACE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0.3		0.9	ns
Receive SCL/SDA Rise Time	t_R				1	µs
Receive SCL/SDA Fall Time	t_{FP}				300	ns
Pulse Width of Spike Suppressed	t_{SP}			50		ns
SDA, SCL Input High Voltage	V_{IH}		1.6			V
SDA, SCL Input Low Voltage	V_{IL}				0.8	V
SDA, SCL Input Hysteresis	V_{HYST}			0.22		V
SDA, SCL Input Current					±1	µA
SDA, SCL Input Capacitance				15		pF
SDA Output Low Voltage	V_{OL}		0.4			V

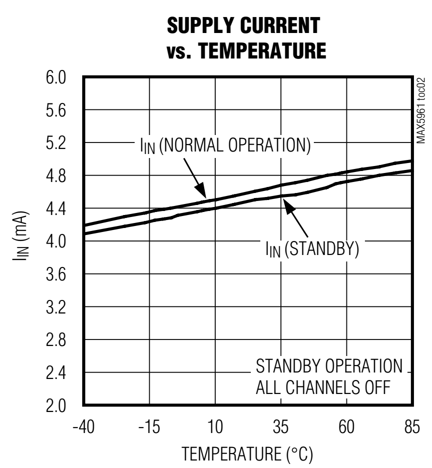
Note 1: All devices 100% production tested at T_A = +25°C and T_A = +85°C. Limits over the temperature range are guaranteed by design.

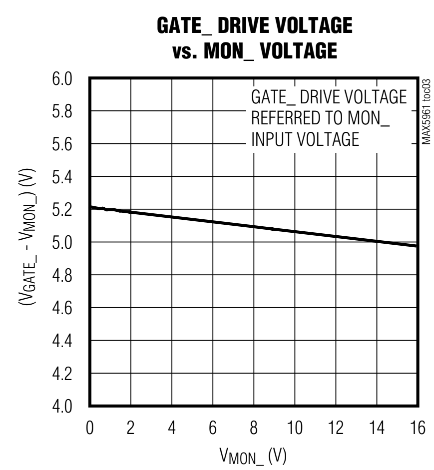
Note 2: Guaranteed by design characterization, not production tested.

Typical Operating Characteristics

($V_{S\_}$ = 12V, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted. See the *Typical Application Circuit*.)





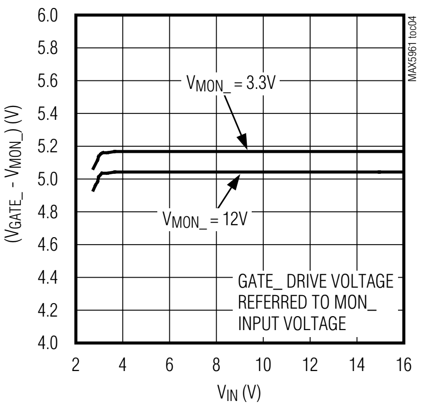


0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

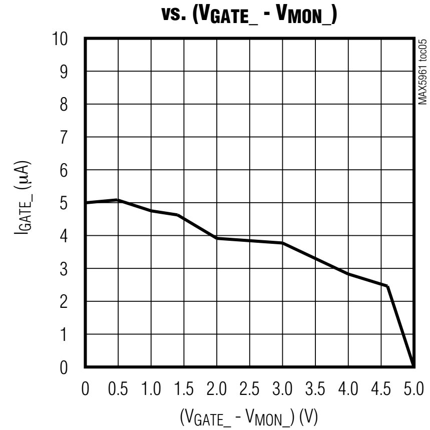
Typical Operating Characteristics (continued)

($V_{S\_}$ = 12V, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted. See the *Typical Application Circuit*.)

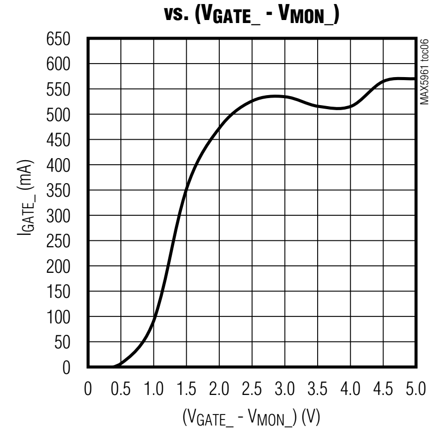
GATE_ DRIVE VOLTAGE vs. IN VOLTAGE



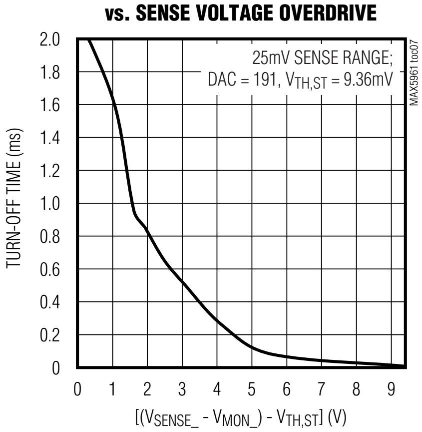
GATE_ DRIVE CURRENT vs. ($V_{GATE\_}$ - $V_{MON\_}$)



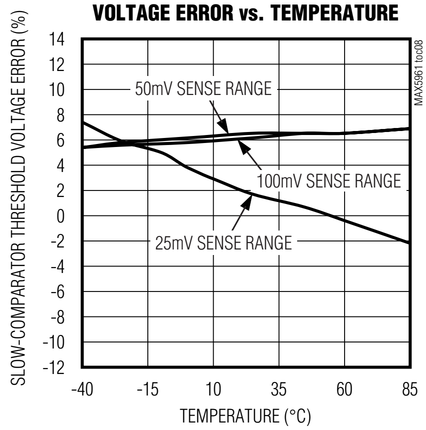
GATE_ DISCHARGE CURRENT vs. ($V_{GATE\_}$ - $V_{MON\_}$)



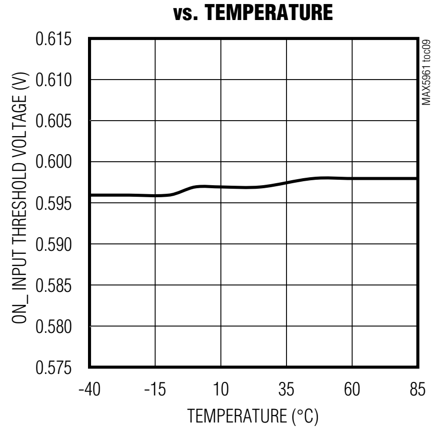
SLOW-COMPARATOR TURN-OFF TIME vs. SENSE VOLTAGE OVERDRIVE



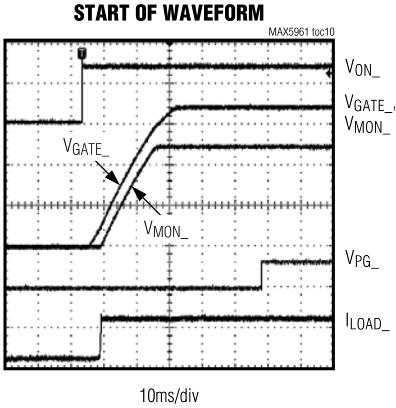
SLOW-COMPARATOR THRESHOLD VOLTAGE ERROR vs. TEMPERATURE



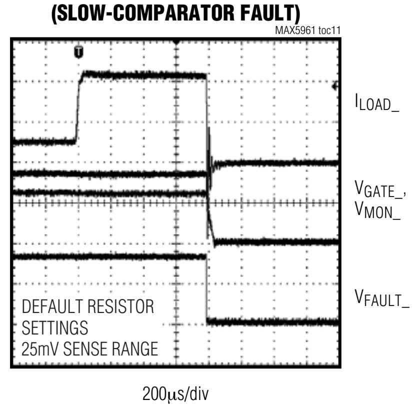
ON_ INPUT THRESHOLD VOLTAGE vs. TEMPERATURE



START OF WAVEFORM

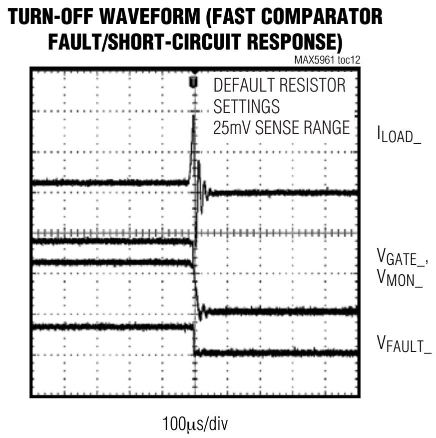


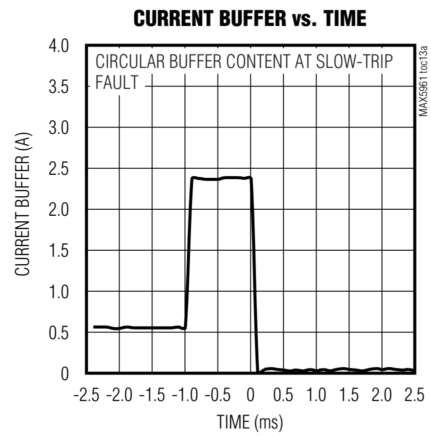
TURN-OFF WAVEFORM (SLOW-COMPARATOR FAULT)

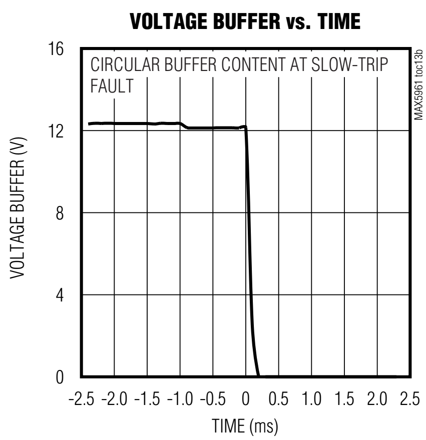


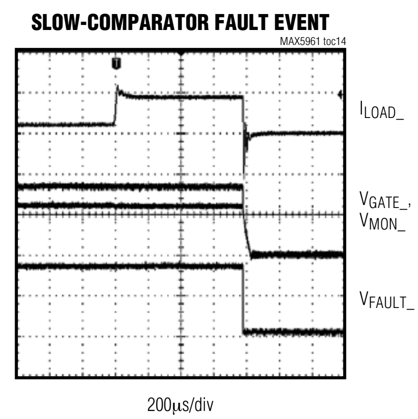
Typical Operating Characteristics (continued)

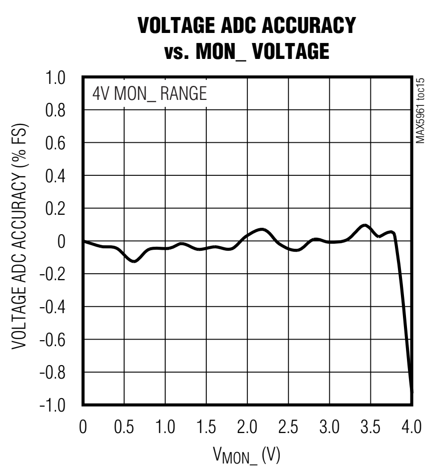
($V_{S\_}$ = 12V, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted. See the *Typical Application Circuit.*)

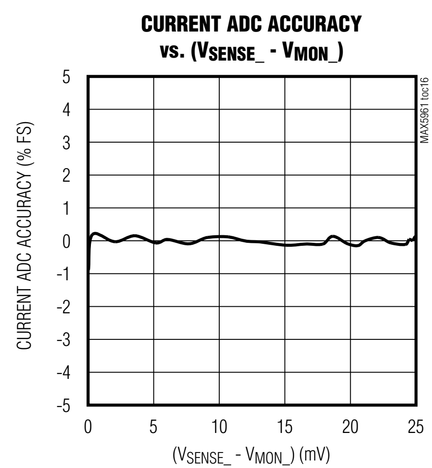








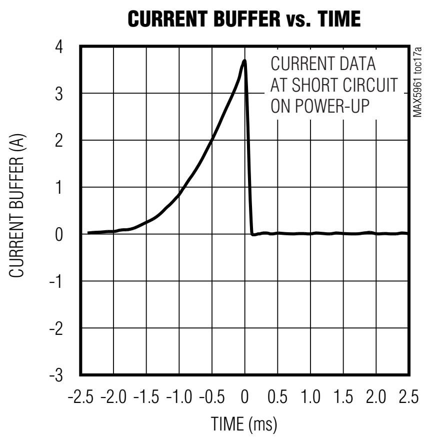


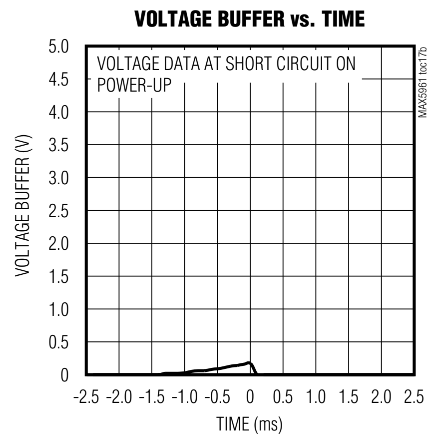


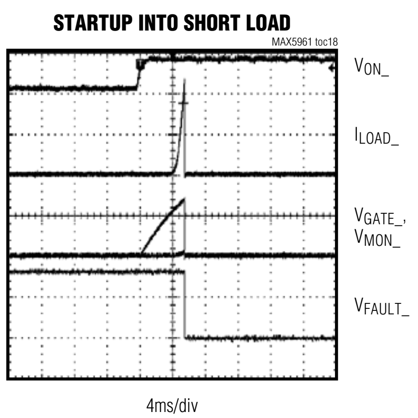
0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

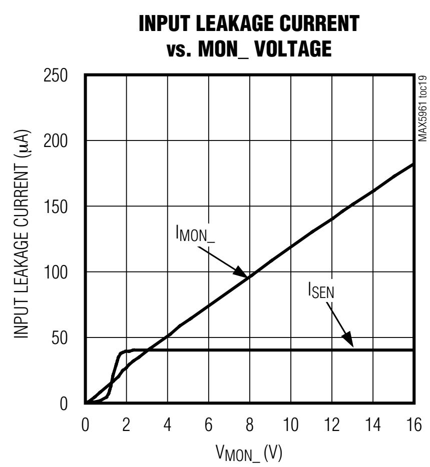
Typical Operating Characteristics (continued)

($V_{S\_}$ = 12V, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted. See the *Typical Application Circuit*.)









Pin Description

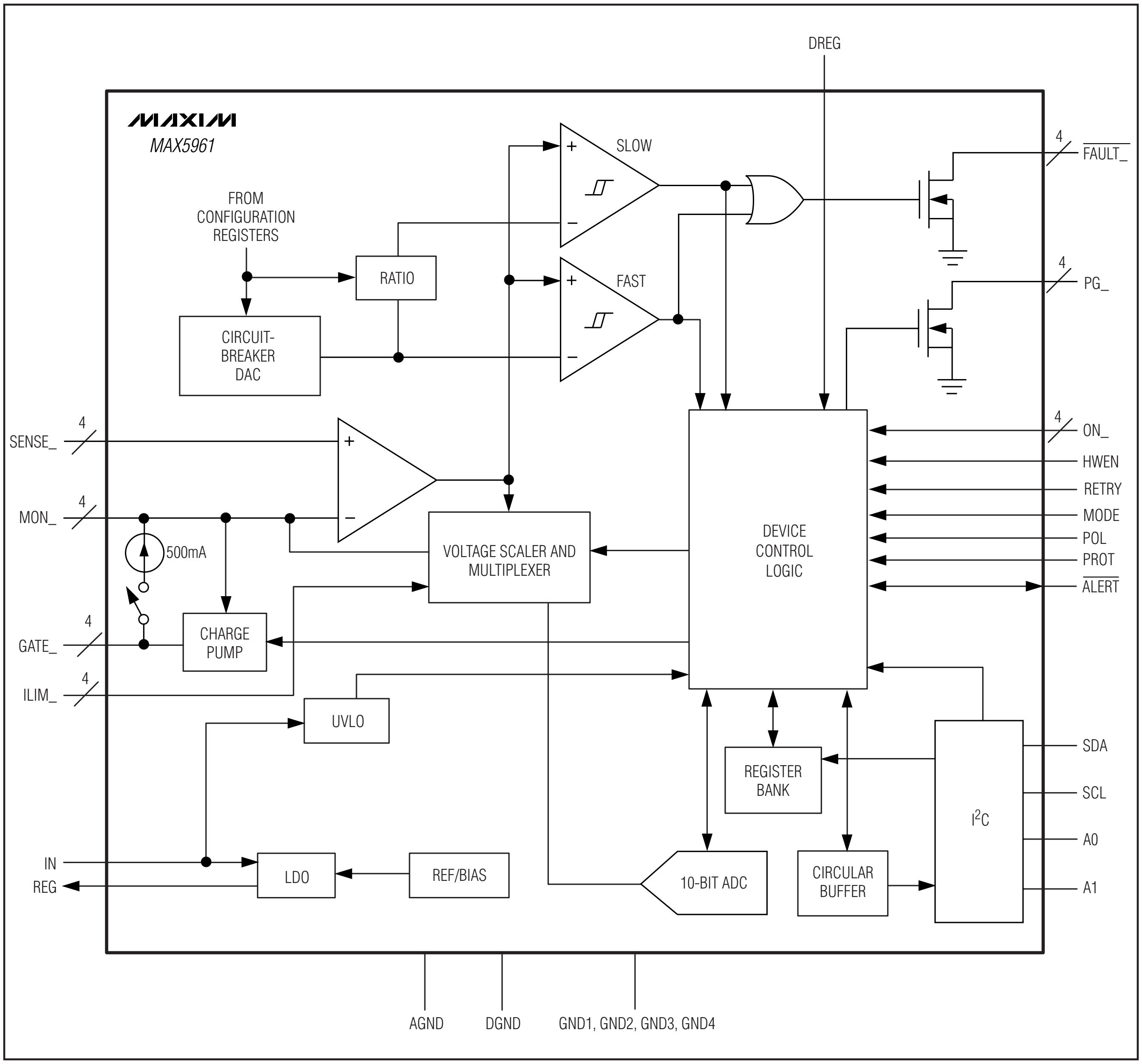
PIN	NAME	FUNCTION
1	SENSE1	Channel 1 Current-Sense Input. Connect SENSE1 to the source of an external MOSFET and to one end of R_{SENSE1} (see the *Typical Application Circuit*).
2	MON1	Channel 1 Voltage Monitoring Input
3	GATE1	Channel 1 Gate-Drive Output. Connect to gate of an external n-channel MOSFET.
4	GND1	Channel 1 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.
5	GND3	Channel 3 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.
6	GATE3	Channel 3 Gate-Drive Output. Connect to the gate of an external n-channel MOSFET.
7	MON3	Channel 3 Voltage Monitoring Input
8	SENSE3	Channel 3 Current-Sense Input. Connect SENSE3 to the source of an external MOSFET and to one end of R_{SENSE3} (see the *Typical Application Circuit*).
9	POL	Polarity Select Input. Connect to DREG for active-high power-good outputs (PG_). Connect to GND_ for active-low power-good outputs.
10	DREG	Logic Power-Supply Input. Connect to REG externally through a 10Ω resistor and to DGND with a 1µF ceramic capacitor.
11	ON1	Channel 1 Precision Turn-On Input
12	ON3	Channel 3 Precision Turn-On Input
13	$\overline{\text{FAULT1}}$	Channel 1 Active-Low Open-Drain Fault Output. $\overline{\text{FAULT1}}$ goes low if an overcurrent shutdown occurs on channel 1.
14	$\overline{\text{FAULT2}}$	Channel 2 Active-Low Open-Drain Fault Output. $\overline{\text{FAULT2}}$ goes low if an overcurrent shutdown occurs on channel 2.
15	$\overline{\text{FAULT3}}$	Channel 3 Active-Low Open-Drain Fault Output. $\overline{\text{FAULT3}}$ goes low if an overcurrent shutdown occurs on channel 3.
16	$\overline{\text{FAULT4}}$	Channel 4 Active-Low Open-Drain Fault Output. $\overline{\text{FAULT4}}$ goes low if an overcurrent shutdown occurs on channel 4.
17	SDA	I^2C Serial-Data Input/Output
18	SCL	I^2C Serial-Clock Input
19	$\overline{\text{ALERT}}$	Open-Drain Alert Output. $\overline{\text{ALERT}}$ goes low during a fault to notify the system of an impending failure.
20	PG1	Channel 1 Open-Drain Power-Good Output
21	PG2	Channel 2 Open-Drain Power-Good Output
22	PG3	Channel 3 Open-Drain Power-Good Output
23	PG4	Channel 4 Open-Drain Power-Good Output
24	DGND	Digital Ground. Connect all GND_ and DGND to AGND externally using a star connection.
25	ON4	Channel 4 Precision Turn-On Input
26	ON2	Channel 2 Precision Turn-On Input
27	RETRY	Autoretry Fault Management Input. Connect to DREG to enable autoretry operation. Connect to DGND to enable latched-off operation.
28	I.C.	Internally Connected. Connect to AGND only.

0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

Pin Description (continued)

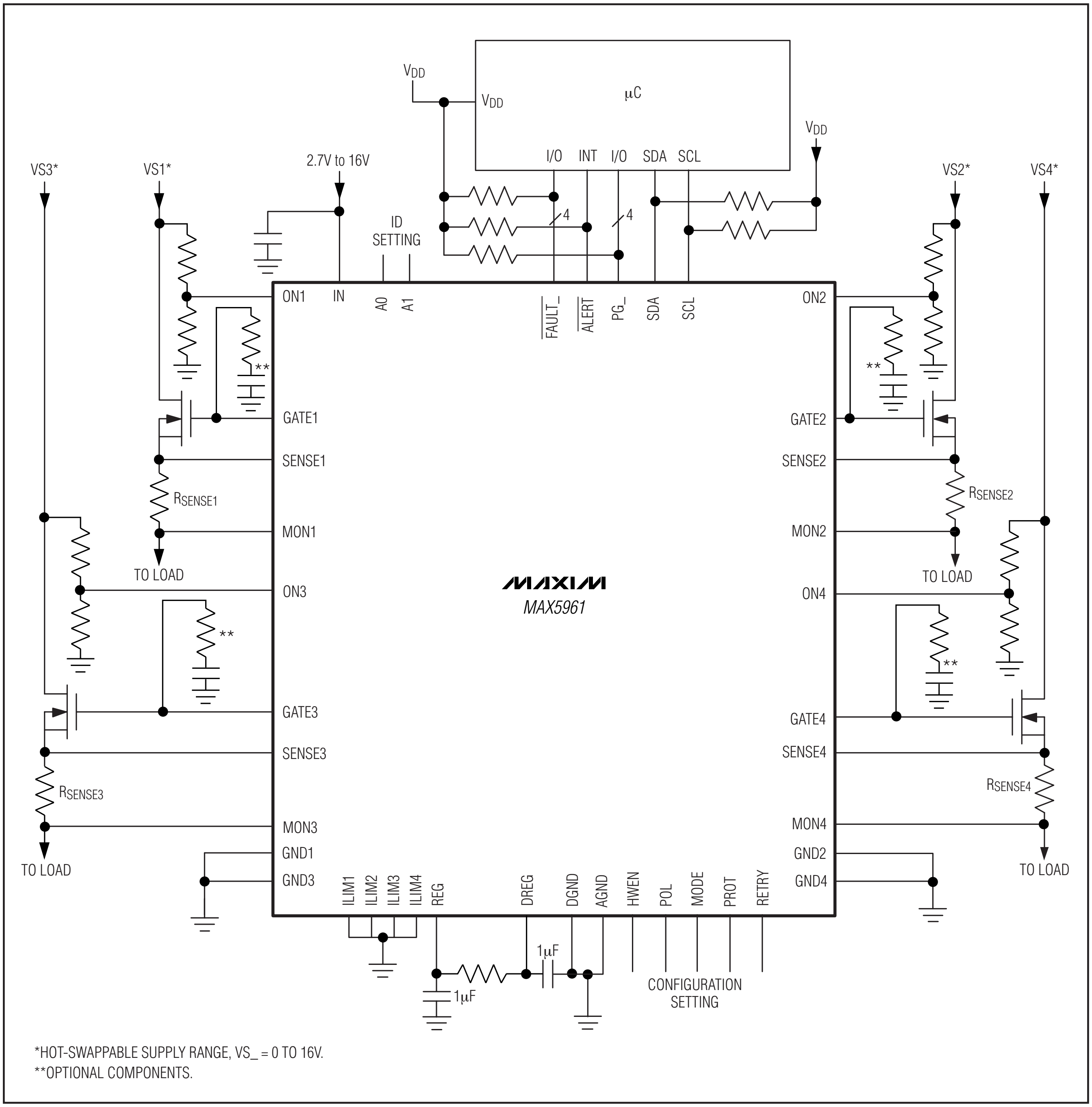
PIN	NAME	FUNCTION
29	SENSE4	Channel 4 Current-Sense Input. Connect SENSE4 to the source of an external MOSFET and to one end of R_{SENSE4} (see the *Typical Application Circuit*).
30	MON4	Channel 4 Voltage Monitoring Input
31	GATE4	Channel 4 Gate-Drive Output. Connect to gate of an external n-channel MOSFET.
32	GND4	Channel 4 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.
33	GND2	Channel 2 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.
34	GATE2	Channel 2 Gate-Drive Output. Connect to gate of an external n-channel MOSFET.
35	MON2	Channel 2 Voltage Monitoring Input
36	SENSE2	Channel 2 Current-Sense Input. Connect SENSE2 to the source of an external MOSFET and to one end of R_{SENSE2} (see the *Typical Application Circuit*).
37	ILIM4	Channel 4 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected (see Table 7b).
38	ILIM3	Channel 3 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected (see Table 7b).
39	ILIM2	Channel 2 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected (see Table 7b).
40	ILIM1	Channel 1 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected (see Table 7b).
41	IN	Power-Supply Input. Connect to a voltage from 2.7V to 16V. Bypass to AGND with a 1µF capacitor.
42	AGND	Analog Ground. Connect all GND_ and DGND to AGND externally using a star connection.
43	REG	Internal Regulator Output. Bypass to ground with a 1µF capacitor. Connect only to DREG and logic-input pullup resistors. Do not use to power external circuitry.
44	A1	Three-State I^2C Address Input 1
45	A0	Three-State I^2C Address Input 0
46	PROT	Protection Behavior Input. Three-state input sets one of three different response options for undervoltage and overvoltage events (see Table 29).
47	MODE	Hot-Swap Three-State Mode Select Input. Connect MODE to DGND, DREG, or leave it unconnected to operate the hot-swap channels independently, in pairs, or as a group of four, respectively (see Table 2).
48	HWEN	Hardware Enable Input. Connect to DREG or DGND. State is read upon power-up as V_{IN} crosses the UVLO threshold and sets Chx_EN2 bits with this value. After UVLO, this input becomes inactive until power is cycled.
—	EP	Exposed Pad. EP is internally grounded. Connect externally to AGND.

Functional Diagram

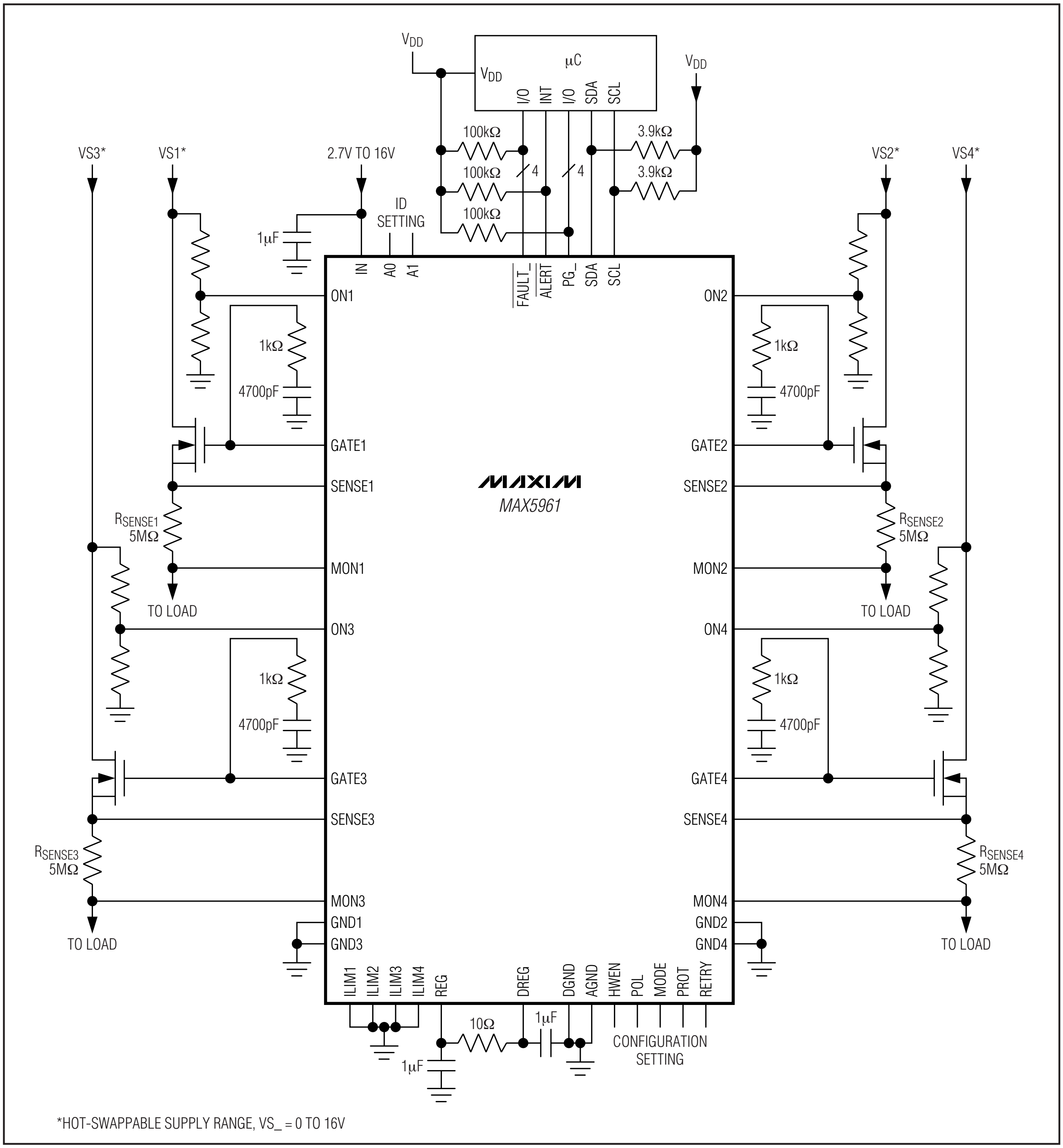


0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

Typical Operating Circuit



Typical Application Circuit



0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

Detailed Description

The MAX5961 0 to 16V, quad, hot-swap controller provides complete protection for multisupply systems. The device allows the safe insertion and removal of circuit cards into live backplanes. The MAX5961 is an advanced hot-swap controller that monitors voltage and current with an internal 10-bit ADC. The device provides two levels of overcurrent circuit-breaker protection; a fast-trip threshold for a fast turn-off and a lower slow-trip threshold for a delayed turn-off. The maximum overcurrent circuit-breaker threshold range is set independently for each channel with a three-state input (ILIM_) or by programming though an I²C interface.

The internal 10-bit ADC is multiplexed to monitor the output voltage and current of each hot-swap channel. The total time to cycle through all the eight measurements is 100µs (typ). Each 10-bit value is stored in an internal circular buffer so that 50 past samples of each signal can be read back through the I²C interface at any time or after a fault condition.

The MAX5961 can be configured as four independent hot-swap controllers, hot-swap controllers operating in pairs, or as a group of four hot-swap controllers.

The device also includes five digital comparators per hot-swap channel to implement overcurrent warning, two levels of overvoltage detection, and two levels of undervoltage detection. The limits for overcurrent, overvoltage, and undervoltage are user-programmable. When any of the measured values violates the programmable limits, an external $\overline{\text{ALERT}}$ signal is asserted. In addition to the $\overline{\text{ALERT}}$ signal, depending on the selected operating mode, the MAX5961 can deassert a power-good signal and/or turn-off the external MOSFET.

Table 1a. Register Address Map (Channel Specific)

REGISTER	DESCRIPTION	ADDRESS (HEX CODE)				RESET VALUE	TABLE
		CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4		
adc_chx_cs_h	High 8 bits ([9:2]) of latest current-signal ADC result	0x00	0x04	0x08	0x0C	0x00	9
adc_chx_cs_l	Low 2 bits ([1:0]) of latest current-signal ADC result	0x01	0x05	0x09	0x0D	0x00	10
adc_chx_mon_h	High 8 bits ([9:2]) of latest voltage-signal ADC result	0x02	0x06	0x0A	0x0E	0x00	19
adc_chx_mon_l	Low 2 bits ([1:0]) of latest voltage-signal ADC result	0x03	0x07	0x0B	0x0F	0x00	20
min_chx_cs_h	High 8 bits ([9:2]) of current-signal minimum value	0x10	0x18	0x20	0x28	0xFF	13
min_chx_cs_l	Low 2 bits ([1:0]) of current-signal minimum value	0x11	0x19	0x21	0x29	0x03	14
max_chx_cs_h	High 8 bits ([9:2]) of current-signal maximum value	0x12	0x1A	0x22	0x2A	0x00	15
max_chx_cs_l	Low 2 bits ([1:0]) of current-signal maximum value	0x13	0x1B	0x23	0x2B	0x00	16
min_chx_mon_h	High 8 bits ([9:2]) of voltage-signal minimum value	0x14	0x1C	0x24	0x2C	0xFF	32
min_chx_mon_l	Low 2 bits ([1:0]) of voltage-signal minimum value	0x15	0x1D	0x25	0x2D	0x03	33
max_chx_mon_h	High 8 bits ([9:2]) of voltage-signal maximum value	0x16	0x1E	0x26	0x2E	0x00	34
max_chx_mon_l	Low 2 bits ([1:0]) of voltage-signal maximum value	0x17	0x1F	0x27	0x2F	0x00	35

Table 1a. Register Address Map (Channel Specific) (continued)

REGISTER	DESCRIPTION	ADDRESS (HEX CODE)				RESET VALUE	TABLE
		CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4		
uv1_chx_h	High 8 bits ([9:2]) of undervoltage warning (UV1) threshold	0x32	0x3C	0x46	0x50	0x00	21
uv1_chx_l	Low 2 bits ([1:0]) of undervoltage warning (UV1) threshold	0x33	0x3D	0x47	0x51	0x00	22
uv2_chx_h	High 8 bits ([9:2]) of undervoltage critical (UV2) threshold	0x34	0x3E	0x48	0x52	0x00	23
uv2_chx_l	Low 2 bits ([1:0]) of undervoltage critical (UV2) threshold	0x35	0x3F	0x49	0x53	0x00	24
ov1_chx_h	High 8 bits ([9:2]) of overvoltage warning (OV1) threshold	0x36	0x40	0x4A	0x54	0xFF	25
ov1_chx_l	Low 2 bits ([1:0]) of overvoltage warning (OV1) threshold	0x37	0x41	0x4B	0x55	0x03	26
ov2_chx_h	High 8 bits ([9:2]) of overvoltage critical (OV2) threshold	0x38	0x42	0x4C	0x56	0xFF	27
ov2_chx_l	Low 2 bits ([1:0]) of overvoltage critical (OV2) threshold	0x39	0x43	0x4D	0x57	0x03	28
oc_chx_h	High 8 bits ([9:2]) of overcurrent warning threshold	0x3A	0x44	0x4E	0x58	0xFF	11
oc_chx_l	Low 2 bits ([1:0]) of overcurrent warning threshold	0x3B	0x45	0x4F	0x59	0x03	12
dac_chx	Fast-comparator threshold setting (8-bit DAC)	0x5A	0x5B	0x5C	0x5D	0xBF	8
cbuf_ba_chx_v	Base address for block read of 50-sample voltage-signal data buffer	0x80	0x82	0x84	0x86	—	41
cbuf_ba_chx_i	Base address for block read of 50-sample current-signal data buffer	0x81	0x83	0x85	0x87	—	41

Table 1b. Register Address Map (General)

REGISTER	DESCRIPTION	ADDRESS (HEX CODE)	RESET VALUE	TABLE
mon_range	MON_ input range selection	0x30	0x00	17, 18
cbuf_chx_store	Selective enabling of individual blocks in the circular buffer	0x31	0xFF	42
ifast2slow	Current threshold ratio setting for the fast comparator vs. slow comparator	0x5E	0xFF	5a, 5b
status0	Slow-trip and fast-trip comparators status register	0x5F	Cx00	50
status1	PROT, MODE, and ON_ inputs status register	0x60	—	2, 4a, 4b, 29
sense_range	ILIM_ inputs status register	0x61	—	6, 7a, 7b
status3	RETRY, POL, $\overline{\text{ALERT}}$, and PG_ status register	0x62	—	30
fault0	Status register for undervoltage detection (warning or critical)	0x63	0x00	47
fault1	Status register for overvoltage detection (warning or critical)	0x64	0x00	48
fault2	Status register for overcurrent detection (warning)	0x65	0x00	49
pgdly	Delay setting between MON_ measurement and PG_ assertion	0x66	0x00	31a, 31b
fokey	Load register with 0xA5 to enable force-on function	0x67	0x00	46
foset	Register that enables force-on function for a channel	0x68	0x00	45
chxen	Channel enable bits	0x69	—	3
dgl_i	OC deglitch enable bits	0x6A	0x00	38
dgl_uv	UV deglitch enable bits	0x6B	0x00	39
dgl_ov	OV deglitch enable bits	0x6C	0x00	40
cbufrd_hibyonly	Circular buffers readout mode: 8 bit or 10 bit	0x6D	0x00	43
cbuf_dly_stop	Circular buffer stop-delay. Number of samples recorded to the circular buffer after channel shutdown.	0x72	0x19	44
peak_log_rst	Reset control bits for peak-detection registers	0x73	0x00	36
peak_log_hold	Hold control bits for peak-detection registers	0x74	0x00	37

Grouping Hot-Swap Channels

Depending on the state of the MODE input, the four-channel MAX5961 can operate as four independent hot-swap controllers, two pairs of controllers, or with all four controllers grouped together (see Tables 2 and 4a).

Table 2. Grouping Hot-Swap Channels

MODE INPUT STATUS	MODE [1]	MODE [0]	FUNCTION	DESCRIPTION
Low	1	0	Independent	Each channel operates as an independent hot-swap controller. A fault shutdown in one channel does not affect operation of other channels.
High	0	1	Paired	Channels 1 and 3 operate together as one pair while channels 2 and 4 operate as another pair. A fault shutdown in one channel of a pair shuts down both channels in the pair.
Unconnected	0	0	Grouped	All channels operate as a group. A fault shutdown in one channel shuts down all four channels.

Hot-Swap Channels On-Off Control

Depending on the configuration of the Chx_EN1 and Chx_EN2 bits, when V_{IN} is above the V_{UVLO} threshold and the ON_ input reaches its internal threshold, the MAX5961 turns on the external n-channel MOSFET for the corresponding channel, allowing power to flow to the load. The channel is enabled depending on the output of a majority function. Chx_EN1, Chx_EN2, and ON_ are the inputs to the majority function and the channel is enabled when two or more of these inputs are 1.

Channel enabled = (Chx_EN1 x Chx_EN2) + (Chx_EN1 x ON_) + (Chx_EN2 x ON_)

The inputs ON_ and Chx_EN2 can be set externally; the initial state of the Chx_EN2 bits in register chxen is set by the state of the HWEN input when IN rises above V_{UVLO}. The ON_ inputs connect to internal precision analog comparators with a 0.6V threshold. Whenever $V_{ON\_}$ is above 0.6V, the corresponding ON_ bit in register status1[3:0] is set to 1. The inputs Chx_EN1 and Chx_EN2 can be set using the I^2C interface; the Chx_EN1 bits have a default value of 0. This makes it possible to enable or disable each of the MAX5961 channels independently with or without using the I^2C interface (see Tables 3, 4a, and 4b).

Table 3. chxen Register Format

Description: Channel enable bits
Register Title: chxen
Register Address: 0x69

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
Ch4_EN2	Ch4_EN1	Ch3_EN2	Ch3_EN1	Ch2_EN2	Ch2_EN1	Ch1_EN2	Ch1_EN1	AA (HWEN = high)
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	00 (HWEN = low)

Table 4a. status1 Register Function

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
0x60	[3:0]	**ON_ Inputs State** 1 = ON_ above 600mV channel enable threshold 0 = ON_ below 600mV channel enable threshold Bit 0: ON1 Bit 1: ON2 Bit 2: ON3 Bit 3: ON4
	[5:4]	**Channel Grouping Mode (MODE Input)** 00 = Grouped (MODE unconnected) 01 = Paired (MODE high) 10 = Independent (MODE low) 11 = (Not possible)
	[7:6]	**Voltage Critical Behavior (PROT Input)** 00 = Assert $\overline{ALERT}$ upon UV/OV critical (same as UV/OV warning behavior) 01 = Assert $\overline{ALERT}$ and deassert PG_ upon UV/OV critical 10 = Assert $\overline{ALERT}$, deassert PG_, and shutdown channel(s) upon UV/OV critical 11 = (Not possible)

Table 4b. status1 Register Format

Description:	Channel grouping (three-state MODE input), fault-detection behavior (three-state PROT input), and ON_ inputs status register
Register Title:	status1
Register Address:	0x60

R	R	R	R	R	R	R	R	RESET VALUE
prot[1]	prot[0]	mode[1]	mode[0]	ON4	ON3	ON2	ON1	—
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Figure 1 shows the detailed logic operation of the hot-swap enable signals Chx_EN1, Chx_EN2, and ON_, as well as the effect of various fault conditions.

An input undervoltage threshold control for enabling the hot-swap channel can be implemented by placing a resistive divider between the drain of the hot-swap FET and ground, with the midpoint connected to ON_. The turn-on threshold voltage for the channel is then:

$$V_{EN} = 0.6V \times (R1 + R2)/R2$$

The maximum rating for the ON_ pin is 6V; do not exceed this value.

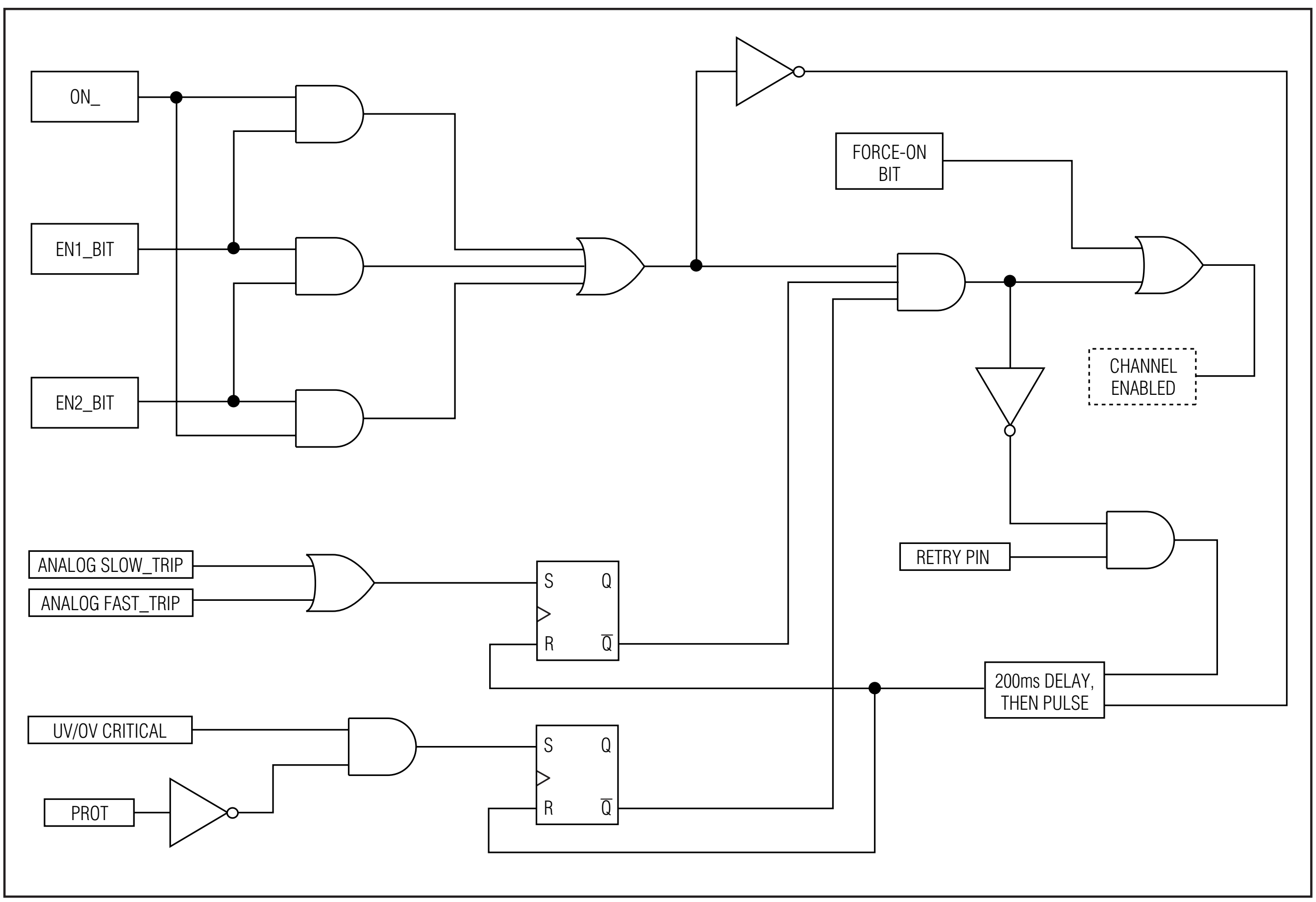


Figure 1. Channel On-Off Control Logic Functional Schematic

Startup

When all conditions for channel turn-on are met, the external n-channel MOSFET switch is fully enhanced with a typical gate-to-source voltage of 5.5V to ensure a low drain-to-source resistance. The charge pump at each GATE_ driver sources 5µA to control the output-voltage turn-on slew rate. An external capacitor can be added from GATE_ to GND_ to further reduce the voltage slew rate. Placing a 1kΩ resistor in series with this capacitance will prevent the added capacitance from increasing the gate turn-off time; see the *Typical Application Circuit*. Total inrush current is the load current summed with the product of the gate voltage slew rate dv/dt and the load capacitance.

To determine the output dv/dt during startup, divide the GATE_ pullup current $I_{G(UP)}$ by the gate-to-ground capacitance. The voltage at the source of the external FET follows the gate voltage, so the load dv/dt is the same as the gate dv/dt. Inrush current is the product of the dv/dt and the load capacitance. The time to start up t_{SU} is the hot-swap voltage VS_ divided by the output dv/dt.

Be sure to choose an external MOSFET that can handle the power dissipated during startup. The inrush current is roughly constant during startup, and the voltage drop across the FET (drain to source) decreases linearly as the load capacitance charges. The resulting power dissipation is therefore roughly equivalent to a single pulse of magnitude (VS_ x $I_{\_INRUSH}$)/2 and duration t_{SU}. Refer to the thermal resistance charts in the MOSFET data sheet to determine the junction temperature rise during startup, and ensure that this does not exceed the maximum junction temperature for worst-case ambient conditions.

Circuit-Breaker Protection

As the channel is turned on and during normal operation, two analog comparators are used to detect an overcurrent condition by sensing the voltage across an external resistor connected between SENSE_ and MON_. If the voltage across the sense resistor is less than the slow-trip and fast-trip circuit-breaker thresholds, the GATE_ output remains high. If either of the thresholds are exceeded due to an overcurrent condition, the gate of the MOSFET is pulled down to MON_ by an internal 500mA current source.

The higher of the two comparator thresholds, the fast-trip, is set by an internal 8-bit DAC (see Table 8), within one of three configurable full-scale current-sense ranges: 25mV, 50mV, or 100mV (see Tables 7a and 7b). The 8-bit fast-trip threshold DAC can be programmed from 40% to 100% of the selected full-scale current-sense range. The slow-trip threshold follows the fast-trip threshold as one of four programmable ratios, set by the ifast2slow register (see Tables 5a and 5b).

Table 5a. ifast2slow Register Format

Description:	Fast-trip to slow-trip threshold ratio setting bits							
Register Title:	ifast2slow							
Register Address:	0x5E							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
Ch4_FS1	Ch4_FS0	Ch3_FS1	Ch3_FS0	Ch2_FS1	Ch2_FS0	Ch1_FS1	Ch1_FS0	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 5b. Setting Fast-Trip to Slow-Trip Threshold Ratio

Chx_FS1	Chx_FS0	FAST-TRIP TO SLOW-TRIP RATIO (%)
0	0	125
0	1	150
1	0	175
1	1	200

The fast-trip threshold is always higher than the slow-trip threshold, and the fast-trip comparator responds very quickly to protect the system against sudden, severe overcurrent events. The slower response of the slow-trip comparator varies depending upon the amount of overdrive beyond the slow-trip threshold. If the overdrive is small and short-lived, the comparator will not shut down the affected channel. As the overcurrent event increases in magnitude, the response time of the slow-trip comparator decreases. This scheme provides good rejection of noise and spurious overcurrent transients near the slow-trip threshold while aggressively protecting the system against larger overcurrent events that occur as a result of a load fault (see Figure 2).

Setting Circuit-Breaker Thresholds

To select and set the MAX5961 slow-trip and fast-trip comparator thresholds, use the following procedure.

1) Select one of four ratios between the fast-trip threshold and the slow-trip threshold: 200%, 175%, 150%, or 125%. A system that experiences brief but large transient load currents should use a higher ratio, whereas a system that operates continuously at higher average load currents might benefit from a smaller ratio to ensure adequate protection. The ratio is set by writing to the ifast2slow register. (The default setting on power-up is 200%.)
2) Determine the slow-trip threshold $V_{TH,ST}$ based on the anticipated maximum continuous load current during normal operation, and the value of the current-sense resistor. The slow-trip threshold should include some margin (possibly 20%) above the maximum load current to prevent spurious circuit-breaker shutdown and to accommodate passive component tolerances:

$$V_{TH,ST} = R_{SENSE\_} \times I_{LOAD,MAX} \times 120\%$$

3) Calculate the necessary fast-trip threshold $V_{TH,FT}$ based on the ratio set in step 1:

$$V_{TH,FT} = V_{TH,ST} \times \text{(ifast2slow ratio)}$$

4) Select one of the three maximum current-sense ranges: 25mV, 50mV, or 100mV. The current-sense range is initially set upon power-up by the state of the associated ILIM_ input, but can be altered at any time by writing to the status2 register. For maximum accuracy and best measurement resolution, select the lowest current-sense range that is larger than the $V_{TH,FT}$ value calculated in step 3.
5) Program the fast-trip and slow-trip thresholds by writing an 8-bit value to the *dac_chx* register. This 8-bit value is determined from the desired $V_{TH,ST}$ value that was calculated in step 2, the threshold ratio from step 1, and the current-sense range from step 4:

$$DAC = V_{TH,ST} \times 255 \times \text{(ifast2slow ratio)/(ILIM\_ current sense range)}$$

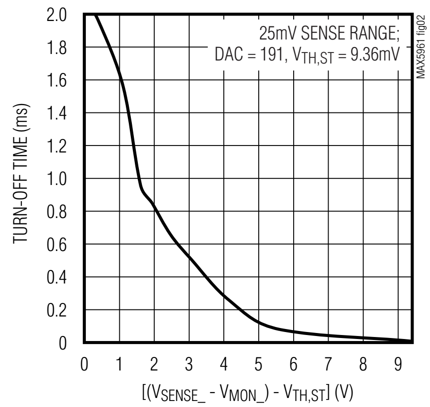


Figure 2. Slow-Comparator Turn-Off Time vs. Overdrive

The MAX5961 provides a great deal of system flexibility because the current-sense range, DAC setting, and threshold ratio can be changed “on the fly” for systems that must protect a wide range of interchangeable load devices, or for systems that control the allocation of power to smart loads. Table 6 shows the specified ranges for the fast-trip and slow-trip thresholds for all combinations of current-sense range and threshold ratio. The fast-trip DAC can be programmed to values below 0x66 (40% of the current-sense range), but accuracy is not specified for operation below 40%.

When an overcurrent event causes the MAX5961 to shut down a channel, a corresponding open-drain FAULT_ output alerts the system. Figure 3 shows the operation and fault-management flowchart for one channel of the MAX5961.

Table 6. Specified Current-Sense and Circuit-Breaker Threshold Ranges

ILIM_ INPUT	CURRENT-SENSE RANGE (mV)	SPECIFIED FAST-TRIP THRESHOLD RANGE (mV)	FAST-TRIP/ SLOW-TRIP RATIO (%)	SPECIFIED SLOW-TRIP THRESHOLD RANGE (mV)
Low	0 to 25	10 to 25 (40% to 100%) (DAC = 0x66 to 0xFF)	200	5.0 to 12.5
			175	5.7 to 14.3
			150	6.7 to 16.7
			125	8 to 20
High	0 to 50	20 to 50 (40% to 100%) (DAC = 0x66 to 0xFF)	200	10 to 25
			175	11.5 to 28.6
			150	13.3 to 33.3
			125	16 to 40
Unconnected	0 to 100	40 to 100 (40% to 100%) (DAC = 0x66 to 0xFF)	200	20 to 50
			175	22.9 to 57.1
			150	26.7 to 66.7
			125	32 to 80

Table 7a. sense_range Register Format

Description:	Fast-trip threshold maximum range setting bits, from ILIM_ three-state inputs
Register Title:	sense_range
Register Address:	0x61

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Ch4_IGS1	Ch4_IGS0	Ch3_IGS1	Ch3_IGS0	Ch2_IGS1	Ch2_IGS0	Ch1_IGS1	Ch1_IGS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Table 7b. Setting Current-Sense Range

ILIM_ INPUT STATE	Chx_IGS1	Chx_IGS0	MAXIMUM CURRENT-SENSE SIGNAL (mV)
Low	1	0	25
High	0	1	50
Unconnected	0	0	100
—	1	1	—

0 to 16V, Quad, Hot-Swap Controller with 10-Bit Current and Voltage Monitor

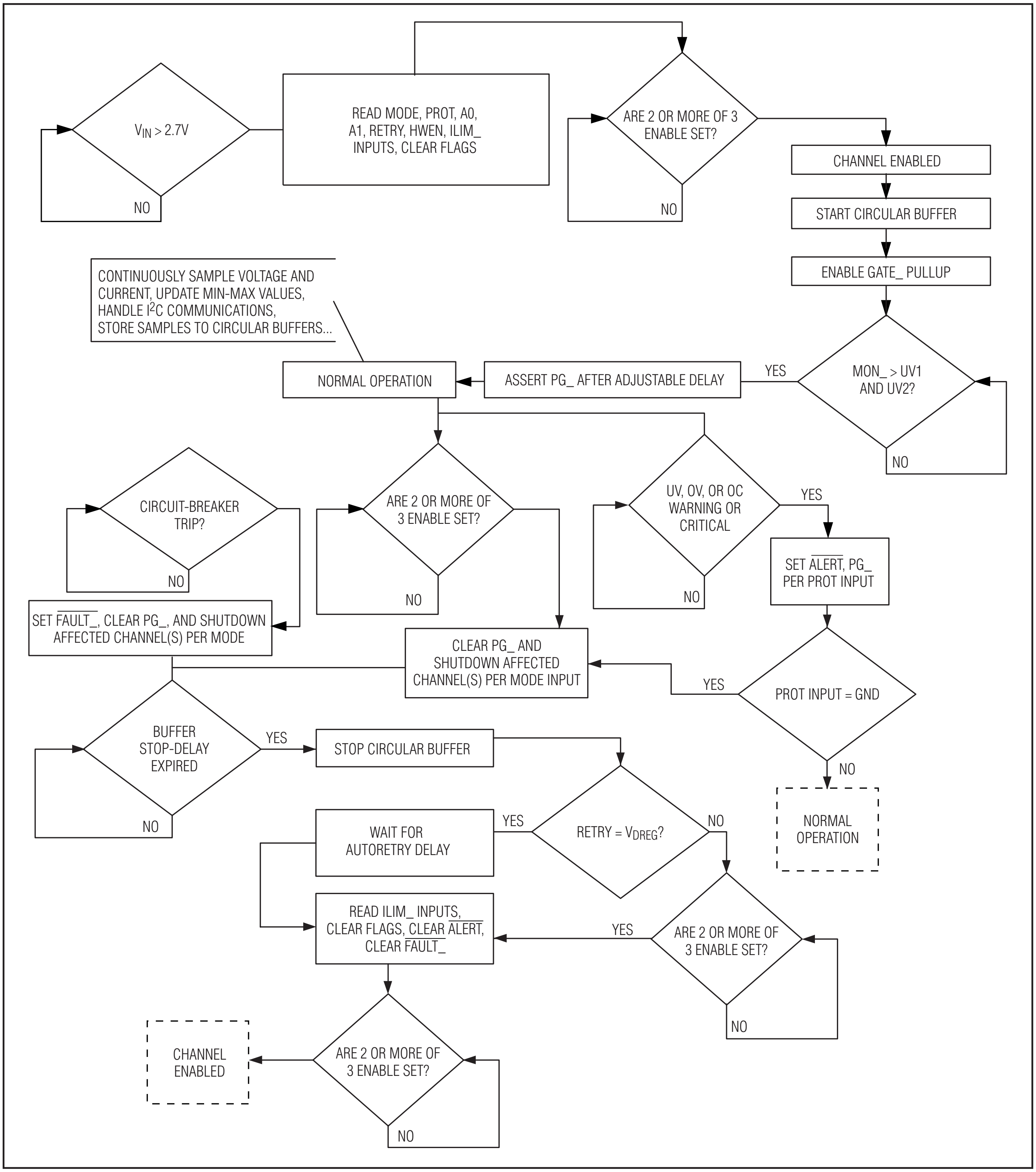


Figure 3. Operation and Fault-Management Flowchart for One Channel

Table 8. dac_chx Register Format

Description:	Fast-comparator threshold DAC setting							
Register Titles:	dac_ch1	dac_ch2	dac_ch3	dac_ch4				
Register Addresses:	0x5A	0x5B	0x5C	0x5D				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
								0xBF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Digital Current Monitoring

The four current-sense signals are sampled by the internal 10-bit ADC, and the most recent results are stored in registers for retrieval through the I²C interface. The current conversion values are 10 bits wide, with the 8 high-order bits written to one 8-bit register and the 2 low-order bits written to the next higher 8-bit register address (Tables 9 and 10). This allows use of just the high-order byte in applications where 10-bit precision is not required. This split 8-bit/2-bit storage scheme is used throughout the MAX5961 for all 10-bit ADC conversion results and 10-bit digital comparator thresholds.

Once the PG_ output is asserted (see the *Digital Voltage Monitoring and Power-Good Outputs* section), the most recent current samples are continuously compared to the programmable overcurrent warning register values. If the measured current value exceeds the warning level, the $\overline{\text{ALERT}}$ output is asserted. The MAX5961 response to the overcurrent digital comparator is not altered by the setting of the PROT input (Tables 11 and 12).

Table 9. ADC Current Conversion Results Register Format (High-Order Bits)

Description:	Most recent current conversion result, high-order bits [9:2]							
Register Titles:	adc_ch1_cs_h	adc_ch2_cs_h	adc_ch3_cs_h	adc_ch4_cs_h				
Register Addresses:	0x00	0x04	0x08	0x0C				
R	R	R	R	R	R	R	R	RESET VALUE
inew_9	inew_8	inew_7	inew_6	inew_5	inew_4	inew_3	inew_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 10. ADC Current Conversion Results Register Format (Low-Order Bits)

Description:	Most recent current conversion result, low-order bits [1:0]							
Register Titles:	adc_ch1_cs_l	adc_ch2_cs_l	adc_ch3_cs_l	adc_ch4_cs_l				
Register Addresses:	0x01	0x05	0x09	0x0D				
R	R	R	R	R	R	R	R	RESET VALUE
						inew_1	inew_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

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Table 11. Overcurrent Warning Threshold Register Format (High-Order Bits)

Description:	Overcurrent warning threshold, high-order bits [9:2]							
Register Titles:	oc_ch1_h	oc_ch2_h	oc_ch3_h	oc_ch4_h				
Register Addresses:	0x3A	0x44	0x4E	0x58				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
oc_9	oc_8	oc_7	oc_6	oc_5	oc_4	oc_3	oc_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 12. Overcurrent Warning Threshold Register Format (Low-Order Bits)

Description:	Overcurrent warning threshold, low-order bits [1:0]							
Register Titles:	oc_ch1_l	oc_ch2_l	oc_ch3_l	oc_ch4_l				
Register Addresses:	0x3B	0x45	0x4F	0x59				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						oc_1	oc_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Minimum and Maximum Value Detection for Current Measurement Values

All current measurement values from the ADC are continuously compared with the contents of minimum- and maximum-value registers, and if the most recent measurement exceeds the stored maximum or is less than the stored minimum, the corresponding register is updated with the new value. These "peak detection" registers are read/write accessible through the I^2C interface (Tables 13–16). The minimum-value registers are reset to 0x3FF, and the maximum-value registers are reset to 0x000. These reset values are loaded upon startup of a channel or at any time as commanded by register peak_log_rst (Table 36).

Table 13. ADC Minimum Current Conversion Register Format (High-Order Bits)

Description:	Minimum current conversion result, high-order bits [9:2]							
Register Titles:	min_ch1_cs_h	min_ch2_cs_h	min_ch3_cs_h	min_ch4_cs_h				
Register Addresses:	0x10	0x18	0x20	0x28				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
imin_9	imin_8	imin_7	imin_6	imin_5	imin_4	imin_3	imin_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 14. ADC Minimum Current Conversion Register Format (Low-Order Bits)

Description:	Minimum current conversion result, low-order bits [1:0]			
Register Titles:	min_ch1_cs_l	min_ch2_cs_l	min_ch3_cs_l	min_ch4_cs_l
Register Addresses:	0x11	0x19	0x21	0x29

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						imin_1	imin_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 15. ADC Maximum Current Conversion Register Format (High-Order Bits)

Description:	Maximum current conversion result, high-order bits [9:2]			
Register Titles:	max_ch1_cs_h	max_ch2_cs_h	max_ch3_cs_h	max_ch4_cs_h
Register Addresses:	0x12	0x1A	0x22	0x2A

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
imax_9	imax_8	imax_7	imax_6	imax_5	imax_4	imax_3	imax_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 16. ADC Maximum Current Conversion Register Format (Low-Order Bits)

Description:	Maximum current conversion result, low-order bits [1:0]			
Register Titles:	max_ch1_cs_l	max_ch2_cs_l	max_ch3_cs_l	max_ch4_cs_l
Register Addresses:	0x13	0x1B	0x23	0x2B

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						imax_1	imax_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

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Digital Voltage Monitoring and Power-Good Outputs

The voltage at the load (MON_ inputs) is sampled by the internal ADC. The MON_ full-scale voltage for each channel can be set to 16V, 8V, 4V, or 2V by writing to register mon_range. The default range is 16V (Tables 17 and 18).

The most recent voltage conversion results can be read from the adc_chx_mon_h and adc_chx_mon_l registers (see Tables 19 and 20).

Table 17. ADC Voltage Monitor Settings Register Format

Description: ADC voltage monitor full-scale range settings (for MON_ inputs)
Register Titles: mon_range
Register Addresses: 0x30

R/W	R/W	R/W	R/W	R/Wxxx	R/W	R/W	R/W	RESET VALUE
MON4_rng1	MON4_rng0	MON3_rng1	MON3_rng0	MON2_rng1	MON2_rng0	MON1_rng1	MON1_rng0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 18. ADC Full-Scale Voltage Setting

MONx_rng1	MONx_rng0	ADC FULL-SCALE VOLTAGE (V)
0	0	16
0	1	8
1	0	4
1	1	2

Table 19. ADC Voltage Conversion Result Register Format (High-Order Bits)

Description:	Most recent voltage conversion result, high-order bits [9:2]			
Register Titles:	adc_ch1_mon_h	adc_ch2_mon_h	adc_ch3_mon_h	adc_ch4_mon_h
Register Addresses:	0x02	0x06	0x0A	0x0E

R	R	R	R	R	R	R	R	RESET VALUE
vnew_9	vnew_8	vnew_7	vnew_6	vnew_5	vnew_4	vnew_3	vnew_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 20. ADC Voltage Conversion Result Register Format (Low-Order Bits)

Description:	Most recent voltage conversion result, low-order bits [1:0]			
Register Titles:	adc_ch1_mon_l	adc_ch2_mon_l	adc_ch3_mon_l	adc_ch4_mon_l
Register Addresses:	0x03	0x07	0x0B	0x0F

R	R	R	R	R	R	R	R	RESET VALUE
						vnew_1	vnew_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Digital Undervoltage and Overvoltage Detection Thresholds

The most recent voltage values are continuously compared to four programmable limits, comprising two undervoltage (UV) levels (see Tables 21–24) and two overvoltage (OV) levels (see Tables 25–28).

Table 21. Undervoltage Warning Threshold Register Format (High-Order Bits)

Description:	Undervoltage warning threshold high-order bits [9:2]			
Register Titles:	uv1_ch1_h	uv1_ch2_h	uv1_ch3_h	uv1_ch4_h
Register Addresses:	0x32	0x3C	0x46	0x50

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
uv1_9	uv1_8	uv1_7	uv1_6	uv1_5	uv1_4	uv1_3	uv1_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 22. Undervoltage Warning Threshold Register Format (Low-Order Bits)

Description:	Undervoltage warning threshold low-order bits [1:0]			
Register Titles:	uv1_ch1_l	uv1_ch2_l	uv1_ch3_l	uv1_ch4_l
Register Addresses:	0x33	0x3D	0x47	0x51

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						uv1_1	uv1_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 23. Undervoltage Critical Threshold Register Format (High-Order Bits)

Description:	Undervoltage critical threshold high-order bits [9:2]			
Register Titles:	uv2_ch1_h	uv2_ch2_h	uv2_ch3_h	uv2_ch4_h
Register Addresses:	0x34	0x3E	0x48	0x52

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
uv2_9	uv2_8	uv2_7	uv2_6	uv2_5	uv2_4	uv2_3	uv2_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 24. Undervoltage Critical Threshold Register Format (Low-Order Bits)

Description:	Undervoltage critical threshold low-order bits [1:0]			
Register Titles:	uv2_ch1_l	uv2_ch2_l	uv2_ch3_l	uv2_ch4_l
Register Addresses:	0x35	0x3F	0x49	0x53

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						uv2_1	uv2_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

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Table 25. Overvoltage Warning Threshold Register Format (High-Order Bits)

Description:	Overvoltage warning threshold high-order bits [9:2]			
Register Titles:	ov1_ch1_h	ov1_ch2_h	ov1_ch3_h	ov1_ch4_h
Register Addresses:	0x36	0x40	0x4A	0x54

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ov1_9	ov1_8	ov1_7	ov1_6	ov1_5	ov1_4	ov1_3	ov1_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 26. Overvoltage Warning Threshold Register Format (Low-Order Bits)

Description:	Overvoltage warning threshold low-order bits [1:0]			
Register Titles:	ov1_ch1_l	ov1_ch2_l	ov1_ch3_l	ov1_ch4_l
Register Addresses:	0x37	0x41	0x4B	0x55

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						ov1_1	ov1_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 27. Overvoltage Critical Threshold Register Format (High-Order Bits)

Description:	Overvoltage critical threshold high-order bits [9:2]			
Register Titles:	ov2_ch1_h	ov2_ch2_h	ov2_ch3_h	ov2_ch4_h
Register Addresses:	0x38	0x42	0x4C	0x56

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ov2_9	ov2_8	ov2_7	ov2_6	ov2_5	ov2_4	ov2_3	ov2_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 28. Overvoltage Critical Threshold Register Format (Low-Order Bits)

Description:	Overvoltage critical threshold low-order bits [1:0]			
Register Titles:	ov2_ch1_l	ov2_ch2_l	ov2_ch3_l	ov2_ch4_l
Register Addresses:	0x39	0x43	0x4D	0x57

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						ov2_1	ov2_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

If PG_ is asserted and the voltage is outside the warning limits, the ALERT output is asserted low. Depending on the status of the prot[] bits in register status1[7:6], the MAX5961 can also deassert the PG_ output or turn off the external MOSFET when the voltage is outside the critical limits (see Figure 4). Table 29 shows the behavior for the three possible states of the PROT input. Note that the PROT input does not affect the MAX5961 response to the UV or OV warning digital comparators; it only determines the system response to the critical digital comparators (see Tables 4a, 4b, and 29).

In a typical application, the UV1 and OV1 thresholds would be set closer to the nominal output voltage, and the UV2 and OV2 thresholds would be set further from nominal (see Figure 4). This provides a “progressive” response to a voltage excursion. However, the thresholds can be configured in any arrangement or combination as desired to suit a given application.

Table 29. PROT Input and prot[] Bits

PROT INPUT STATE	prot[1]	prot[0]	UV/OV WARNING ACTION	UV/OV CRITICAL ACTION
Unconnected	0	0	Assert ALERT	Assert ALERT
High	0	1	Assert ALERT	Assert ALERT, clear PG_
Low	1	0	Assert ALERT	Assert ALERT, clear PG_, and shutdown channel(s)

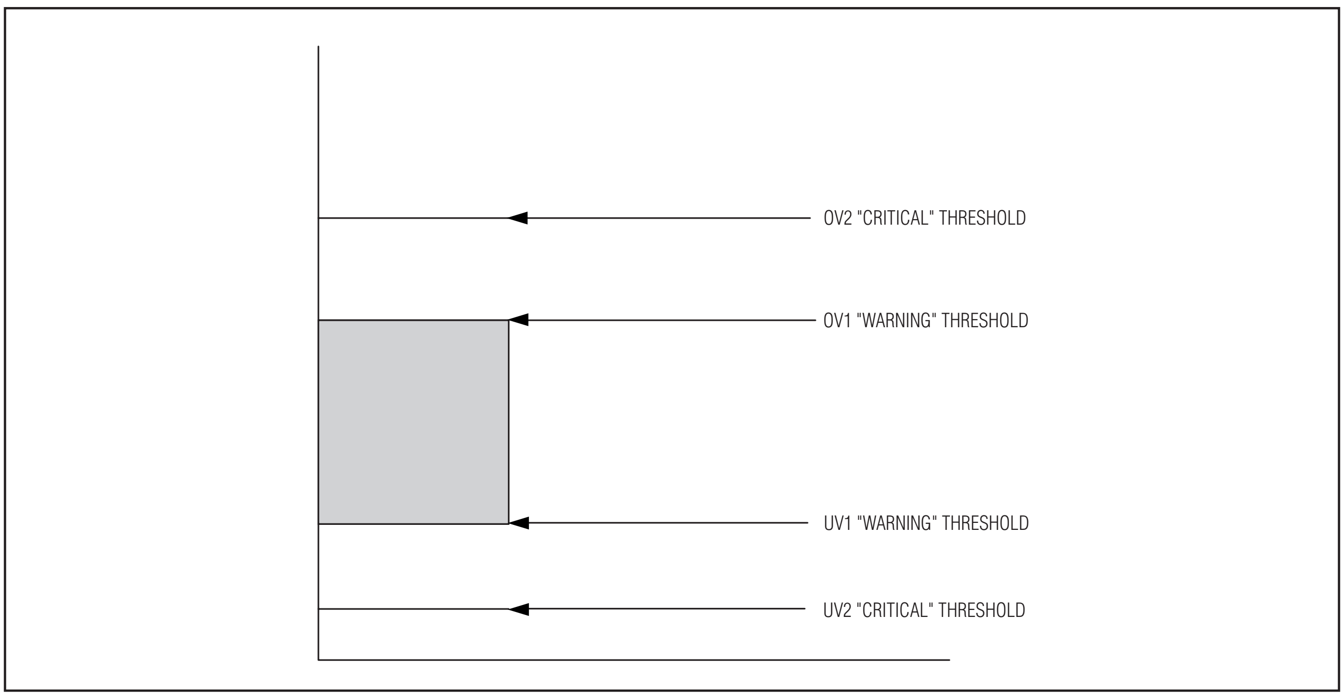

Figure 4. Graphical Representation of Typical UV and OV Thresholds Configuration

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Power-Good Detection and PG_ Outputs

The PG_ output for a given channel is asserted when the voltage at MON_ is between the undervoltage and overvoltage critical limits. The status of the power-good signals is maintained in register status3[3:0]. A value of 1 in any of the pg[] bits indicates a power-good condition, regardless of the POL setting, which only affects the PG_ output polarity. The open-drain PG_ output can be configured for active-high or active-low status indication by the state of the POL input (see Table 30).

The POL input sets the value of bit 5 of the status3 register, which is a read-only bit; the state of the POL input can be changed at any time during operation and the polarity of the PG_ outputs will change accordingly.

The assertion of the PG_ output is delayed by a user-selectable time delay of 50ms, 100ms, 200ms, or 400ms (see Tables 31a and 31b).

Table 30. status3 Register Format

Description:	Power-good status register; RETRY, POL, and alert bits							
Register Title:	status3							
Register Address:	0x62							
R	R	R	R/W	R	R	R	R	RESET VALUE
	RETRY	POL	alert	pg[4]	pg[3]	pg[2]	pg[1]	—
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 31a. Power-Good Assertion Delay-Time Register Format

Description:	Power-good assertion delay-time register							
Register Title:	pgdly							
Register Address:	0x66							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
Ch4_dly1	Ch4_dly0	Ch3_dly1	Ch3_dly0	Ch2_dly1	Ch2_dly0	Ch1_dly1	Ch1_dly0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 31b. Power-Good Assertion Delay

Chx_dly1	Chx_dly0	PG_ ASSERTION DELAY (ms)
0	0	50
0	1	100
1	0	200
1	1	400

Minimum and Maximum Value Detection for Voltage Measurement Values

All voltage measurement values are compared with the contents of minimum- and maximum-value registers, and if the most recent measurement exceeds the stored maximum or is less than the stored minimum, the corresponding register is updated with the new value.

These peak detection registers are read/write accessible through the I^2C interface (see Tables 32–35). The minimum-value registers are reset to 0x3FF, and the maximum-value registers are reset to 0x000. These reset values are loaded upon startup of a channel or at any time as commanded by register peak_log_rst (see Table 36).

Table 32. ADC Minimum Voltage Conversion Register Format (High-Order Bits)

Description: Minimum voltage conversion result, high-order bits [9:2]

Register Titles:	min_ch1_mon_h	min_ch2_mon_h	min_ch3_mon_h	min_ch4_mon_h
Register Addresses:	0x14	0x1C	0x24	0x2C

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
vmin_9	vmin_8	vmin_7	vmin_6	vmin_5	vmin_4	vmin_3	vmin_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 33. ADC Minimum Voltage Conversion Register Format (Low-Order Bits)

Description: Minimum voltage conversion result, low-order bits [1:0]

Register Titles:	min_ch1_mon_l	min_ch2_mon_l	min_ch3_mon_l	min_ch4_mon_l
Register Addresses:	0x15	0x1D	0x25	0x2D

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						vmin_1	vmin_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 34. ADC Maximum Voltage Conversion Register Format (High-Order Bits)

Description: Maximum voltage conversion result, high-order bits [9:2]

Register Titles:	max_ch1_mon_h	max_ch2_mon_h	max_ch3_mon_h	max_ch4_mon_h
Register Addresses:	0x16	0x1E	0x26	0x2E

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
vmax_9	vmax_8	vmax_7	vmax_6	vmax_5	vmax_4	vmax_3	vmax_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 35. ADC Maximum Voltage Conversion Register Format (Low-Order Bits)

Description:	Maximum voltage conversion result, low-order bits [1:0]							
Register Titles:	max_ch1_mon_l	max_ch2_mon_l	max_ch3_mon_l	max_ch4_mon_l				
Register Addresses:	0x17	0x1F	0x27	0x2F				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
						vmax_1	vmax_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Using the Voltage and Current Peak-Detection Registers

The voltage and current minimum- and maximum-value records in register locations 0x10 through 0x2F can be reset by writing a 1 to the appropriate location in register peak_log_rst (see Table 36). The minimum-value registers are reset to 0x3FF, and the maximum-value registers are reset to 0x000.

As long as a bit in register peak_log_rst is 1, the corresponding peak-detection registers are disabled and are “cleared” to their power-up reset values. The voltage and current minimum- and maximum-detection register contents for each signal can be “held” by setting bits in register peak_log_hold (see Table 37). Writing a 1 to a location in register peak_log_hold locks the register contents for the corresponding signal and stops the min/max detection and logging; writing a 0 enables the detection and logging. Note that the peak-detection registers cannot be cleared while they are held by register peak_log_hold.

The combination of these two control registers allows the user to monitor voltage and current peak-to-peak values during a particular time period.

Table 36. Peak-Detection Reset-Control Register Format

Description:	Reset control bits for peak-detection registers							
Register Title:	peak_log_rst							
Register Address:	0x73							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ch4_v_rst	ch4_i_rst	ch3_v_rst	ch3_i_rst	ch2_v_rst	ch2_i_rst	ch1_v_rst	ch1_i_rst	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 37. Peak-Detection Hold-Control Register Format

Description:	Hold control bits for peak-detection registers; per signal							
Register Title:	peak_log_hold							
Register Address:	0x74							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ch4_v_hld	ch4_i_hld	ch3_v_hld	ch3_i_hld	ch2_v_hld	ch2_i_hld	ch1_v_hld	ch1_i_hld	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Deglitching of Digital Comparators

The five digital comparators per hot-swap channel (undervoltage/overvoltage warning and critical, overcurrent warning) all have a user-selectable deglitching feature that requires two consecutive positive compares before the MAX5961 takes action as determined by the particular compare and the setting of the PROT input.

The deglitching function is enabled or disabled per comparator by registers dgl_i, dgl_uv, and dgl_ov (Tables 38, 39, and 40). Writing a 1 to the appropriate bit location in these registers enables the deglitch function for the corresponding digital comparator.

Table 38. OC Warning Comparators Deglitch Enable Register Format

Description: Deglitch enable register for overcurrent warning digital comparators
Register Title: dgl_i
Register Address: 0x6A

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	RESET VALUE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Field					Ch4_dgl_i	Ch3_dgl_i	Ch2_dgl_i	Ch1_dgl_i	0x00

Table 39. UV Warning and Critical Comparators Deglitch Enable Register Format

Description: Deglitch enable register for undervoltage warning and critical digital comparators
Register Title: dgl_uv
Register Address: 0x6B

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	RESET VALUE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Field	Ch4_dgl_uv2	Ch4_dgl_uv1	Ch3_dgl_uv2	Ch3_dgl_uv1	Ch2_dgl_uv2	Ch2_dgl_uv1	Ch1_dgl_uv2	Ch1_dgl_uv1	0x00

Table 40. OV Warning and Critical Comparators Deglitch Enable Register Format

Description: Deglitch enable register for overvoltage warning and critical digital comparators
Register Title: dgl_ov
Register Address: 0x6C

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	RESET VALUE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Field	Ch4_dgl_ov2	Ch4_dgl_ov1	Ch3_dgl_ov2	Ch3_dgl_ov1	Ch2_dgl_ov2	Ch2_dgl_ov1	Ch1_dgl_ov2	Ch1_dgl_ov1	0x00

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Circular Buffer

The MAX5961 features eight 10-bit circular buffers (in volatile memory) that contain a history of the 50 most-recent voltage and current digital conversion results for each hot-swap channel. These circular buffers can be read back through the I^{2}C interface. The recording of new data to the buffer for a given signal is stopped under any of the following conditions:

- The corresponding channel is shut down because of a fault condition
- A read of the circular buffer base address is performed through the I^{2}C interface
- The corresponding channel is turned off by a combination of the Chx_EN1, Chx_EN2, or ON_ signals

The buffers allow the user to recall the voltage and current waveforms for analysis and troubleshooting. The buffer contents are accessed through the I^{2}C interface at eight fixed addresses in the MAX5961 register address space (see Table 41).

Each of the eight buffers can also be stopped under user control by register cbuf_chx_store (see Table 42).

The contents of a buffer can be retrieved as a block read of either 50 10-bit values (spanning 2 bytes each) or of 50 high-order bytes, depending on the per-signal bit settings of register cbufrd_hibyonly (see Table 43).

Table 41. Circular Buffer Read Addresses

ADDRESS	NAME	DESCRIPTION
0x80	cbuf_ba_ch1_v	Base address for channel 1 voltage buffer block read
0x81	cbuf_ba_ch1_i	Base address for channel 1 current buffer block read
0x82	cbuf_ba_ch2_v	Base address for channel 2 voltage buffer block read
0x83	cbuf_ba_ch2_i	Base address for channel 2 current buffer block read
0x84	cbuf_ba_ch3_v	Base address for channel 3 voltage buffer block read
0x85	cbuf_ba_ch3_i	Base address for channel 3 current buffer block read
0x86	cbuf_ba_ch4_v	Base address for channel 4 voltage buffer block read
0x87	cbuf_ba_ch4_i	Base address for channel 4 current buffer block read

Table 42. Circular Buffer Control Register Format

Description: Circular buffer run-stop control register (per-buffer control: 1 = run, 0 = stop)

Register Title: cbuf_chx_store

Register Address: 0x31

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ch4_i_run	ch4_v_run	ch3_i_run	ch3_v_run	ch2_i_run	ch2_v_run	ch1_i_run	ch1_v_run	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 43. Circular Buffer Resolution Register Format

Description: Circular buffer read-out resolution: high-order byte only, or 8-2 split 10-bit data (per-buffer control: 1 = high-order byte output, 0 = full-resolution 10-bit output)

Register Title: cbufrd_hibyonly

Register Address: 0x6D

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ch4_i_res	ch4_v_res	ch3_i_res	ch3_v_res	ch2_i_res	ch2_v_res	ch1_i_res	ch1_v_res	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

If the circular buffer contents are retrieved as 10-bit data, the first byte read-out is the high-order 8 bits of the 10-bit sample, and the second byte read-out contains the two least-significant bits (LSBs) of the sample. This is repeated for each of the 50 samples in the buffer. Thus, 2 bytes must be read for each 10-bit sample retrieved. Conversely, if the buffer contents are retrieved as 8-bit data, then each byte read-out contains the 8 MSB of each successive sample. It is important to remember that in 10-bit mode, 100 bytes must be read to extract the entire buffer contents, but in 8-bit mode, only 50 bytes must be read.

The circular buffer system has a user-programmable “stop delay” that specifies a certain number of sample cycles to continue recording to the buffer after a shutdown occurs. This delay value is stored in register cbuf_dly_stop[5:0] (see Table 44).

The default (reset) value of the buffer stop-delay is 25 samples, which means that an equal number of samples are stored in the buffer preceding and following the moment of the shutdown event. The buffer stop delay is analogous to an oscilloscope trigger delay, because it allows the MAX5961 to record what happened both immediately before and after a shutdown. In other words, when the contents of a circular buffer are read-out of the MAX5961, the shutdown event will by default be located in the middle of the recorded data. The balance of data before and after an event can be altered by writing a different value (between 0 and 50) to the buffer stop-delay register.

Autoretry or Latched-Off Fault Management

In the event of an overcurrent, undervoltage, or overvoltage condition that results in the shutdown of one or more channels, the MAX5961 device can be configured to either latch off or automatically restart the affected channel. The MAX5961 stays off if the RETRY input is set low (latched-off), and will autoretry if the RETRY input is high. The RETRY input is read once during initialization and sets the value of bit 6 of the status3 register (see Table 30).

The autoretry feature has a fixed 200ms timeout delay between fault shutdown and the autorestart attempt. Be aware that if the MAX5961 is configured for autoretry operation, the startup event will occur every 200ms if a short circuit occurs. A short circuit during startup causes the output current to increase rapidly as the MOSFET is enhanced, until the slow-trip threshold is reached and the gate is pulled low again. Be sure to evaluate the MOSFET junction temperature rise for this repeated-stress condition if autoretry is used.

To restart a channel that has been shut down in latched-off operation (RETRY low), the user must either cycle power to the IN pin, or toggle one or more of the ON_ input, Chx_EN1 bit, or the Chx_EN2 bit for the affected channel.

Force-On Function

When the force-on bit for a channel is set to 1 in register foset[3:0] (see Table 45), the channel is enabled regardless of the ON_ pin voltage or the Chx_EN1 and Chx_EN2 bits in register chxen. In forced-on operation, all functions operate normally with the notable exception that the channel will not shut down due to any fault conditions that may arise.

There is a force-on key register, fokey, that must be set to 0xA5 for the force-on function to become active (see Table 46). If this register contains any value other than 0xA5, writing 1 to the force-on bits in register *foset* will have no effect. This provides protection against accidental force-on operation that might otherwise be caused by an erroneous I^{2}C write.

Table 44. Circular Buffer Stop-Delay Register Format

Description:	Circular buffer stop-delay: any integer number between 0 and 50 samples that are to be recorded to a buffer after a shutdown event, before the buffer stops storing new data.
Register Title:	cbuf_dly_stop
Register Address:	0x72

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	RESET VALUE
R	R	R/W	R/W	R/W	R/W	R/W	R/W	
0	0							0x19

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Table 45. Force-On Control Register Format

Description:	Force-on control register							
Register Title:	foset							
Register Address:	0x68							
R	R	R	R	R/W	R/W	R/W	R/W	RESET VALUE
0	0	0	0	ch4_fo	ch3_fo	ch2_fo	ch1_fo	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 46. Force-On Key Register Format

Description:	Force-on key register (must contain 0xA5 to unlock force-on feature)							
Register Title:	fokey							
Register Address:	0x67							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
fokey[7]	fokey[6]	fokey[5]	fokey[4]	fokey[3]	fokey[2]	fokey[1]	fokey[0]	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Fault Logging and Indications

The MAX5961 provides detailed information about any fault conditions that have occurred. Independent $\overline{\text{FAULT\_}}$ outputs specifically indicate circuit-breaker shutdown events, while an $\overline{\text{ALERT}}$ output is asserted whenever a problem has occurred that requires attention or interaction.

Fault Dependency

If a fault event occurs (digital UV warning/critical, digital OV warning/critical, or digital overcurrent warning) the fault is logged by setting a corresponding bit in registers fault0, fault1, or fault2 (see Tables 47, 48, and 49).

Likewise, circuit-breaker shutdown events are logged in register status0[7:0] (see Table 50).

Table 47. Undervoltage Status Register Format

Description:	Undervoltage digital-compare status register (warning [3:0] and critical [7:4] undervoltage event detection status)							
Register Title:	fault0							
Register Address:	0x63							
R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	RESET VALUE
ch4_uv2	ch3_uv2	ch2_uv2	ch1_uv2	ch4_uv1	ch3_uv1	ch2_uv1	ch1_uv1	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 48. Overvoltage Status Register Format

Description:	Overvoltage digital-compare status register (warning [3:0] and critical [7:4] overvoltage event detection status)
Register Title:	fault1
Register Address:	0x64

R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	RESET VALUE
ch4_ov2	ch3_ov2	ch2_ov2	ch1_ov2	ch4_ov1	ch3_ov1	ch2_ov1	ch1_ov1	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 49. Overcurrent Warning Status Register Format

Description:	Overcurrent digital-compare status register (overcurrent warning event detection status)
Register Title:	fault2
Register Address:	0x65

R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	RESET VALUE
				ch4_oi	ch3_oi	ch2_oi	ch1_oi	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 50. Circuit-Breaker Event Logging Register Format

Description:	Circuit-breaker slow- and fast-trip event logging
Register Title:	status0
Register Address:	0x5F

R	R	R	R	R	R	R	R	RESET VALUE
ch4_st	ch3_st	ch2_st	ch1_st	ch4_ft	ch3_ft	ch2_ft	ch1_ft	--
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

These fault register bits latch upon a fault condition, and must be reset manually by writing a zero to the register, or by restarting the affected channel as described in the *Autoretry or Latched-Off Fault Management* section.

$\overline{\text{FAULT\_}}$ Outputs

When an overcurrent event (fast-trip or slow-trip) causes the MAX5961 to shut down the affected channel(s), a corresponding open-drain $\overline{\text{FAULT\_}}$ output is asserted low. Note that the $\overline{\text{FAULT\_}}$ outputs are not asserted for shutdowns caused by critical undervoltage or overvoltage.

The $\overline{\text{FAULT\_}}$ output is cleared when the channel is disabled by pulling ON_ low or by clearing the Chx_EN1 or Chx_EN2 bits in register chxen.

$\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ output is an open-drain output that is asserted low any time that a fault or other condition requiring attention has occurred. The state of the $\overline{\text{ALERT}}$ output is also indicated by bit 4 of the status3 register.

$\overline{\text{ALERT}}$ is the NOR of registers 0x5F, 0x63, 0x64, and 0x65, so when the $\overline{\text{ALERT}}$ output goes low, the system microcontroller (µC) should query these registers through the I^2C interface to determine the cause of the $\overline{\text{ALERT}}$ assertion.

I²C Serial Interface

The MAX5961 features an I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL allow bidirectional communication between the MAX5961 and the master device at clock rates from 100kHz to 400kHz. The I²C bus can have several devices (e.g., more than one MAX5961, or other I²C devices in addition to the MAX5961) attached simultaneously. The A0 and A1 inputs set one of nine possible I²C addresses (see Table 51).

The 2-wire communication is fully compatible with existing 2-wire serial-interface systems; Figure 5 shows the interface timing diagram. The MAX5961 is a transmit/receive slave-only device, relying upon a master device to generate a clock signal. The master device (typically a µC) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX5961 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is a logic-input/open-drain output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Table 51. Slave Address Settings

ADDRESS INPUT STATE		I²C ADDRESS BITS							
A1	**A0**	**ADDR 7**	**ADDR 6**	**ADDR 5**	**ADDR 4**	**ADDR 3**	**ADDR 2**	**ADDR 1**	**ADDR 0**
Low	Low	0	1	1	1	0	1	0	R/W
Low	High	0	1	1	1	0	0	1	R/W
Low	Unconnected	0	1	1	1	0	0	0	R/W
High	Low	0	1	1	0	1	1	0	R/W
High	High	0	1	1	0	1	0	1	R/W
High	Unconnected	0	1	1	0	1	0	0	R/W
Unconnected	Low	0	1	1	0	0	1	0	R/W
Unconnected	High	0	1	1	0	0	0	1	R/W
Unconnected	Unconnected	0	1	1	0	0	0	0	R/$\overline{W}$

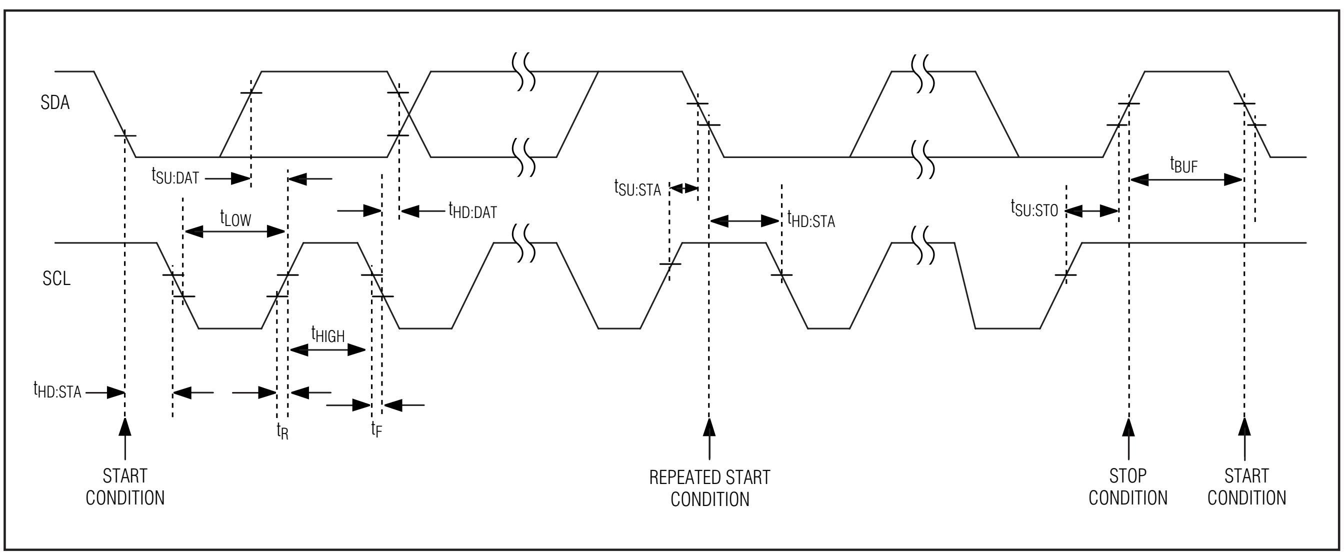

Figure 5. Serial-Interface Timing Details

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (see Figure 6), otherwise the MAX5961 registers a START or STOP condition (see Figure 7) from the master. SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START condition (see Figure 7) by transitioning SDA from high to low while SCL is high. The master device issues a STOP condition (see Figure 7) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 8).

Early STOP Conditions

The MAX5961 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I^2C format. At least one clock pulse must separate any START and STOP condition.

REPEATED START Conditions

A REPEATED START condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 8). SR may also be used when the bus master is writing to several I^2C devices and does not want to relinquish control of the bus. The MAX5961 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

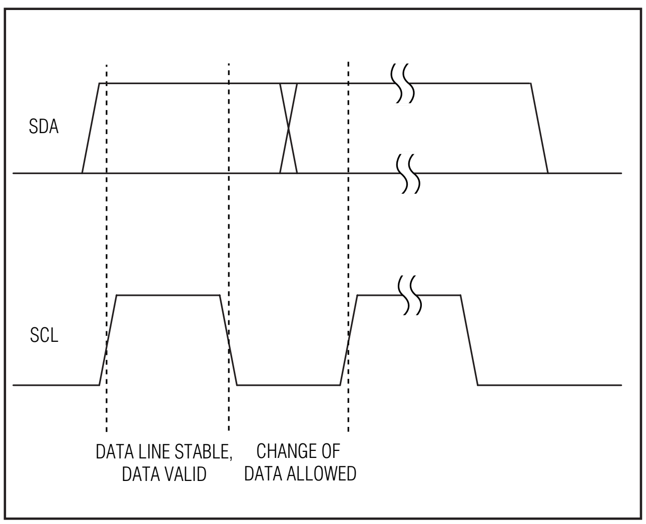

Figure 6. Bit Transfer

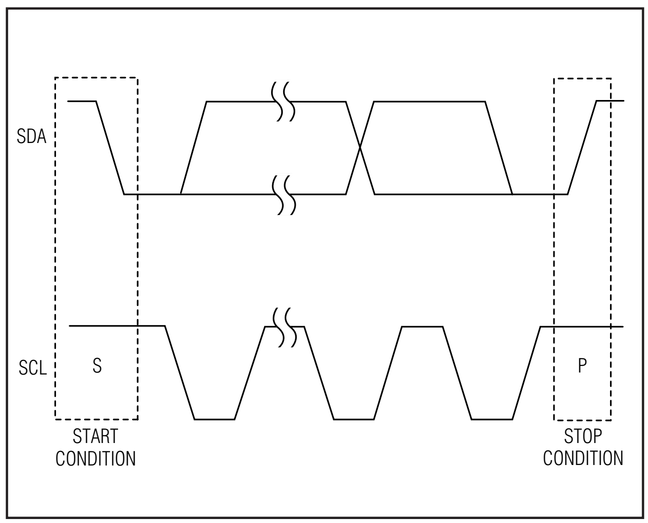

Figure 7. START and STOP Conditions

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SEND BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–PRESETS THE INTERNAL ADDRESS POINTER.

WRITE WORD FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE– MSB OF THE EEPROM REGISTER BEING WRITTEN.

DATA BYTE–FIRST BYTE IS THE LSB OF THE EEPROM ADDRESS. SECOND BYTE IS THE ACTUAL DATA.

RECEIVE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	$\overline{ACK}$	P
	7 BITS	1		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–READS DATA FROM THE REGISTER COMMANDED BY THE LAST READ BYTE OR WRITE BYTE TRANSMISSION. ALSO DEPENDENT ON A SEND BYTE.

WRITE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE– SELECTS REGISTER BEING WRITTEN.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE IF THE COMMAND IS BELOW 50h. IF THE COMMAND IS 80h, 81h, or 82h, THE DATA BYTE PRESETS THE LSB OF AN EEPROM ADDRESS.

BLOCK WRITE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	BYTE COUNT= N	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS		8 BITS		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE– PREPARES DEVICE FOR BLOCK OPERATION.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE.

BLOCK READ FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	SR	ADDRESS	$\overline{WR}$	ACK	BYTE COUNT= 16	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS			7 BITS	1		10h		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE– PREPARES DEVICE FOR BLOCK OPERATION.

SLAVE ADDRESS– EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE.

S = START CONDITION.
P = STOP CONDITION.

SHADED = SLAVE TRANSMISSION.
SR = REPEATED START CONDITION.

Figure 8. I²C Protocols

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX5961 generates an ACK when receiving an address or data by pulling SDA low during the 9th clock period (see Figure 9). When transmitting data, such as when the master device reads data back from the MAX5961, the MAX5961 waits for the master device to generate an ACK. Monitoring ACK allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX5961 generates a not acknowledge (NACK) after the slave address during a software reboot or when receiving an illegal memory address.

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 8). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed. If the master sends a STOP condition, the internal address pointer does not change. The send byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit data byte.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a STOP condition.

Write Byte

The write byte/word protocol allows the master device to write a single byte in the register bank or to write to a series of sequential register addresses. The write byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit command code.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The addressed slave increments its internal address pointer.
9) The master sends a STOP condition or repeats steps 6, 7, and 8.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The data byte is written to the register bank if the command code is valid.

The slave generates a NACK at step 5 if the command code is invalid. The command code must be in the range of 0x00 to 0x74. The internal address pointer returns to 0x00 after incrementing from the highest register address.

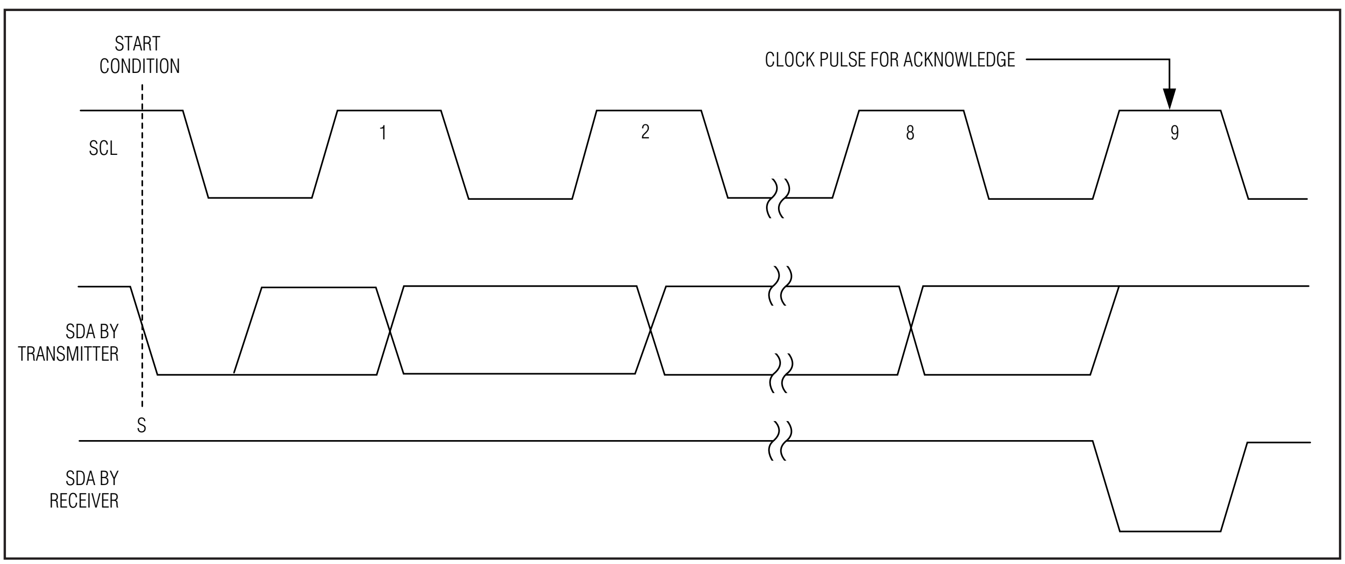

Figure 9. Acknowledge

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Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX5961 (see Figure 8). The EEPROM or register address must be preset with a send byte protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5) The slave increments its internal address pointer.
6) The master asserts an ACK on SDA and repeats steps 4 and 5 or asserts a NACK and generates a STOP condition.

The internal address pointer returns to 0x00 after incrementing from the highest register address.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 0x00 to 0x74, and the circular buffer addresses are 0x80 to 0x87. Register addresses outside this range result in a NACK being issued from the MAX5961.

Circular Buffer Read

The circular buffer read operation is similar to the receive byte operation. The read operation is triggered after any one of the circular buffer base addresses is loaded. During a circular buffer read, although all is transparent from the external world, internally the autoincrement function in the I^2C controller is disabled. Thus, it is possible to read one of the circular buffer blocks with a burst read without changing the virtual internal address corresponding to the base address. Once the master issues a NACK, the circular reading stops, and the default functions of the I^2C slave bus controller are restored.

In 8-bit read mode, every I^2C read operation shifts out a single sample from the circular buffer. In 10-bit mode, two subsequent I^2C read operations shift out a single 10-bit sample from the circular buffer, with the high-order byte read first, followed by a byte containing the right-shifted 2 LSBs. Once the master issues a NACK, the read circular buffer operation terminates and normal I^2C operation returns.

The data in the circular buffers is read back with the next-to-oldest sample first, followed by progressively more recent samples until the most recent sample is retrieved, followed finally by the oldest sample (see Table 52).

Table 52. Circular Buffer Readout Sequence

READ-OUT ORDER	1st OUT	2nd OUT	…	48th OUT	49th OUT	50th OUT
Chronological Number	1	2	…	48	49	0

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN	T4877-6	21-0144