19-4344; Rev 0; 10/08

EVALUATION KIT AVAILABLE

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

MAX5963

General Description

The MAX5963 dual hot-swap and diode ORing controller provides complete protection for dual-supply high availability systems. The device operates from 7.5V to 76V and provides hot-swap and low voltage-drop diode ORing functionality for two 7.5V to 76V outputs.

The MAX5963 allows for the safe insertion and removal of system line cards and FireWire® peripherals into a live backplane by providing inrush current control and active current limiting. The device controls external n-channel power MOSFETs to perform low-voltage-drop ORing, inrush current control, and current limiting functions. The current-limit function actively limits the current drawn by the load, protecting the load from a short-circuit condition. The MAX5963 also features a circuit-breaker function that disconnects the power to the load if the load current exceeds the circuit-breaker limit for a programmable circuit-breaker timeout.

The MAX5963 features an autoretry/latchoff input. In autoretry mode, the MAX5963 automatically restarts the turned-off channel after a programmable delay. In latchoff mode, the MAX5963 latches the channel off.

The MAX5963 consumes less than 10µA from the PWR supply in system power-off mode.

The MAX5963 is available in a 40-pin TQFN package (6mm x 6mm) and operates over the 0°C to +85°C upper commercial temperature range.

Applications

Blade Servers

Base-Station Line Cards

Network Switches/Routers

FireWire Desktops/Notebook Ports

FireWire Hubs

Typical Operating Circuit appears at end of data sheet.

FireWire is a registered trademark of Apple, Inc.

Features

- ♦ **Hot Swaps Two 7.5V to 76V Supplies**
- ♦ **Integrates Low-Voltage-Drop ORing Controller**
- ♦ **±5% Accuracy Bilevel Active Current Limit/Circuit Breaker**
- ♦ **Programmable Current-Limit/Circuit-Breaker Timeout**
- ♦ **10µA Power-Off Mode Current**
- ♦ **Protects Up to Two FireWire Ports**
- ♦ **System Power-On/Off ORing**
- ♦ **Latchoff or Autoretry Power Management**
- ♦ **Independent ON/OFF Control Allows Undervoltage Lockout Programming**
- ♦ **Fast Load Disconnect through FOSO Input (FireWire Port)**

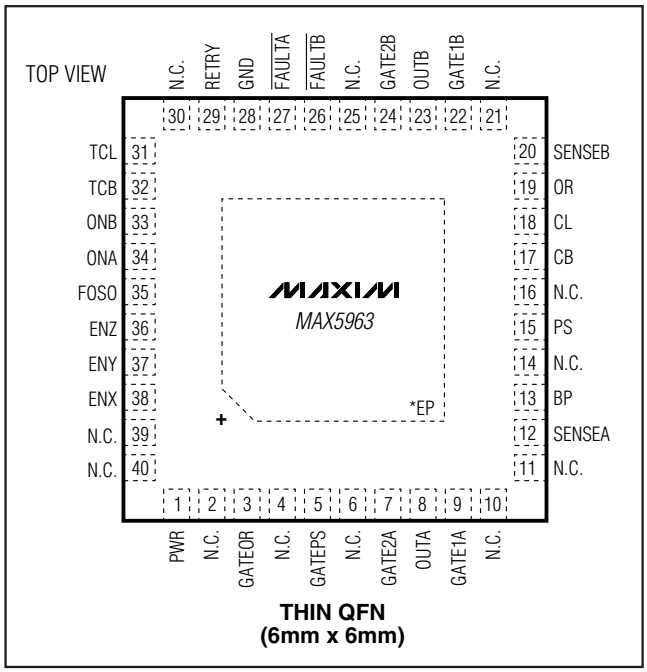
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5963UTL+	0°C to +85°C	40 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



THIN QFN (6mm x 6mm)

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

ABSOLUTE MAXIMUM RATINGS

PWR, PS to GND .....-0.3V to +85V
OUTA, OUTB, BP, RETRY to GND .....-0.3V to +85V
BP to PS .....-0.3V to +85V
BP to PWR .....-85V to +85V
OUTA, OUTB to PS.....-40V to +85V
SENSEA, SENSEB to PS.....-1V to +0.3V
SENSEA, SENSEB, CL, CB, OR to GND .....-0.3V to +85V
SENSEA, SENSEB to CL, CB, OR .....-5V to +5V
CL, CB, OR to PS .....-1V to +0.3V
GATE1A, GATE2A, GATE1B, GATE2B, GATEPS, GATEOR to GND .....-0.3V to +85V
GATE1A, GATE2A to OUTA .....-0.3V to +8V
GATE1B, GATE2B to OUTB .....-0.3V to +8V
GATEPS to PS .....-0.3V to +8V
GATEOR to PWR .....-0.3V to +8V
$\overline{FAULTA}$, $\overline{FAULTB}$ to GND.....-0.3V to +85V
ONA, ONB, FOSO, TCL, TCB to GND.....-0.3V to the lesser of +85V or (V_{BP} + 0.3V)
TCL, TCB to GND.....-0.3V to (V_{PS} + 0.3V)
ENX, ENY, ENZ to GND.....-0.3V to +85V
Continuous Power Dissipation
40-Pin TQFN (derate 37mW/°C above +70°C) 2963mW
Thermal Resistance (Note 1)
θ_{JA}.....28°C/W
θ_{JC}.....1°C/W
Operating Temperature Range.....0°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PS} = V_{PWR} = 12V, V_{FOSO} = 0, V_{ENX} = V_{ENY} = V_{ENZ} = V_{PWR}, and T_A = T_J = 0°C to +85°C, unless otherwise noted. See the *Typical Operating Circuit* for connections. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PS Voltage Range	V_{PS}		7.5		76	V
PS Supply Current	I_{PS}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}, V_{ONA} = V_{ONB} = 3V, no load		4.5	7	mA
PWR Voltage Range	V_{PWR}		7.5		76	V
PWR Supply Current	I_{PWR}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}, V_{ONA} = V_{ONB} = 3V, no load		400	600	µA
PWR Shutdown Current	I_{PWR_SHDN}	7.5V ≤ V_{PWR} ≤ 12V, V_{ENX} = V_{ENY} = V_{ENZ} = 0.4V, PS is open		5	10	µA
		12V ≤ V_{PWR} ≤ 76V, V_{ENX} = V_{ENY} = V_{ENZ} = 0.4V, PS is open		12	24	
PWR Standby Current	I_{PWR_SB}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}, V_{ENX} = V_{ENY} = V_{ENZ} = 0.4V		50	75	µA
PS Undervoltage Lockout Threshold	V_{PS_UVLO}	PS rising, V_{ENX} = V_{ENY} = V_{ENZ} = 0, V_{ONA} = V_{ONB} = V_{BP}	6.0	6.5	7.0	V
PS Undervoltage Lockout Hysteresis				0.35		V
PWR Undervoltage Lockout Threshold	V_{PWR_UVLO}	V_{PWR} rising, PS = GND, V_{ONA} = V_{ONB} = V_{BP}	6.0	6.5	7.0	V
PWR Undervoltage Lockout Hysteresis				0.35		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PS} = V_{PWR} = 12V, V_{FOSO} = 0, V_{ENX} = V_{ENY} = V_{ENZ} = V_{PWR}, and T_A = T_J = 0°C to +85°C, unless otherwise noted. See the *Typical Operating Circuit* for connections. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
ON_ Threshold	V_{ONTH}	$V_{ON\_}$ rising	1.150	1.240	1.350	V
ON_ Hysteresis	V_{ONTH_HYS}			70		mV
ON_ Input Bias Current	I_{ON}	$V_{ON\_}$ = 76V			1	µA
EN_ Input Logic-Low Voltage Threshold	V_{EN_L}				0.7	V
EN_ Input Logic-High Voltage Threshold	V_{EN_H}		1.8			V
EN_ Input Bias Current	$I_{EN\_}$	$V_{EN\_}$ = 76V, V_{FOSO} = 0			1	µA
RETRY Pulldown Current	I_{RTRY}	V_{RETRY} = 0.7V		20		µA
RETRY Input Logic-Low Voltage Threshold	V_{RTRYL}				0.7	V
RETRY Input Logic-High Voltage Threshold	V_{RTRYH}		1.8			V
FOSO Threshold	V_{FOSO_TH}	V_{ONA} or V_{ONB} = 3V	1.150	1.240	1.350	V
FOSO Hysteresis		V_{ONA} or V_{ONB} = 3V		70		mV
FOSO Input Leakage Current	I_{FOSOL}	V_{ENZ} = 0, V_{FOSO} = V_{PWR} = 76V			1	µA
TCL, TCB Input Bias Current in Shutdown	I_{TCL}, I_{TCB}	V_{ENZ} = 0, V_{PS} = 76V, V_{TCL} = V_{TCB} = 76V			4	µA
$\overline{FAULT}$_ Output Low Voltage	V_{OL}	Low-impedance state, $I_{\overline{FAULTA}}$ = $I_{\overline{FAULTB}}$ = 5mA		0.12	0.275	V
$\overline{FAULT}$_ Output High Leakage Current	I_{OH}	High-impedance state, $V_{\overline{FAULTA}}$ = $V_{\overline{FAULTB}}$ = 76V			1	µA
OUT_ Input Current	$I_{OUT\_}$	V_{ENZ} = 0, V_{PS} = 76V, V_{OUTA} = V_{OUTB} = 76.1V	15	50	100	µA
SENSE_ Input Current	$I_{SENSE\_}$	V_{ENZ} = 0, V_{PS} = V_{OR} = V_{CL} = V_{CB} = 76V, V_{SENSEA} = V_{SENSEB} = 76V	1		4	µA
CIRCUIT-BREAKER, CURRENT-LIMIT, AND ORING THRESHOLDS						
Circuit-Breaker Set Current	I_{CBSET}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	97.0	100.0	103.2	µA
Circuit-Breaker Comparator Offset Voltage		7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	-2.5		+2.5	mV
Current-Limit Set Current	I_{CLSET}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	97.0	100.0	103.2	µA
Current-Limit Comparator Offset Voltage		7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	-2.5		+2.5	mV
ORing Threshold Set Current	I_{ORSET}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	96.5	100	103.5	µA
ORing Threshold Set Current Hysteresis	I_{ORHYS}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}	47.5	50	52.5	µA

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

ELECTRICAL CHARACTERISTICS (continued)

(V_{PS} = V_{PWR} = 12V, V_{FOSO} = 0, V_{ENX} = V_{ENY} = V_{ENZ} = V_{PWR}, and T_A = T_J = 0°C to +85°C, unless otherwise noted. See the *Typical Operating Circuit* for connections. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ORing Threshold Comparator Offset Voltage		7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR} (Note 3)	-0.4	0	+0.4	mV
ORing Threshold Comparator Total Offset Voltage Supply Drift		7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}		100		µV
ORing Threshold Comparator Total Offset Temperature Drift		0°C ≤ T_A ≤ +85°C, V_{PS} = V_{PWR}		40		µV
Fast Pulldown Current-Limit Threshold Voltage	V_{THF}	7.5V ≤ V_{PWR} ≤ 76V, V_{PS} = V_{PWR}		V_{CL} + 57		mV
TIMING						
Circuit-Breaker Timeout	t_{CB}	R_{TCB} = 4kΩ (Note 4)	0.85	1.02	1.23	ms
Circuit-Breaker Default Timeout		V_{TCB} = V_{BP}	2.2	3.0	3.8	ms
Circuit-Breaker Timeout Count-Down/Count-Up Ratio				1		
Current-Limit Timeout	t_{CL}	R_{TCL} = 4kΩ (Note 4)	0.85	1.02	1.23	ms
Current-Limit Default Timeout		V_{TCL} = V_{BP}	0.85	1.02	1.23	ms
Current-Limit Timeout Count-Down/Count-Up Ratio				128		
Automatic Restart Delay after Current-Limit Timeout	t_{OFFCL}			t_{CL} x 128		ms
Automatic Restart Delay after Circuit-Breaker Timeout	t_{OFFCB}			t_{CB} x 128		ms
Channel A/Channel B FOSO Turn-On Delay	t_{FOSOF}	V_{ONA} = V_{ONB} = 3V, FOSO falling	0.4	1.0	1.5	s
ON_ Turn-On Response Time (Time from ON_ Pulled High to GATE_ Pulled High)	$t_{ON\_}$			2		ms
ON_ Turn-Off Response Time (Time from ON_ Pulled Low to GATE_ Pulled Low)	t_{ON_OFF}	$V_{ON\_}$ < V_{ONTH_HYST}, ($V_{GATE\_}$ - $V_{OUT\_}$) < 1V, GATE_A and GATE_B are open		10		µs
FOSO Turn-Off Response Time (Time from FOSO Rising Edge to GATE_ Pulled Low)	t_{FOSO_OFF}	(V_{GATE_A} - V_{OUTA}) < 1V, (V_{GATE_B} - V_{OUTB}) < 1V, GATE_A and GATE_B are open		0.34	0.60	µs
Minimum Delay from ENZ Low to Low-Current Shutdown Mode	t_{SHDN}	ENZ steps from 1.3V to 0.4V		50		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{PS} = V_{PWR} = 12V, V_{FOSO} = 0, V_{ENX} = V_{ENY} = V_{ENZ} = V_{PWR}, and T_A = T_J = 0°C to +85°C, unless otherwise noted. See the *Typical Operating Circuit* for connections. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE CONTROLS							
GATE_ Pullup Current	$I_{GU\_}$			35	48	60	µA
GATE_ High Voltage	V_{GATE1A}, V_{GATE2A}, V_{GATE1B}, V_{GATE2B}, V_{GATEPS}, V_{GATEOR}	V_{GATE1A} - V_{OUTA}, V_{GATE2A} - V_{OUTA}, V_{GATE1B} - V_{OUTB}, V_{GATE2B} - V_{OUTB}, V_{GATEPS} - V_{PS}, V_{GATEOR} - V_{PWR}	V_{PWR} = V_{PS} , 7.5V ≤ V_{PWR} ≤ 8V, V_{OUTA} = V_{OUTB} = V_{PS}	4.00	4.75	6.00	V
			V_{PWR} = V_{PS} , 8V ≤ V_{PWR} ≤ 76V, V_{OUTA} = V_{OUTB} = V_{PS}	4.50	5.50	6.50	
GATE_ Pulldown Current	I_{GDA1}, I_{GDA2}, I_{GDB1}, I_{GDB2}	V_{CL} < (V_{PS} - $V_{SENSE\_}$) < V_{THF}		350	500	650	µA
GATE_ Fast Pulldown Current	I_{GDFA1}, I_{GDFA2}, I_{GDFB1}, I_{GDFB2}	(V_{PS} - $V_{SENSE\_}$) > V_{THF}, $V_{GATE\_}$ = ($V_{OUT\_}$ + 4.5V)		40	125	190	mA
GATE_ Peak Pulldown Current	I_{GDPA1}, I_{GDPA2}, I_{GDPB1}, I_{GDPB2}	(V_{PS} - $V_{SENSE\_}$) = 1V			1.0		A
GATE_ Pulldown Current During Any GATE_ Turn-Off Condition	I_{GOFFA1}, I_{GOFFA2}, I_{GOFFB1}, I_{GOFFB2}	$V_{GATE\_}$ = ($V_{OUT\_}$ + 4.5V), V_{PS} > V_{PS_UVLO}		40	125	200	mA
		$V_{GATE\_}$ = ($V_{OUT\_}$ + 4.5V), V_{PS} = 6V		30		150	
GATEPS Pulldown Current	I_{GDPS}	V_{ENZ} = 0, V_{GATEPS} - V_{PS} = 4.5V		45	125	200	mA
GATEOR Turn-Off Switch On-Resistance	R_{GATEOR}	Measured between GATEOR and V_{PWR}, (V_{SENSEA} + V_{SENSEB})/2 > V_{OR}, V_{GATEOR} - V_{PWR} = 2V			2	3	Ω

Note 2: All min/max parameters are tested at T_A = +25°C and T_A = +85°C. Limits through the temperature range are guaranteed by design.

Note 3: This is the offset value immediately after initialization. The MAX5963 minimizes offset at startup according to the temperature at that time. After initialization the temperature offset voltage drift and supply voltage drift apply.

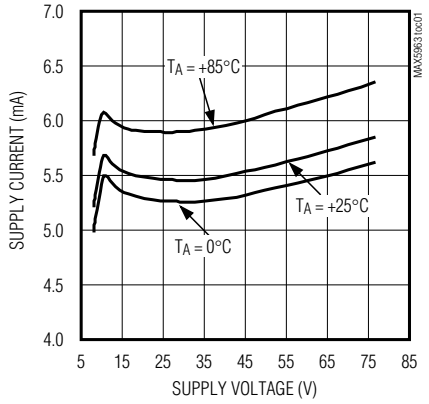
Note 4: Connect TCL/TCB to BP or PS for the default timeout period or connect a resistor from TCL/TCB to GND to program the current-limit timeout.

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

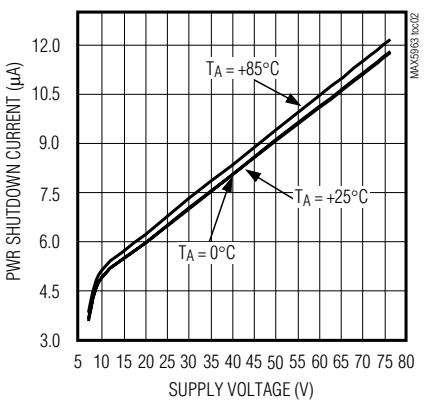
Typical Operating Characteristics

(V_{PS} = V_{PWR} = 12V, V_{GND} = V_{FOSO} = 0. T_A = +25°C, unless otherwise noted.)

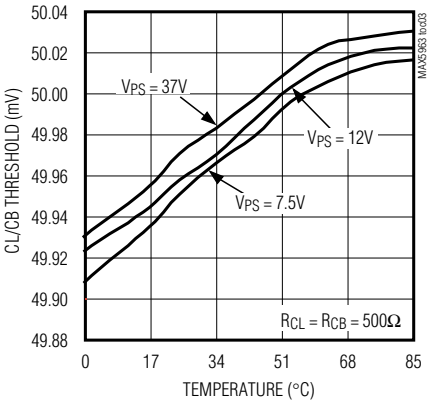
SUPPLY CURRENT vs. SUPPLY VOLTAGE



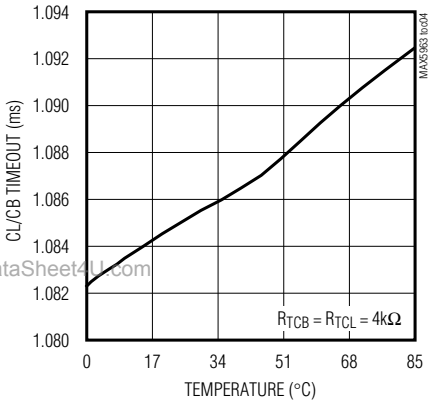
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



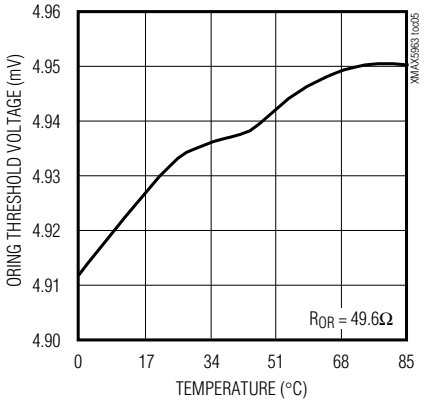
CURRENT-LIMIT/CIRCUIT-BREAKER THRESHOLD vs. TEMPERATURE



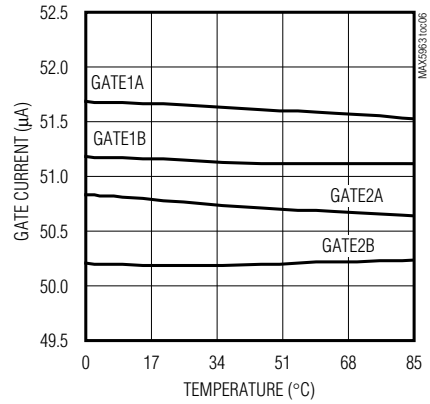
CURRENT-LIMIT/CIRCUIT-BREAKER TIMEOUT vs. TEMPERATURE



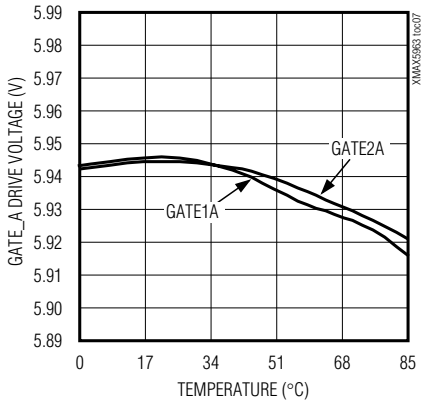
ORING THRESHOLD vs. TEMPERATURE



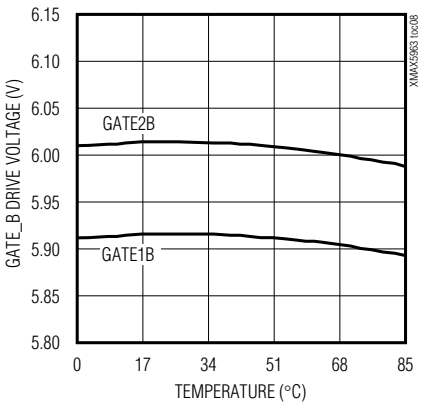
GATE CURRENTS vs. TEMPERATURE



GATE1A AND GATE2A DRIVE VOLTAGE vs. TEMPERATURE



GATE1B AND GATE2B DRIVE VOLTAGE vs. TEMPERATURE

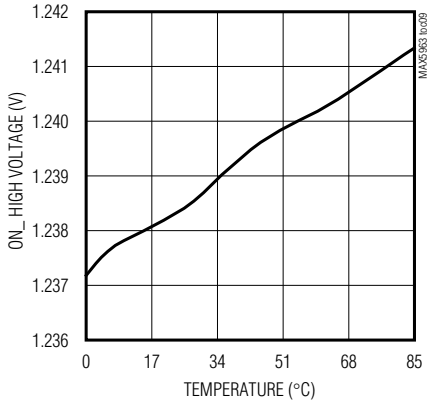


Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

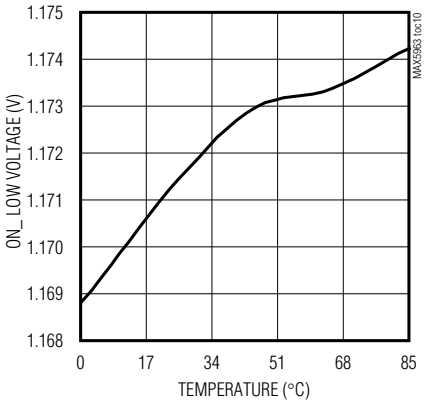
Typical Operating Characteristics (continued)

(V_{PS} = V_{PWR} = 12V, V_{GND} = V_{FOSO} = 0. T_A = +25°C, unless otherwise noted.)

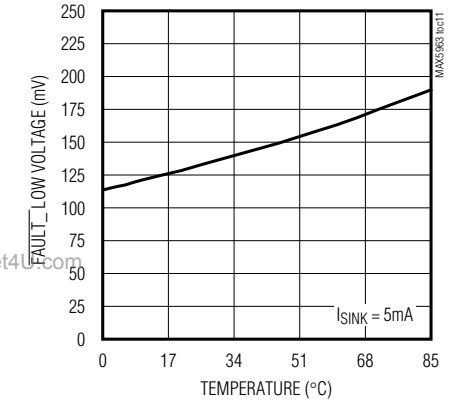
ON_ HIGH VOLTAGE vs. TEMPERATURE



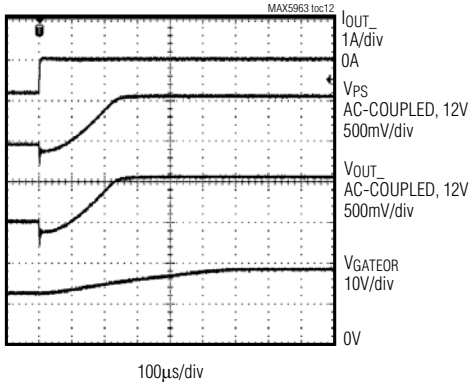
ON_ LOW VOLTAGE vs. TEMPERATURE



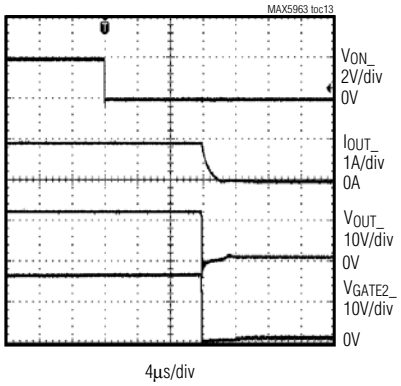
$\overline{\text{FAULT}}$_ LOW VOLTAGE vs. TEMPERATURE



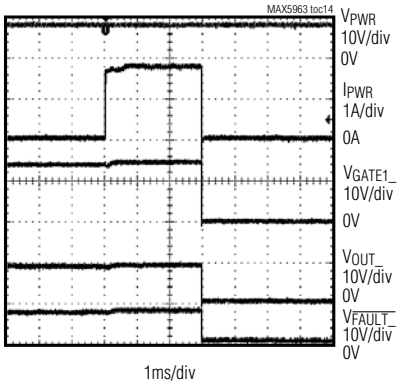
ORING THRESHOLD RESPONSE TIME



TURN-OFF RESPONSE TIME



CIRCUIT-BREAKER EVENT

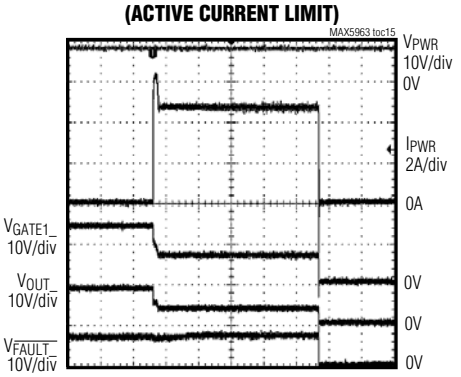


Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Typical Operating Characteristics (continued)

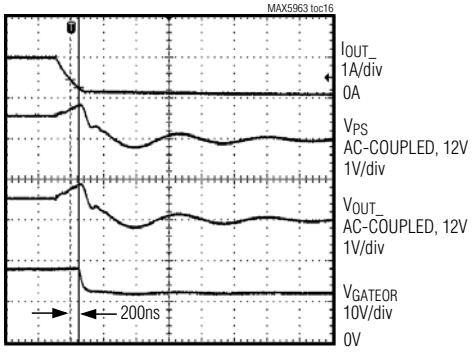
(V_{PS} = V_{PWR} = 12V, V_{GND} = V_{FOSO} = 0. T_A = +25°C, unless otherwise noted.)

SHORT-CIRCUIT EVENT (ACTIVE CURRENT LIMIT)



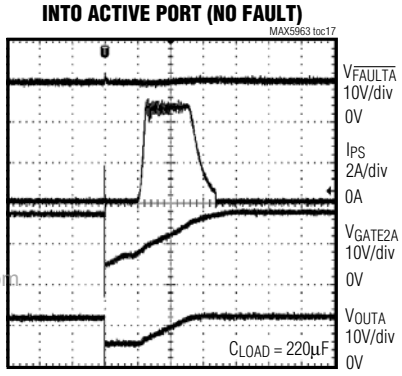
200µs/div

ORING SWITCHOVER WAVEFORM



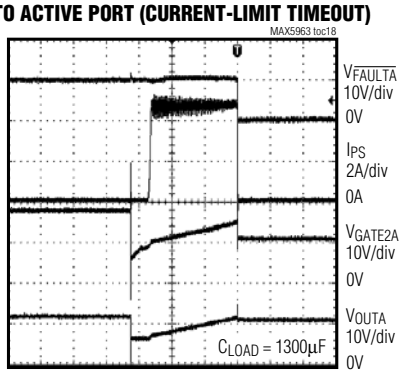
1µs/div

HOT PLUG-IN LOAD CAPACITANCE INTO ACTIVE PORT (NO FAULT)



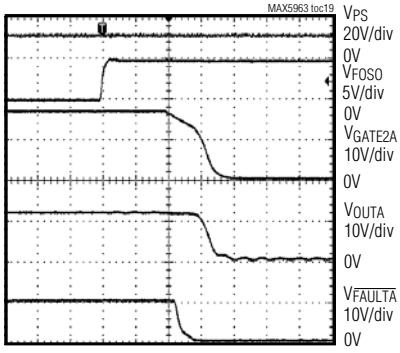
200µs/div

HOT PLUG-IN LOAD CAPACITANCE INTO ACTIVE PORT (CURRENT-LIMIT TIMEOUT)



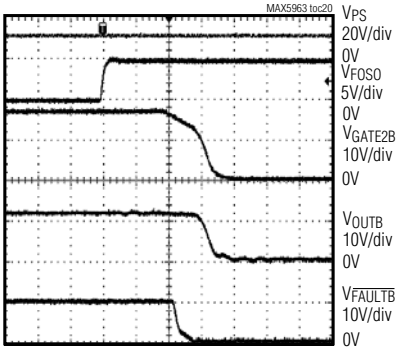
400µs/div

CHANNEL A FOSO TURN-OFF TIME



100ns/div

CHANNEL B FOSO TURN-OFF TIME



100ns/div

Pin Description

PIN	NAME	FUNCTION
1	PWR	System Power Input. Connect to the system power source. The MAX5963 draws less than 10µA of current from this input when GATEPS is off. Bypass PWR to GND with a 0.1µF ceramic capacitor.
2, 4, 6, 10, 11, 14, 16, 21, 25, 30, 39, 40	N.C.	No Connection. Not internally connected.
3	GATEOR	ORing MOSFET Gate-Drive Output. Referenced to PWR. GATEOR is a charge pump with a 50µA pullup current to 5.5V (typ) above V_{PWR} when active.
5	GATEPS	System Power MOSFET Gate-Drive Output. Referenced to PS. GATEPS is a charge pump with a 50µA pullup current to 5.5V (typ) above V_{PS} when active.
7	GATE2A	Channel A Current-Limiter Switch Gate-Drive Output 2. Referenced to OUTA. Connect GATE2A to the gate of the second n-channel MOSFET (see the *Typical Operating Circuit).* GATE2A is a charge pump with a 50µA pullup current to 5.5V (typ) above OUTA when active. GATE2A is identical to, but independent of, GATE1A.
8	OUTA	Channel A Output-Voltage Sense. Connect to the output.
9	GATE1A	Channel A Current-Limiter Switch Gate-Drive Output 1. Referenced to OUTA. Connect GATE1A to the gate of the first n-channel MOSFET (see the *Typical Operating Circuit).* GATE1A is a charge pump with a 50µA pullup current to 5.5V (typ) above OUTA when active. GATE1A is identical to, but independent of, GATE2A.
12	SENSEA	Channel A Current-Sense Negative Input. Connect the negative voltage-sensing terminal of a current-sense resistor, R_{SENSEA}, to SENSEA. Connect the positive voltage-sensing terminal of R_{SENSEA} to PS.
13	BP	Output of Diode OR Connection between PWR and PS. Bypass BP to GND with a 1µF capacitor.
15	PS	Power Priority Input. Connect to the source of the external QPS FET. The MAX5963 draws most of its power from PS whenever possible. Bypass PS to GND with a 0.1µF ceramic capacitor. Ensure that the bypass capacitance on PS is less than or equal to the bypass capacitance on PWR.
17	CB	Circuit-Breaker Threshold Programming Input. Connect a resistor from PS to CB to program the circuit-breaker threshold. A capacitor connected from CB to PS is recommended for impedance matching.
18	CL	Current-Limit Threshold Programming Input. Connect a resistor from PS to CL to program the current-limit threshold. A capacitor connected from CL to PS is recommended for impedance matching.
19	OR	ORing Threshold Programming Input. Connect a resistor from PS to OR to program the ORing current threshold. A capacitor connected from OR to PS is recommended for impedance matching.
20	SENSEB	Channel B Current-Sense Negative Input. Connect the negative voltage-sensing terminal of a current-sense resistor, R_{SENSEB}, to SENSEB. Connect the positive voltage-sensing terminal of R_{SENSEB} to PS.
22	GATE1B	Channel B Current-Limiter Switch Gate-Drive Output 1. Referenced to OUTB. Connect GATE1B to the gate of the 1st n-channel MOSFET (see the *Typical Operating Circuit).* GATE1B is a charge pump with a 50µA pullup current to 5.5V (typ) above OUTB when active. GATE1B is identical to, but independent of, GATE2B.
23	OUTB	Channel B Output-Voltage Sense. Connect to the output.

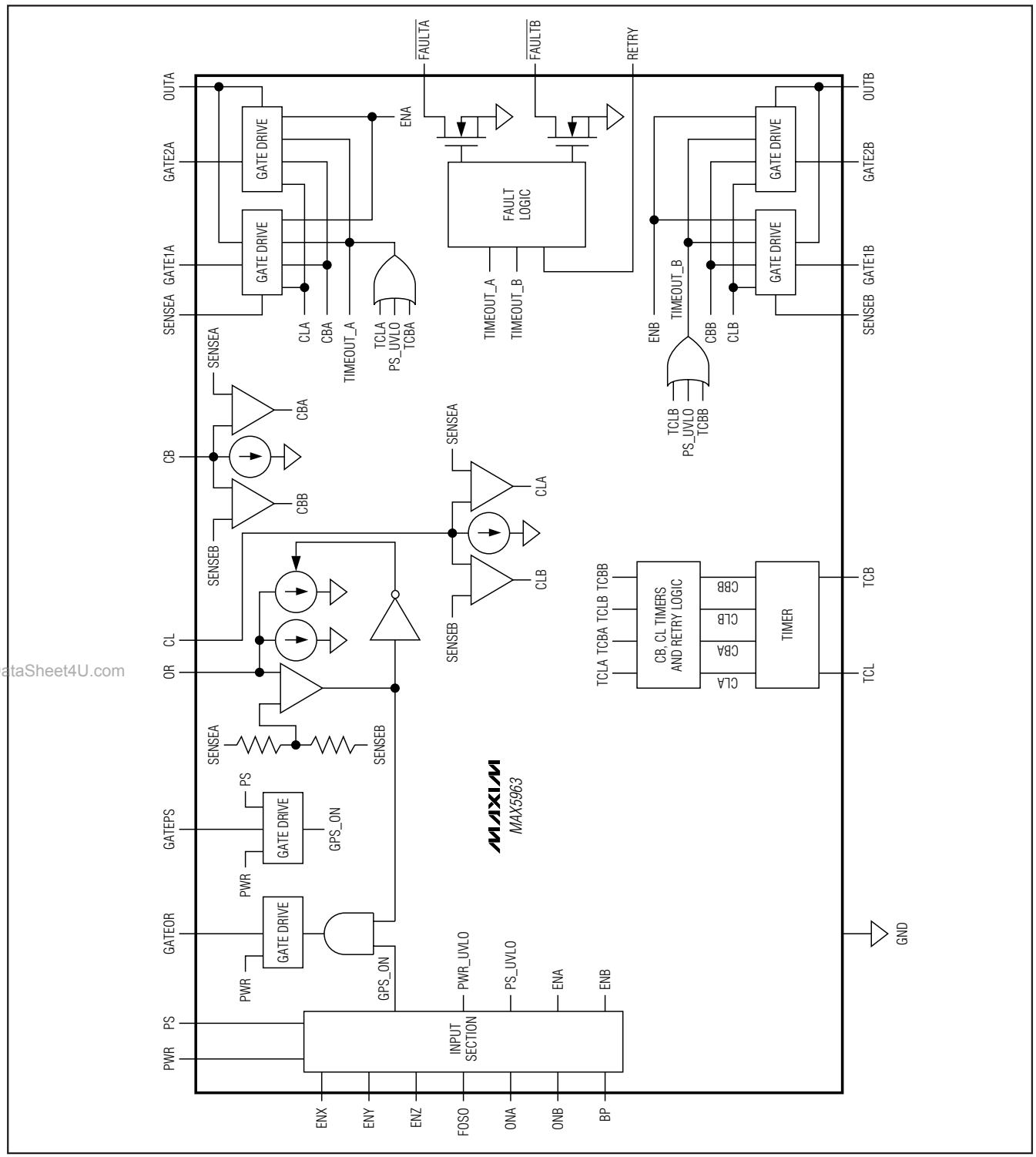
Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Pin Description (continued)

PIN	NAME	FUNCTION
24	GATE2B	Channel B Current-Limiter Switch Gate-Drive Output 2. Referenced to OUTB. Connect GATE2B to the gate of the second n-channel MOSFET (see the *Typical Operating Circuit).* GATE2B is a charge pump with a 50µA pullup current to 5.5V (typ) above OUTB when active. GATE2B is identical to, but independent of, GATE1B.
26	$\overline{\text{FAULTB}}$	Channel B Current-Fault Status Output. $\overline{\text{FAULTB}}$ is an open-drain output. $\overline{\text{FAULTB}}$ goes low after a current-limit or circuit-breaker fault on channel B has exceeded the current-limit or circuit-breaker timeout period (see the *Current-Fault Status Output ($\overline{\text{FAULT}}$_)* section).
27	$\overline{\text{FAULTA}}$	Channel A Current-Fault Status Output. $\overline{\text{FAULTA}}$ is an open-drain output. $\overline{\text{FAULTA}}$ goes low after a current-limit or circuit-breaker fault on channel A has exceeded the current-limit or circuit-breaker timeout period (see the *Current-Fault Status Output ($\overline{\text{FAULT}}$_)* section).
28	GND	Ground
29	RETRY	Latch or Autoretry Fault Management Selection Input. Internally pulled to ground. Connect RETRY to BP or PS for autorestart mode. Leave RETRY floating to select latchoff mode after a current-limit/circuit-breaker timeout.
31	TCL	Current-Limit Timer Programming Input. Connect TCL to BP or PS for the default timeout period or connect a resistor from TCL to GND to program the current-limit timeout.
32	TCB	Circuit-Breaker Timer Programming Input. Connect TCB to BP or PS for the default timeout period or connect a resistor from TCB to GND to program the circuit-breaker timeout.
33	ONB	Channel B On/Off Control Input. ONB sets the undervoltage lockout threshold for channel B and resets the channel after a fault latch. Drive ONB high (>1.24V (typ)) to turn on channel B. Drive ONB low to disable the channel. Connect a resistive-divider from PS to ONB and to GND to program the desired undervoltage lockout threshold for the channel.
34	ONA	Channel A On/Off Control Input. ONA sets the undervoltage lockout threshold for channel A and resets the channel after a fault latch. Drive ONA high (>1.24V (typ)) to turn on channel A. Drive ONA low to disable the channel. Connect a resistive-divider from PS to ONA and to GND to program the desired undervoltage lockout threshold for the channel.
35	FOSO	Fast-Off/Slow-On Logic Input. GATE1A, GATE2A, GATE1B, and GATE2B immediately pull low when FOSO exceeds the 1.24V (typ) threshold. The MAX5963 waits for the 1s (typ) turn-on delay once FOSO falls below the threshold hysteresis before allowing either channel to turn back on.
36	ENZ	Enable Z Logic Input. Pull ENZ up to PWR for logic-high. ENZ is a logic input that is ANDed with the OR combination of ENX and ENY. The output of this logic determines whether the MAX5963 goes into PWR shutdown mode. In PWR shutdown mode, the MAX5963 draws less than 10µA from PWR. However, if the logic combination of ENX, ENY, and ENZ is low, the chip can still be powered through either channel. See the *Power-Supply Enables (ENX, ENY, and ENZ)* section.
37	ENY	Logic-Enable Input Control GATEPS On/Off. Pull up to PWR for logic-high. See the *Power-Supply Enables (ENX, ENY, and ENZ)* section.
38	ENX	Logic-Enable Input Control GATEPS On/Off. Pull up to PWR for logic-high. See the *Power-Supply Enables (ENX, ENY, and ENZ)* section.
—	EP	Exposed Pad. Connect EP to the GND plane. EP functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

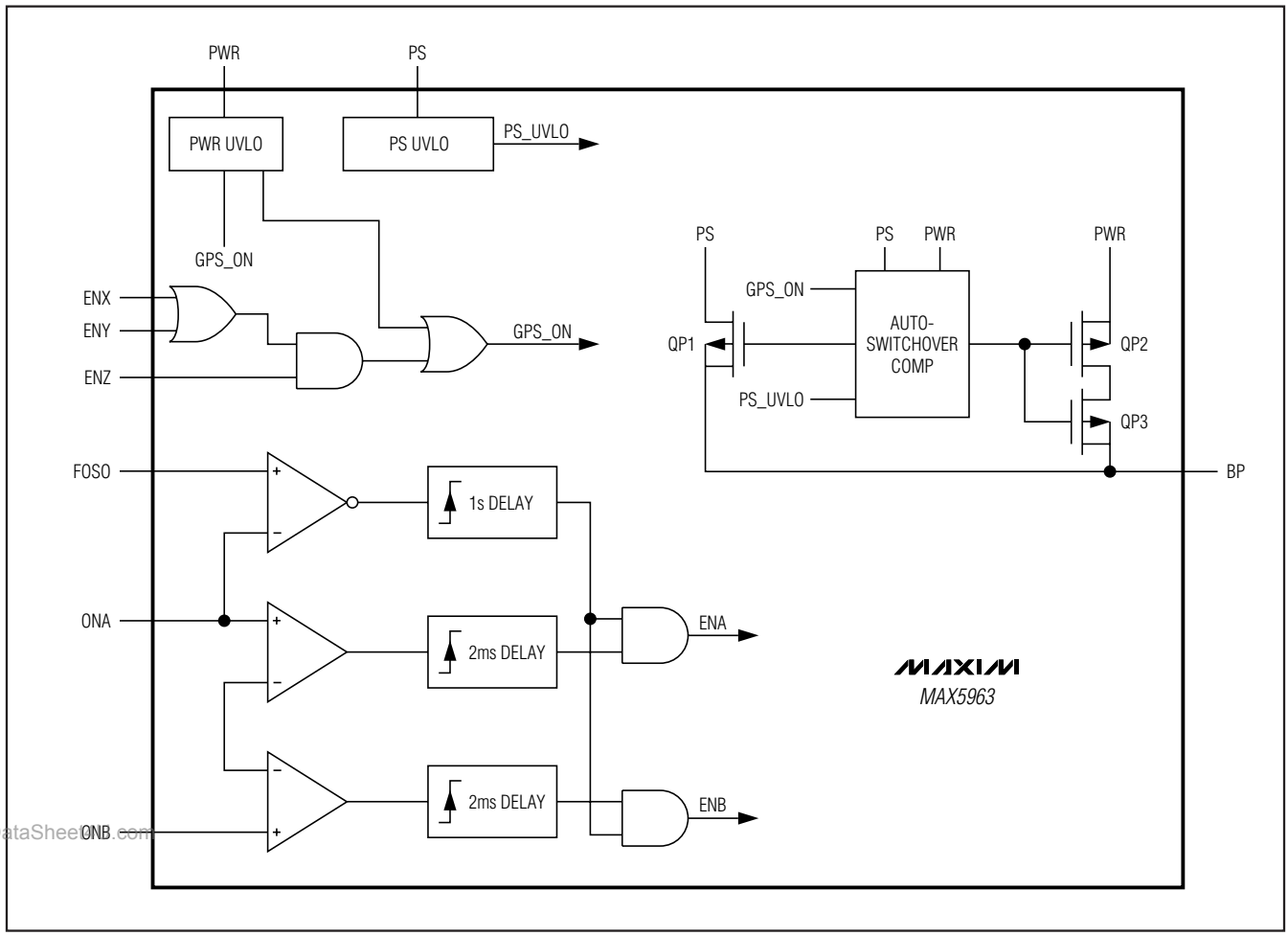
Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Functional Diagram



Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Functional Diagram (Input Section)



Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Detailed Description

The MAX5963 dual-channel, hot-swap controller IC performs hot-swapping, power-supply ORing, and current limiting for high availability systems. The MAX5963 incorporates six MOSFET drivers (GATEPS, GATEOR, GATE1_, and GATE2_) to control external n-channel power MOSFETs to perform low-voltage-drop power-supply ORing (GATEOR), hot-swapping, and current limiting from the input power supply to the load. A sense resistor provides accurate current limiting for each independent channel. GATE1_ and GATE2_ provide load disconnect to prevent current flow from PS to OUT_. GATEOR and GATEPS provide true load disconnect from PS to PWR.

The MAX5963 independent channels remain in low-current PWR shutdown mode when ENZ is low or when both ENX and ENY are low. Low-current shutdown mode disables the MAX5963 channels resulting in less than 10µA drawn from PWR. However, if the logic combination of ENX, ENY, and ENZ is low, the chip can still be powered through either channel.

When the input supply voltage (V_{PS}) is above the 6.5V (typ) PS_UVLO threshold, and $V_{ON\_}$ is above the 1.24V (typ) V_{ONTH} threshold, the MAX5963 channel turns on, sourcing 50µA (typ) current from GATE_, to enhance Q_ slowly. If the voltage across the current-sense resistor, $V_{SENSE\_}$, is greater than the current-limit threshold, the MAX5963 regulates the GATE_ voltage to limit the load current at the current-limit level so that $V_{SENSE\_}$ is equal to the current-limit threshold voltage, V_{CL}. In normal operation, $V_{SENSE\_}$ drops below V_{CL} and GATE_ rises to approximately 5.5V (typ) above OUT_.

If the channel continues to operate in current limit beyond the current-limit timeout (t_{CL}), the MAX5963 either latches off the channel or retries depending on the state of RETRY. If the voltage across the current-sense resistor, $V_{SENSE\_}$, is greater than the circuit-breaker threshold for longer than the circuit-breaker timeout (t_{CB}), the MAX5963 either latches off the channel or retries depending on the state of RETRY. See the *Current-Limit Timeout* and *Circuit-Breaker Timeout* sections for more information on setting TCL and TCB.

GATEOR controls the MAX5963 ORing function. Initially, GATEOR is off and the load current conducts through the body diode of QOR. GATEOR rises to 5.5V above V_{PWR} when (V_{SENSEA} + V_{SENSEB})/2 exceeds V_{OR_TH}, thereby enhancing QOR and reducing the voltage drop, power dissipation, and heat generation in the power-supply pathway. When a voltage greater than V_{PWR} is connected at OUTA or OUTB the higher voltage source provides current to the load(s). The MAX5963 turns off GATEOR rapidly upon $V_{SENSE\_}$ falling below the V_{OR} hysteresis, thus blocking the higher voltage from backdriving V_{PWR}. When the load current drops, causing $V_{SENSE\_}$ to fall below the hysteresis, GATEOR turns off.

Current Limiting

The MAX5963 limits the load current by monitoring the voltage across $R_{SENSE\_}$ and regulating the current to the load, ensuring that the voltage across the resistor is below the programmable current-limit threshold voltage (V_{CL}). Set the maximum current limit (I_{CL_LIMIT}) by placing the appropriate sense resistor between PS and SENSE_ and the appropriate current-limit threshold set resistor (R_{CL}) between CL and PS. When the load current is less than the maximum current limit, GATE_ rises to 5.5V (typ) above $V_{OUT\_}$ to fully enhance MOSFET Q1_ and Q2_. See the *Current-Limit Threshold* section for more information on setting the current-limit threshold.

When the load attempts to draw more current than I_{CL_LIMIT}, the MAX5963's GATE_ pulldown current ($I_{GD\_}$) regulates the current through Q1_ and Q2_, causing OUT_ to act as a constant current source. The output current is limited to I_{CL_LIMIT}. If the current-limit condition persists after the adjustable current-limit timeout period (t_{CL}) has expired, the GATE_ fast pulldown current ($I_{GDF\_}$) quickly turns off GATE_ to disconnect the load from the power supply. $\overline{FAULT\_}$ asserts low under these conditions (Figure 1).

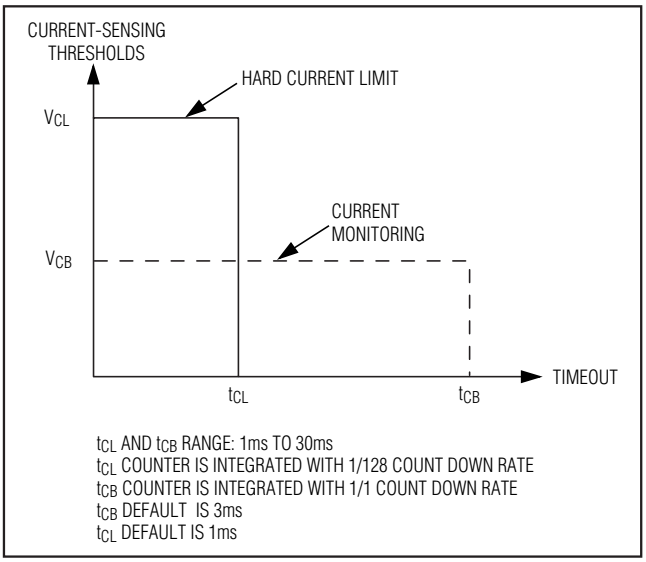


Figure 1. Bilevel Current-Limit/Circuit-Breaker Functionality

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

An external resistor connected to TCL and an internal 1/128 integrating counter determines the current-limit timeout. If the current-limit threshold is exceeded for more than roughly 100ns (comparator and logic delays), the timer counts up. Note that multiple consecutive overcurrent occurrences may cause the current-limit timer to trip (Figure 2).

During an output short-circuit event or a gross overload, the load current overshoots and causes $V_{SENSE\_}$ to exceed the fast pulldown current-limit threshold voltage (V_{THF}). The MAX5963 responds with much stronger GATE_ pulldown currents ($I_{GDP\_}$ and/or $I_{GDF\_}$) to quickly bring the load current back down to the programmed current limit.

In extreme cases where $V_{SENSE\_}$ is less than V_{PS} by more than 700mV (typ), the MAX5963 immediately pulls GATE1_ and GATE2_ low with a 1A (typ) peak pulldown current to disconnect the load from the power supply.

Following an overcurrent event, the gates of the external MOSFETs are held low (latched) if the device is in latchoff mode. Toggle ON_ to restart the device under these conditions. If RETRY is pulled high or connected to BP or PS, the device pulls the gates high again following the automatic restart delay t_{OFFCL}.

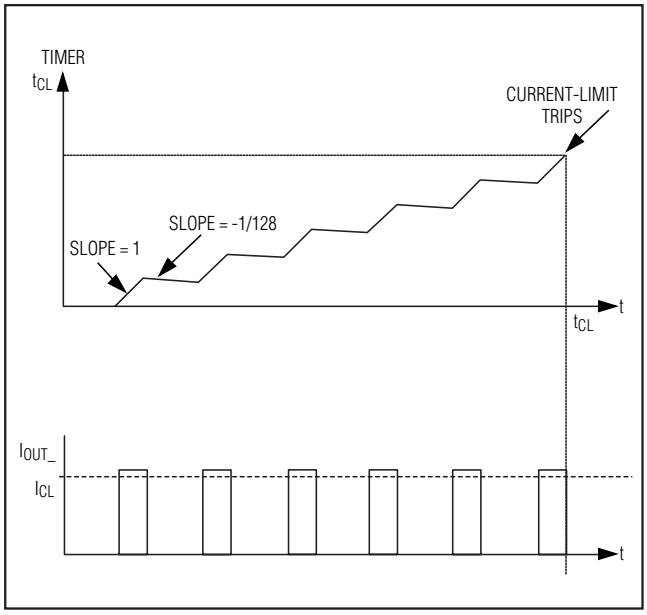


Figure 2: Current-Limit Timeout Following Consecutive Overcurrent Events

Current-Limit Threshold

The MAX5963 features adjustable current limits for channel A and channel B. Set the current-limit threshold voltage (V_{CL_TH}) for both channels by connecting a resistor, R_{CL}, from CL to PS. Calculate V_{CL_TH} using the following equation:

$$V_{CL\_TH} = I_{CLSET} \times R_{CL}$$

where I_{CLSET} is the 100µA (typ) current-limit set current shown in the *Electrical Characteristics* table.

Connect a sense resistor ($R_{SENSE\_}$) between PS and SENSE_ to set the individual current limits for channel A and channel B. Calculate the required sense resistor for each channel using the following equation:

$$R_{SENSE\_} = \frac{V_{CL\_TH}}{I_{CL\_LIMIT}}$$

where I_{CL_LIMIT} is the maximum channel current limit.

Current-Limit Timeout

The MAX5963 autoretry feature attempts to restart the device following the adjustable current-limit timeout, limiting the duty cycle of the MOSFETs under continuous fault conditions. The autoretry timeout is equal to 128 times the current-limit timeout:

$$t_{OFFCL}\ (ms) = 128 \times t_{CL}\ (ms)$$

Set the current-limit timeout from 1ms to 30ms by connecting a resistor between TCL and ground. See Figure 3 for resistor values and associated timeouts. Connect TCL to BP to select the 1ms (typ) default current-limit timeout.

Circuit Breaker

The MAX5963 features internal circuit-breaker circuitry that functions as a current monitor. Once the output current exceeds the circuit-breaker limit (I_{CB_LIMIT}), the circuit-breaker timer begins. When the circuit-breaker timeout (t_{CB}) is reached, GATE_ is pulled low and a fault condition is asserted (Figure 1).

An external resistor connected to TCB and an internal 1/1 integrating counter determines the circuit-breaker timeout. If the circuit-breaker threshold is exceeded for more than roughly 100ns (comparator and logic delays), the timer counts up. Note that multiple consecutive circuit-breaker overcurrent occurrences may cause the circuit-breaker timer to trip (Figure 4).

Following a circuit-breaker event, the gates of the external MOSFETs are held low (latched) if the device is in latchoff mode. If RETRY is pulled high or connected to BP, the device pulls the gates high again following the automatic restart delay t_{OFFCB}.

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Circuit-Breaker Threshold

The MAX5963 features adjustable circuit-breaker limits for channels A and B. Set the circuit-breaker threshold voltage (V_{CB_TH}) for both channels by connecting a resistor, R_{CB}, from CB to PS. Calculate V_{CB_TH} using the following equation:

$$V_{CB\_TH} = I_{CBSET} \times R_{CB}$$

where I_{CBSET} is the 100µA (typ) circuit-breaker set current shown in the *Electrical Characteristics* table.

A sense resistor ($R_{SENSE\_}$) between PS and SENSE_ sets the individual circuit-breaker limits for channels A and B. Calculate the circuit-breaker current limit (I_{CB_LIMIT}) for each channel using the following equation:

$$I_{CB\_LIMIT} = \frac{V_{CB\_TH}}{R_{SENSE\_}}$$

Circuit-Breaker Timeout

The MAX5963 autoretry feature attempts to restart after an adjustable circuit-breaker timeout. The autoretry timeout is equal to 128 times the circuit-breaker timeout:

$$t_{OFFCB}\ (ms) = 128 \times t_{CB}\ (ms)$$

Set the circuit-breaker timeout from 1ms to 30ms by connecting a resistor between TCB and ground. See Figure 3 for resistor values and associated timeouts. Connect TCB to BP to select the 3ms (typ) default circuit-breaker timeout.

Power-Supply ORing (GATEPS and GATEOR)

The MAX5963 controls two back-to-back n-channel power MOSFETs, QPS and QOR (see the *Typical Operating Circuit*), for system power-on/power-off control and ORing functionality. GATEPS is pulled high once V_{PWR} exceeds the UVLO threshold and a valid combination of EN_ inputs is received. Initially, GATEOR is off and the load current conducts through the body diode of QOR.

GATEOR rises to 5.5V above V_{PWR} when the voltage across the sense resistors (V_{SENSEA} + V_{SENSEB})/2 exceeds the ORing threshold, enhancing QOR. QOR's low $R_{DS(ON)}$ provides a very low voltage drop across its source to drain, which results in less power dissipation and heat generation in the power-supply path than a traditional diode.

Connect a resistor from OR to PS to set the ORing threshold (V_{OR_TH}). Calculate the ORing threshold using the following equation:

$$V_{OR\_TH} = R_{OR} \times I_{ORSET}$$

where I_{ORSET} is the 100µA (typ) ORing threshold set current, and R_{OR} is the resistance connected between OR and PS.

The MAX5963 continuously monitors the voltage drops across the sense resistors, V_{SENSEA} and V_{SENSEB}. QOR turns off rapidly when the voltage across the sense resistors decreases below the V_{OR} threshold minus its hysteresis. See Table 1.

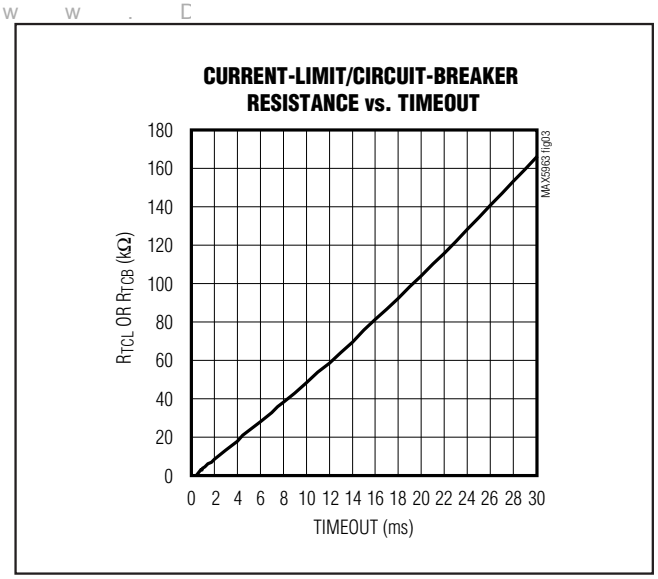


Figure 3: Current-Limit/Circuit-Breaker Timeout vs. R_{TCL} and R_{TCB} Resistor Values

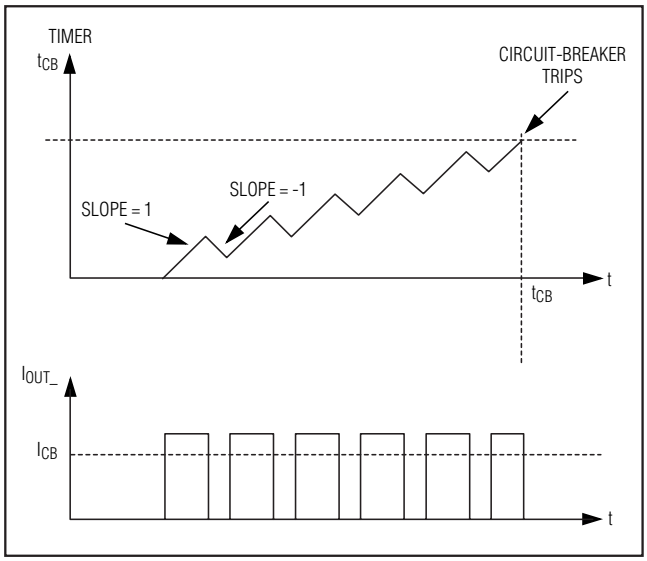


Figure 4: Circuit-Breaker Timeout Following Consecutive Overcurrent Events

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Table 1. ORing Protection Truth Table

INPUT	OUTPUT	DESCRIPTION
(V_{SENSEA} + V_{SENSEB})/2 > V_{OR}	GATEOR	
Yes	On	Normal operation. ORing MOSFET (QOR) is on to minimize power dissipation.
No	Off	ORing protection. ORing MOSFET (QOR) is off, preventing current flowing backward into the system's power supply, V_{PWR}.

Undervoltage Lockout

The MAX5963 dual-channel, independent current-limit switches have independent ON/OFF control. Both channels operate from 7.5V to 76V and have default 6.5V (typ) undervoltage lockout thresholds. The external MOSFETs remain off as long as V_{PS} < 6.5V or $V_{ON\_}$ < V_{ONTH}. The UVLO thresholds are programmable by connecting a resistive voltage-divider between ON_ and GND. When V_{PS} is greater than 7.5V and $V_{ON\_}$ exceeds the 1.24V (typ) threshold, GATE1_ and GATE2_ enhance to 5.5V, with respect to OUT_ and the MAX5963 switch goes into normal operation.

Calculate the resistor values to program the switches' individual turn-on threshold voltages using the following formula:

$$R_1 = \left(\frac{V_{TURN\_ON}}{1.24V} - 1\right) \times R_2$$

where V_{TURN_ON} is the desired turn-on voltage of channel A and/or B. R_1 and R_2 create a resistive divider from PS to ON_ (see the *Typical Operating Circuit*).

When operating the MAX5963, ON_ must remain above its 1.24V (typ) threshold. If $V_{ON\_}$ falls below the threshold and hysteresis for more than 10µs (typ), the power-supply MOSFETs turn off. This allows the power supply to disconnect from the load in the event of a fault condition such as shorting of the output to a different power-supply voltage or to a FireWire signal pin. If possible transient conditions exist that may exceed 10µs (typ) at the main power-supply line (PS), place an RC filter at ON_ to reject transient voltage dips to prevent unnecessary power-supply interruptions.

Current-Fault Status Output ($\overline{FAULT\_}$)

$\overline{FAULTA}$ and $\overline{FAULTB}$ are high-voltage, open-drain outputs that pull low when a current-limit or circuit-breaker fault shutdown has occurred. $\overline{FAULTA}$ and $\overline{FAULTB}$ remain low until the next startup cycle. $\overline{FAULTA}$ and $\overline{FAULTB}$ are capable of sinking up to 5mA when asserted.

Autoretry/Latchoff Fault Management

The MAX5963 autoretry feature attempts to restart after an adjustable current-limit or circuit-breaker timeout, limiting the duty cycle of the MOSFETs under continuous fault conditions. Connect RETRY to BP or PS for autorestart mode. Leave RETRY floating to select latchoff mode after a current-limit/circuit-breaker timeout.

$\overline{FAULT\_}$ deasserts every time a restart attempt is made.

Logic Inputs

Power-Supply Enables (ENX, ENY, and ENZ)

Three enable inputs, ENX, ENY, and ENZ, can be used to control power-on/power-off.

ENZ is a logic input that is ANDed with the OR combination of ENX and ENY. Apply a voltage greater than 1.8V (min) to ENZ to ensure that GATEPS is pulled high when V_{PWR} rises above the 6.5V (typ) PWR undervoltage lockout threshold.

Pull ENZ low to put the MAX5963 into PWR standby or shutdown mode. The MAX5963 draws less than 10µA from PWR in shutdown. See Table 2.

Table 2. Logic Input Truth Table

INPUT	OUTPUT	DESCRIPTION
(ENX OR ENY) AND ENZ	GATEPS	
L	Off	System Power-Off Mode. The MAX5963 draws < 10µA from PWR after [(ENX or ENY) and ENZ] goes low for more than t_{SHDN} time.
H	On	Enable System Power. The system power supply, V_{SUPPLY}, provides power to the FireWire ports.

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

The MAX5963 is capable of being powered through PWR or through channel A or B. Pull ENZ low and apply a voltage to either channel to power the device. In this mode, BP is powered by V_{PS} according to Table 3.

Fast-Off/Slow-On (FOSO) Protection

GATE1A, GATE2A, GATE1B, and GATE2B immediately pull low when FOSO exceeds the 1.24V (typ) threshold. The MAX5963 waits for the 1s (typ) turn-on delay once FOSO falls below the threshold hysteresis before allowing either channel to turn back on. See the *FireWire Power Management* section for more information.

Applications Information

Startup Considerations

Set the appropriate current-limit threshold for successful startup. A successful startup is dependent on the MAX5963 current-limit threshold and timeout period. A large capacitor at the output results in a charging current equivalent to the current-limit threshold and may cause the MAX5963 to exceed its 1ms (typ) default timeout period if the current-limit threshold is set too low. Use the following formula to compute the minimum current-limit setting:

$$I_{CL\_LIMIT} > \frac{C_{OUT} \times V_{PS}}{t_{CL}} + I_{LOAD}$$

where I_{CL_LIMIT} is the programmed current limit, C_{OUT} is the capacitor at OUT_, V_{PS} is the supply voltage, t_{CL} is the adjustable current-limit timeout period, and I_{LOAD} is the load current during startup. With V_{PS} = 12V, C_{OUT} = 220µF, t_{CL} = 1ms, and I_{LOAD} = 0, set the MAX5963 current limit greater than 2.6A. This calculation does not include tolerances.

Choosing $R_{SENSE\_}$

Select sense resistors, R_{SENSEA} and R_{SENSEB}, which cause the circuit-breaker voltage drop at a current-limit/circuit-breaker level above the maximum normal operating current. Typically, set the current limit at 1.2 to 1.5 times the nominal load current.

Choose the sense resistor power rating to accommodate a current-limit condition:

$$P_{SENSE\_} = (V_{CB\_TH})^2 / R_{SENSE\_}$$

where $P_{SENSE\_}$ is the power dissipated across $R_{SENSE\_}$ during a current-limit/circuit-breaker fault.

MOSFET Selection

Select external MOSFETs according to the application current level. The MOSFETs' on-resistance ($R_{DS(ON)}$) should be chosen low enough to have minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ also causes large output ripple if there is a pulsating load. Determine the device power rating to accommodate a short-circuit condition on the board, at startup, and when the device is in autoretry mode. During normal operation, the external MOSFETs dissipate little power. The power dissipated in normal operation is:

$$P = I_{LOAD}^2 \times R_{DS(ON)}$$

The most power dissipation occurs during a current-limit event, resulting in high power dissipated in Q_ during the current-limit period for the MAX5963. Calculate the power dissipated across Q_ during this period using the following equation:

$$P_{Q\_\_} = (V_{PS} - V_{SENSE\_}) \times I_{CL\_LIMIT}$$

where $V_{SENSE\_}$ is the voltage across the current-sense resistor, $R_{SENSE\_}$, V_{PS} is the input voltage and I_{CL_LIMIT} is the programmed current limit. Though there are two MOSFETs in series at the outputs, the safest assumption is that all of the current-limiting power dissipation occurs in one of the two MOSFETs; perfect sharing of the current-limit voltage drop is unlikely.

Table 3. BP Voltage in Standby Mode

PWR AND PS CONFIGURATION	ENZ	PS_UVLO	V_{BP} (V)
$V_{PS} > V_{PWR}$ - 0.1V	Low	High	V_{PS} - 0.7V
$V_{PS} > V_{PWR}$ - 0.1V	Low	Low	V_{PS}
$V_{PS} < V_{PWR}$ - 0.1V	Low	Low	V_{PS}
$V_{PS} < V_{PWR}$ - 0.1V	High*	Low	V_{PS}
$V_{PS} < V_{PWR}$ - 0.1V	High*	High	V_{PWR}

**ENX or ENY must be high to turn on GATEPS.*

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

FireWire Power Management

The MAX5963 is an excellent solution for FireWire port control and protection. In a two-port power-sourcing application, the MAX5963 can route system power to both ports, or it can allow either port to pass power to the other port, while blocking reverse current to the system power supply.

In these applications, it is important that no loads be placed on the PS node of the application circuit because V_{PS} is not protected against overcurrent faults. Loads should be placed at the port connections OUTA and OUTB instead, as shown in Figure 5.

The fast-off, slow-on input can be used to implement late VG protection for FireWire ports. In the event that a FireWire device makes connection with VP prior to VG, protection diodes in the load device can apply high voltage to the signal lines, damaging the host PHY. Connect the FOSO input as shown in Figure 5 to sense high voltage on the signal lines, and the MAX5963 immediately disconnects until VG is connected.

Transient Protection

If PS or OUT_ experiences a fast transient rise in voltage, the drain-to-gate overlap capacitance of GATE1_ and/or GATE2_ FETs may be sufficient to enhance both of the transistors, allowing current to flow. If the circuit is subjected to large transients, connect capacitors from the gate to source across the appropriate MOSFET to prevent the overlap capacitance from turning on the device. This causes the turn-off time of the FETs to increase due to the additional discharge of the capacitor. Use the minimum capacitor value that prevents reverse currents from flowing in hot-plug situations.

Table 4. FireWire Port Powering and Late V_G (FOSO) Protection Truth Table

INPUT			OUTPUT		DESCRIPTION
FOSO	ONA	ONB	GATE_A	GATE_B	
H	X	X	Off	Off	Late V_G event, all ports are off.
L	H	X	On	—	Enable port A power.
L	L	X	Off	—	Disable port A power.
L	X	H	—	On	Enable port B power.
L	X	L	—	Off	Disable port B power.
L	H	H	On	On	Enable port A, B power and power routing between the ports.

X = Don't care.

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

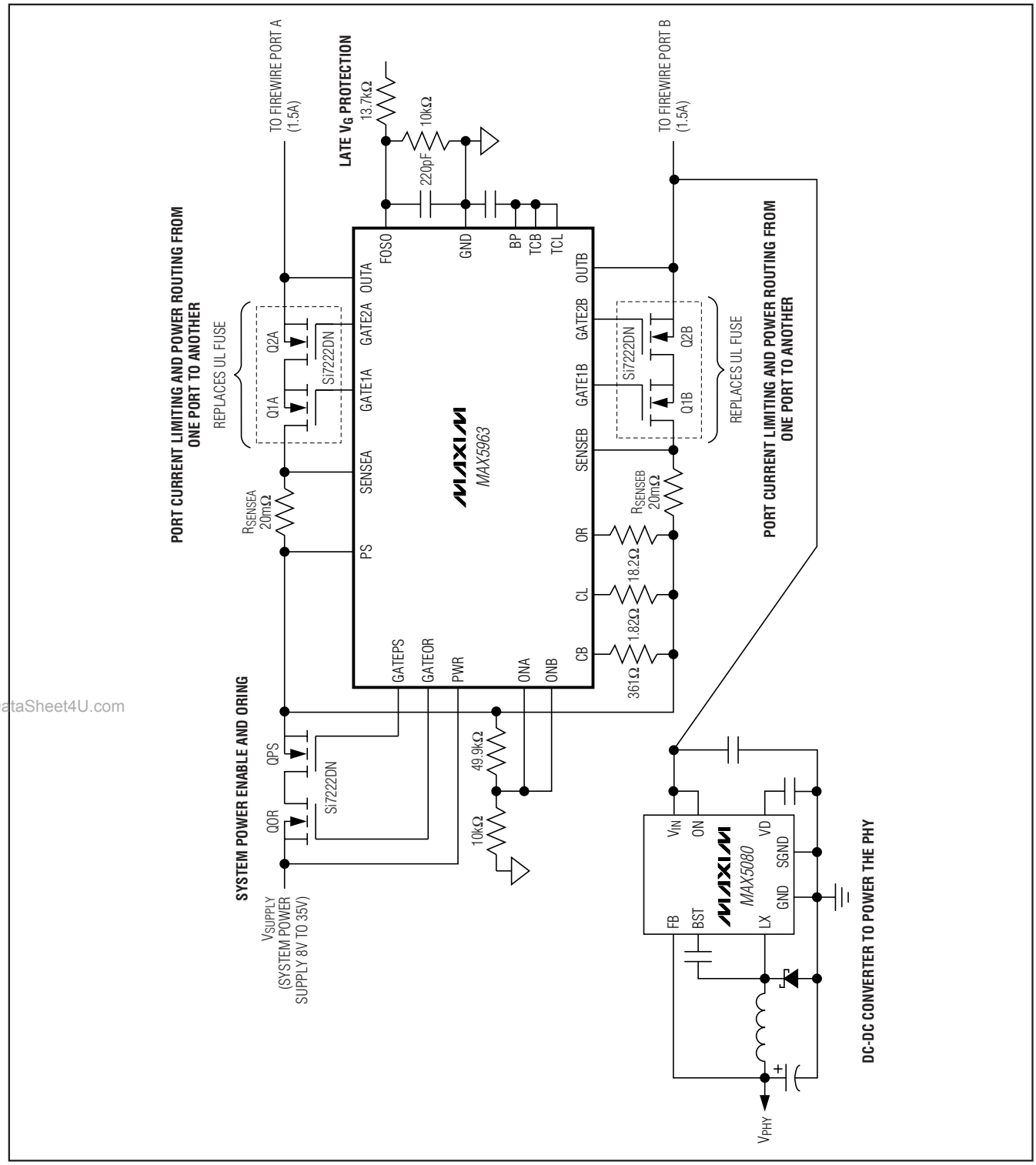
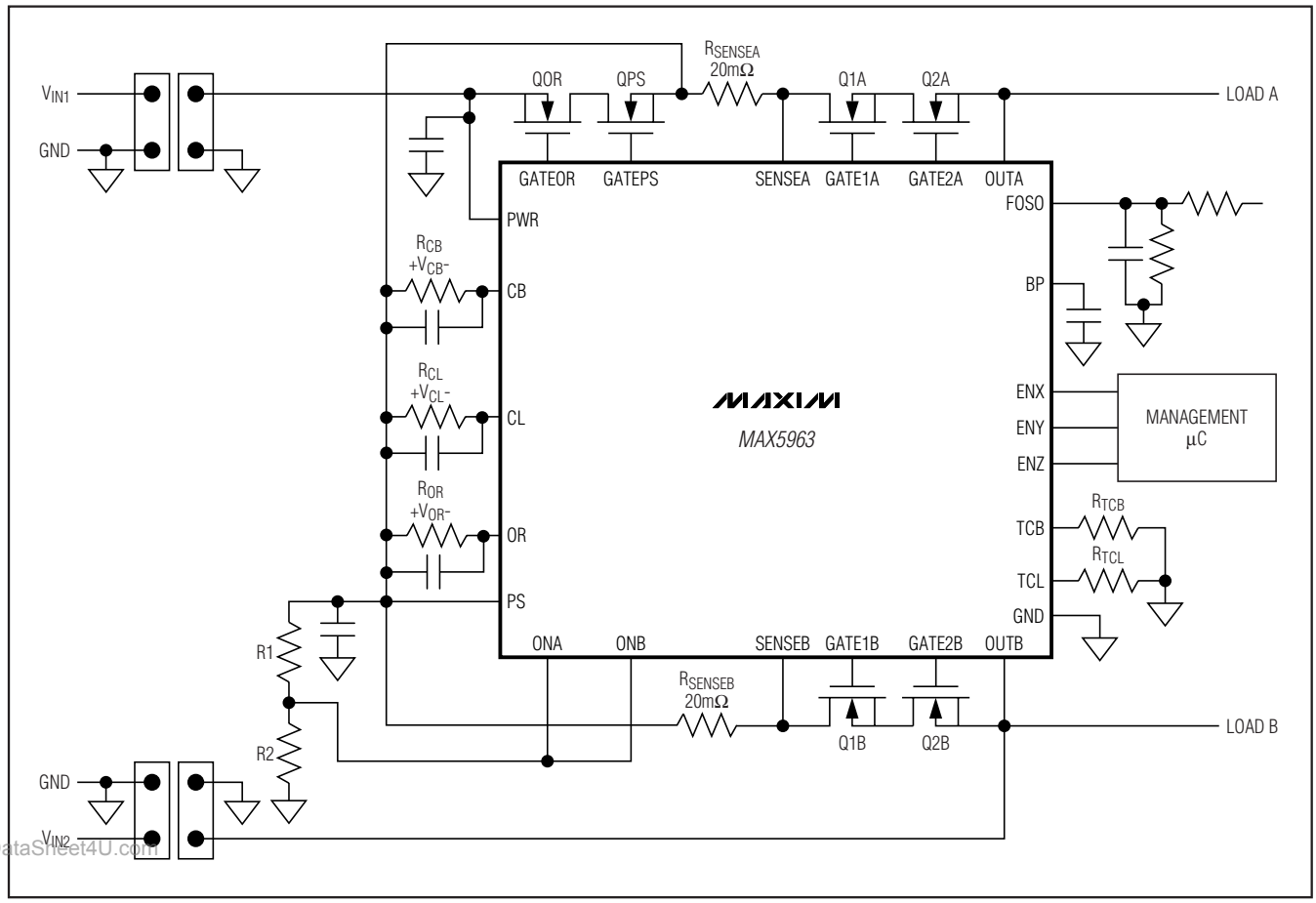


Figure 5. MAX5963 FireWire Application

Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller

Typical Operating Circuit



Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN-EP	T4066+5	21-0141