19-5115; Rev 1; 2/10

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

General Description

The MAX5968 soft-switch and ideal diode controller protects systems with redundant DC-DC converter modules against failure of the converter by controlling external n-channel MOSFETs at the input and output of the converter. Input short-circuit and overload current protection is provided by means of a current-sense amplifier connected to a sense resistor that resides at the source of the external protection MOSFET. If a failure occurs at the input of the associated converter, the MAX5968 protects the input supply by pulling the gate of the input protection MOSFET low and disconnecting the failed converter. Similarly, if there is a failure at the output of the redundant converter, the MAX5968 detects the reverse potential across the output MOSFET and pulls the gate low to disconnect the failed converter from the load. The MAX5968 features VariableSpeed/BiLevel™ input circuit-breaker protection.

The MAX5968 also integrates a 10-bit ADC that monitors converter input current, load voltage, and output MOSFET forward voltage. An analog input (ADCIN) is provided to monitor a temperature signal from the associated converter. The MAX5968 features two 10-bit circular buffers that contain a history of the 50 most recent input current and output load voltage digital conversion results. This data helps to diagnose and troubleshoot converter failures. All ADC results, including circular buffers and several configuration registers are accessible through a 400kHz I²C interface.

Digital limits for overvoltage and undervoltage warning are user programmable. An $\overline{\text{ALERT}}$ output notifies the system controller of any failure condition that arises or requires attention. When any of the measured signals violates digitally programmable limits, the $\overline{\text{ALERT}}$ output is asserted.

A precision ON comparator input can be used to implement programmable undervoltage lockout for the input and output MOSFET drivers.

An open-drain $\overline{\text{READY}}$ output can be used to enable the associated DC-DC converter by releasing the converter's enable input when both the input and output MOSFETs are fully enhanced.

Two general-purpose I/Os can be fully configured through the I²C interface to provide external indications or to control additional peripheral devices.

The MAX5968 is available in a 28-pin thin QFN package and operates over the -40°C to +125°C temperature range.

Features

- **10-Bit ADC for Temperature, Voltage, Output MOSFET Forward Voltage, and Input Current Monitoring**
- **Circular Buffers Store 50 Most Recent Voltage and Current Values for Fault Transient Analysis**
- **Input Circuit-Breaker Controller Drives External Low-Side n-Channel MOSFET**
- **Output Reverse-Current Protection Controller Drives Parallel External n-Channel MOSFETs**
- **Programmable VariableSpeed/BiLevel Fault Protection Provides Electronic Circuit-Breaker Function**
- **Internal 4A Pulldown Current for Fast Shutdown of the Circuit Breaker**
- **Internal 600mΩ Gate Drive for Fast On-Off Control of the ORing FETs**
- **Minimum- and Maximum-Value Detection Registers for All Digitized Signals**
- **Two GPIO Pins**
- **400kHz I²C Interface**
- **Small, 5mm x 5mm, 28-Pin TQFN Package**

Applications

Redundant DC-DC Converter Protection

Servers

High-Reliability Systems

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5968ATI+	-40°C to +125°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

ABSOLUTE MAXIMUM RATINGS

ADCIN, INM to AGND .....-0.3V to +60V
PWR to AGND .....-0.3V to +16V
$\overline{READY}$, $\overline{ALERT}$ to AGND ..... -0.3V to (V_{DD} + 0.3V)
V_{DD}, REG, SCL, SDA to AGND .....-0.3V to +6V
GOR to AGND .....-0.3V to (V_{REG} + 0.3V)
ON, GPS to AGND ..... -0.3V to (V_{PWR} + 0.3V)
OUT, DOR, SOR, CB+, CB-, A1, A0,
GPIO1, GPIO2 to AGND ..... -0.3V to (V_{DD} + 0.3V)
CB+ to CB -.....-1V to +1V
GPS to CB+.....-0.3V to +8V (internally clamped)
DOR to SOR .....-0.3V to +3.3V
PGND, DGND, OUTM to AGND.....-0.3V to +0.3V
SDA, $\overline{ALERT}$, $\overline{READY}$, GPIO1, GPIO2 Current ..-1mA to +100mA
Input/Output Current (all other pins)..... +20mA (Note 1)
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C)....2758.6mW
Thermal Resistance, θ_{JA} (Note 2).....29°C/W
Thermal Resistance, θ_{JC} (Note 2).....2°C/W
Operating Temperature Range..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: During GPS/GOR pulldown, GPS, GOR, REG, AGND, and PGND could carry 1.5A to 7A transient current for several microseconds.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PWR} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{PWR}		9		14	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on V_{PWR} to ensure operation, V_{PWR} rising	7.9	8.4	8.9	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{PWR} falling		500		mV
Supply Current	I_{PWR}	f_{SCL} = 400kHz		3.5	6	mA
REG Regulator Output Voltage	V_{REG}	With 5mA load	4.5	4.8	5.0	V
REG Undervoltage Lockout	V_{REGUV}			3.5		V
REG Undervoltage Lockout Hysteresis	V_{REGUV_HYS}			500		mV
V_{DD} Regulator Output Voltage	V_{DD}	With 5mA load	4.5	5	5.5	V
V_{DD} Power-On Reset	V_{POR}			3.5		V
V_{DD} Power-On Reset Hysteresis	V_{POR_HYS}			500		mV
Internal Oscillator Frequency	f_{INT}		3.6	4.0	4.4	MHz
ANALOG-TO-DIGITAL CONVERTER						
Resolution				10		Bits
Total Unadjusted Error					1	%FS
Integral Nonlinearity	INL			1		LSB
Differential Nonlinearity	DNL			1		LSB
Offset Error			-5		+5	LSB
DC Gain Error			-7		+7	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{PWR} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Total Monitoring Cycle Time				100		µs
ADCIN Input Full-Scale Voltage		Conversion = 1023, LSB = 4.88mV		5		V
ADCIN Measurement Accuracy			-7		+7	LSB
ADCIN Input Resistance		ADCIN to INM	300	500	700	kΩ
OUT Full-Scale Voltage		LV_range = 0, conversion = 1023, LSB = 1.955mV		2		V
		LV_range = 1, conversion = 1023, LSB = 3.910mV		4		
OUT Leakage Current	I_{OUT}	V_{OUT} = 2.0V	10	25	40	µA
		V_{OUT} = 4.0V	50	100	150	
OUTM Leakage Current	I_{OUTM}	V_{OUT} = 4.0V, V_{OUTM} = 0V	-150	-100	-50	µA
		V_{OUT} = 2.0V, V_{OUTM} = 0V	-40	-25	-10	
OUT Measurement Accuracy		LV_range = 0	-7		+7	LSB
		LV_range = 1	-7		+7	
V_{CB+} - V_{CB-} Full-Scale Voltage		At code = 1023		40		mV
		At code = 0		-10		
Input Bias Current	I_{CB+}	V_{CB+} = 40mV, V_{CB-} = 0V		5	2	µA
	I_{CB-}	V_{CB+} = 40mV, V_{CB-} = 0V		5	2	
Input Current Measurement Accuracy		V_{CB+} = 0V, V_{CB-} = 0V, T_A = -40°C to +25°C	-1.2		+1.2	mV
		V_{CB+} = 0V, V_{CB-} = 0V, T_A = +25°C to +125°C	-0.6		+0.6	
		V_{CB-} = 0V, V_{CB+} = 5mV	-1.2		+1.2	
		V_{CB-} = 0V, V_{CB+} = 20mV	-1.2		+1.2	
V_{DOR} - V_{SOR} Range Voltage		At code = 1023		-40		mV
		At code = 0		10		
V_{DOR} - V_{SOR} Measurement Accuracy		V_{SOR} = 0V, V_{DOR} = -20mV	-1.2		+1.2	mV
		V_{SOR} = 0V, V_{DOR} = -5mV	-1.2		+1.2	
SOR Input Bias Current	I_{SOR}	V_{SOR} = 0mV, V_{DOR} = -40mV		2	5	µA
DOR Input Bias Current	I_{DOR}	V_{SOR} = 0mV, V_{DOR} = -40mV		2	5	µA
INPUT CIRCUIT-BREAKER PROTECTION						
Fast Comparator Threshold Full Scale		Code = 255		40		mV
Circuit-Breaker Accuracy (Slow Comparator)	V_{OS,CB_S}	V_{CB-} = 0V, code = 191 or 15mV (typ) input referred, full scale = 200%	-2.7		+2.7	mV
		V_{CB-} = 0V, code = 102 or 8mV (typ) input referred, full scale = 200%	-2.7		+2.7	

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

ELECTRICAL CHARACTERISTICS (continued)

(V_{PWR} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

Circuit-Breaker Accuracy (Fast Comparator)	V_{OS,CB_F}	V_{CB-} = 0V, code = 191 or 30mV (typ) input referred, full scale = 200%	-1.5		+1.5	mV
		V_{CB-} = 0V, code = 102 or 16mV (typ) input referred, full scale = 200%	-1.0		+1.0	
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Fast Comparator Threshold Programming Resolution		DAC resolution		8		Bits
Slow Circuit-Breaker Response Time	t_{SCD}	V_{CB+} - V_{CB-} = $V_{TH,SC}$ + 2mV		2.4		ms
		V_{CB+} - V_{CB-} = $V_{TH,SC}$ + 4mV		1.2		
Fast Circuit-Breaker Response Time	t_{FCD}	V_{CB+} - V_{CB-} = $V_{TH,FC}$ + 10mV		0.1		µs
OUTPUT REVERSE-CURRENT PROTECTION						
Reverse-Current Detection Threshold	V_{RCD}	V_{DOR} relative to V_{SOR} (when GOR turns off)	2.9	4	4.9	mV
Forward-Current Detection Threshold	V_{FCD}	V_{DOR} relative to V_{SOR} (when GOR turns on)	1	2	3.5	mV
GOR Off Threshold Hysteresis	V_{HCD}			2		mV
Reverse-Current Blocking Response Time	t_{RCD}	V_{DOR} - V_{SOR} = V_{RCD} + 1mV, C_{GOR} = 10nF		2		µs
		V_{DOR} - V_{SOR} = V_{RCD} + 10mV, C_{GOR} = 10nF		100		ns
OUTPUT UNDERVOLTAGE FAST COMPARATOR (OUT)						
OUT UV Comparator Threshold	$V_{THUVDAC}$	LV_range = 0, code = 127	0.79	0.8	0.81	V
		LV_range = 1, code = 127	1.58	1.6	1.62	
OUT UV Comparator Threshold Programming Resolution		DAC resolution		8		Bits
OUT UV Comparator Propagation Delay	t_{OUT}	With 10mV overdrive		100		ns
ON COMPARATOR INPUT (ON)						
ON Input Threshold	V_{THON}	Rising	1.209	1.228	1.246	V
ON Input Hysteresis		Falling		62.5		mV
ON Input Current	I_{ON}		-1		+1	µA
INPUT MOSFET GATE DRIVE (GPS)						
GPS High Voltage	V_{GPSH}	Relative to AGND	6.5	8	9.6	V
GPS High Comparator Threshold	V_{THGPS}	V_{GPS} - V_{CB+}	4.9	5	5.1	V
GPS Pullup Current	I_{GPSUP}	V_{GPS} is 1V below V_{GPSH}	45	50	55	µA
GPS Pulldown Current	I_{GPSDN}	V_{GPS} = 2V		1.5		A
GPS Pulldown Resistance	R_{DGPS}				2.5	Ω
OUTPUT MOSFET GATE DRIVE (GOR)						
GOR High Voltage	V_{GORH}	Relative to AGND	4.5	4.8	5.0	V
GOR High Comparator Threshold	V_{THGOR}	V_{GOR} - V_{SOR}	2.9	3.0	3.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PWR} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GOR Pullup Resistance	R_{UGOR}				5	Ω
GOR Pulldown Resistance	R_{DGOR}				2.5	Ω
GOR Pullup Current	I_{GORUP}	V_{GOR} is 1V below V_{GORH}		2.5		A
GOR Pulldown Current	I_{GORDN}	V_{GOR} = 2V		7		A
OUTPUTS ($\overline{ALERT}$, $\overline{READY}$, GPIO_)						
$\overline{ALERT}$ Voltage Low		I_{SINK} = 5mA			0.4	V
$\overline{ALERT}$ Output Leakage (Open Drain)		$V_{\overline{ALERT}}$ = V_{DD}	-1		+1	µA
$\overline{READY}$ Voltage Low		I_{SINK} = 5mA			0.4	V
$\overline{READY}$ Output Leakage (Open Drain)		$V_{\overline{READY}}$ = V_{DD}	-1		+1	µA
GPIO_ Input Logic-High Threshold					1.4	V
GPIO_ Input Logic-Low Threshold			0.4			V
GPIO_ Voltage Low		I_{SINK} = 5mA			0.4	V
GPIO_ Weak Pullup Current	I_{WKPU}	$V_{GPIO\_}$ = 2V	-5	-10	-20	µA
I²C INTERFACE (SCL, SDA, A0, A1) (Figure 3)						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Pulse Width of Spike Suppressed	t_{SP}		50			ns
SDA, SCL Input Current		SDA is not in pulldown, V_{SCL} = V_{SDA} = 5.5V	-1		+1	µA
SDA, SCL Logic-Low					0.8	V
SDA, SCL Logic-High			1.6			V
SDA, SCL Input Capacitance				15		pF
SDA Voltage Low		I_{SINK} = 5mA			0.4	V
A0, A1 Low Voltage					0.4	V
A0, A1 High Voltage			1.4			V
A0, A1 Input Current		V_{A0} = V_{A1} = V_{DD}	-1		+1	µA

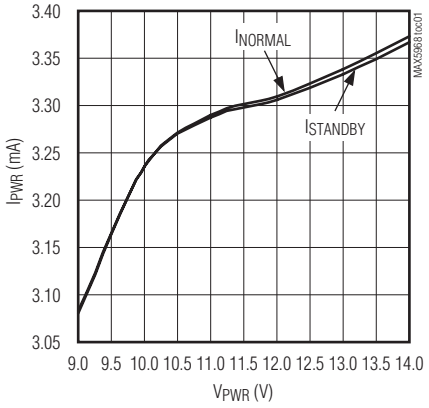
Note 3: All devices 100% production tested at T_A = +25°C and T_A = +125°C. Limits at T_A = -40°C are guaranteed by design.

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

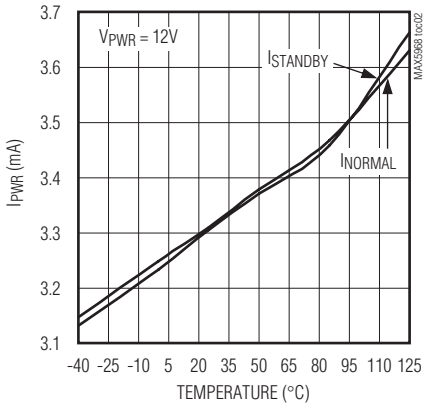
Typical Operating Characteristics

(V_{PWR} = 12V, T_A = +25°C, unless otherwise noted.)

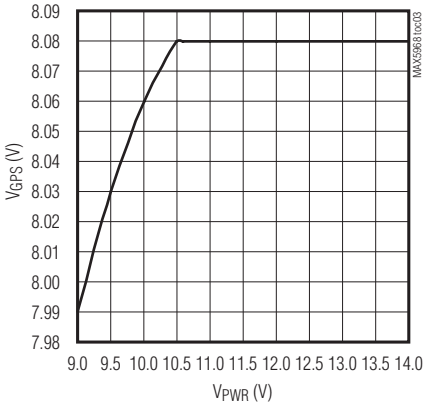
PWR CURRENT vs. PWR VOLTAGE



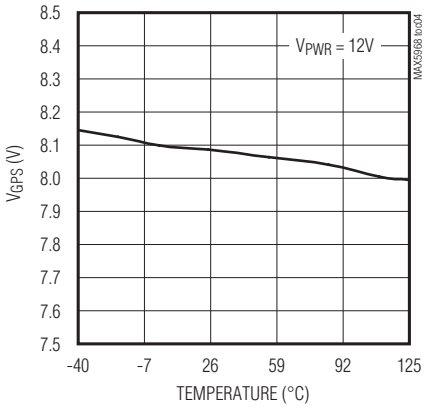
PWR CURRENT vs. TEMPERATURE



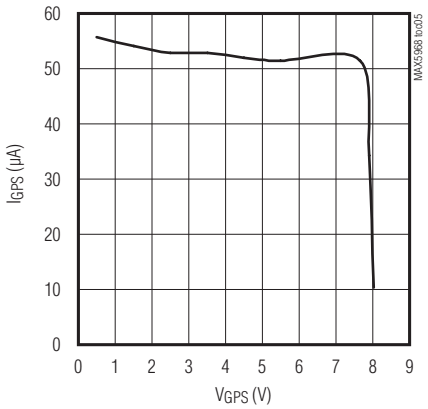
GPS VOLTAGE vs. PWR VOLTAGE



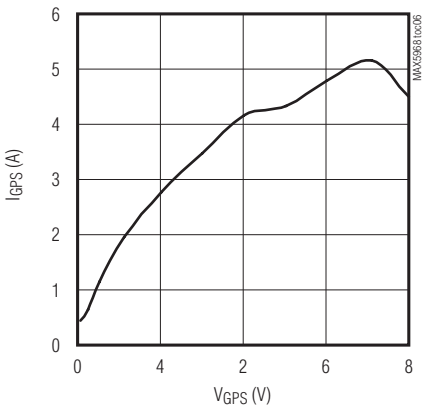
GPS VOLTAGE vs. TEMPERATURE



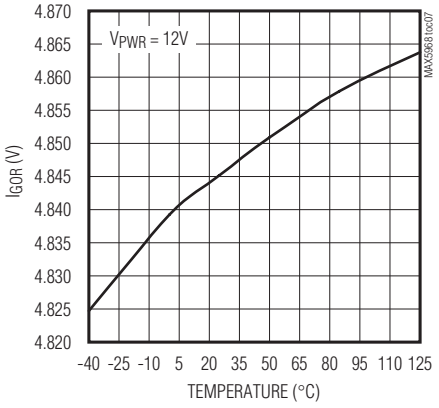
GPS DRIVE CURRENT vs. GPS VOLTAGE



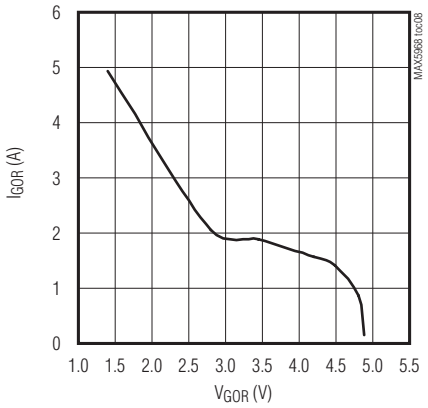
GPS DISCHARGE CURRENT vs. GPS VOLTAGE



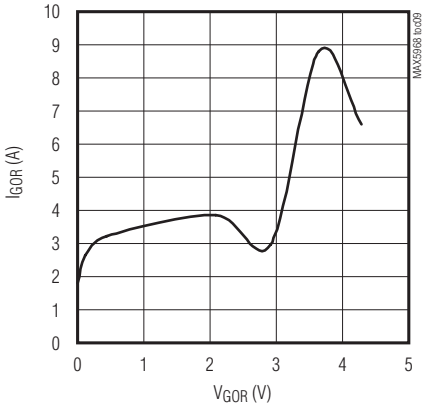
GOR VOLTAGE vs. TEMPERATURE



GOR DRIVE CURRENT vs. GOR VOLTAGE



GOR DISCHARGE CURRENT vs. GOR VOLTAGE

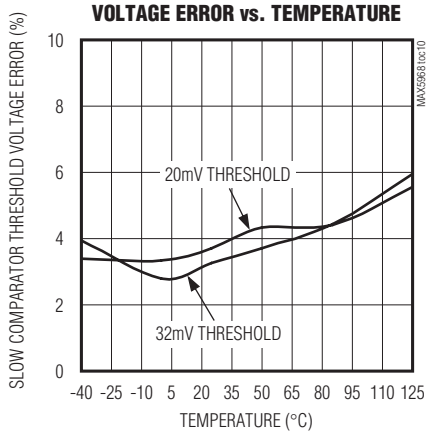


Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

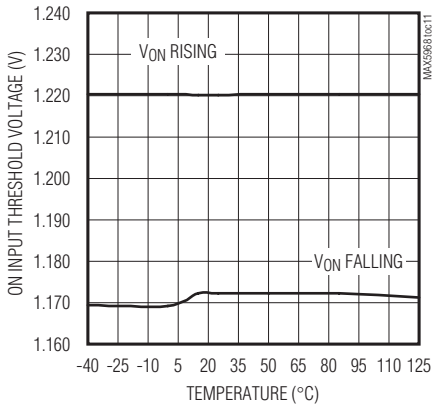
Typical Operating Characteristics (continued)

(V_{PWR} = 12V, T_A = +25°C, unless otherwise noted.)

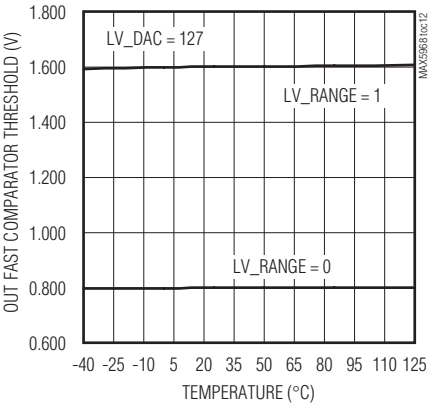
SLOW COMPARATOR THRESHOLD VOLTAGE ERROR vs. TEMPERATURE



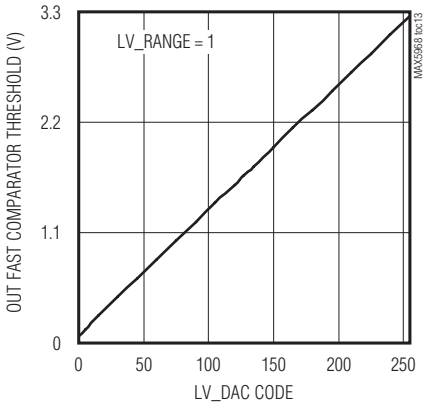
ON INPUT THRESHOLD VOLTAGE vs. TEMPERATURE



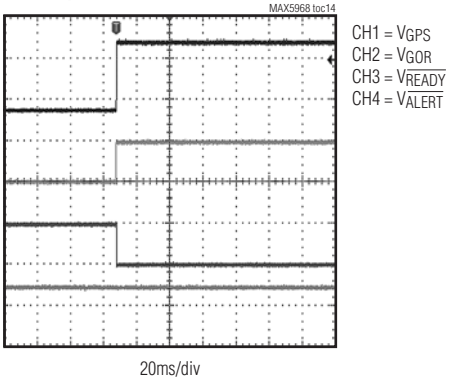
OUT FAST COMPARATOR THRESHOLD vs. TEMPERATURE



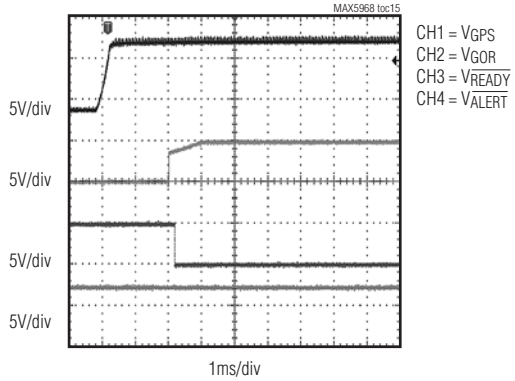
OUT FAST COMPARATOR THRESHOLD vs. LV_DAC CODE



STARTUP WAVEFORM (ON FROM LOW TO HIGH)



STARTUP WAVEFORM (PWR FROM 0V TO 16V)

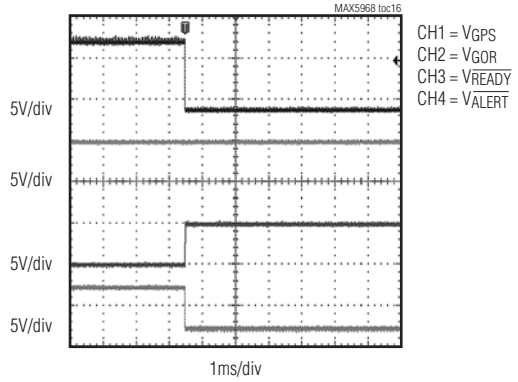


Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

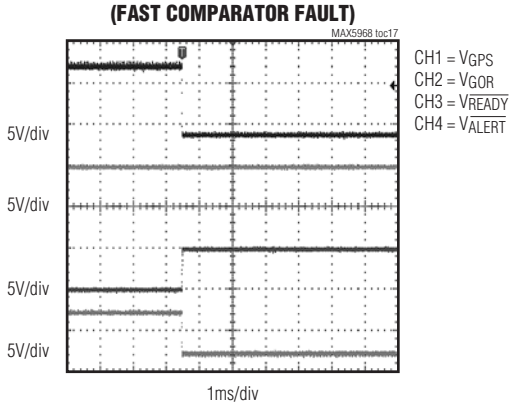
Typical Operating Characteristics (continued)

(V_{PWR} = 12V, T_A = +25°C, unless otherwise noted.)

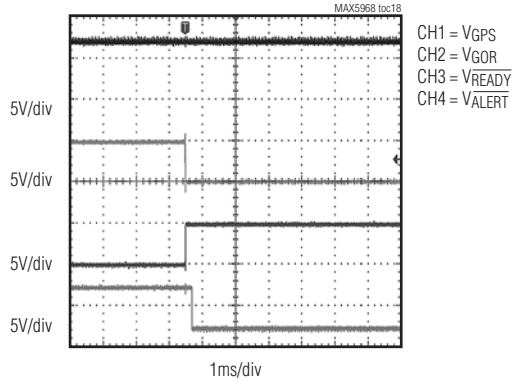
TURN-OFF WAVFORM (SLOW COMPARATOR FAULT)



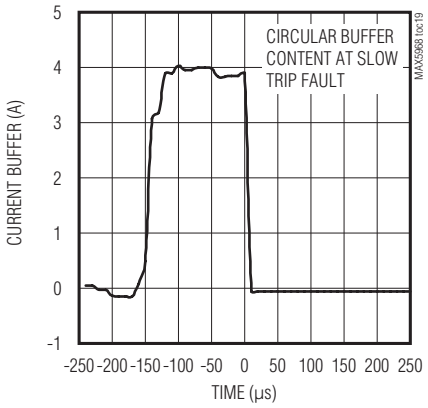
TURN-OFF WAVFORM (FAST COMPARATOR FAULT)



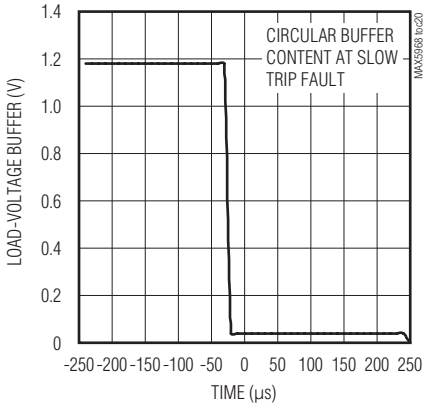
ORING FET OFF WAVEFORM



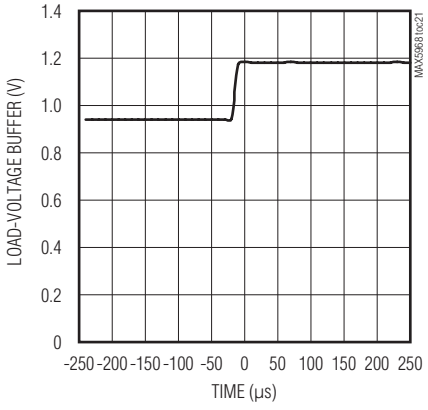
CURRENT BUFFER vs. TIME



LOAD-VOLTAGE BUFFER vs. TIME



REVERSE LOAD-VOLTAGE BUFFER vs. TIME

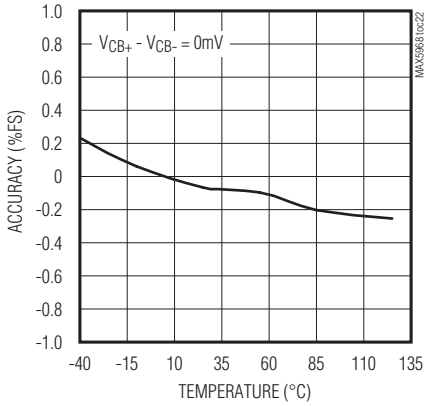


Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

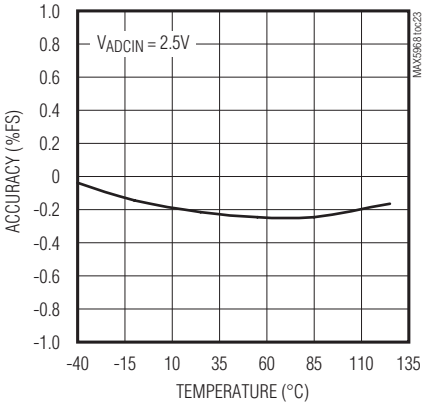
Typical Operating Characteristics (continued)

(V_{PWR} = 12V, T_A = +25°C, unless otherwise noted.)

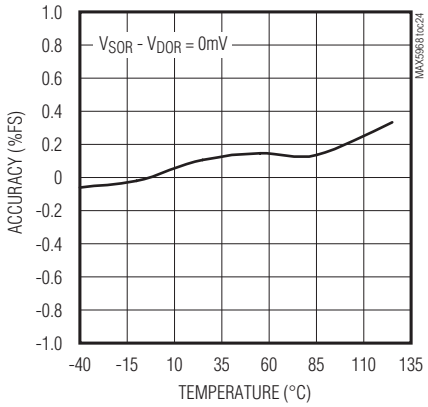
V_{CB+} - V_{CB-} ACCURACY vs. TEMPERATURE



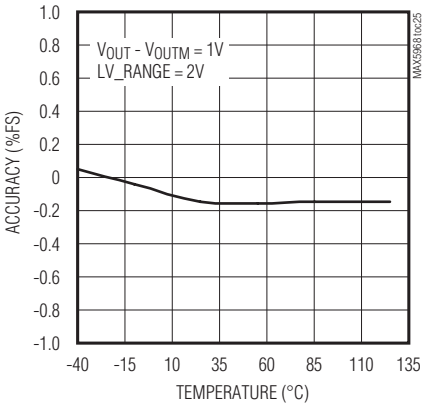
V_{ADCIN} - V_{INM} ACCURACY vs. TEMPERATURE



V_{SOR} - V_{DOR} ACCURACY vs. TEMPERATURE

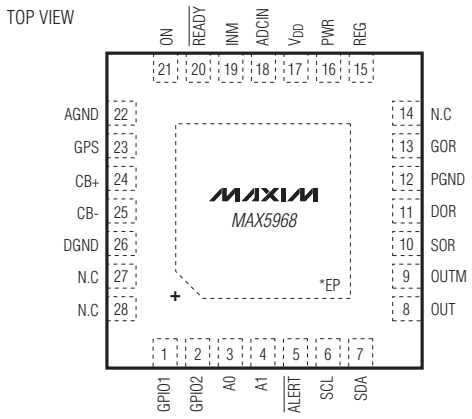


LOAD-VOLTAGE ACCURACY vs. TEMPERATURE



Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

Pin Configuration



TQFN

*CONNECT EXPOSED PAD TO GROUND.

Pin Description

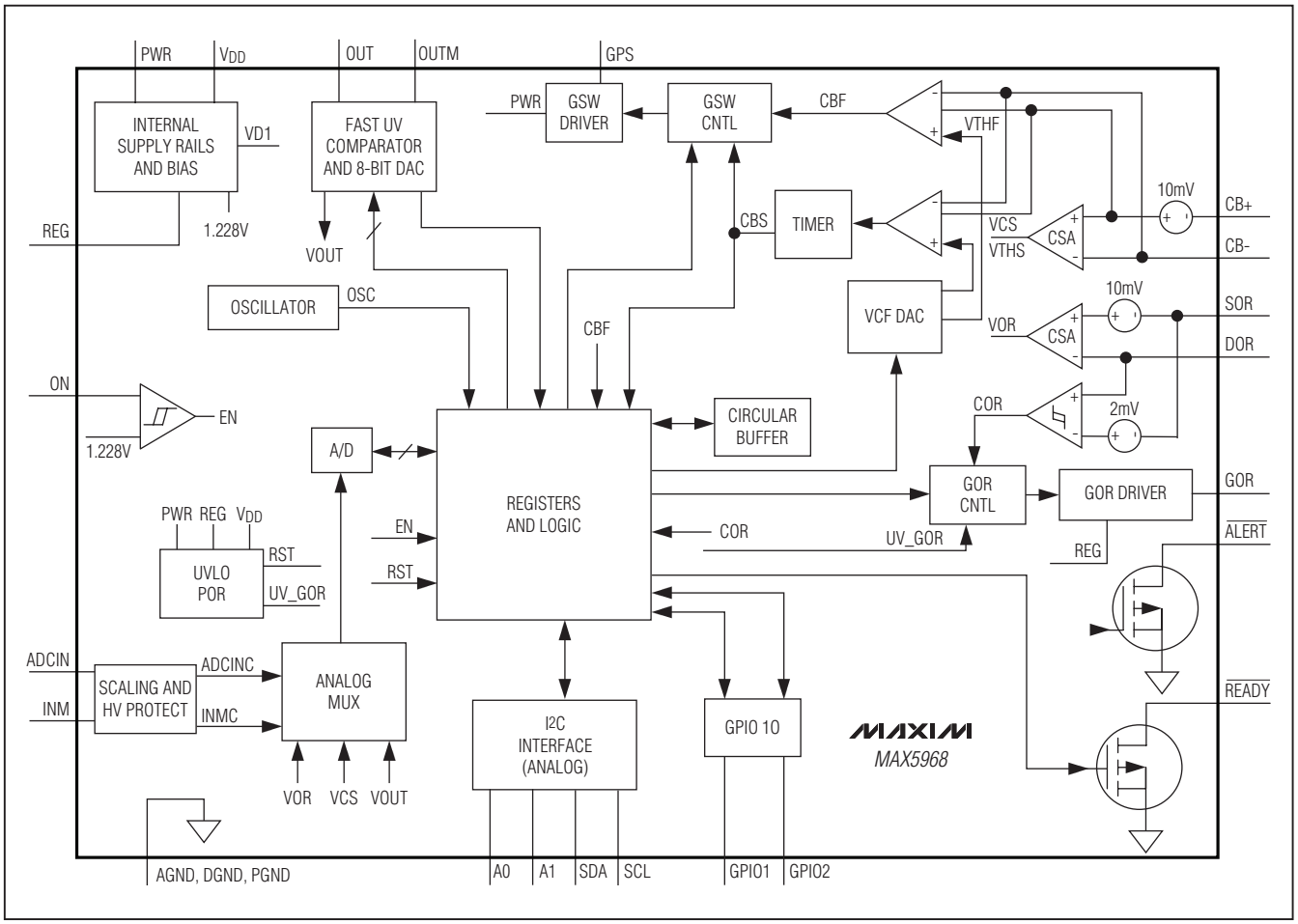
PIN	NAME	FUNCTION
1	GPIO1	General-Purpose Input/Output 1. Configured by internal registers.
2	GPIO2	General-Purpose Input/Output 2. Configured by internal registers.
3	A0	I²C Address Selection Input 1
4	A1	I²C Address Selection Input 2
5	$\overline{\text{ALERT}}$	Active-Low Fault Status Open-Drain Output. Driven low if a failure condition is detected.
6	SCL	I²C Clock Input
7	SDA	I²C Serial-Data Input/Output
8	OUT	Load-Voltage ADC Monitor Positive Input
9	OUTM	Load-Voltage ADC Monitor Negative Input. Connect to the load ground.
10	SOR	Reverse-Current Protection External MOSFET Source Connection. Connect to the source of the output reverse-current protection n-channel MOSFETs and the load ground.
11	DOR	Reverse-Current Protection External MOSFET Drain Connection. Connect to the drain of the reverse-current protection n-channel MOSFETs and to the converter negative output.
12	PGND	Power Ground
13	GOR	Reverse-Current Protection External MOSFET Gate-Drive Output. Connect to gate of the reverse-current protection n-channel MOSFETs.
14, 27, 28	N.C.	No Connection. Not internally connected.
15	REG	Internal Regulator Output External Bypass Capacitor Connection. Bypass to ground with a 10µF ceramic capacitor.
16	PWR	Device Power Input
17	V_{DD}	Digital Supply. Bypass V_{DD} to DGND with a 1µF capacitor.
18	ADCIN	Converter Temperature and Fault Monitoring Input. Connect to converter temperature output signal. This input is multiplexed to the internal ADC for temperature monitoring.

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

Pin Description (continued)

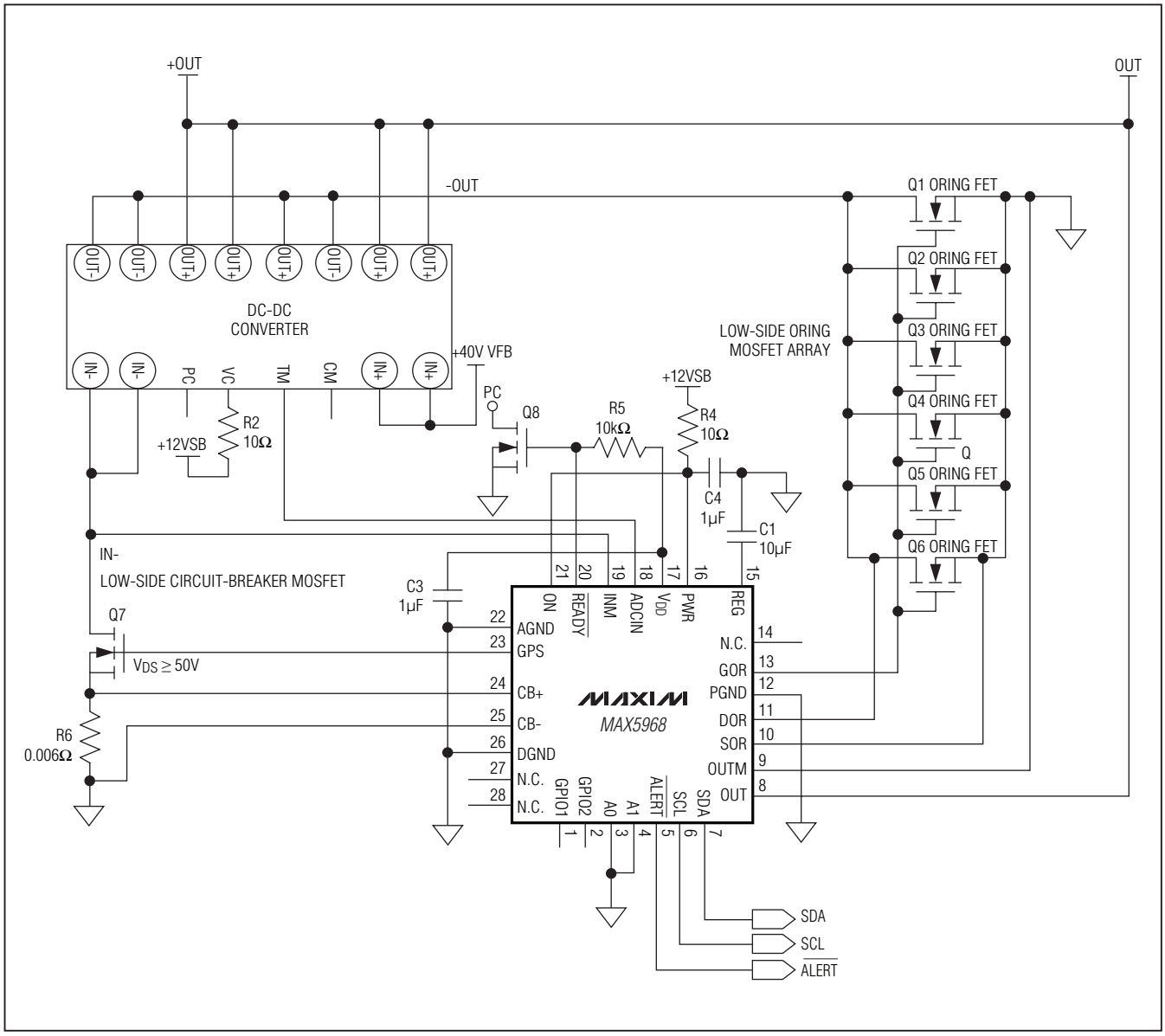
PIN	NAME	FUNCTION
19	INM	ADCIN Differential Amplifier Reference Input. Connect to the drain of the input protection low-side MOSFET to remove ground bias from the signal at ADCIN.
20	$\overline{\text{READY}}$	Active-Low Converter Enable Open-Drain Output. $\overline{\text{READY}}$ goes low when both GPS and GOR output voltages are high (or enhanced).
21	ON	Enable Input. Precision enable input to adjust undervoltage lockout. Connect to PWR for enabled operation.
22	AGND	Analog Ground
23	GPS	Converter Input Power MOSFET Gate Drive. Connect to the gate of the external n-channel low-side power MOSFET.
24	CB+	Converter Input Current-Sense Amplifier Positive Input
25	CB-	Converter Input Current-Sense Amplifier Negative Input
26	DGND	Digital Ground
—	EP	Exposed Pad. Connect to the ground plane.

Functional Diagram



Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

Typical Application Circuit



Detailed Description

The MAX5968 is a soft-switch and ideal diode controller that protects systems with redundant DC-DC converter modules by isolating failed modules from the common input and output power. During normal operation, both the input and output MOSFET switches are fully enhanced. The gate of the high-voltage MOSFET at GPS is driven to +8V (typ) to ensure low on-resistance and high-efficiency operation. The gate of the reverse-current blocking MOSFET at GOR is driven to 4.8V (typ) for fast on-off response, low on-resistance, and to stay within the gate-to-source voltage rating of the low-voltage MOSFETs used in this application.

The MAX5968 provides input protection by means of a current-sense amplifier connected to a sense resistor that resides at the source of the input protection MOSFET. The current-sense signal is supplied to two precision analog comparators to implement circuit-breaker protection. One comparator has a lower threshold and a slow response time, while the other comparator has a higher threshold and a fast response. This provides good rejection of noise and brief load-current transients, while still protecting the system against slow-onset and short-circuit failures. If either the slow-comparator or fast-comparator threshold is exceeded for sufficient duration, the gate of the input protection MOSFET is pulled low with 1.5A peak current and latched off, disconnecting the converter input from the power supply bus. The fast-trip threshold is programmed through the I²C interface to a value from 0 to 40mV with an 8-bit DAC, and the slow-trip threshold can be set to 50%, 57%, 67%, or 80% of the fast-trip threshold.

Converter output protection consists of a precision amplifier and comparator circuit that compares the voltage between the source and drain of an external MOSFET. If the drain rises above the source by 2mV (typ), a reverse-current condition is detected and the gate of the MOSFET immediately pulls low with 7A peak current, blocking the flow of current from the output bus back into the failed converter. As soon as the drain falls to within 1mV (typ) of source potential, the gate of the MOSFET pulls high again with 2.5A peak current to allow forward current flow. This fast, unlatched driver allows the converter module to quickly return to normal operation after a reverse-current transient.

A 10-bit ADC is multiplexed to monitor the DC-DC converter input current, the voltage at an auxiliary input, the output MOSFET forward voltage drop, and the load voltage. All ADC results, including circular buffers and the configuration registers, are accessible through a 400kHz I²C interface. The auxiliary ADC input can be connected to a 0 to 5V signal from the converter, typically a combined temperature and fault signal.

Two 10-bit circular buffers that contain a history of the 50 most recent input switching current and output load-voltage digital conversion results help diagnose DC-DC converter faults.

A precision on-comparator input can be used to enable or disable the input and output MOSFET drivers by connecting to an external voltage signal, allowing ON to be used as a programmable undervoltage threshold.

All inputs are equipped with programmable warning comparators. If an input signal falls outside its digital thresholds, a warning condition is registered, and the $\overline{ALERT}$ output can be programmed to assert for any or all of these conditions. All monitored signals are equipped with resettable peak-detection registers that store the minimum and maximum values measured since they were last cleared. This peak-detection system reduces or eliminates the need for continuous polling of conversion results. A fast analog comparator continuously monitors OUT voltage and latches the UV_warn register that asserts $\overline{ALERT}$.

An open-drain $\overline{READY}$ output can be used to enable the associated DC-DC converter by driving the converter enable input when the input and output MOSFET drivers are fully enhanced, or it can be programmed through the I²C interface to arbitrarily disable the converter at any time.

Two general-purpose I/Os can be fully configured through the I²C interface to provide external indications or to control additional peripheral devices. These outputs have sufficient sink-current capability to drive LED indicators. These pins have internal 10µA pullups and sufficient sink-current capability to directly drive LED indicators.

SOR/DOR Comparator

The SOR/DOR comparator monitors the V_{DS} voltage of the external low-side ORing FET. When V_{DOR} - V_{SOR} exceeds the trip point (+4mV), this comparator trips and commands the ORing FET gate driver to pull GOR to ground, turning off the FET and blocking reverse current. When V_{DOR} - V_{SOR} falls below +2mV, the GOR driver immediately drives GOR high again.

During normal operation, transient conditions cause temporary reversal of potential across the ORing FET. The MAX5968 ORing function is intended to block any

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

reverse current that could occur in this condition, while quickly returning the FET to the on state, immediately after the reverse potential condition is gone. There is a user-selectable timeout period for reverse-current blocking notification. If the GOR output remains low for longer than this timer period, a fault status indicator flag is set in bit 2 of register 0x27. This feature is intended to alert the system to a persistent reverse potential at the ORing FET that is indicative of a failure at the output of the associated converter module. The time delay can be programmed to 192µs, 128µs, 64µs, or 32µs by writing to the two bits of register 0x39. The default timer value is 192µs.

SOR/DOR Voltage Amplifier

The MAX5968 measures the ORing MOSFET forward voltage (V_{SOR} - V_{DOR}) and sends this value to the ADC for conversion and communication through the I^2C bus. The total ADC conversion range is 50mV: full-scale input voltage is -40mV, and there is an offset added to the signal to allow ADC measurement of reverse potential as high as 10mV.

GOR Gate Driver

The GOR gate driver includes a 5Ω MOSFET driver that pulls up to +4.8V (typ) and pulls down to ground to allow forward current and block reverse current, respectively. The GOR driver is capable of 2.5A peak pullup and 7A peak pulldown currents. A coarse 3V comparator is used to indicate FET full enhancement and sets a GOR gate-drive good flag in register 0x29.

ON Comparator

The ON input enables and disables the MAX5968 GPS and GOR outputs. A comparator compares the ON voltage against the internal bandgap voltage with 62.5mV hysteresis. Upon system fault, the input FET pulls low and is latched off. In this situation, the user can toggle the ON input to reset the fault latch and reenable the FETs. In addition, the ON enabling/disabling functionality can be masked or overridden by the chxen register bits. See Figure 2.

PWR UVLO and V_{DD} Power-On Reset

If the voltage at PWR is below 8.9V or V_{DD} voltage is below +3.5V (typ), the MAX5968 enters power-on reset and all the registers are restored to their default states. For normal operation, the PWR input must be greater than or equal to +9V and V_{DD} must be greater than or equal to +4.5V. A flag is set in register 0x27 whenever the MAX5968 exits the reset state to indicate that all registers are in their default states.

CB+/CB- Current-Sense Amplifier

The CB+/CB- current-sense amplifier feeds the differential voltage across a current-sense resistor to the internal ADC. The total conversion range is 50mV: the full-scale input voltage is 40mV, and there is an input offset added to allow measurement of reverse current as high as -10mV.

GPS Fast Comparator

The fast circuit-breaker comparator compares the output of the CB+/CB- current-sense amplifier to the threshold voltage generated by the 8-bit fast circuit-breaker threshold DAC. The DAC voltage is set by writing to register 0x25. This fast comparator commands a quick turn off of the GPS output as soon as its threshold is exceeded, and the fast-trip shutdown flag is set in register 0x27.

GPS Slow Comparator

The slow circuit-breaker comparator compares the output of the CB+/CB- current-sense amplifier to a threshold voltage generated by the combination of the fast circuit-breaker threshold DAC and the fast-to-slow threshold ratio setting in register 0x26; see Table 1. When the slow circuit-breaker threshold is exceeded, it starts an analog timer designed so that the timer duration is proportional to comparator overdrive voltage. When the timer expires, the GPS output is driven low and the slow-trip shutdown flag is set in register 0x27.

Table 1. Fast and Slow Circuit-Breaker Comparator Threshold Ranges

FAST-TRIP COMPARATOR 8-BIT DAC RANGE (REGISTER 0x25) (mV)	F2S_RATIO[1:0] (REGISTER 0x26)	FAST-TRIP TO SLOW-TRIP RATIO (%)	VALID SLOW-TRIP THRESHOLD RANGE (mV)	SPECIFIED SLOW-TRIP THRESHOLD RANGE (mV)
0 to 40	00	125	0 to 32	12.8 to 32
	01	150	0 to 26.67	10.67 to 26.67
	10	175	0 to 22.86	9.14 to 22.86
	11	200	0 to 20	8 to 20

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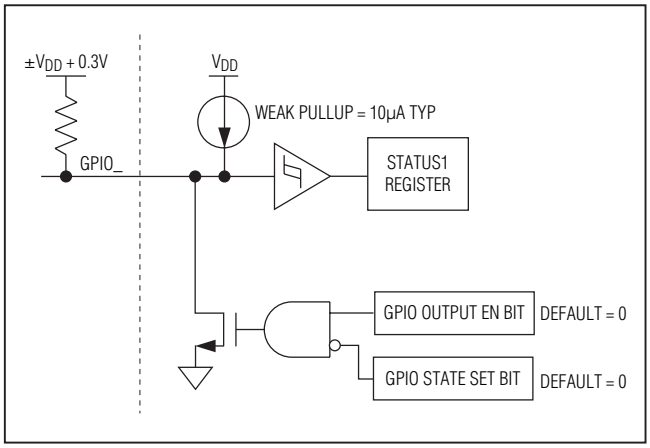

Figure 1. GPIO Driver

GPS Gate Driver

The GPS output is designed to drive the gate of a low-side external n-channel MOSFET. When commanded high, GPS is pulled up to an internal 8V rail with a 50µA current source. A 5V comparator is used to indicate full enhancement and set a gate-drive good flag in register 0x29. Upon turn-off, GPS is driven to ground with peak current of 1.5A.

OUT Undervoltage Fast Comparator and ADC Full-Scale Range

The output load voltage is monitored by the ADC. The load voltage is measured differentially between OUT and OUTM. The full-scale conversion voltage is set to either 2V or 4V by writing to the 1-bit register at address 0x18. See Table 2.

The load-voltage monitoring amplifier is also connected to a precision fast comparator. The reference for this comparator is generated by an 8-bit DAC, programmed by register 0x24. This sets an undervoltage value from 0 to 1.6V for the 2V OUT range, or 3.2V for the 4V OUT range as shown in Table 2. If V_{OUT} - V_{OUTM} falls below the programmed comparator threshold, the UV warning register bit asserts in register 0x2A. This feature detects load-voltage glitches during fault-protection events that can occur when one of several redundant converters is disabled, causing the load to shift to the other converters. This analog comparator allows detection of fast glitches that are asynchronous to the ADC sample cycle.

GPIO1, GPIO2

Two general-purpose open-drain I/Os can be independently configured by output-enable register 0x37 and output-state register 0x38. The actual voltage state of these I/Os can be read through status register 0x28, regardless of whether they are configured as inputs or outputs. Upon power-on reset, both GPIOs are configured as inputs with 10µA weak pullups. When configured as outputs, both GPIOs have sufficient pulldown strength to directly drive LED indicators (Figure 1).

$\overline{ALERT}$ Output

$\overline{ALERT}$ is an active-low, open-drain output. The $\overline{ALERT}$ output defaults to only indicate a failure condition that includes either a circuit-breaker or reverse-current shutdown. A bit can be cleared to unmask the digital and analog warning (UV, OV, or OC) comparator inputs, allowing these conditions to also assert the $\overline{ALERT}$ output, if desired. $\overline{ALERT}$ has sufficient pulldown strength to directly drive an LED indicator.

$\overline{READY}$ Output

An open-drain $\overline{READY}$ pin goes low after the input and output protection MOSFETs are fully enhanced, and remains low until a circuit-breaker fault occurs or until $\overline{READY}$ is set high impedance by writing to a register. $\overline{READY}$ can be used to provide an active-high enable signal to the associated converter by driving an external n-channel transistor, thus allowing high-voltage operation. $\overline{READY}$ has sufficient pulldown strength to directly drive an LED indicator.

Table 2. OUT Undervoltage Fast Comparator

LV_RANGE[0] VALUE	LOAD-VOLTAGE ADC CONVERSION RANGE (OUT RANGE) (V)	LOAD-VOLTAGE FAST UNDERVOLTAGE COMPARATOR DAC RANGE (V)
0	$0 \le V_{OUT} \le 2.0$	$0 \le V_{THUVDAC} \le 1.6$
1	$0 \le V_{OUT} \le 4.0$	$0 \le V_{THUVDAC} \le 3.2$

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Register Map

If a register is less than 8 bits wide and writable, the non-existent bits are ignored during a write operation. During a read operation they are read back as 0. Because the I²C protocol uses 8-bit data, the master must write 2 bytes to sequential registers to program the 10-bit settings of the MAX5968. To read 10-bit data, the master should perform a 2-byte burst read, starting on the MSB byte address. See Table 3 for the register address map.

Table 3. Register Address Map

NAME	ADDR	ACCESS	BIT RANGE	RESET VALUE	DESCRIPTION
CS_MSB	0x00	R	[7:0]	0x00	Latest ADC results of CB- amplifier output, bits [9:2]
CS_LSB	0x01	R	[1:0]	0x00	Latest ADC results of CB- amplifier output, bits [1:0]
ADCIN_MSB	0x02	R	[7:0]	0x00	Latest ADC results of ADCIN, bits [9:2]
ADCIN_LSB	0x03	R	[1:0]	0x00	Latest ADC results of ADCIN, bits [1:0]
ORFET_MSB	0x04	R	[7:0]	0x00	Latest ADC results of output-MOSFET forward voltage, bits [9:2]
ORFET_LSB	0x05	R	[1:0]	0x00	Latest ADC results of output-MOSFET forward voltage, bits [1:0]
LV_MSB	0x06	R	[7:0]	0x00	Latest ADC results of load voltage, bits [9:2]
LV_LSB	0x07	R	[1:0]	0x00	Latest ADC results of load voltage, bits [1:0]
min_CS_MSB	0x08	R	[7:0]	0xFF	Minimum value of CS amplifier output, bits [9:2]
min_CS_LSB	0x09	R	[1:0]	0x03	Minimum value of CS amplifier output, bits [1:0]
max_CS_MSB	0x0A	R	[7:0]	0x00	Maximum value of CS amplifier output, bits [9:2]
max_CS_LSB	0x0B	R	[1:0]	0x00	Maximum value of CS amplifier output, bits [1:0]
min_ADCIN_MSB	0x0C	R	[7:0]	0xFF	Minimum value of ADCIN, bits [9:2]
min_ADCIN_LSB	0x0D	R	[1:0]	0x03	Minimum value of ADCIN, bits [1:0]
max_ADCIN_MSB	0x0E	R	[7:0]	0x00	Maximum value of ADCIN, bits [9:2]
max_ADCIN_LSB	0x0F	R	[1:0]	0x00	Maximum value of ADCIN, bits [1:0]
min_ORFET_MSB	0x10	R	[7:0]	0xFF	Minimum value of output-MOSFET forward voltage, bits [9:2]
min_ORFET_LSB	0x11	R	[1:0]	0x03	Minimum value of output-MOSFET forward voltage, bits [1:0]
max_ORFET_MSB	0x12	R	[7:0]	0x00	Maximum value of output-MOSFET forward voltage, bits [9:2]
max_ORFET_LSB	0x13	R	[1:0]	0x00	Maximum value of output-MOSFET forward voltage, bits [1:0]
min_LV_MSB	0x14	R	[7:0]	0xFF	Minimum value of load voltage, bits [9:2]
min_LV_LSB	0x15	R	[1:0]	0x03	Minimum value of load voltage, bits [1:0]
max_LV_MSB	0x16	R	[7:0]	0x00	Maximum value of load voltage, bits [9:2]
max_LV_LSB	0x17	R	[1:0]	0x00	Maximum value of load voltage, bits [1:0]
LV_range	0x18	R/W	[0]	0x00	Load voltage ADC input range setting: 0 = 2V, 1 = 4V
buf_enable	0x19	R/W	[2:0]	0x05	Selective enabling of circular buffer blocks
			[0]	1	Current-sense buffer enable bit
			[1]	1	Load-voltage buffer enable bit
			[2]	1	Load-voltage buffer stop upon persistent reverse-current fault
ocw_CS_MSB	0x1A	R/W	[7:0]	0xFF	Digital warning threshold value for overcurrent, bits [9:2]
ocw_CS_LSB	0x1B	R/W	[1:0]	0x03	Digital warning threshold value for overcurrent, bits [1:0]
uvw_ADCIN_MSB	0x1C	R.W	[7:0]	0x00	Digital warning undervoltage threshold value for ADCIN, bits [9:2]

Table 3. Register Address Map (continued)

NAME	ADDR	ACCESS	BIT RANGE	RESET VALUE	DESCRIPTION
uvw_ADCIN_LSB	0x1D	R/W	[1:0]	0x00	Digital warning undervoltage threshold value for ADCIN, bits [1:0]
ovw_ADCIN_MSB	0x1E	R/W	[7:0]	0xFF	Digital warning overvoltage threshold value for ADCIN, bits [9:2]
ovw_ADCIN_LSB	0x1F	R/W	[1:0]	0x03	Digital warning overvoltage threshold value for ADCIN, bits [1:0]
ovw_ORFET_MSB	0x20	R/W	[7:0]	0xFF	Digital warning overvoltage threshold value for output-MOSFET voltage, bits [9:2]
ovw_ORFET_LSB	0x21	R/W	[1:0]	0x03	Digital warning overvoltage threshold value for output-MOSFET voltage, bits [1:0]
ovw_LV_MSB	0x22	R/W	[7:0]	0xFF	Digital warning overvoltage threshold value for load voltage, bits [9:2]
ovw_LV_LSB	0x23	R/W	[1:0]	0x03	Digital warning overvoltage threshold value for load voltage, bits [1:0]
DAC_LV_fc	0x24	R/W	[7:0]	0x00	DAC setting for the load-voltage fast undervoltage detection comparator
DAC_CS_fc	0x25	R/W	[7:0]	0xBF	DAC setting for the circuit-breaker fast-trip comparator
f2s_ratio	0x26	R/W	[1:0]	0x03	Settings for circuit-breaker fast comparator to slow comparator ratio
			[0]	1	f2s_ratio[0]
			[1]	1	f2s_ratio[1]
fault	0x27	R	[3:0]	0x08	Fault shutdown event logging
			[0]	—	Fast-trip shutdown flag
			[1]	—	Slow-trip shutdown flag
			[2]	—	Persistent reverse-current fault flag
			[3]	—	Default state indicator flag. This bit is set to 1 on initialization (coming out of UVLO). This bit clears to 0 after an I^2C write to any writable register.
status1	0x28	R	[2:0]	—	External input status
			[0]	—	ON state
			[1]	—	GPIO1 state
			[2]	—	GPIO2 state
status2	0x29	R	[3:0]	—	External output status
			[0]	—	$\overline{\text{READY}}$ state
			[1]	—	$\overline{\text{ALERT}}$ flag
			[2]	—	GPS-GOOD state
			[3]	—	GOR-GOOD state
UV_warn	0x2A		[2:0]	0x00	Undervoltage warning comparators status
		R	[0]	0	ADCIN undervoltage warning flag
		R	[1]	0	Load-voltage fast undervoltage comparator warning flag
		R/W	[2]	0	Undervoltage warning flag $\overline{\text{ALERT}}$ unmask bit; 1 to unmask $\overline{\text{ALERT}}$

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Table 3. Register Address Map (continued)

NAME	ADDR	ACCESS	BIT RANGE	RESET VALUE	DESCRIPTION
OV_warn	0x2B		[3:0]	0x00	Digital overvoltage warning comparators status
		R	[0]	0	ADCIN overvoltage warning flag
		R	[1]	0	ORing FET forward overvoltage warning flag
		R	[2]	0	Load-voltage overvoltage warning flag
		R/W	[3]	0	Overvoltage warning flag $\overline{\text{ALERT}}$ unmask bit; 1 to unmask $\overline{\text{ALERT}}$
OC_warn	0x2C		[1:0]	0x00	Digital overcurrent warning comparator status
		R	[0]	0	Overcurrent warning flag
		R/W	[1]	0	Overcurrent warning flag $\overline{\text{ALERT}}$ unmask bit;1 to unmask $\overline{\text{ALERT}}$
fokey	0x2D	R/W	[7:0]	0x00	Key to allow force on function
foset	0x2E	R/W	[2:0]	0x00	Force-on activation (valid only when fokey = 0xA5)
			[0]	0	Force-on for input switch (GPS output)
			[1]	0	Force-on for reverse-current protection switch (GOR output)
			[2]	0	Force reset on all registers, also resets itself
chxen	0x2F	R/W	[3:0]	0x00	Channel activation bits (combinational functioning with ON comparator)
			[0]	0	GPS master enable
			[1]	0	GPS ON-enabling mask bit; 1 to mask ON-enabling
			[2]	0	GOR master enable
			[3]	0	GOR ON-enabling mask bit; 1 to mask ON-enabling
dgl_i	0x30	R/W	[0]	0x00	Input overcurrent warning comparator deglitch on/off
dgl_uv	0x31	R/W	[0:0]	0x00	Deglitch setting bit for ADCIN undervoltage comparator
dgl_ov	0x32	R/W	[1:0]	0x00	Deglitch setting bits for overvoltage comparators
			[0]	0	ADCIN overvoltage warning deglitch on/off
			[1]	0	ORing FET forward overvoltage warning deglitch on/off
			[2]	0	Load-voltage overvoltage warning deglitch on/off
buf_read_8bit	0x33	R/W	[1:0]	0x00	Select 10-bit or 8-bit read-out from circular buffers
			[0]	0	Set to 1 for 8-bit read-out mode on current-sense buffer
			[1]	0	Set to 1 for 8-bit read-out mode on load-voltage buffer
buf_stp_dly	0x34	R/W	[5:0]	0x19	Number of samples to be stored before stopping buffers (valid 0 to 63)
peak_log_rst	0x35	R/W	[3:0]	0x00	When a bit is 1 the related signal peak detection is cleared to startup values
			[0]	0	Input current min/max clear
			[1]	0	ADCIN min/max clear
			[2]	0	ORing switch voltage min/max clear
			[3]	0	Load voltage min/max clear

Table 3. Register Address Map (continued)

NAME	ADDR	ACCESS	BIT RANGE	RESET VALUE	DESCRIPTION
peak_log_hold	0x36	R/W	[3:0]	0x00	When a bit is 1 the related signal peak detection is held (no change allowed)
			[0]	0	Input current min/max hold
			[1]	0	ADCIN min/max hold
			[2]	0	ORing switch voltage min/max hold
			[3]	0	Load voltage min/max hold
GPIO_out_en	0x37	R/W	[1:0]	0x00	GPIO output enable
			[0]	0	Set to 1 to enable GPIO1 as open-drain output (0 for CMOS input with weak pullup)
			[1]	0	Set to 1 to enable GPIO2 as open-drain output (0 for CMOS input with weak pullup)
GPIO_state_set	0x38	R/W	[1:0]	0x00	GPIO output state
			[0]	0	Set to 0 to pull down GPIO1 when in output mode; set to 1 to allow GPIO1 to go high (internal weak pullup to V_{DD})
			[1]	0	Set to 0 to pull down GPIO2 when in output mode; set to 1 to allow GPIO2 to go high (internal weak pullup to V_{DD})
or_fault_timer	0x39	R/W	[1:0]	0x03	ORing fault flag time delay setting. Default is 192µs.
			[0]	1	00 = 32µs 01 = 64µs 10 = 128µs 11 = 192µs
			[1]	1	
buf_base_CS	0x3A	R	[7:0]	—	Base address for the input current circular buffer
buf_base_LV	0x3B	R	[7:0]	—	Base address for the load-voltage circular buffer

Setting Circuit-Breaker Thresholds

To select and set the MAX5968 slow-trip and fast-trip comparator thresholds, use the following procedure:

1) Select one of four ratios between the fast-trip threshold and the slow-trip threshold: 200%, 175%, 150%, or 125%. The ratio is set by writing to the f2s_ratio register (the default setting on power-up is 200%).
2) Determine the slow-trip threshold $V_{TH,ST}$ based on the anticipated maximum continuous module input current during normal operation, and the value of the current-sense resistor. The slow-trip threshold should include some margin above the maximum input current to prevent spurious circuit-breaker shutdown and to accommodate passive component tolerances:

$$V_{TH,ST} = R_{SENSE} \times I_{INPUT,MAX} \times 120\%$$

3) Calculate the necessary fast-trip threshold $V_{TH,FT}$ based on the ratio set in step 1:

$$V_{TH,FT} = V_{TH,ST} \times \text{(fast-to-slow threshold ratio)}$$

4) Program the fast-trip and slow-trip thresholds by writing an 8-bit value to the DAC_CS_fc register. This 8-bit value is determined from the desired $V_{TH,ST}$ value that was calculated in step 2, the threshold ratio from step 1, and the current-sense range of +40mV:

$$DAC = V_{TH,ST} \times 255 \times \text{(fast-to-slow threshold ratio)}/(40mV)$$

Table 1 shows the specified ranges for the fast-trip and slow-trip thresholds for all selections of the fast-to-slow threshold ratio. The fast-trip DAC can be programmed to values below 0x26 (40% of the current-sense range), but accuracy is not specified for operation below 40%.

Force-On Bit

When the force-on bit is set to 1, the input and output switches are enabled and do not shut down. The overcurrent and reverse current comparator outputs are ignored. The power-on reset value of this bit is 0. There is a Force-On Key register that must be set to 0xA5 for the force-on function to become active. If this register

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contains any value other than 0xA5, setting the force-on bit to 1 has no effect. The power-on default value of the Force-On Key register is 0x00.

ADC Result Registers

Result registers contain the most recent ADC values. Because the ADC is multiplexed to four different channels sequentially, at any time the result registers can contain values from the current ADC cycle and the previous cycle. For example, if the conversion for channel 2 was just stored in the ADC Result register, registers for channels 0, 1, and 2 would contain values from the present scan and the registers for channel 3 would contain the values from the previous scan. The registers can be read at any time through the I²C interface. The registers are buffered so that reading any ADC result register does not interrupt or delay the ADC cycle, nor does it cause missed readings.

Min/Max Registers

Each ADC channel features a min and a max register; there are four min registers and four max registers. In each ADC cycle for each signal, the ADC reading is compared to the contents of the min register. If the current value is less than min register value, the current value is stored in the min register. If the current value is greater than the value in the max register, the current value is stored in the max register. The input current and load-voltage min/max registers do not update when the circular buffers are stopped because of a fault condition or shutdown.

The power-on reset value of the min registers is 0x3FF. To reset a min register, write 0x3FF.

The power-on reset value of the max registers is 0x000. To reset a max register, write 0x000.

Control registers are provided to hold and clear the min and max registers independently for each signal.

Digital Warning Comparators

Each monitored signal is equipped with one or more programmable digital warning comparators. If the most recent conversion result exceeds the programmed overvoltage or overcurrent value, or is less than the undervoltage value, the warning flag registers are set. Each group of warning flag registers has a mask bit that masks or unmasks $\overline{\text{ALERT}}$ bit response to these warning flags.

The default value of the overvoltage and overcurrent thresholds is 0x3FF, and the default value for the undervoltage threshold is 0x000. These default values disable the associated digital comparator. When the values are programmed to some value other than the default, the comparator is active.

Reading the under/over warning flag registers automatically clears the contents of the registers, eliminating the need for a second I²C write operation to clear the flags. See Table 4.

Circular Buffer

The circular buffer includes two banks—one for the voltage measurement across the input current-sense resistor, and another for the load-voltage measurement; each comprises 50 10-bit samples.

A block read is triggered by the I²C interface when a read operation is attempted from one of the circular buffer block base addresses. Readings can be either of the whole 10-bit samples or of the 8-bit upper bytes, according to the buf_read_8bit register.

Internal writing to either or both of the buffers can be inhibited directly by the user through a dedicated register at 0x19. Writing to the buffers also stops when the input switch is shut down. When a buffer block is read through the I²C interface, new load voltage and input current measurements are not written into the circular buffer.

When a circular buffer is commanded to stop for any reason, the MAX5968 continues to write a number of samples equal to the digital value stored in register 0x34. This allows the buffer(s) to store data that precedes and follows the stop command, forming a complete picture of the conditions immediately before and after a fault or normal shutdown.

If a reverse-current condition persists for more than the programmable ORing-fault timeout, the load-voltage buffer stops, and the load-voltage buffer-enable bit

Table 4. Digital Warning Comparators Warnings

TYPE	CHANNEL 0: CURRENT SENSE	CHANNEL 1: ADCIN	CHANNEL 2: ORING VOLTAGE	CHANNEL 3: LOAD VOLTAGE
Undervoltage		•		Analog comparator
Overvoltage		•	•	•
Overcurrent	•			

at 0x19[1] is cleared. This allows the user to read the contents of the circular buffer after a persistent reverse-current condition, even if the condition clears. The buffer is then restarted by writing a 1 to bit 2 of 0x19. However, if this function is not desired, bit 3 of register 0x19 can be cleared to prevent a reverse-current fault condition from stopping the load-voltage buffer by blocking the logic that would otherwise clear the buffer enable bit 0x19. See Table 5.

GPS and GOR Enable/Disable

Use the chxen register 0x2F to enable or disable the GOR and GPS driver logic in combination with (or regardless of) the ON comparator output, as shown in Figure 2. Bits 0 and 2 of register 0x2F are master enable bits for the GPS and GOR drivers, respectively. Bits 1 and 3 of register 0x2F mask the status of the ON comparator. Note that the master-enable bits override the ON masking bits.

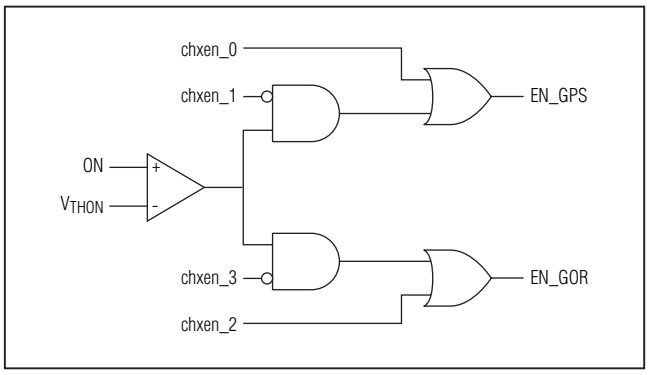

Figure 2. Enable Logic for GPS and GOR Drivers

I²C Serial Interface

The MAX5968 features an I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL allow bidirectional communication between the MAX5968 and the master device at clock rates from 100kHz to 400kHz. The I²C bus can have several devices (e.g., more than one MAX5968, or other I²C devices in addition to the MAX5968) attached simultaneously. The A0 and A1 inputs set one of four possible I²C addresses (see Table 6).

The 2-wire communication is fully compatible with existing 2-wire serial interface systems. Figure 2 shows the interface timing diagram. The MAX5968 is a transmit/receive slave-only device, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates with the MAX5968 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is a logic input/open-drain output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Table 5. Circular Buffer Registers

CONDITION	0x19[2]	INPUT CURRENT BUFFER	LOAD-VOLTAGE BUFFER	RECOVERY
Input circuit-breaker fault	X	Stopped	Stopped	Toggle input switch enable off-on
Clear 0x19[0]	X	Stopped	Running	Write 1 to 0x19[0]
Clear 0x19[1]	X	Running	Stopped	Write 1 to 0x19[1]
Persistent reverse-current fault flag set	1	Running	Stopped	Write 1 to 0x19[1]
	0	Running	Running	None required
Input switch disabled	X	Stopped	Stopped	Reenable input switch
ORing switch disabled	X	Running	Stopped	Reenable ORing switch
Reading load-voltage buffer base address	X	Running	Stopped	Read/write from any other register address
Reading input current buffer	X	Stopped	Running	Read/write from any other register address

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Table 6. Slave Address Settings

ADDRESS INPUT STATE		I²C ADDRESS BITS							
A1	A0	ADDR 7	ADDR 6	ADDR 5	ADDR 4	ADDR 3	ADDR 2	ADDR 1	ADDR 0
Low	Low	0	1	1	1	1	0	0	R/W
Low	High	0	1	1	1	1	0	1	R/W
High	Low	0	1	1	1	1	1	0	R/W
High	High	0	1	1	1	1	1	1	R/W

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (see Figure 3), otherwise the MAX5968 registers a START or STOP condition (see Figure 4) from the master. SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START condition (see Figure 5) by transitioning SDA from high to low while SCL is high. The master device issues a STOP condition (see Figure 4) by

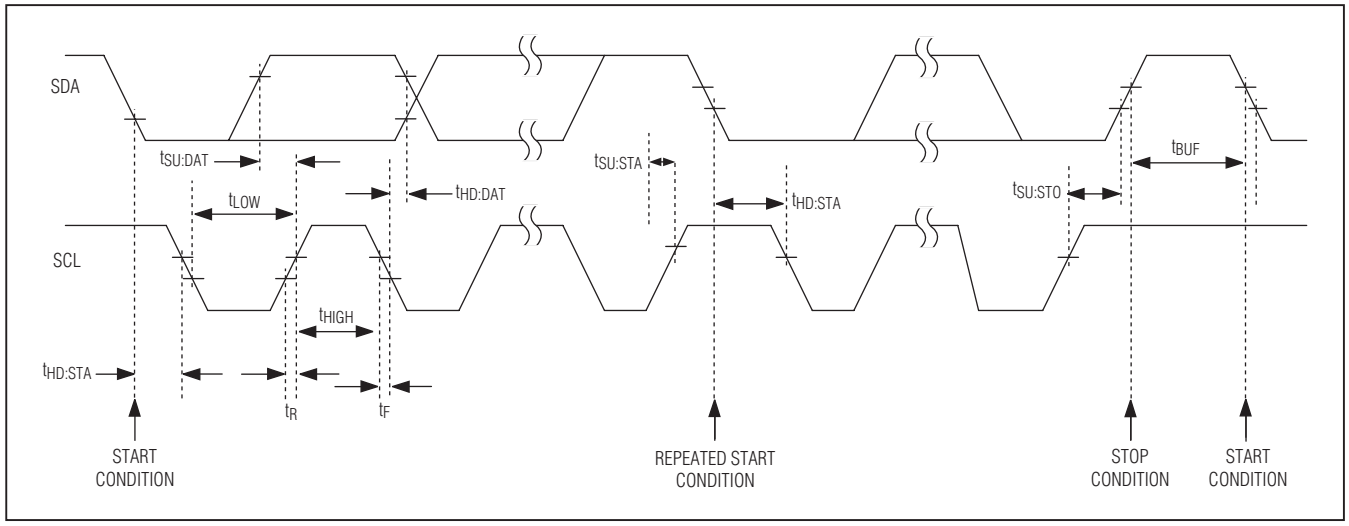

Figure 3. Serial-Interface Timing Details

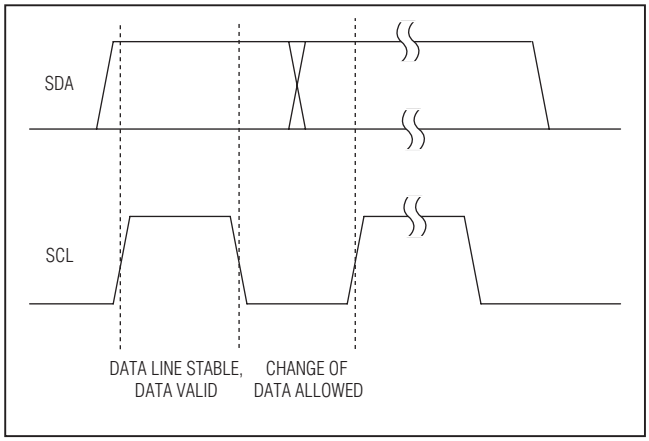

Figure 4. Bit Transfer

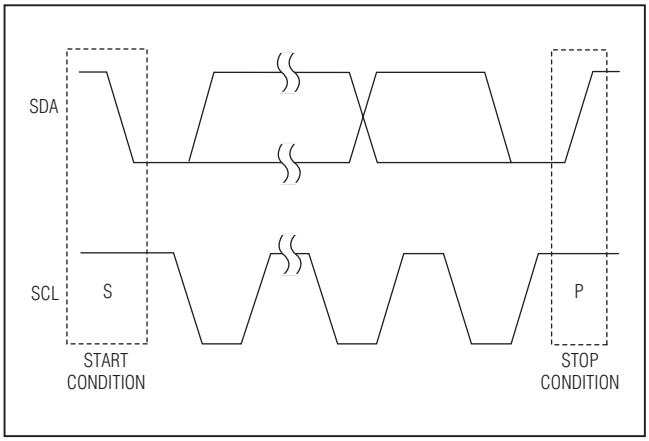

Figure 5. START and STOP Conditions

transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 5).

Early STOP Conditions

The MAX5968 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I²C format. At least one clock pulse must separate any START and STOP condition.

SEND BYTE FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–PRESETS THE INTERNAL ADDRESS POINTER.

WRITE WORD FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE–MSB OF THE EEPROM REGISTER BEING WRITTEN.

DATA BYTE–FIRST BYTE IS THE LSB OF THE EEPROM ADDRESS. SECOND BYTE IS THE ACTUAL DATA.

RECEIVE BYTE FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	DATA	$\overline{ACK}$	P
	7 BITS	1		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–READS DATA FROM THE REGISTER COMMANDED BY THE LAST READ BYTE OR WRITE BYTE TRANSMISSION. ALSO DEPENDENT ON A SEND BYTE.

WRITE BYTE FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE–SELECTS REGISTER BEING WRITTEN.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE IF THE COMMAND IS BELOW 50h. IF THE COMMAND IS 80h, 81h, OR 82h, THE DATA BYTE PRESETS THE LSB OF AN EEPROM ADDRESS.

BLOCK WRITE FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	BYTE COUNT= N	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS		8 BITS		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE–PREPARES DEVICE FOR BLOCK OPERATION.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE.

BLOCK READ FORMAT

S	ADDRESS	R/$\overline{W}$	ACK	COMMAND	ACK	Sr	ADDRESS	R/$\overline{W}$	ACK	BYTE COUNT= 16	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS			7 BITS	1		10h		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

COMMAND BYTE–PREPARES DEVICE FOR BLOCK OPERATION.

SLAVE ADDRESS–EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE–DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE.

S = START CONDITION.
P = STOP CONDITION.

SHADED = SLAVE TRANSMISSION.
Sr = REPEATED START CONDITION.

Figure 6. SMBUS/I²C Protocols

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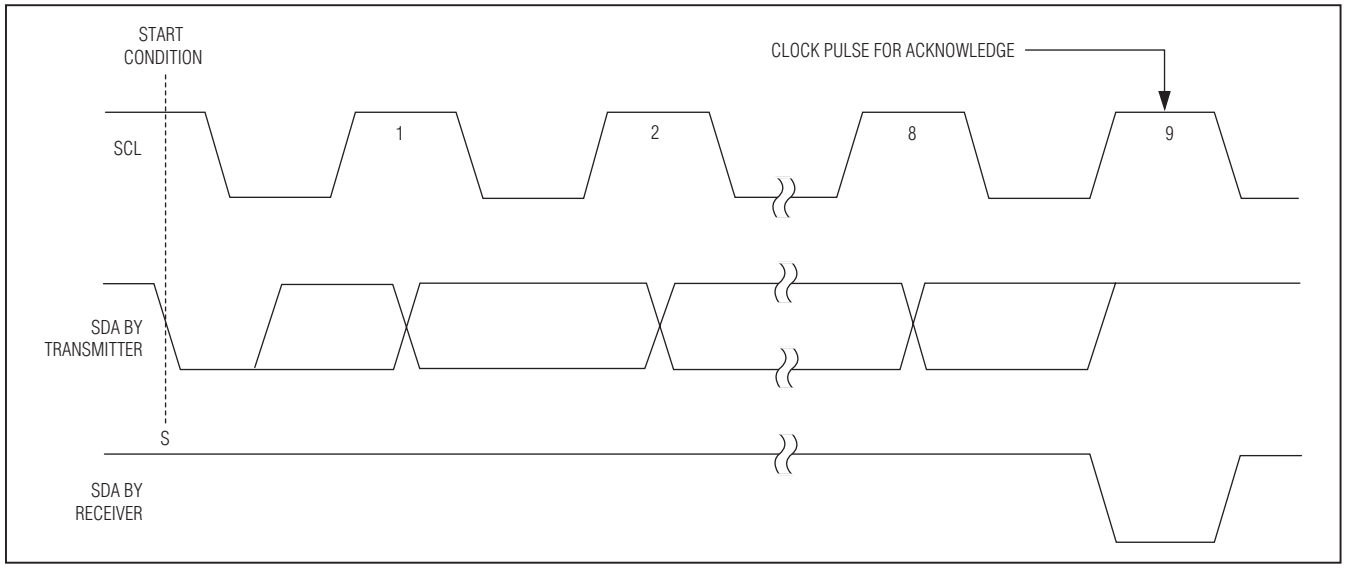

Figure 7. Acknowledge

REPEATED START Conditions

A REPEATED START (Sr) condition can indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 5). Sr can also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5968 serial interface supports continuous write operations with or without an Sr condition separating them. Continuous read operations require Sr conditions because of the change in direction of data flow.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX5968 generates an ACK when receiving an address or data by pulling SDA low during the 9th clock period (see Figure 6). When transmitting data, such as when the master device reads data back from the MAX5968, the MAX5968 waits for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX5968 generates a NACK after the slave address during a software reboot or when receiving an illegal memory address.

Send Byte

The send byte protocol allows the master device to send 1 byte of data to the slave device (see Figure 5). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed. If the master sends a STOP condition, the internal address pointer does not change. The send byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit data byte.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a STOP condition.

Write Byte

The write byte/word protocol allows the master device to write a single byte in the register bank or to write to a series of sequential register addresses. The write byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit command code.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.

Table 7. Circular Buffer Readout Sequence

READ-OUT ORDER	1st OUT	2nd OUT	…	48th OUT	49th OUT	50th OUT
Chronological Number	1	2	…	48	49	0

8) The addressed slave increments its internal address pointer.
9) The master sends a STOP condition or repeats steps 6, 7, and 8.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The data byte is written to the register bank if the command code is valid.

The slave generates a NACK at step 5 if the command code is invalid. The command code must be in the range of 0x00 to 0x3B. The internal address pointer returns to 0x00 after incrementing from the highest register address.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX5968 (see Figure 6). The EEPROM or register address must be preset with a send byte protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5) The slave increments its internal address pointer.
6) The master asserts an ACK on SDA and repeats steps 4 and 5 or asserts a NACK and generates a STOP condition.

The internal address pointer returns to 0x00 after incrementing from the highest register address.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 0x00 to 0x3B, and the circular buffer addresses are 0x3A to 0x3B. Register addresses outside of this range result in a NACK being issued from the MAX5968.

Circular Buffer Read

The circular buffer read operation is similar to the receive byte operation. The read operation is triggered after any one of the circular buffer base addresses is loaded. During a circular buffer read, although all is transparent from the external world, internally the autoincrement function in the I²C controller is disabled. Thus, it is possible to read one of the circular buffer blocks with a burst read without changing the virtual internal address corresponding to the base address. Once the master issues a NACK, the circular reading stops, and the default functions of I²C slave bus controller are restored.

In 8-bit read mode, every I²C read operation shifts out a single sample from the circular buffer. In 10-bit mode, two subsequent I²C read operations shift out a single 10-bit sample from the circular buffer, with the high-order byte read first, followed by a byte containing the right-shifted two least-significant bits. Once the master issues a NACK, the read circular buffer operation terminates and normal I²C operation returns.

The data in the circular buffers is read back with the next-to-oldest sample first, followed by progressively more recent samples until the most recent sample is retrieved, followed finally by the oldest sample (see Table 7).

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855+6	21-0140

Circuit-Breaker and Ideal Diode Controller with Digital Monitoring Functions

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	2/10	Updated the *Absolute Maximum Ratings and Electrical Characteristics.*	2, 3