19-3704; Rev 2; 1/12

EVALUATION KIT AVAILABLE

308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

General Description

The MAX7042 fully integrated, low-power, CMOS superheterodyne RF receiver is designed to receive frequency-shift-keyed (FSK) data at rates up to 66kbps nonreturn-to-zero (NRZ) (33kbps Manchester). The MAX7042 requires only a few external components to realize a complete wireless RF receiver at 308, 315, 418, and 433.92MHz.

The MAX7042 includes all the active components required in a superheterodyne receiver including a low-noise amplifier (LNA), an image-rejection (IR) mixer, a fully integrated phase-locked loop (PLL), local oscillator (LO), 10.7MHz IF limiting amplifier with received-signal-strength indicator (RSSI), low-noise FM demodulator, and a 3V regulator. Differential peak-detecting data demodulators are included for baseband data recovery.

The MAX7042 is available in a 32-pin TQFN and is specified over the automotive -40°C to +125°C temperature range.

Applications

Remote Keyless Entry
Tire-Pressure Monitoring
Home and Office Lighting Control
Remote Sensing
Smoke Alarms
Home Automation
Local Telemetry Systems
Security Systems

Typical Application Circuit appears at end of data sheet.

Features

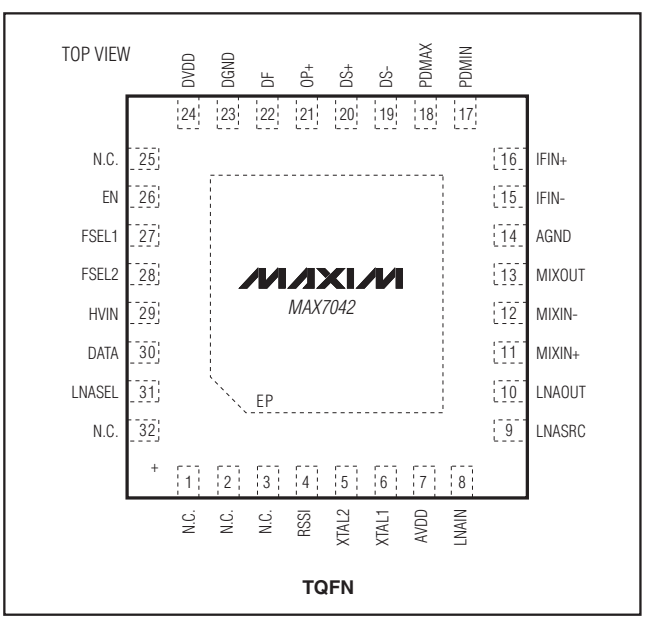
- **+2.4V to +3.6V or +4.5V to +5.5V Single-Supply Operation**
- **Four User-Selectable Carrier Frequencies 308, 315, 418, and 433.92MHz**
- **-110dBm RF Input Sensitivity at 315MHz**
- **-109dBm RF Input Sensitivity at 433.92MHz**
- **Fast Startup (< 250µs)**
- **Small 32-Pin TQFN Package**
- **Low Operating Supply Current**
  6.2mA Continuous
  20nA Power-Down
- **Integrated PLL, VCO, and Loop Filter**
- **45dB Integrated Image Rejection**
- **Selectable IF BW with External Filter**
- **Positive and Negative Peak Detectors**
- **RSSI Output**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7042ATJ+	-40°C TO +125°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

ABSOLUTE MAXIMUM RATINGS

HVIN to AGND or DGND .....-0.3V to +6.0V
AVDD, DVDD to AGND or DGND.....-0.3V to +4.0V
FSEL1, FSEL2, LNASEL,
EN, DATA.....(DGND - 0.3V) to (HVIN + 0.3V)
All Other Pins.....(AGND - 0.3V) to (AVDD + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C).....2759mW
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Maximum RF Input Power .....+0dBm
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 308, 315, 418, and 433.92MHz; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 433.92MHz, P_{RFIN} ≤ -80dBm, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (3V)	V_{DD}	HVIN, AVDD, and DVDD connected to power supply		2.4	3.0	3.6	V
Supply Voltage (5V)	HVIN	HVIN connected to power supply, AVDD and DVDD unconnected from HVIN, but connected together		4.5	5.0	5.5	V
Supply Current	I_{DD}	315MHz (3V)	Operating, 1x I_{LNA}		6.2		mA
			Operating, 2x I_{LNA}		6.8		
		315MHz (5V)	Operating, 1x I_{LNA}		6.4		
			Operating, 2x I_{LNA}		7.0		
		434MHz (3V)	Operating, 1x I_{LNA}		6.4	8.7	
			Operating, 2x I_{LNA}		7.0	8.6	
		434MHz (5V)	Operating, 1x I_{LNA}		6.6	8.4	
			Operating, 2x I_{LNA}		7.2	9.2	
Shutdown Current (3V)	I_{SHDN}	All digital inputs low	T_A = +25°C		0.02		µA
			T_A = +85°C		0.1		
			T_A = +125°C		0.85	6	
Shutdown Current (5V)	I_{SHDN}	All digital inputs low	T_A = +25°C		0.6		µA
			T_A = +85°C		1.4		
			T_A = +125°C		4	7	
Startup Time	t_{ON}	Time from EN = high to final signal detection; does not include baseband filter or data-slicer reference settling			250		µs
DIGITAL I/O							
Input High Threshold	V_{IH}			0.9 x V_{HVIN}			V
Input Low Threshold	V_{IL}					0.1 x V_{HVIN}	V

DC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 308, 315, 418, and 433.92MHz; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 433.92MHz, P_{RFIN} ≤ -80dBm, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Pulldown Current	I_{IH}	V_{HVIN} = +3.6V		8	15	µA
		V_{HVIN} = +5.5V		20	40	
Input Low-Leakage Current	I_{IL}	V_{HVIN} = +3.6V		< 1	1	µA
		V_{HVIN} = +5.5V		< 1	1	
Output High Voltage	V_{OH}	I_{SOURCE} = 500µA		V_{HVIN} - 0.4		V
Output Low Voltage	V_{OL}	I_{SINK} = 500µA		0.4		V
VOLTAGE REGULATOR						
Output Voltage	V_{REG}		2.5	3.0	3.5	V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 308, 315, 418, and 433.92MHz; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 433.92MHz, P_{RFIN} ≤ -80dBm, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Input Level					0		dBm
Sensitivity (Note 1)		315MHz setting	Operating, 1x I_{LNA}		-107		dBm
			Operating, 2x I_{LNA}		-110		
		434MHz setting	Operating, 1x I_{LNA}		-106		
			Operating, 2x I_{LNA}		-109		
Receiver Image Rejection					45		dB
LNA/MIXER							
Input Impedance (Note 2)	Z_{IN_LNA}	Normalized to 50Ω	2x I_{LNA} 315MHz		0.94 - j3.2		
			2x I_{LNA} 433.92MHz		0.94 - j2.1		
1dB Input Compression Point	P_{1dB}	1x I_{LNA} 315MHz			-47		dBm
		2x I_{LNA} 315MHz			-52		
Input-Referred 3rd-Order Intercept Point	IIP3	1x I_{LNA} 315MHz			-37		dBm
		2x I_{LNA} 315MHz			-42		
LO Signal Feedthrough to Antenna					-80		dBm
Mixer Output Impedance	$Zout_{MIX}$				330		Ω
Voltage Conversion Gain		330Ω IF filter load (Note 3)	1x I_{LNA} 315MHz		52		dB
			2x I_{LNA} 315MHz		57		
			1x I_{LNA} 433.92MHz		47		
			2x I_{LNA} 433.92MHz		52		
IF LIMITING AMPLIFIER							
Input Impedance	Z_{IN_IF}				330		Ω
-3dB Bandwidth					10		MHz

308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 308, 315, 418, and 433.92MHz; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 433.92MHz, P_{RFIN} ≤ -80dBm, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{IF}			10.7		MHz
RSSI Slope			10	16	21	mV/dB
FSK DEMODULATOR						
Conversion Gain			1.1	2.1	3.0	mV/kHz
ANALOG BASEBAND						
Maximum Peak-Detector Bandwidth				50		kHz
Maximum Data-Filter Bandwidth	BW_{DF}			50		kHz
Maximum Data-Slicer Bandwidth	BW_{DS}			100		kHz
Maximum Data Rate		Manchester coded		33		kHz
		NRZ		66		
CRYSTAL OSCILLATOR						
Crystal Frequency	f_{XTAL}			(f_{RF} - 10.7) / 32		MHz
Crystal Load Capacitance				4.5		pF

Note 1: 0.2% BER, 4kbps, Manchester coded, 280kHz IF BW, ±50kHz frequency deviation.

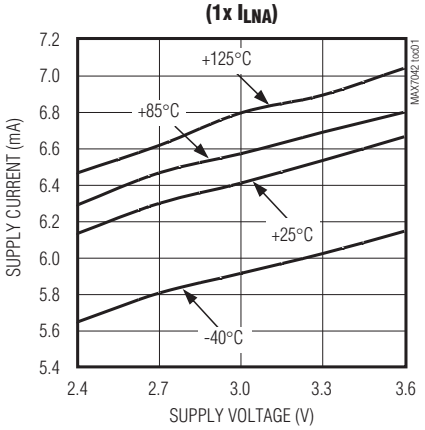
Note 2: Input impedance is measured at the LNAIN pin. Note that the impedance at 315MHz includes the 3.9nH inductive degeneration from the LNA source to ground. The impedance at 433.92MHz includes a 0nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is 47Ω in series with 3.2pF at 315MHz and 47Ω in series with 3.5pF at 433.92MHz.

Note 3: The voltage conversion gain is measured with the LNA input matching inductor, the degeneration inductor, and the LNA/mixer resonator in place, and does not include the IF filter insertion loss.

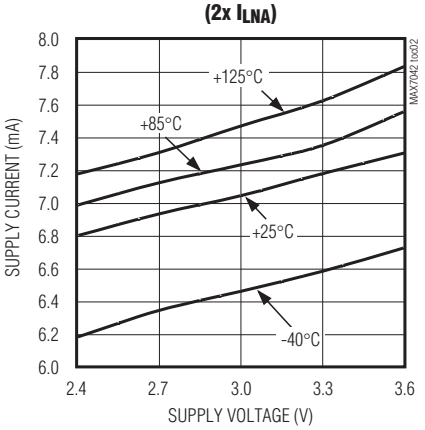
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DD} = 3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2%, T_A = +25°C, unless otherwise noted.)

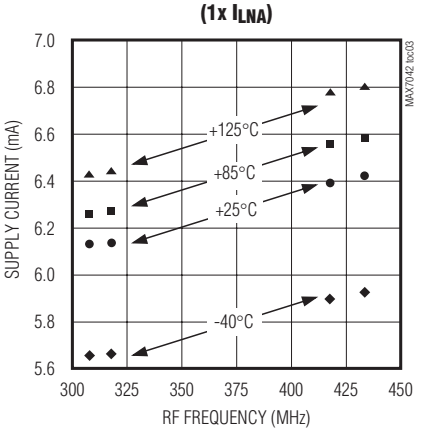
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1x I_{LNA})



SUPPLY CURRENT vs. SUPPLY VOLTAGE (2x I_{LNA})



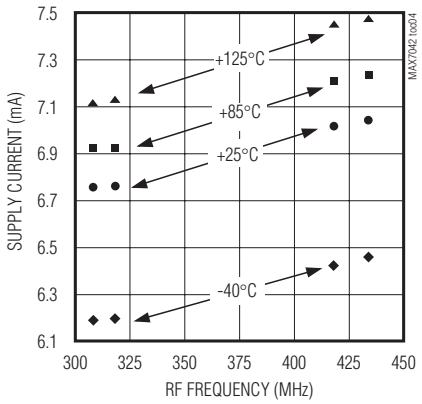
SUPPLY CURRENT vs. RF FREQUENCY (1x I_{LNA})



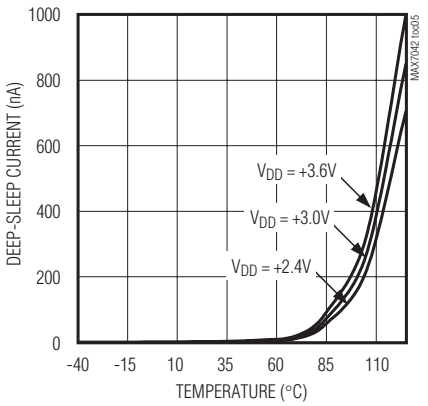
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD} = 3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2%, T_A = +25°C, unless otherwise noted.)

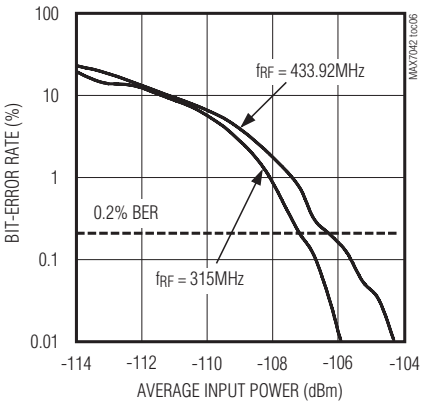
SUPPLY CURRENT vs. RF FREQUENCY (2x I_{LNA})



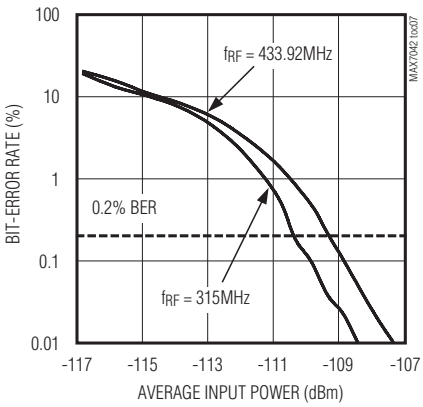
DEEP-SLEEP CURRENT vs. TEMPERATURE



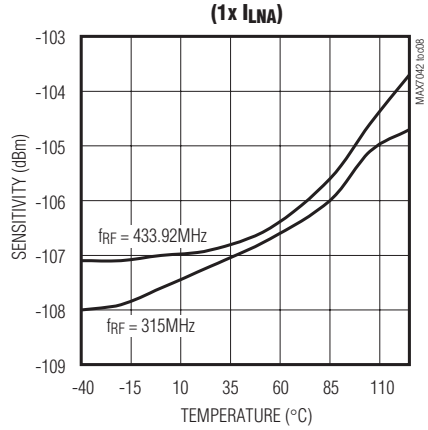
BIT-ERROR RATE vs. AVERAGE INPUT POWER (1x I_{LNA})



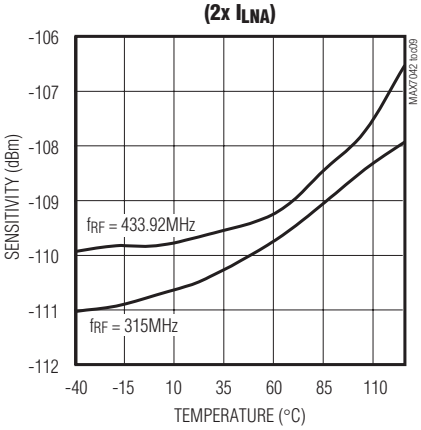
BIT-ERROR RATE vs. AVERAGE INPUT POWER (2x I_{LNA})



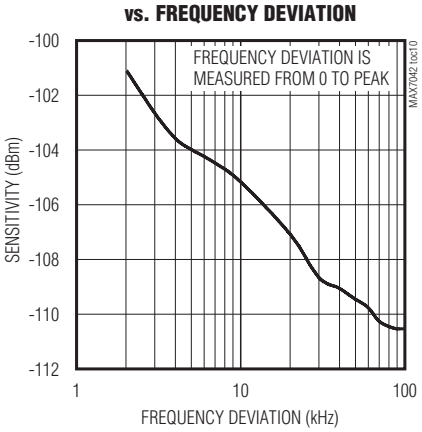
SENSITIVITY vs. TEMPERATURE (1x I_{LNA})



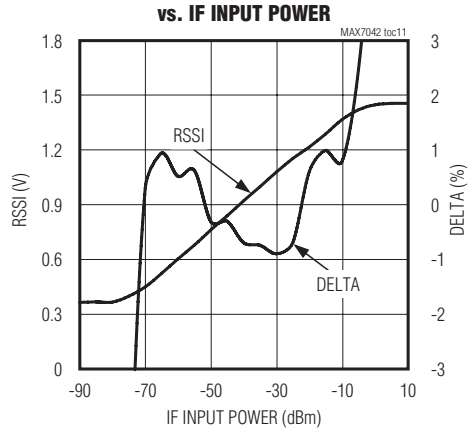
SENSITIVITY vs. TEMPERATURE (2x I_{LNA})



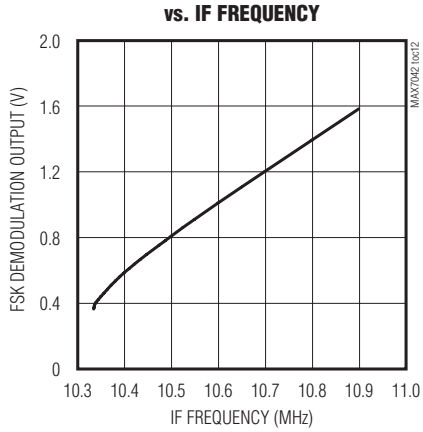
SENSITIVITY vs. FREQUENCY DEVIATION



RSSI AND DELTA vs. IF INPUT POWER



FSK DEMODULATOR OUTPUT vs. IF FREQUENCY

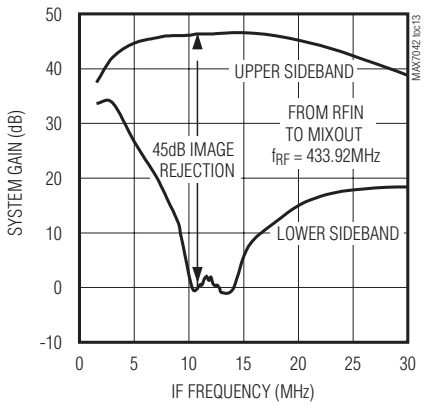


308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD} = 3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2%, T_A = +25°C, unless otherwise noted.)

SYSTEM GAIN vs. IF FREQUENCY (1x I_{LNA})



SYSTEM GAIN vs. IF FREQUENCY (2x I_{LNA})

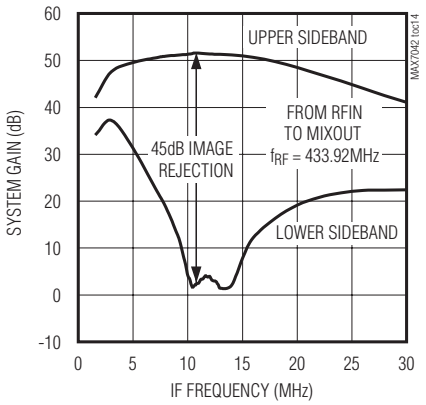


IMAGE REJECTION vs. TEMPERATURE (1x I_{LNA})

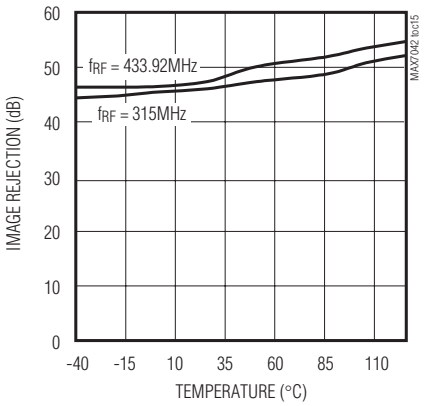
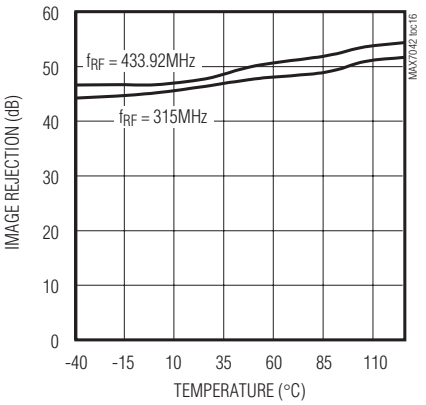
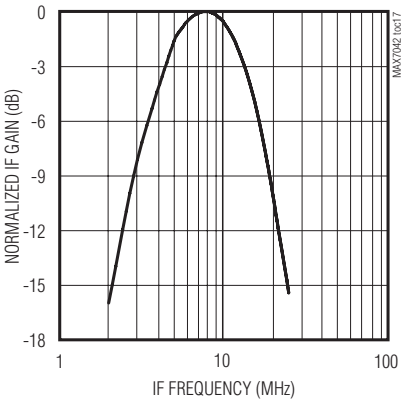


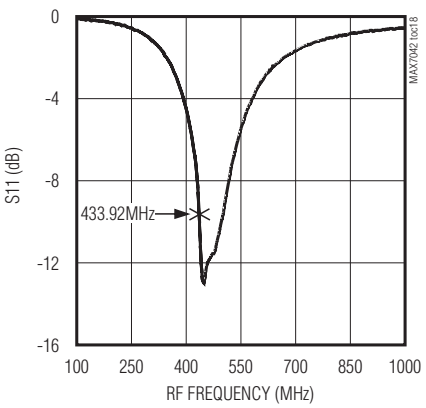
IMAGE REJECTION vs. TEMPERATURE (2x I_{LNA})



NORMALIZED IF GAIN vs. IF FREQUENCY



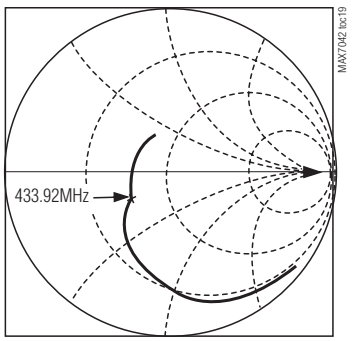
S11 vs. RF FREQUENCY



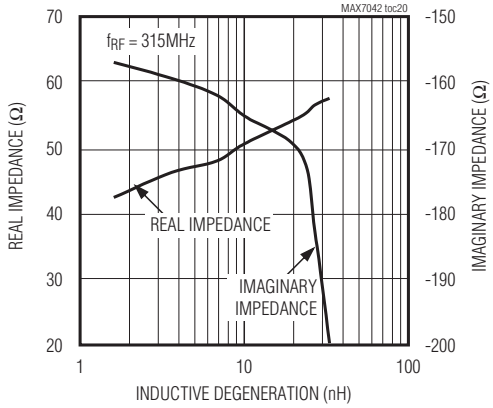
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD} = 3.0V, f_{RF} = 433.92MHz, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2%, T_A = +25°C, unless otherwise noted.)

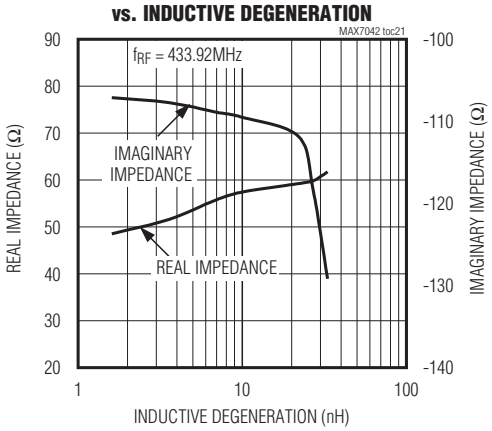
S11 SMITH PLOT OF R_{FIN}



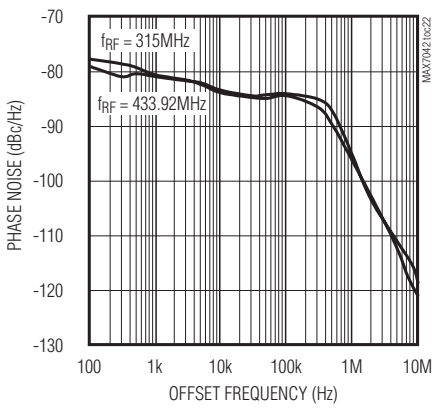
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



PHASE NOISE vs. OFFSET FREQUENCY



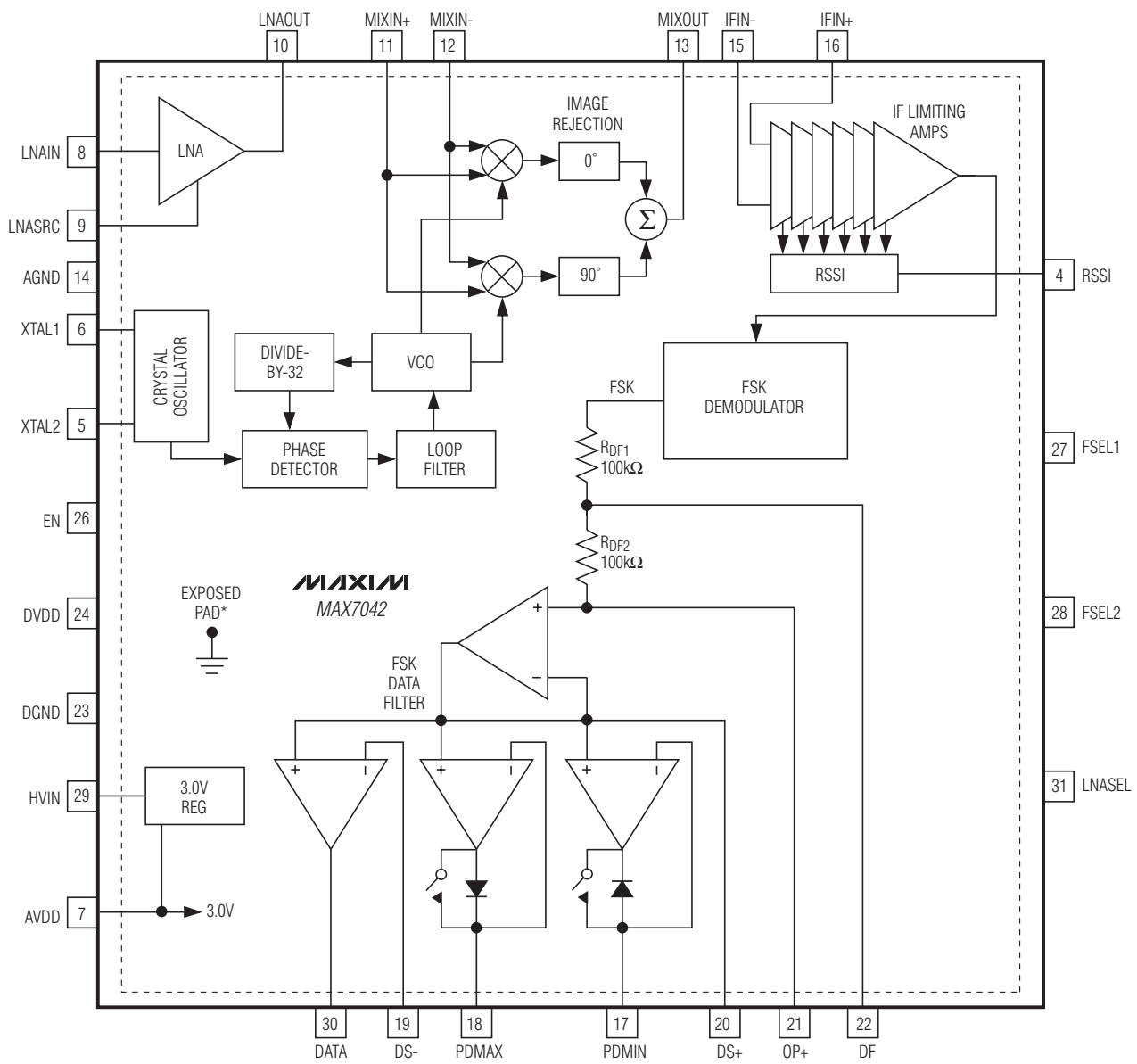
308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

Pin Description

PIN	NAME	FUNCTION
1, 2	N.C.	No Connection. Internally pulled down.
3, 25, 32	N.C.	No Connection. Not internally connected.
4	RSSI	Buffered Received-Signal-Strength-Indicator Output
5	XTAL2	Crystal Input 2. XTAL2 can be driven from an AC-coupled external reference.
6	XTAL1	Crystal Input 1. Bypass to GND if XTAL2 is driven by an AC-coupled external reference.
7	AVDD	Analog Power-Supply Voltage. AVDD is connected to an on-chip +3.0V regulator in +5V operation. Bypass AVDD to GND with 0.1µF and 220pF capacitors placed as close to the pin as possible.
8	LNAIN	Low-Noise Amplifier Input. Must be AC-coupled.
9	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect an inductor to GND to set the LNA input impedance.
10	LNAOUT	Low-Noise Amplifier Output. Connect to V_{AVDD} through a parallel LC tank filter. AC-couple to MIXIN+.
11	MIXIN+	Noninverting Mixer Input. Must be AC-coupled to the LNA output.
12	MIXIN-	Inverting Mixer Input. Bypass to V_{AVDD} or AGND with a capacitor.
13	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz IF filter.
14	AGND	Analog Ground
15	IFIN-	Inverting 330Ω IF Limiter Amplifier Input. Bypass to AGND with a capacitor.
16	IFIN+	Noninverting 330Ω IF Limiter Amplifier Input. Connect to the output of the 10.7MHz IF filter.
17	PDMIN	Minimum-Level Peak Detector for Demodulator Output
18	PDMAX	Maximum-Level Peak Detector for Demodulator Output
19	DS-	Inverting Data-Slicer Input
20	DS+	Noninverting Data-Slicer Input
21	OP+	Noninverting Op-Amp Input for the Sallen-Key Data Filter
22	DF	Data-Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
23	DGND	Digital Ground
24	DVDD	Digital Power-Supply Voltage. Bypass to DGND with 0.01µF and 220pF capacitors placed as close to the pin as possible.
26	EN	Enable. Internally pulled down. Drive high for normal operation. Drive low or leave unconnected to put the device into shutdown mode.
27	FSEL1	Frequency-Select Pin 1 (see Table 1). Internally pulled down. Connect to EN for logic-high operation.
28	FSEL2	Frequency-Select Pin 2 (see Table 1). Internally pulled down. Connect to EN for logic-high operation.
29	HVIN	High-Voltage Supply Input. For +3V operation, connect HVIN to AVDD and DVDD. For +5V operation, connect only HVIN to +5V. Bypass HVIN to AGND with 0.01µF and 220pF capacitors placed as close to the pin as possible.
30	DATA	Receiver Data Output
31	LNASEL	LNA Bias Current Select Pin. Internally pulled down. Set LNASEL to logic-low for low LNA current and set LNASEL to logic-high for high LNA current. Connect to EN for logic-high operation.
EP	GND	Exposed Pad. **Connect to ground.**

308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

Functional Diagram



*MUST BE CONNECTED TO AGND.

308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver

Detailed Description

The MAX7042 CMOS superheterodyne receiver and a few external components provide a complete FSK receive chain from the antenna to the digital output data. FSK uses the difference in frequency of the carrier to represent a logic 0 and logic 1. Depending on signal power and component selection, data rates as high as 66kbps NRZ can be achieved.

Frequency Selection

The MAX7042 can be tuned to one of four frequencies using the 2 frequency-select bits FSEL1 and FSEL2: 308, 315, 418, and 433.92MHz, as shown in Table 1. The LO frequencies are 32 times the crystal reference frequencies of 9.29063, 9.50939, 12.72813, and 13.22563MHz. The selected crystal frequency is used to calibrate the FSK detector PLL so that it operates at the middle of the 10.7MHz IF.

Table 1. Frequency Selection Table

FSEL2	FSEL1	FREQUENCY (MHz)
0	0	308
0	1	315
1	0	418
1	1	433.92

Low-Noise Amplifier (LNA)

The LNA is a cascode amplifier with off-chip inductive degeneration. The gain and the noise figure are dependent on both the antenna matching network at the LNA input and the LC tank network between the LNA output and the mixer input.

The MAX7042 allows for user programmability of the LNA bias current. Input LNASEL programs 1x to 2x bias currents in increments of 0.6mA from 0.6mA to 1.2mA. Setting LNASEL to logic-low programs the LNA to consume 1x bias current and setting LNASEL to logic-high programs the LNA to consume 2x bias current. Larger bias currents yield better sensitivity and gain at the expense of current drain.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible match to a low-input impedance such as printed circuit board (PCB) trace antenna. A nominal value of this inductor for a 50Ω input impedance is 3.9nH at 315MHz and 0nH (short) at 433.92MHz, but is affected by the PCB trace. See the *Typical Operating Characteristics* for the relationship between the inductance and input impedance.

The LC tank filter connected to LNAOUT consists of L2 and C9 (see the *Typical Application Circuit*). Select L2 and C9 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where $L_{TOTAL} = L2 + L_{PARASITICS}$ and $C_{TOTAL} = C9 + C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation is required to optimize the center frequency of the tank. The parasitic capacitance is generally 5pF to 7pF.

There are two ways to verify experimentally that the resonant frequency of the tank is centered at the desired RF frequency:

1) Drive the crystal oscillator externally and sweep both the RF frequency and the LO frequency (FXTAL x 32) to keep the IF at 10.7MHz while monitoring the RSSI voltage (pin 4). There is a peak in the RSSI voltage at resonance. The external source must be AC-coupled into XTAL1 and the XTAL2 pin must have an AC bypass to ground. The recommended drive power is -10dBm.
2) Use a network analyzer to measure the resonance. The port 1 power from the network analyzer is input to the receiver, and this power must be -30dBm or less. A coaxial stub with the center conductor exposed (commonly called an RF “sniffer” is used to monitor the tank power and serves as the port 2 input to the network analyzer. The sniffer should be placed in close proximity to, but not actually touching, the tank inductor.

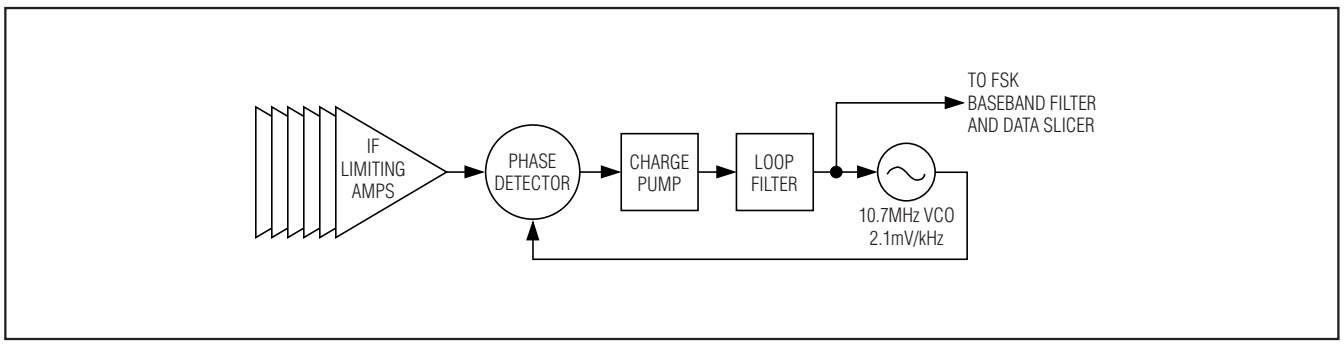


Figure 1. FSK Demodulator PLL Block Diagram

Mixer

A unique feature of the MAX7042 is the integrated image rejection of the mixer. This device is designed to eliminate the need for a costly front-end SAW filter in many applications. The advantages of not using a SAW filter are increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double-balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz intermediate frequency (IF) with low-side injection (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve a typical image rejection of approximately 45dB. Low-side injection is required as high-side injection is not possible due to the on-chip image rejection. The IF output is driven by a source follower, biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. Note that MIXIN+ and MIXIN- are functionally identical.

Phase-Locked Loop (PLL)

The PLL block contains a phase detector, charge pump/integrated loop filter, voltage-controlled oscillator (VCO), asynchronous 32x frequency divider, and crystal oscillator. This PLL does not require any external components. The relationship between the RF, IF, and crystal reference frequencies is given by:

$$f_{XTAL} = \frac{(f_{RF} - f_{IF})}{32}$$

For additional information on proper crystal selection, see the *Crystal Oscillator* and *Frequency Tolerance* sections.

Intermediate Frequency (IF)

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The internal six AC-coupled limiting amplifiers produce an overall gain of approximately 65dB. The limiting amplifiers have a bandpass-filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz. The limiter output is fed into a PLL to demodulate the IF, producing a baseband voltage with a demodulation slope of 2.1mV/kHz. The RSSI circuit produces a DC output proportional to the log of the IF signal level with a slope of approximately 16mV/dB.

FSK Demodulator

The FSK demodulator uses an integrated 10.7MHz PLL that tracks the input RF modulation and determines the difference between frequencies as logic ones and zeros. The PLL is illustrated in Figure 1. The input to the PLL comes from the output of the IF limiting amplifiers. The PLL control voltage responds to changes in the frequency of the input signal with a nominal gain of 2.1mV/kHz. For example, an FSK peak-to-peak deviation of 50kHz generates a $105mV_{P-P}$ signal on the control line. This control line is then filtered and sliced by the FSK baseband circuitry.

The FSK demodulator PLL requires calibration to overcome variations in process, voltage, and temperature. The maximum calibration time is 120µs, which is included in the startup time. Recalibration is necessary after a significant change in temperature or supply voltage. Calibration occurs automatically each time the MAX7042 is powered up. Drive EN low and then high to force a recalibration. EN must be driven from low to high after the MAX7042 supply voltage is stable for proper initial FSK calibration.

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Crystal Oscillator

The XTAL oscillator in the MAX7042 is used to generate the LO for mixing with the received signal. The XTAL oscillator frequency sets the received signal frequency as:

$$f_{RECEIVE} = (f_{XTAL} \times 32) + 10.7MHz$$

The received image frequency at:

$$f_{IMAGE} = (f_{XTAL} \times 32) - 10.7MHz$$

is suppressed by the integrated quadrature image-rejection circuitry.

The XTAL oscillator in the MAX7042 is designed to present a capacitance of approximately 3pF between XTAL1 and XTAL2. In most cases, this corresponds to a 4.5pF load capacitance applied to the external crystal when typical PCB parasitics are added. It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX7042 crystal oscillator plus PCB parasitics. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its intended operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher.

In reality, the oscillator pulls every crystal. A crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_p = \frac{C_m}{2}\left(\frac{1}{C_{case}+C_{load}} - \frac{1}{C_{case}+C_{spec}}\right) \times 10^6$$

where:

f_p is the amount the crystal frequency is pulled in ppm.

C_m is the motional capacitance of the crystal.

C_{case} is the case capacitance.

C_{spec} is the specified load capacitance.

C_{load} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{load} = C_{spec}$, the frequency pulling equals zero.

Frequency Tolerance

The frequency tolerance of the crystal, the frequency and bandwidth tolerance of the IF filter, and the desired modulation bandwidth of the signal are all interrelated. The combination of these characteristics should be such to ensure that the modulated signal bandwidth stays within the passband of the IF filter after downconversion. As is shown below, a 50ppm tolerance crystal in combination with a 280kHz bandwidth IF filter is sufficient for most FSK-modulated signals.

Smaller IF filter bandwidths can be used if high-tolerance crystals are used for generating both transmitter and MAX7042 receiver PLL references. The modulated spectrum of the transmitted signal must be downconverted by the MAX7042 to fall within the passband of the IF filter. The crystal tolerances must take into account the initial +25°C tolerance, aging, load capacitance tolerances, and temperature drift for both the transmitter and MAX7042 receiver. To achieve acceptable signal reception, the following equation must hold:

$$2 \times (\Delta F_{TX} + \Delta F_{RX} + \Delta F_{IF} + F_{DEV} + 5 \times F_{MOD}) < IFBW_{min}$$

where:

ΔF_{TX} = (transmitter crystal tolerance in ppm) x (carrier frequency in MHz). This includes aging, load capacitance, and temperature effects for the crystal tolerance.

ΔF_{RX} = (MAX7042 crystal tolerance in ppm) x (carrier frequency in MHz). This includes aging, load capacitance, and temperature effects for the crystal tolerance.

ΔF_{IF} = The center frequency tolerance of the selected IF filter. This includes temperature drift of the IF filter center frequency.

F_{DEV} = ±FSK frequency deviation from carrier frequency.

F_{MOD} = One half of NRZ data rate, or the data rate if Manchester coding is used.

$IFBW_{min}$ = The minimum bandwidth of the selected IF filter.

As an example, assume 315MHz carrier frequency, ±50ppm crystal tolerances for both transmitter and MAX7042, ±30kHz IF filter center frequency tolerance, ±50kHz frequency deviation, and 4.8kHz Manchester data rate:

$$2 \times [(315 \times 50) + (315 \times 50) + 30000 + 50000 + 5 \times 4800] = 271kHz < IFBW_{min}$$

This operating condition necessitates a 280kHz IF filter.

Data Filters

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency in kHz should be to approximately the fastest expected data rate in kbps for NRZ and twice the fastest expected data rate in kbps for Manchester coding from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 2 creates a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of the capacitors, use the following equations along with the coefficients in Table 2:

$$C_{F1} = \frac{b}{a(100k\Omega)(\pi)(f_C)}$$

$$C_{F2} = \frac{a}{4(100k\Omega)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, choose a Butterworth filter response with a 5kHz corner frequency:

$$C_{F1} = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C_{F2} = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C_{F1} to 470pF and C_{F2} to 220pF. In the *Typical Application Circuit*, C_{F1} and C_{F2} are named C4 and C3, respectively.

Table 2. Coefficients to Calculate C_{F1} and C_{F2}

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

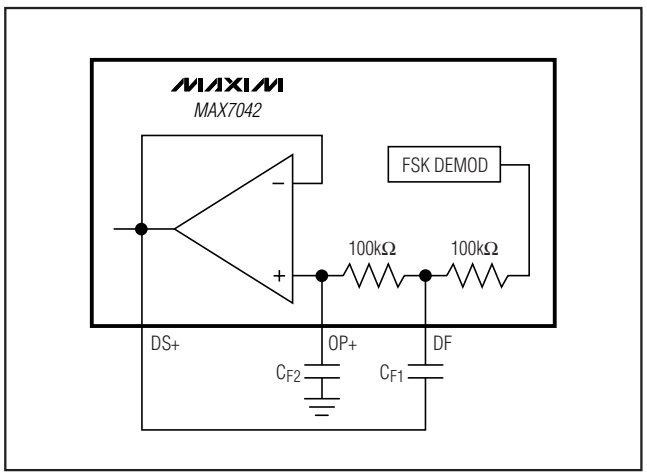

Figure 2. Sallen-Key Lowpass Data Filter

Data Slicer

The purpose of a data slicer is to take the analog output of a data filter and convert it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. The threshold voltage is set by the voltage on the DS- pin, which is connected to the negative input of the data-slicer comparator. The positive input of the data-slicer comparator is connected to the output of the data filter internally.

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Numerous configurations can be used to generate the data-slicer threshold. For example, the circuit in Figure 3 shows a simple method using only one resistor and one capacitor. This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R and C affect how fast the threshold tracks the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

With this configuration, a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

Figure 4 shows a configuration that uses the positive and negative peak detectors to generate the threshold. This configuration sets the threshold to the midpoint between a high output and a low output of the data filter.

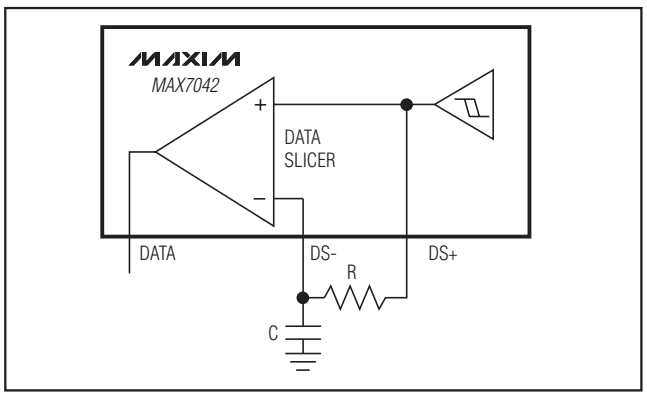

Figure 3. Generating Data-Slicer Threshold

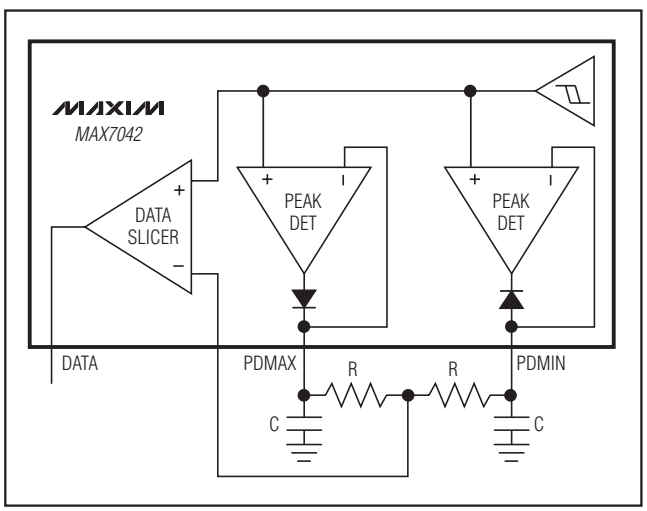

Figure 4. Generating Data-Slicer Threshold Using the Peak Detectors

Peak Detectors

The maximum peak detector (PDMAX) and minimum peak detector (PDMIN) outputs, in conjunction with a resistor and capacitor connected to GND, create DC output voltages proportional to the high- and low-peak values of the data signal. The resistor provides a path for the capacitor to discharge, allowing the peak detector to dynamically follow peak changes of the data-filter output voltage.

The positive and negative peak detectors can be used together to form a data-slicer threshold voltage at a midvalue between the most positive and most negative voltage levels of the data stream (see the *Data Slicers* section and Figure 4). Set the RC time constant of the peak-detector combining network to at least 5 times the data period.

The MAX7042 peak detectors track the baseband filter output voltage until all internal circuits are stable following an enable pin low-to-high transition. This feature allows for an extremely fast startup because the peak detectors never “catch” a false level created by a startup transient. The peak detectors exhibit a fast-attack/slow-decay response.

Power-Supply Connections

The MAX7042 can be powered from a 2.4V to 3.6V supply or a 4.5V to 5.5V supply. The device has an on-chip linear regulator that reduces the 5V supply to 3V needed to operate the chip.

To operate the MAX7042 from a 3V supply, connect DVDD, AVDD, and HVIN to the 3V supply. When using a 5V supply, connect the supply to HVIN only, and connect AVDD to DVDD. In both cases, bypass DVDD and HVIN with a 0.01µF capacitor and AVDD with a 0.1µF capacitor. Place all bypass capacitors as close to the respective supply pin as possible.

Control Interface Considerations

When operating the MAX7042 with a +4.5V to +5.5V supply voltage, the LNASEL, FSEL1, FSEL2, and EN pins can be driven by a microcontroller with either 3V or 5V interface logic levels. When operating the MAX7042 with a +2.4V to +3.6V supply, the microcontroller must produce logic levels tha conform to the V_{IH} and V_{IL} specifications in the *DC Electrical Characteristics Table*.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all power-supply connections.

Typical Application Circuit

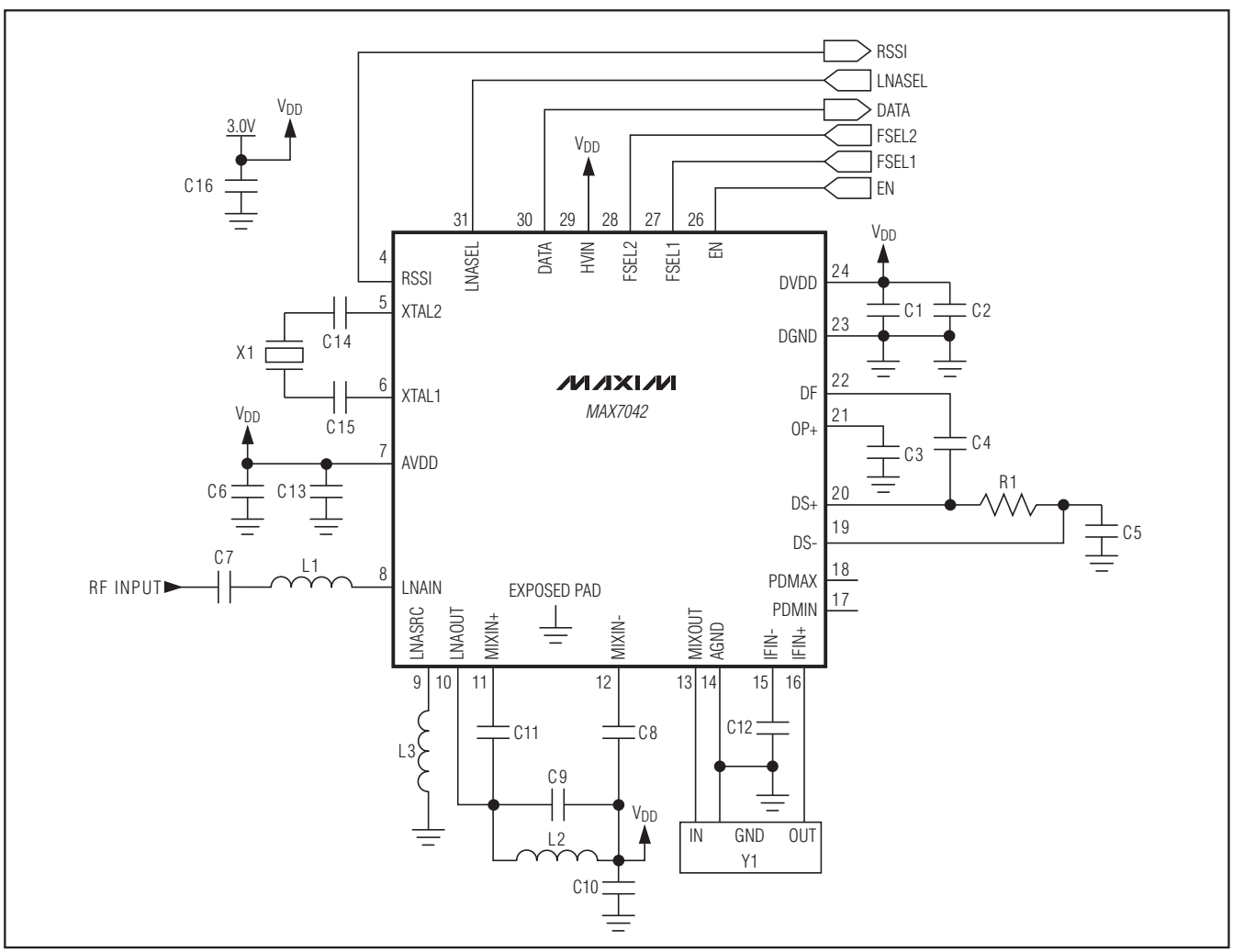

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Table 3. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR 315MHz RF	VALUE FOR 433.92MHz RF	DESCRIPTION
C1	0.01µF	0.01µF	5%
C2	220pF	220pF	5%
C3	220pF	220pF	5%
C4	470pF	470pF	5%
C5	0.047µF	0.047µF	10%
C6	0.1µF	0.1µF	10%
C7	100pF	100pF	10%
C8	100pF	100pF	10%
C9	1.2pF	Open	±0.1pF
C10	220pF	220pF	10%
C11	100pF	100pF	10%
C12	1500pF	1500pF	10%
C13	220pF	220pF	10%
C14	100pF	100pF	10%
C15	100pF	100pF	10%
C16	0.01µF	0.01µF	10%
L1	82nH	39nH	5% or better*
L2	30nH	16nH	5% or better*
L3	3.9nH	Short	5% or better*
R1	100kΩ	100kΩ	5%
X1	9.50939MHz	13.22563MHz	Crystal, 4.5pF C_{LOAD}, Crystek or Hong Kong X'tals
Y1	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata

*Wirewound recommended.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	21-0140	90-0001

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/12	Updated *Ordering Information*, *Absolute Maximum Ratings*, *DC and AC Electrical Characteristics*, TOCs 5, 6, 7, 11; updated *Pin Configuration*, *Pin Description*, *Functional Diagram*, *Phase-Locked Loop* section, *Power-Supply Connections* section, Typical Application Circuit, and Table 3.	1–5, 8, 9, 11, 14, 15, 16