MAX71020A

Energy Measurement AFE

General Description

The MAX71020A is a single-chip analog front-end (AFE) for use in embedded energy measurement applications. It contains the compute engine (CE) found in fourth-generation Teridian meter system-on-chips (SoCs) and an improved analog-to-digital converter (ADC). It interfaces to a host controller of choice over a SPI interface.

The MAX71020A comes in a 28-pin TQFN package.

Applications

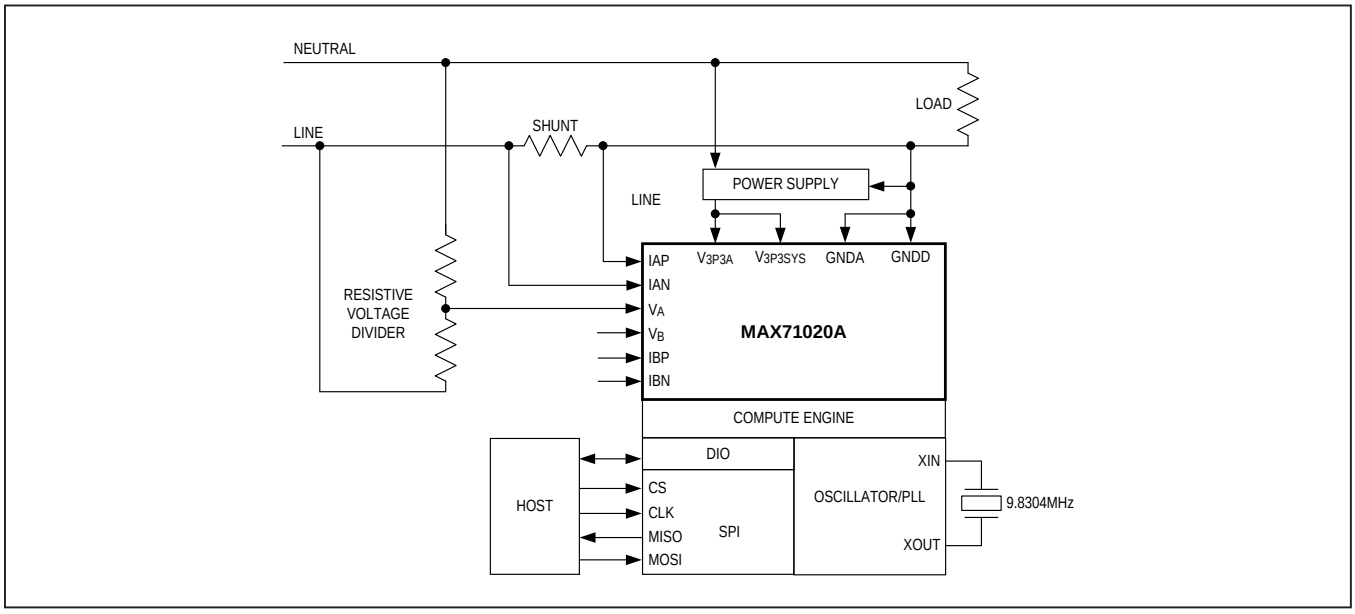
- Grid-Friendly Appliances and Smart Plugs
- Power Distribution Units
- Building Automation Systems

***Ordering Information* appears at end of data sheet.**

Benef ts and Features

- Best-in-Class Embedded Algorithms Support Highly Accurate Electricity Measurements
  - Voltage, Current, and Frequency
  - Active, Reactive, and Apparent Power/Energy
  - Digital Temperature Compensation
  - 40Hz–70Hz Line Frequency Range and Phase Compensation (±10°)
- Advanced AFE with Exceptional Accuracy and Temperature Stability
  - Voltage Reference Temperature Coeff cient: 40ppm/°C (max)
  - On-Chip Digital Temperature Sensor
  - 24-Bit 2nd Order Delta-Sigma ADCs with Differential and Single-Ended Inputs
  - ±0.1% Wh Accuracy over 2000:1 Current Range
- Highly Integrated Features Support Compact Design Cycles and Reduced Bill of Materials
  - Small, 28-Pin TQFN Package
  - Digital Temperature Compensation
  - Low Power Consumption
  - Less Than 5mA (typ) Consumption at 3.3V
  - Simple Host Interface
  - SPI Slave
  - Atomic Measurements Outputs
  - DIO or SPI-Based Status Signals

Typical Operating Circuit



Absolute Maximum Ratings

(All voltages with respect to GNDA.)

Voltage and Current Supplies and Ground Pins

V_{3P3SYS}, V_{3P3A} .....-0.5V to +4.6V
GNDD .....-0.1V to +0.1V

Analog Input Pins

AP, IAN, IBP, IBN,
VA, VB .....(-10mA to +10mA), (-0.5V to +0.5V)
XIN, XOUT.....(-10mA to +10mA), (-0.5V to +3.0V)

Digital Pins

Inputs.....(-10mA to +10mA), (-0.5V to +6V)
Outputs .....(-10mA to +10mA), (-0.5V to (V_{3P3SYS} + 0.5V)

Temperature and ESD Stress

Operating Junction Temperature (peak, 100ms).....+140°C
Operating Junction Temperature (continuous) .....+125°C
Storage Temperature Range ..... -45°C to +165°C
ESD Stress on All Pins.....±4kV, HBM
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS					
V_{3P3SYS} and V_{3P3A} Supply Voltage	Precision metering operation	3.0		3.6	V
	Digital operation (Notes 2, 3)	2.8		3.6	
Operating Temperature		-40		+85	°C
INPUT LOGIC LEVELS					
Digital High-Level Input Voltage (V_{IH})			2		V
Digital Low-Level Input Voltage (V_{IL})			0.8		V
Input Pullup Current (I_{IL}) RESETZ	V_{3P3SYS} = 3.6V, V_{IN} = 0V	41	78	115	µA
Input Pullup Current (I_{IL}) Other Digital Inputs	V_{3P3SYS} = 3.6V, V_{IN} = 0V	-1	0	+1	µA
Input Pulldown Current (I_{IH}) All Pins	V_{IN} = V_{3P3SYS}	-1	0	+1	µA

Electrical Characteristics (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS					
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{3P3SYS} - 0.4			V
	I_{LOAD} = 15mA (Note 3)	V_{3P3SYS} - 1.1			
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA (Note 3)	0		0.96	
TEMPERATURE MONITOR					
TNOM (Nominal value at 22°C)	V_{3P3A} = 3.3V		956		LSB
Temperature Measurement Equation			Temp = 0.33 x STEMP + 21.77		°C
Temperature Error (Note 4)	T_A = -40°C to +85°C	-6		+6	°C
	T_A = -20°C to +60°C	-4.8		+4.8	
Duration of Temperature Measurement After Setting TEMP_START	TEMP_PER = 0	15		60	ms
SUPPLY CURRENT PERFORMANCE SPECIFICATIONS					
V_{3P3A} + V_{3P3SYS} Current (Note 4)	V_{3P3A} = V_{3P3SYS} = 3.3V, CE_E = 1, ADC_E = 1		3	4.3	mA
INTERNAL POWER-FAULT COMPARATOR SPECIFICATIONS					
Overall Response Time	100mV overdrive, falling	20		200	µs
	100mV overdrive, rising	8		200	
Falling Threshold	3.0V comparator	2.83	2.93	3.03	V
	2.8V comparator	2.75	2.81	2.89	V
	Difference 3.0V and 2.8V comparators	50	136	220	mV
Hysteresis (Rising Threshold Falling Threshold)	3.0V comparator, T_A = +22°C	17	45	74	mV
	2.8V comparator, T_A = +22°C	15	42	70	
PLL PERFORMANCE SPECIFICATIONS					
PLL Power-Up Settling Time	V_{3P3A} = 0 to 3.3V step, measured from f rst edge of MCK		75		µs
PLL_FAST Settling Time	V_{3P3A} = 3.3V, PLL_FAST rise		10		µs
	V_{3P3A} = 3.3V, PLL_FAST fall		10		
PLL Lock Frequency at XOUT	V_{3P3A} = 3.3V, MCK frequency error < 1%	7	9.8	13	MHz

Electrical Characteristics (continued)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} PERFORMANCE SPECIFICATIONS						
V_{REF} Output Voltage, $V_{REF\ (22)}$	T_A = +22°C		1.200	1.205	1.210	V
V_{REF} Power-Supply Sensitivity (DVREF/DV3P3A)	V_{3P3A} = 3.0V to 3.6V		-1.5		+1.5	mV/V
V_{NOM} Def nition			$V_{NOM(T)} = V_{REF(22)} + TC1 (T - 22) + TC2(T - 22)2$			V
V_{NOM} Temperature Coeff cient TC1			29.32 - 1.05 x TRIMT			µV/°C
V_{NOM} Temperature Coeff cient TC2			-0.56 - 0.004 x TRIMT			µV/°C^2
VREF(T) Deviation from VNOM(T): $\frac{VREF(T) - VNOM(T)10^6}{VNOM(T)\ 62}$	(Note 4)		-40		+40	ppm/°C
ADC CONVERTER PERFORMANCE SPECIFICATIONS						
Recommended Input Range (with Respect to GNDA)	V_A, V_B, IBP, IBN		-250		+250	mV_{PK}
Recommended Input Range (with Respect to GNDA)	IAP, IAN: preamplif er enabled		-27.78		+27.78	mVpk
	IAP, IAN: preamplif er disabled		-250		+250	
Input Impedance, No Preamplif er	f_{IN} = 65Hz		50		100	kΩ
ADC Gain Error Vs. % of Supply Variation $\frac{10^6 \Delta NOUT_{PK}\,357nV/V_{IN}}{100\,\Delta V_{3P3A}\ /\ 3.3}$	V_{IN} = 200mV peak, 65Hz; V_{3P3A} = 3.0V, 3.6V				81	ppm/%
Input Offset	IAP = IAN = GNDA		-10		+10	mV
Total Harmonic Distortion at $250mV_{PK}$	V_{IN} = 55Hz, $250mV_{PK}$, 64kpts FFT, Blackman-Harris window			-85		dB
Total Harmonic Distortion at $20mV_{PK}$	V_{IN} = 55Hz, $20mV_{PK}$, 64kpts FFT, Blackman-Harris window			-90		dB
LSB Size (LSB Values Do Not Include the 9-Bit Left Shift at the CE Input)	V_{IN} = 55Hz, $20mV_{PK}$, 64kpts FFT, Blackman-Harris window, 10MHz ADC clock	FIRLEN = 15		120.46		nV
		FIRLEN = 14		146.20		
		FIRLEN = 13		179.82		
		FIRLEN = 12		224.59		
		FIRLEN = 11		285.54		
		FIRLEN = 10		370.71		

Electrical Characteristics (continued)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Full Scale	V_{IN} = 55Hz, 400mV$_{PK}$, 10MHz ADC clock	FIRLEN = 15		±2621440		LSB
		FIRLEN = 14		±2160000		
		FIRLEN = 13		±1756160		
		FIRLEN = 12		±1406080		
		FIRLEN = 11		±1105920		
		FIRLEN = 10		±851840		
PREAMPLIFIER PERFORMANCE SPECIFICATIONS						
Differential Gain (V_{IN} = 28mV Differential)	T_A = +25°C, V_{3P3A} = 3.3V, preamplif er enabled			8.9		
Differential Gain (V_{IN} = 15mV Differential)	T_A = +25°C, V_{3P3A} = 3.3V, preamplif er enabled			8.9		V/V
Gain Variation vs. V_{3P3A} (V_{IN} = 28mV Differential)	V_{3P3A} = 3.0V, 3.6V			-72		ppm/%
Gain Variation vs. Temperature (V_{IN} = 28mV Differential)	T_A = -40°C to +85°C			-45		ppm/°C
Phase Shift (V_{IN} = 28mV Differential)	T_A = +25°C, V_{3P3A} = 3.3V (Note 4)		0		8	m°
Preamplif er Input Current (I_{IAP})	Preamplif er enabled, I_{ADC0} = I_{ADC1} = GNDA		9	15	20	µA
Preamplif er Input Current (I_{IAN})						
Preamplif er and ADC Total Harmonic (V_{IN} = 28mV Differential)	T_A = +25°C; V_{3P3A} = 3.3V, PRE_E = 1			-80		dB
Preamplif er and ADC Total Harmonic Distortion (V_{IN} = 15mV Differential)	T_A = +25°C; V_{3P3A} = 3.3V, PRE_E = 1			-85		dB
SPI SLAVE TIMING SPECIFICATIONS						
SPI Setup Time	SPI_DI to SPI_CK rise		10			ns
SPI Hold Time	SPI_CLK rise to SPI_DI		10			ns
SPI Output Delay	SPI_CLK fall to SPI_D0				40	ns
SPI Recovery Time	SPI_CSZ fall to SPI_CLK		10			ns
SPI Removal Time	SPI_CLK to SPI_CSZ rise		15			ns
SPI Clock High			40			ns
SPI Clock Low			40			ns
SPI Clock Frequency					10	MHz
SPI Transaction Space (SPI_ CSZ Rise to SPI_CSZ Fall)			1			µs

Electrical Characteristics (continued)

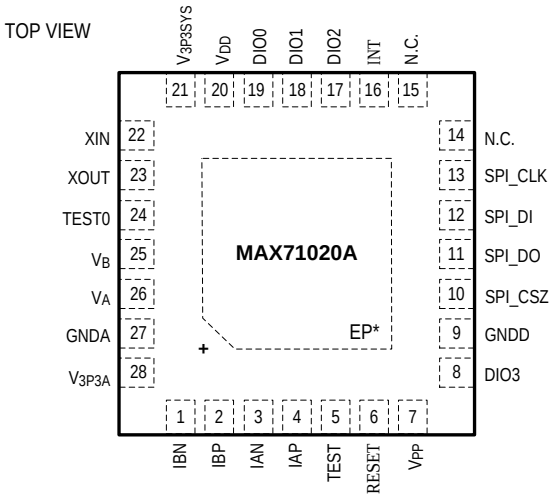
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET TIMING					
Reset Pulse Width	Following power-on	1			ms
	At all other times	5			µs
Reset Pulse Rise Time	(Note 4)			1	µs
VOLTAGE MONITOR					
Nominal Value at +22°C (V_{NOM})	V_{3P3A} = 3.3V		130		LSB
Voltage Measurement Equation			$V_{3P3SYS(CALC)}$ = 3.29V + (V_{SENSE} - 130) x 0.025V + STEMP x 242µV		
Voltage Error $100\left(\frac{V_{3P3SYS}(CALC)}{V_{3P3SYS}}-1\right)$		-4		+4	%

Note 2: V_{3P3SYS} and V_{3P3A} must be connected together.
Note 3: GNDA and GNDD must be connected together.
Note 4: Guaranteed by design, not production tested.

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	V_{3P3A}	GNDA	Bypass capacitor for 3.3V supply	≥ 0.1 ±20%	µF
CSYS	V_{3P3SYS}	GNDD	Bypass capacitor for V_{3P3SYS}	≥ 1.0 ±30%	µF
C1P8	V_{DD}	GNDD	Bypass capacitor for V_{1P8} regulator	0.1 ±20%	µF
XTAL	XIN	XOUT	Crystal	9.8304	MHz
CXS	XIN	GNDA	Load capacitor values for crystal depend on crystal specif cations and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance.	32 ±10%	pF
CXL	XOUT	GNDA		32 ±10%	pF

Pin Conf guration



Pin Description

PIN	SIGNAL	TYPE	FUNCTION
1	IBN	I	Negative Current Input Channel B. Not used. Connect to GNDA.
2	IBP	I	Positive Current Input Channel B. Not used. Connect to GNDA.
3	IAN	I	Negative Current Input Channel A
4	IAP	I	Positive Current Input Channel A
5	TEST	I	Test Input. Connect to GNDD.
6	RESET	I	Active-Low Reset Input
7	V_{PP}	I	Programming Voltage. Not used; connect to GNDD.
8	DIO3	I/O	Multiple-Use Pins. Conf gurable as DIO.
9	GNDD	P	Digital Ground. GNDD should be connected directly to the ground plane.
10	SPI_CSZ	I	SPI Slave Select
11	SPI_DO	O	SPI Serial Data Master Input Slave Output
12	SPI_DI	I	SPI Serial Data Master Output Slave Input
13	SPI_CLK	I	SPI Serial Clock
14, 15	N.C.	I	No Connection
16	INT	I/O	Active-Low Interrupt Request
17	DIO2	I/O	Multiple-Use Pins. Conf gurable as DIO.
18	DIO1	I/O	Multiple-Use Pins. Conf gurable as DIO.
19	DIO0	I/O	Multiple-Use Pins. Conf gurable as DIO.
20	V_{DD}	I/O	Output of the 1.8V Regulator. Connect a 0.1µF bypass capacitor to ground to this pin.

Pin Description (continued)

PIN	SIGNAL	TYPE	FUNCTION
21	V_{3P3SYS}	P	System 3.3V Supply. Connect V_{3P3SYS} to a 3.3V power supply.
22	XIN	I	Crystal Input
23	XOUT	O	Crystal Output
24	TEST0	I	Test Input. Connect to GNDD.
25	V_B	I	Line Voltage Sense Input VB. Unused, connect to GNDA.
26	V_A	I	Line Voltage Sense Inputs V_A
27	GNDA	P	Analog Ground. Connect GNDA directly to the ground plane.
28	V_{3P3A}	P	Analog Power Supply. Connect a 3.3V power supply to V_{3P3A}. V_{3P3A} must be the same voltage as V_{3P3SYS}.
—	—	—	Exposed Pad. On bottom.

Detailed Description

Hardware Description

The MAX71020A analog front-end (AFE) integrates the functional blocks required to implement accurate energy measurement functions. Included on the chip are:

- An analog front-end (AFE) featuring a 22-bit second order delta-sigma ADC
- An independent 32-bit digital computation engine (CE) implementing DSP functions
- A precision voltage reference (VREF)
- A temperature sensor for digital temperature sensing and compensation
- Four I/O pins
- A zero-crossing detector with interrupt output
- Resistive shunt and current transformers are supported
- A SPI slave for connection to a host controller

In a typical application, the 32-bit compute engine (CE) of the MAX71020A sequentially processes ADC samples from the Voltage and Current inputs and performs calculations to measure voltage and current RMS, power, active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the host processor. In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement. Temperature-dependent external components such as crystal oscillator, resistive shunts, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to further improve system's accuracy. The MAX71020A features an SPI (slave) interface for communication with the host processor. The communication protocol between the host and the MAX71020A provides a redundant information transfer ensuring the correctness of commands transferred from the host to the AFE, and of data transferred from the AFE to the host.

In addition, the MAX71020A has one pin dedicated as an interrupt output to the host. This pin notifies the host of asynchronous events.

ADC Description

Analog Inputs

The MAX71020A has four analog inputs: two single-ended inputs for voltage measurement, and two differential inputs for current measurement.

The IAP, IAN, IBP, and IBN pins are current sensor inputs. IBP/IBN input are not used and should be connected to GNDA. The differential inputs feature preamplifiers with a selectable gain of 1 or 9, and are intended for direct connection to a shunt resistor sensor or a current transformer (CT).

The voltage inputs in the MAX71020A are single-ended, and are intended for sensing the line voltage via resistive dividers. These single-ended inputs are referenced to the GNDA pin..

All analog signal input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. In the case of current transformers (CT), the current is measured as a voltage across a burden resistor that is connected to the secondary winding of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers.

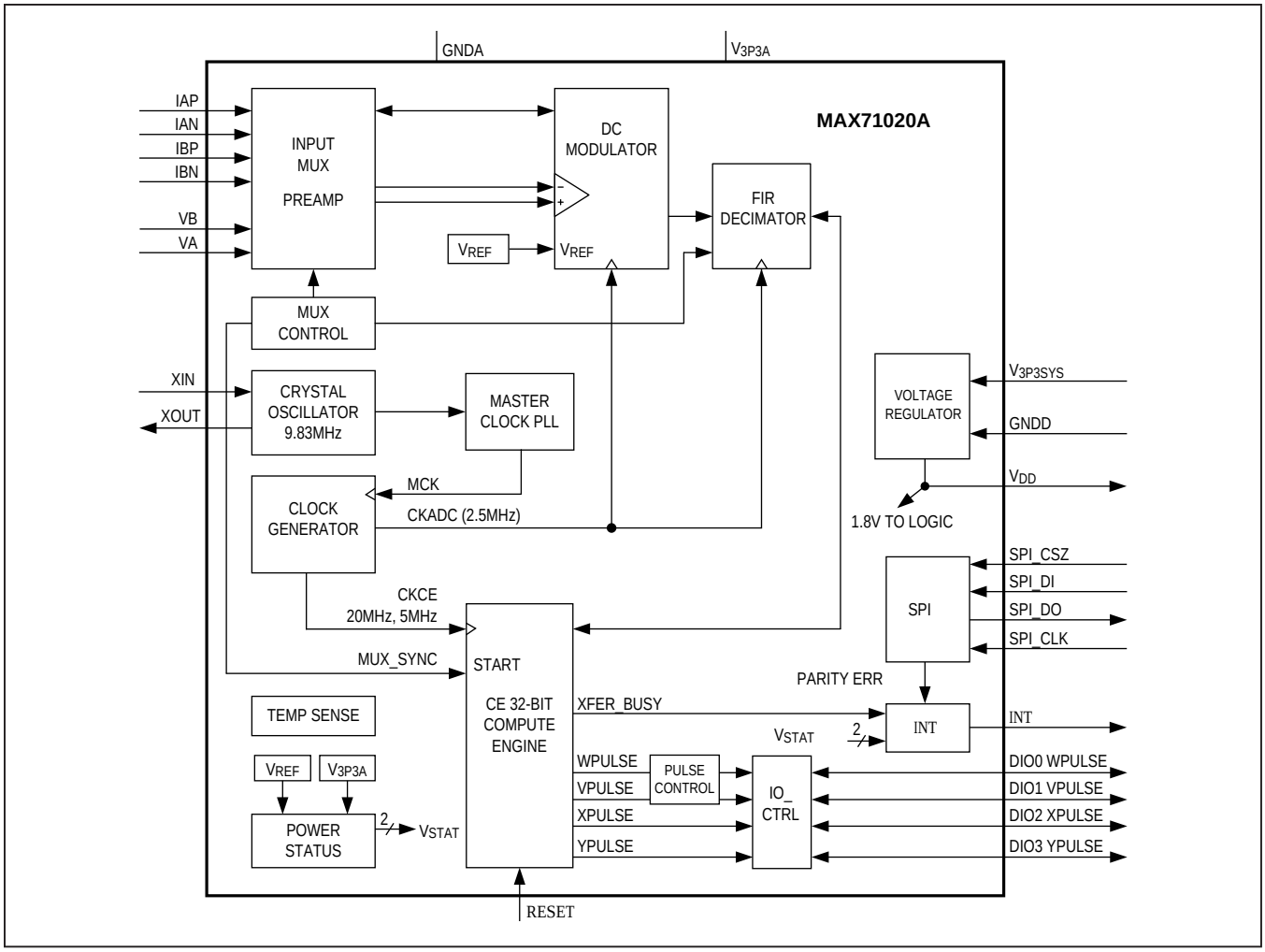


Figure 1. Functional Diagram

ADC Preamplif er

The ADC preamplifier is a low-noise differential amplifier with a fixed gain of 8.9 available on the IAP and IAN current-sensor input pins. When using a device with the preamplifier enabled, the input signal amplitude cannot be greater than 27.78mV peak. The preamplifier can be enabled/disabled through register settings.

Analog-to-Digital Converter (ADC)

A single second-order delta-sigma ADC digitizes the voltage and current inputs to the device. The resolution of the ADC is dependent on several factors. Initiation of each ADC conversion is automatically controlled by logic internal to the MAX71020A. At the end of each ADC conversion, the FIR filter output data is stored into the register determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left 9 bits.

FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the register determined by the multiplexer selection.

Voltage References

A bandgap circuit provides the reference voltage (V_{REF}) to the ADC. Since the V_{REF} bandgap amplifier is chopper stabilized, the DC offset voltage, which is the most significant long-term drift mechanism in the voltage reference (V_{REF}), is automatically removed by the chopper circuit.

Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time)
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme)
- 90° phase shifter (for VAR calculations)
- Monitoring of the input signal frequency (for frequency and phase information)
- Monitoring of the input signal amplitude (for sag detection)
- Scaling of the processed samples based on calibration coeff cients
- Scaling of samples based on temperature compensation information
- Gain and phase compensation

Temperature Sensor

The MAX71020A includes an on-chip temperature sensor for determining the temperature of its bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system for the compensation of current, voltage, and energy measurement. The temperature sensor is awakened on command from the host controller by setting the TEMP_START control bit. The host controller must wait for the TEMP_START bit to clear before reading STEMP[15:0] and before setting the TEMP_START bit once again. The result of the temperature measurement can be read from the STEMP[15:0] register. The 16-bit value is in two's complement form and ranges from -1024 to +1023 (decimal). The sensed temperature can be computed from the 16-bit STEMP[15:0] reading using the following formula:

$$\text{Temp (°C)} = 0.33 \times \text{STEMP} + 21.77$$

An additional register, VSENSE[7:0], senses the level of the supply voltage. Table 1 shows the registers used for temperature measurement.

Table 1. Temperature Measurement Registers

NAME	RST	DIR	DESCRIPTION	
TEMP_PER[1:0]	0	R/W	Sets the period between temperature measurements.	
			TEMP_PER	**TIME**
			0	Manual updates (see TEMP_START description)
			1	Every accumulation cycle
			2	Continuous
			3	No updates
TEMP_START	0	R/W	TEMP_PER[1:0] must be zero in order for TEMP_START to function. If TEMP_PER[1:0] = 0, then setting TEMP_START starts a temperature measurement. Hardware clears TEMP_START when the temperature measurement is complete. The host controller must wait for TEMP_START to clear before reading STEMP[10:0] and before setting TEMP_START again.	
STEMP[15:0]	—	R	The result of the temperature measurement.	
VSENSE[7:0]	—	R	The result of the temperature measurement. See the formula listed in the *Electrical Characteristics* table.	

Digital I/O

On reset or power-up, all DIO pins are configured as high impedance. DIO pins can be configured independently by the host controller by manipulating the D0, D1, D2, and D3 bit fields.

SPI Slave Port

The slave SPI port communicates directly with the host controller and allows it to read and write the device control registers. The interface to the slave port consists of the SPI_CSZ, SPI_CLK, SPI_DI, and SPI_DO pins. The host can also reset the MAX71020A through the SPI port by writing a data pattern to the RESET register.

SPI Transactions

SPI transactions are configured to provide immunity to electrical noise through redundancy in the command segment and error checking in the data field. The MAX71020A SPI transaction is exactly 64 bits; transactions of any other length are rejected. Each SPI transaction has the following fields (Table 2):

- A 24-bit setting packet, consisting of:
  - 11-bit address, MSB f rst
  - 1-bit direction (1 means read)
  - 11-bit inverted address, MSB f rst
  - 1-bit inverted direction
- An 8-bit status, consisting of the following bits concerning the last transaction, starting from bit 7:
  - Parity of the status byte (0 or 1 could be correct)
  - FIFO overf ow status bit (1 means error)
  - FIFO underrun status bit (1 means error)
  - Read or write data parity (0 or 1 could be correct) (never both read and write; address is not included in the parity)
  - Address or direction mismatch error bit (1 means error) (1: error, 0: no error)
  - A bit indicating whether or not the bit count was exactly 64 (1 means error)
  - Out of bounds address, most likely due to SPI safe bit or the memory manager (1 means error)
- A 32-bit packet of data, MSB f rst

If extra clocks are provided at the end during a read, all zero is output and the status continues to be updated, signaling an error. If extra clocks are provided at the end during a write, the write is aborted and the status is updated to signal an error.

- None of the f elds above are optional.
- If an error is detected during the address or direction phase, no action is taken.
- SPI_DO is high-Z while SPI_CSZ is high.
- SPI safe mode is supported, and SPI is not locked out of this bit during SPI safe.

A typical SPI transaction is as follows. While SPI_CSZ is high, the port is held in an initialized/reset state. During this state, SPI_DO is held in high-Z state and all transitions on SPI_CLK and SPI_DI are ignored. When SPI_CSZ falls, the port begins the transaction on the first rising edge of SPI_CLK. A transaction consists of the fields shown in Table 2.

Note that the status byte indicates the status of the previous SPI transaction except for the status byte parity.

Table 2. SPI Transaction (64 Bits)

24-BIT SETTING FIELD				8-BIT STATUS								32-BIT DATA
Address	Dir	Inv Address	Inv Dir	Status from Previous Transaction: Status[7:0]								Data
addr[10:0]	RD	addr_b[10:0]	RD_b	Status Parity	FIFO OverRun	FIFO UnderRun	Data Parity	Setting Mismatch	Reserved	Bad CK Cnt	Bad Address	data[31:0]

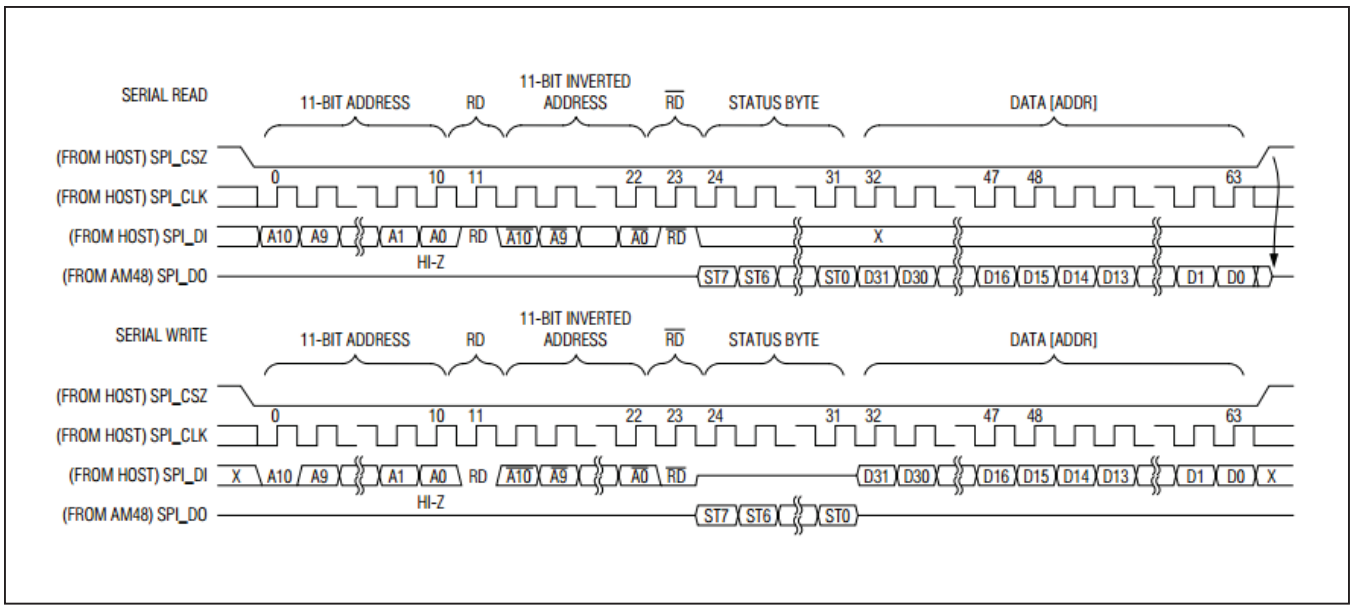


Figure 2. SPI Slave Port—Typical Read and Write Operations

SPI Safe Mode

Sometimes it is desirable to prevent the SPI interface from writing to arbitrary registers and possibly disturbing the CE operation. For this reason, the SPI_SAFE mode was created. In this mode, all SPI writes are disabled except to the word containing the SPI_SAFE bit. This affords the host one more layer of protection from inadvertent writes.

Fault and Reset Behavior

Events at power-down power fault detection is performed by internal comparators that monitor the voltage at the V_{3P3A} pin and also monitor the internally generated V_{DD} pin voltage (1.8V DC). V_{3P3SYS} and V_{3P3A} must be connected together at the PCB level so that the comparators, which are internally connected only to the V_{3P3A} pin, are able to simultaneously monitor the common V_{3P3SYS} and V_{3P3A} voltage. The following discussion assumes that V_{3P3A} and V_{3P3SYS} are connected together at the PCB level. See Table 3.

During a power failure, as V_{3P3A} falls, two thresholds are detected. The first threshold, at 3.0V, warns the host controller that the analog modules are no longer accurate. The second threshold, at 2.8V, warns the host controller that a serious reduction in supply voltage has occurred and that the reliability of OTP reads may be affected.

Reset Sequence

The MAX71020A does not provide automatic reset generation. The reset needs to be generated by the host controller or by external circuitry connected to the RESET pin. When the MAX71020A receives a reset signal, either from the RESET pin or from the SPI (using a write to the RESET register at address 0x322), it asynchronously halts what it was doing. It then clears the RAM and invokes the load engine (LE). The LE initializes RAM and hardware control registers from the CE code image that is stored in OTP memory. Only RAM cells and hardware registers that need not change dynamically are loaded. All other RAM cells and registers have to be loaded by

Table 3. VSTAT[1:0]

VSTAT[1:0]	DESCRIPTION
00	System Power-OK. V_{3P3A} > 3.0V. Analog modules are functional and accurate.
01	System Power is low. 2.8V < V_{3P3A} < 3.0V. Analog modules not accurate.
11	System power below 2.8V. Ability to monitor power is about to fail.

the host controller. The LE automatically refreshes the values of the registers it is tasked with loading during the operation of the MAX71020A. This refresh happens in increments of one register at a time and at a rate of one register per second. An errant reset can occur during EMI events. If this happens, the host controller is notified. This is accomplished by the holding the INT pin low until the host clears the event (the F_RESET bit in the M_STAT register is set to indicate that a reset has occurred).

Connecting to a Host Processor

Host connections include the INT pin, the RESET pin. In the host processor, the DIO pin connected to INT should generate an interrupt. This interrupt signals to the host that an accumulation cycle has been completed and the calculations performed during it, are available in the relevant transfer registers. They remain constant throughout each accumulation interval.

Sensors Connection

Figure 3 shows a typical MAX71020A configuration. The IAP-IAN current channel can be directly connected to either a shunt resistor or a CT. The voltage input V_A is connected to a resistive voltage divider. The IBP-IBN channel, as well as V_B are not used and should be connected to GNDA.

Signal Flow Description

This section reviews the signal processing calculations performed by the compute engine (CE) processor. The sample ADC sample rate is 2520 samples/s. Most of the calculations are performed over a fixed accumulation interval of 2520 samples corresponding to approximately 1s.

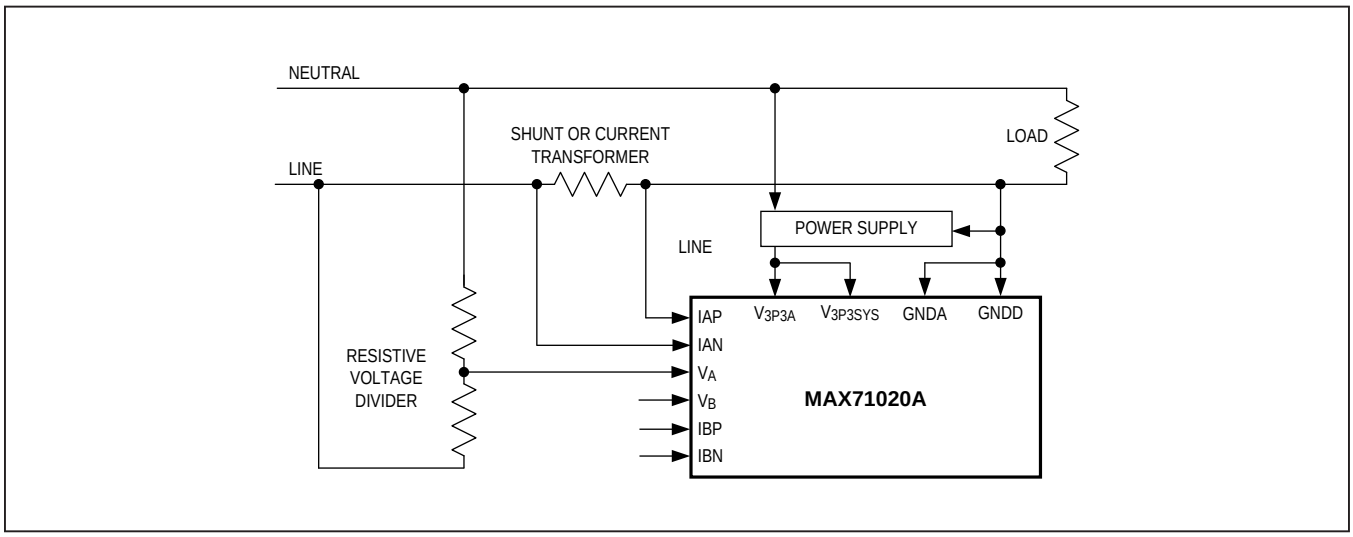


Figure 3. Typical Connection Diagram

Current Input Calculations

The calculation of the current is performed only on the IAN/IAP differential input. Figure 4 shows the signal processing relevant to the current input. In the darker boxes are represented the register accessible through the SPI interface.

The value of N represents the number of samples (SUM_SAMP) in an accumulation interval and it is fixed.

I0SQSUM_X is the sum of the squared voltage samples acquired during the last accumulation interval:

$$I0SQSUM\_X = \sum_{n=0}^{N-1} I0n^2$$

The host processor can complete the RMS calculation as follows:

$$IRMS = \frac{\sqrt{I0SQSUM\_X}}{N}$$

or simply access the I0RMS_X register where the RMS is calculated by the compute engine.

$$I0RMS\_X = \sqrt{I0SQSUM\_X} \times \frac{I0SCALE}{2^{14}}$$

Voltage Input Calculations

The calculation of the current is performed only on the VA single ended input. Figure 5 and Figure 6 show the signal processing relevant to the voltage input. The darker boxes represent the registers that are accessible through the SPI interface.

The value of N represents the number of samples (SUM_SAMP) in an accumulation interval and it is fixed.

V0SQSUM_X is the sum of the squared voltage samples acquired during the last accumulation interval:

$$V0SQSUM\_X = \sum_{n=0}^{N-1} V0n^2$$

The host processor can complete the RMS calculation as follows:

$$VRMS = \frac{\sqrt{V0SQSUM\_X}}{N}$$

or simply access the V0RMS_X register where the RMS is calculated by the compute engine.

$$V0RMS\_X = \sqrt{V0SQSUM\_X} \times \frac{V0SCALE}{2^{14}}$$

Power Calculation

Active power is calculated as the product of the voltage and current waveforms (Figure 7). The resulting waveform is the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The instantaneous power is available as WATTSUM_X as:

$$WATTSUM\_X = \sum_{n=0}^{N-1} V0n \times 10n$$

$$WATTS\_X = WATTSUM\_X \times \left(\frac{PSCALE}{2^{14}} \right)$$

Reactive Power Calculation Energy

All variables are signed 32-bit integers. Accumulated variables such as WSUM are internally scaled so that internal values are no more than 50% of the full-scale range when the integration time is 1s. Additionally, the hardware does not permit output values to fold back upon overflow. WSUM_X and VARSUM_X are the Watt hour and VAR hour signed sum of Phase-A and Phase-B Wh or VARh values according to the metering equation implemented by the CE code. WxSUM_X (x = 0 or 1, registers 0x085 and 0x086) is the watt-hour value accumulated for phase x in the last accumulation interval and can be computed based on the specified LSB value.

Compute Engine (CE) Status and Control

The CE Status Word, CESTATUS, is useful for generating early warnings to the host controller. It contains sag warnings for phase A and B, as well as F0, the derived clock operating at the line frequency. The host controller can read the CE status word at every CE_BUSY interrupt.

CESTATUS provides information about the status of voltage and input AC signal frequency that are useful for generating an early power-fail warning to initiate necessary data storage. CESTATUS represents the status flags for the preceding CE code pass (CE_BUSY interrupt). The CE is initialized by the host controller using CECONFIG. This register contains the SAG_CNT, PULSE_SLOW, and PULSE_FAST fields. The CECONFIG bit. When the SAG_INT bit (register 0x020[20]) is set to 1, a sag event generates.

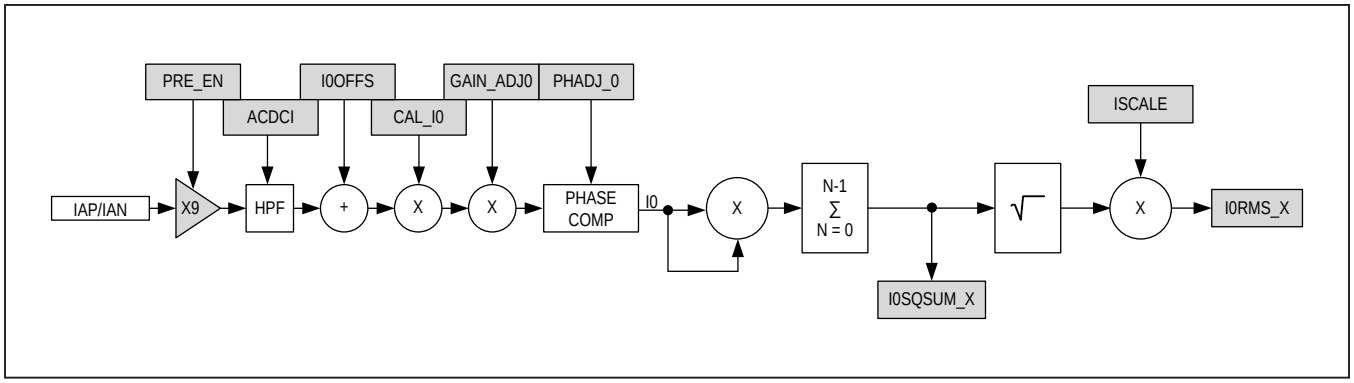


Figure 4. RMS Current Data Path

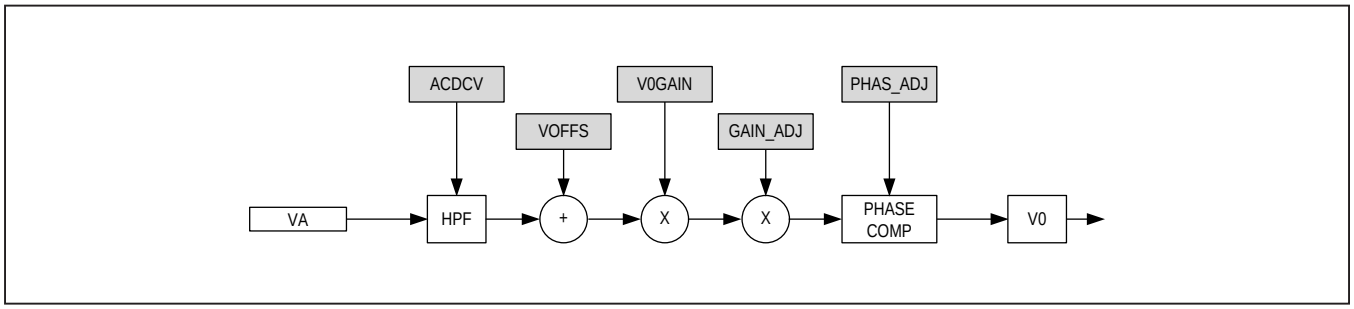


Figure 5. Voltage Signal Data Path

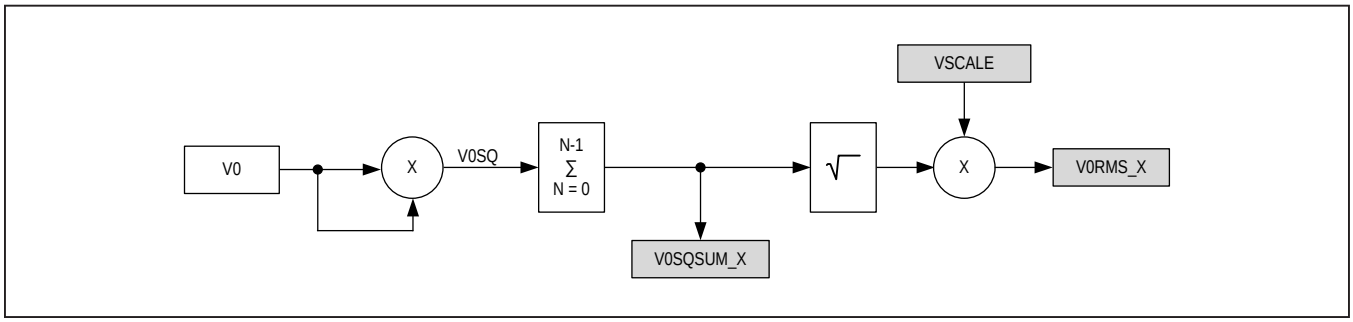


Figure 6. Voltage RMS Data Path

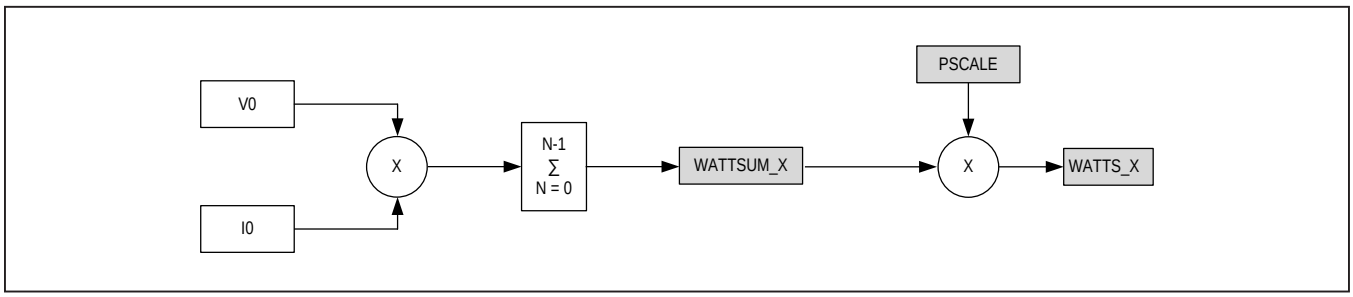


Figure 7. Power Data Path

Register Map

All words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement format (-1 = 0xFFFFFFFF). Calibration parameters are copied to CE data memory by the host controller before enabling the CE. Internal variables are used in internal CE calculations. Input variables allow the MPU to control the behavior of the CE code.

The registers can be read (R), write (W), or read/write (R/W) accessible by the host. The register output register (O) are measurement registers and can only be read by the host processor.

Table 4. Register Map

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	DESCRIPTION	LOADED BY
CAL_I0	0x010	R/W	0x0000 4000	Calibration coeff cient for current channel A.	Host
CAL_V0	0x011	R/W	0x0000 4000	Calibration coeff cient for voltage channel A.	Host
PHADJ_0	0x012	R/W	0x0000 0000	Phase adjust coeff cient for channel A.	Host
I0OFFS	0x013	R/W	0x0000 4000	DC offset constant current channel A	Host
V0OFFS	0x014	R/W	0x0000 4000	DC offset constant voltage channel A	Host
TEMP22	0x015	R/W	0x0000024D	Device temperature default reading	Host
I_SCALE	0x016	R/W	0x00000f6b	Current-scaling constant. See the *User Scaling* section.	Host
V_SCALE	0x017	R/W	0x0000766C	Current-scaling constant. See the *User Scaling* section.	Host
P_SCALE	0x018	R/W	0x0000490A	Current-scaling constant. See the *User Scaling* section.	Host
DEGSCALE	0x01A	R/W	0x0000 6A8F	Device temperature scaling (internal constant)	LE
PPMC1	x01B0	R/W	0x000 0000	Linear coeff cient for temperature compensation. A default coeff cient can be established by copying PPMCATE into PPMC.	Host
PPMC2	x01C	R/W	0x00000000	Quadratic coeff cient for temperature compensation. A default coeff cient can be obtained by copying PPMC2ATE into PPMC2.	Host
PPMCATE1	0x01D	R	N/A	Linear coeff cient for temperature compensation populated at reset.	LE
PPMCATE2	0x01E	R	N/A	Quadratic coeff cient for temperature compensation populated at reset.	LE

Table 4. Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	DESCRIPTION			LOADED BY
CECONFIG	0x020	R/W	0x0030 3301	**Conf guration Register for CE Operation**			Host
				BIT	**NAME**	**DESCRIPTION**	
				31	Reserved		
				30	ACDCV	Voltage HPF controls 1 = enable, 0 = disable	
				29	ACDCV	Current HPF controls 1 = enable, 0 = disable	
				28	DGNDM	Ground reference measurement 1 = enable, 0 = disable	
				27:2324	Reserved	1 = enable, 0 = disable	
				2			
				22	EXT_TEMP	External control of GAIN_ADJn if set	
				21	EDGE_INT	Enables zero-crossing output on XPULSE 1 = enabled, 0 = disabled	
				20	SAG_INT	Enables a sag detect output on YPULSE 1 = enabled, 0 = disabled	
				19:8	SAG_CNT	Number of consecutive samples below SAG_THR before a sag even is declared	
				7:0	Reserved		
WRATE	0x021	R/W	0x00001227	Sets the meter constant for pulses.			Host
KVAR	0x022	R/W	0x00001929	Internal scaling factor for VARh measurements.			LE
SUM_PRE	0x023	O	0x00000800	Actual length of Accumulation interval in samples as measured by the CE. (Information Only)			Host
SAG_THR	0x024	R/W	0x016D 2490	Voltage threshold for sag warnings.			Host
QUANT_V0	0x025	R/W	0x0000 0000	Truncation/noise compensation for voltage in phase A			Host
QUANT_I0	0x026	R/W	0x0000 0000	Truncation/noise compensation for current in phase A			Host
QUANT_P0	0x027	R/W	0x0000 0000	Truncation/noise compensation for real power in phase A			Host

Table 4. Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	DESCRIPTION	LOADED BY
QUANT_QA	0x028	R/W	0x0000 0000	Truncation/noise compensation for reactive power in phase A	Host
CREEP_THR	0x029	R/W	0x0000 9C40	WSUM threshold below which the device squelches outputs	Host
GAINADJ_V0	0x040	R/W	0x0000 4000	Adjusts the amplitude for voltage input VA for temperature compensation. Default = unity gain.	Host
GAINADJ_I0	0x041	R/W	0x0000 4000	Adjusts the amplitude for current input IA. Default = unity gain.	Host
Reserved	0x042–0x043	R/W	0x0000 0000	Reserved register	Host
Reserved	0x044	R/W	0x0000 0000	Reserved register	Host
WPULSE_CTR	0x045	R	—	Pulse counter for Wh (real power)	—
WPULSE_FRAC	0x046	R	—	Pulse generator numerator for Wh (real power)	—
Reserved	0x047	R/W	0x0000 0000	Reserved register	Host
Reserved	0x048	R/W	0x0000 0000	Reserved register	Host
VPULSE_CTR	0x049		—	Pulse counter for VARh (real power)	—
VPULSE_FRAC	0x04A		—	Pulse generator numerator for VARh (real power)	—
Reserved	0x04B		0x0000 0000	Reserved register	Host
	0x04C–0x07F		—	Used by CE for internal variables	—
CESTATUS	0x080	R	—	**Status of Compute Engine** **BIT** — 0 — 1 Reserved 2 Reserved 3 Square wave at exact line frequency 31:4 Reserved	—
TEMP_X	0x81	R		Temperature deviation from TEMP22	—
FREQ_X	0x82	R		Fundamental line frequency (LSB = 2520.6/232Hz)	—
MAINEDGE_X	0x83	R		Number of voltage zero crossings of either direction during the previous accumulation interval	—
—	—	—	—	Reserved	—
W0SUM_X	0x85	R	—	Signed sum of real energy (Wh) from wattmeter element A	—
—	—	—	—	Reserved	—
—	—	—	—	Reserved	—

Table 4. Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	DESCRIPTION	LOADED BY
VAR0SUM_X	0x89	R		Signed sum of reactive energy (VARh) from wattmeter element A	—
—	—	—	—	Reserved	—
I0SQSUM_X	0x8C	R		Sum of squared samples from current sensor in phase A	—
—	—	—	—	Reserved	—
V0SQSUM_X	0x90	R		Sum of squared samples from voltage sensor in phase A	—
V1SQSUM_X	0x91	R		Sum of squared samples from voltage sensor in phase B	—
I0SQRES_X	0x96	R		Residual current from current sensor in phase A	—
VB_AVG_X	0x97	R		Average DC value of VB input sensor	—
I0RMS_X	0x098	R		Scaled current RMS	
V0RMS_X	0x099	R		Scaled voltage RMS	
P0_X	0x09A	R		Scaled active power	
Q0_X	0x09B	R		Scaled reactive power	
I0_RAW_DC	0x09C	R		RAW DC offset/level of current input	
V0_RAW_DC	0x09D	R		RAW DC offset/Level of voltage input	

Table 5. Hardware Control Register Map

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE*	DESCRIPTION
DEVICEID	0x301	R	0x0000(H) 0x1100(L)	Contains identifying information for the device. Loaded by the LE.
STEMP	0x30A	R	—	Result of the temperature measurement. Only bits 26:16 are signif cant; all other bits return zero.
VSENSE	0x30B	R	—	Result of the device V_{3P3SYS} measurement. Only bits 23:16 are signif cant; all other bits return zero.

Table 5. Hardware Control Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE*	DESCRIPTION		
IOCFG	0x30C	R/W	0x0000 0F00	**Contains the Characteristics of the Four Digital I/O Pins**		
				BIT	**NAME**	**DESCRIPTION**
				0	DI0	Ref ects logic state on DIO0
				1	DI1	Ref ects logic state on DIO1
				2	DI2	Ref ects logic state on DIO2
				3	DI3	Ref ects logic state on DIO3
				7:4	Reserved	—
				8	D_OD0	Conf gures DIO0 as open drain if conf gured as output
				9	D_OD1	Conf gures DIO1 as open drain if conf gured as output
				10	D_OD2	Conf gures DIO2 as open drain if conf gured as output
				11	D_OD3	Conf gures DIO3 as open drain if conf gured as output
				15:12	Reserved	—
				17:16	DO	Conf gures DIO0. 00: High impedance 01: WPULSE 10: Logic 1 11: Logic 0
				19:18	D1	Conf gures DIO1. 00: High impedance 01: VPULSE 10: Logic 1 11: Logic 0
				21:20	D2	Conf gures DIO2. 00: High impedance 01: XPULSE 10: XFER_BUSY 11: Logic 0
				23:22	D3	Conf gures DIO3. 00: High impedance 01: YPULSE 10: CE_BUSY 11: Logic
				31:24	Reserved	—
METER_CFG	0x30D	R/W	0xFF00 0080	**Conf gures Hardware Aspects of the AFE**		
				BIT	**NAME**	**DESCRIPTION**
				14:0	Reserved	—
				15	PLS_INV	Force meter pulses to be positive-going rather than negative-going
				23:16	Reserved	—
				31:24	PLS_MAXWID	Determines the maximum width of a meter pulse

Table 5. Hardware Control Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE*	DESCRIPTION		
INT_CFG	0x30F	R/W	0x0000 8000	**Interrupt Conf guration Register: Conf gure the Behavior of the INT Pin**		
				BIT	**NAME**	**DESCRIPTION**
				0	IE_WPULSE	Enables an interrupt to occur on the leading edge of WPULSE
				1	IE_VPULSE	Enables an interrupt to occur on the leading edge of VPULSE
				2	IE_YPULSE	Enables an interrupt to occur on the leading edge of YPULSE
				3	IE_XPULSE	Enables an interrupt to occur on the leading edge of XPULSE
				4	IE_XDATA	Enables an interrupt to occur at the conclusion of the accumulation interval, indicating that fresh data is available
				5	IE_CEBUSY	Enables an interrupt to occur when the CE cycles is complete
				6	Reserved	—
				7	IE_VSTAT	Enables an interrupt to occur when the VSYS status changes
				11:8	INT_POL	Interrupt polarity for the PULSE edges. The default polarity is falling edge. INT_POL[3]=1: Interrupt on rising edge of YPULSE INT_POL[2]=1: Interrupt on rising edge of XPULSE INT_POL[1]=1: Interrupt on rising edge of VPULSE INT_POL[0]=1: Interrupt on rising edge of WPULSE
				14:12	Reserved	—
				15	D_ODINTZ	Enable open-drain on the INT output. By default, the pin is conf gured as a CMOS totem-pole output.
				31:16	Reserved	—

Table 5. Hardware Control Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE*</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="20">M_STAT</td><td rowspan="20">0x310</td><td rowspan="20">R</td><td rowspan="20">0x0100 0100</td><td colspan="3">Ref ects the status of several asynchronous events in the AFE. Bits are automatically cleared after the host controller reads M_STAT.</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>F_WPULSE</td><td>Set on start of WPULSE</td></tr>
<tr><td>1</td><td>F_VPULSE</td><td>Set on start of VPULSE</td></tr>
<tr><td>2</td><td>F_XPULSE</td><td>Set on start of XPULSE</td></tr>
<tr><td>3</td><td>F_YPULSE</td><td>Set on start of YPULSE</td></tr>
<tr><td>4</td><td>F_XDATA</td><td>Set when data available</td></tr>
<tr><td>5</td><td>F_CEBUSY</td><td>Set at end of CE code pass</td></tr>
<tr><td>6</td><td>Reserved</td><td>—</td></tr>
<tr><td>7</td><td>F_VSTAT</td><td>Set when VSYS status changes</td></tr>
<tr><td>8</td><td>F_RESET</td><td>Set following AFE reset</td></tr>
<tr><td>15:9</td><td>Reserved</td><td>—</td></tr>
<tr><td>16</td><td>F_WPULSE</td><td>Copy of bit 0</td></tr>
<tr><td>17</td><td>F_VPULSE</td><td>Copy of bit 1</td></tr>
<tr><td>18</td><td>F_XPULSE</td><td>Copy of bit 2</td></tr>
<tr><td>19</td><td>F_YPULSE</td><td>Copy of bit 3</td></tr>
<tr><td>20</td><td>F_XDATA</td><td>Copy of bit 4</td></tr>
<tr><td>21</td><td>F_CEBUSY</td><td>Copy of bit 5</td></tr>
<tr><td>23:22</td><td>Reserved</td><td>—</td></tr>
<tr><td>24</td><td>F_RESET</td><td>Copy of bit 8</td></tr>
<tr><td>31:25</td><td>Reserved</td><td>—</td></tr>
</table>

Table 5. Hardware Control Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE*</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="20">M_STAT_B</td><td rowspan="20">0x311</td><td rowspan="20">R</td><td rowspan="20">0x0000 0000</td><td colspan="3">Backup of M_STAT. Updated when M_STAT is read. If M_STAT_B is different from M_STAT, it signals to the host that something has changed (status change detect).</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>FB_WPULSE</td><td>Set on start of WPULSE</td></tr>
<tr><td>1</td><td>FB_VPULSE</td><td>Set on start of VPULSE</td></tr>
<tr><td>2</td><td>FB_XPULSE</td><td>Set on start of XPULSE</td></tr>
<tr><td>3</td><td>FB_YPULSE</td><td>Set on start of YPULSE</td></tr>
<tr><td>4</td><td>FB_XDATA</td><td>Set when data available</td></tr>
<tr><td>5</td><td>FB_CEBUSY</td><td>Set at end of CE code pass</td></tr>
<tr><td>7:6</td><td>Reserved</td><td>—</td></tr>
<tr><td>8</td><td>FB_RESET</td><td>Set following AFE reset</td></tr>
<tr><td>15:9</td><td>Reserved</td><td>—</td></tr>
<tr><td>16</td><td>FB_WPULSE</td><td>Copy of bit 0</td></tr>
<tr><td>17</td><td>FB_VPULSE</td><td>Copy of bit 1</td></tr>
<tr><td>18</td><td>FB_XPULSE</td><td>Copy of bit 2</td></tr>
<tr><td>19</td><td>FB_YPULSE</td><td>Copy of bit 3</td></tr>
<tr><td>20</td><td>FB_XDATA</td><td>Copy of bit 4</td></tr>
<tr><td>21</td><td>FB_CEBUSY</td><td>Copy of bit 5</td></tr>
<tr><td>23:22</td><td>Reserved</td><td>—</td></tr>
<tr><td>24</td><td>FB_RESET</td><td>Copy of bit 8</td></tr>
<tr><td>31:25</td><td>Reserved</td><td>—</td></tr>
<tr><td>VSTAT</td><td>0x312</td><td>R</td><td>—</td><td colspan="3">AFE Supply Voltage Status. Bits 1:0 ref ect system power status: 00: System power-OK: V_{3P3A} > 3.0V
01: System power-low: 2.8V < V_{3P3A} < 3.0V 11: System power-fail: V_{3P3A} < 2.8V</td></tr>
<tr><td>RESET</td><td>0x322</td><td>WO</td><td>—</td><td colspan="3">Write 0x8100 0000 to this register to reset the AFE.</td></tr>
<tr><td rowspan="5">TEMP_CNF</td><td rowspan="5">0x323</td><td rowspan="5">R/W</td><td rowspan="5">0x0000 0000</td><td colspan="3">Conf gures Aspects of the Temperature Measurement Subsystem. Loaded by the LE.</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>—</td></tr>
<tr><td>3:2</td><td>TEMP_PER</td><td>Sets the period between temperature measurements.
01: Measure every accumulation cycle
10: Continuous measurement
Other values disable automatic updates.</td></tr>
<tr><td>4</td><td>TEMP_SYS</td><td>When set, V_{3P3SYS} is measured at every temperature measurement cycle</td></tr>
<tr><td>31:5</td><td>Reserved</td><td>—</td></tr>
</table>

Table 5. Hardware Control Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE*	DESCRIPTION
TEMP_START	0x324	R/W	0x0000 0000	Write 0x8000 0000 to start a temperature conversion cycle. When conversion is complete, the AFE clears bit 31 and returns the register to zero.
SPI_SAFE	0x325	R/W	0x0000 0000	Write 0x8000 0000 to this word to lock the SPI port. When the SPI port is locked, no read or write operations are possible except to the SPI_SAFE register. Clearing this register to zero disables the SPI lock and restores normal operation.
METER_EN	0x326	R/W	0x0000 0000	**Enables Aspects of the AFE**

BIT	NAME	DESCRIPTION
0	ADC_E	Enable ADC and VREF buffer. Must be set by host following initialization.
1	CE_E	Enable CE. Must be set by host following initialization.
31:2	Reserved	—

**Default values given for standard CE code (2520 sample frequency, gain = 9).*

Constants Description

FS: ADC sampling rate expressed as $FS = \frac{2^{15}}{13} = 2520.6$

f_0: Fundamental frequency of the mains phase.

SUM_SAMP: Number of ADC samples per accumulation interval. SUM_SAMP = 2520.

X: gain constant of the pulse generators. Its value is determined by PULSE_FAST and PULSE_SLOW.

FSV: Peak line voltage at which the ADC input reaches 0.250 V_{PK}.

VMAX: Represents the line RMS voltage (sine) corresponding to a peak of 250mV_{PK}.

$$V_{MAX} = \frac{FSV}{\sqrt{2}} = 176.8mV_{RMS}$$

FSI: Peak Line current at which the ADC input reaches 0.250 V_{PK} or in case the preamplifer is enabled 27.78mV.

IMAX: Line RMS currents corresponding to the maximum allowed voltage on the current inputs. Corresponding to 176.8mV_{RMS} (or 19.64mV_{RMS} in case the preamplifier is enabled). Example: For a 250µΩ shunt resistor, IMAX becomes 78A (19.64mV_{RMS}/250µΩ = 78.57A) with preamplifier enabled and 707A (176.8mV_{RMS}/250µΩ = 707.2A_{RMS}) with preamplifier disabled.

WOSUM_X LSB = 6.08040 x 10^{-13} x V_{MAX} x I_{MAX} Wh

VAROSUM LSB = 6.08040 x 10^{-13} x V_{MAX} x I_{MAX} VARh

VSAG_THR LSB = V_{MAX} x 7.879810^{-9}V.

The system constants I_{MAX} and V_{MAX} are used by the host controller to convert internal digital quantities (as used by the CE) to external, real-world metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual measurement. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80V_{RMS} is desired at the meter input, the digital value that should be programmed into SAG_THR would be 80V_{RMS} x SQRT(2)/SAG_THR_{LSB}, where SAG_THR_{LSB} is the LSB value in the description of SAG_THR.

Ordering Information

PART	PIN-PACKAGE	IC MARKING
MAX71020AETI+	28 TQFN	7 1 0 2 0 A Y Y W W $ $ # # # @ @
MAX71020AETI+T	28 TQFN	7 1 0 2 0 A Y Y W W $ $ # # # @ @

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

yy: To be substituted with last two digits of year of assembly.

ww: To be substituted with week of assembly.

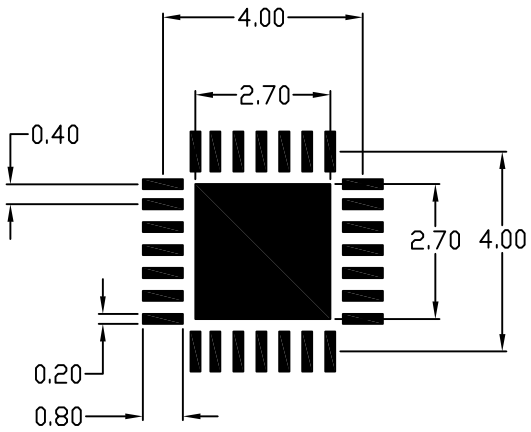
$$: To be substituted with the package revision code from the reliability database.

###: To be substituted with the last 3 numeric characters from the lot number.

@@: To be substituted with the first two alpha characters after the numeric characters from the lot number.

Package Information

Package outline information is appended to this document. Land patterns (footprints) are inserted below.

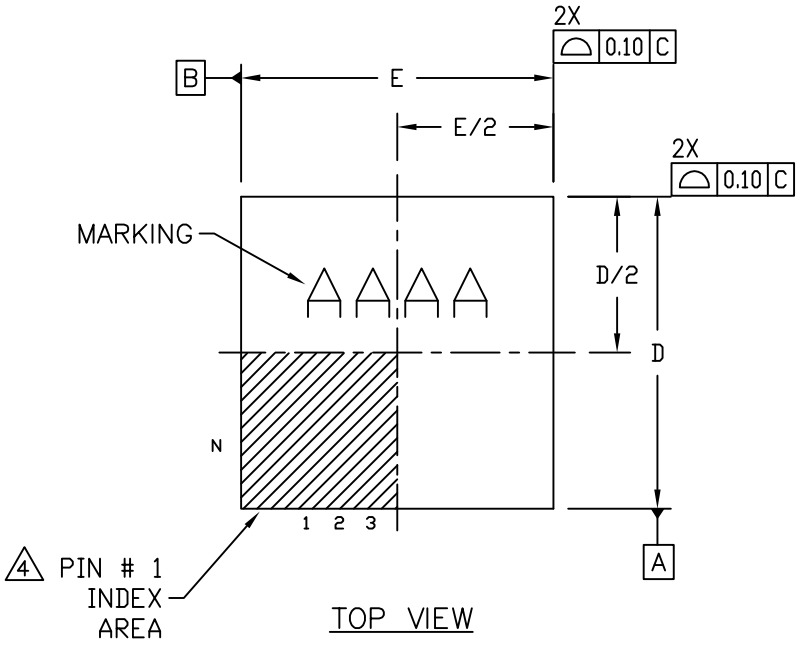


NOTES:

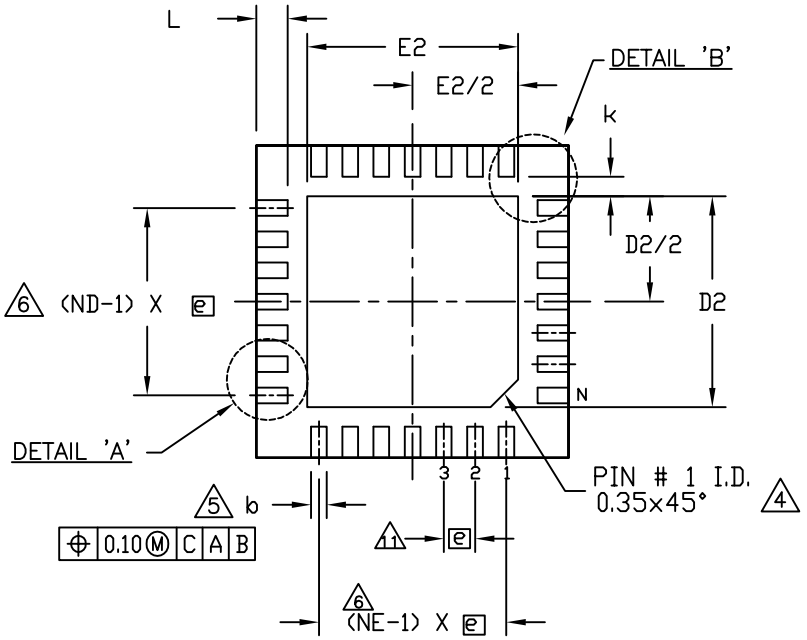
1. LAND PATTERN COMPLIES TO: IPC7351A.
2. TOLERANCE: +/- 0.02 MM.
3. ALL DIMENSIONS IN MM.

Revision History

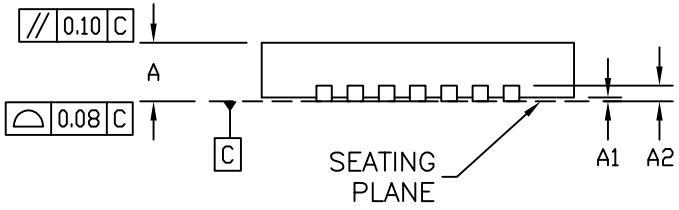
REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	4/16	Rebrand Only	



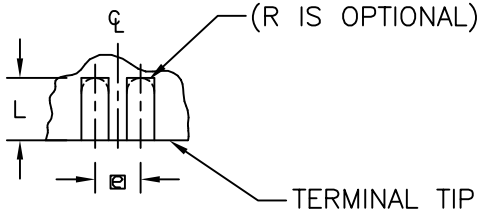
TOP VIEW



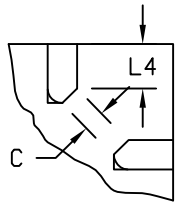
BOTTOM VIEW



SIDE VIEW



DETAIL 'A'



CORNER LEAD CHAMFER VARIATION

DETAIL 'B'

—DRAWING NOT TO SCALE—

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

DIMENSION VARIATIONS										
PKG. CODE	D2			E2			L			R (LEAD TIP RADIUS)
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35	0.125 REF
T2044-4C	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35	0.125 REF
T2044-5	2.60	2.70	2.80	2.60	2.70	2.80	0.35	0.40	0.45	0.203 REF
T2044-5C	2.60	2.70	2.80	2.60	2.70	2.80	0.35	0.40	0.45	0.203 REF

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-3C	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3C	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4C	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2C	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2C	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-3C	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4C	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444MK-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70
2844-1C	2.50	2.60	2.70	2.50	2.60	2.70
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75

Pkg Code: T2844-1

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
14. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–