MAX71071
Dual-Channel Isolated Metrology ADCs

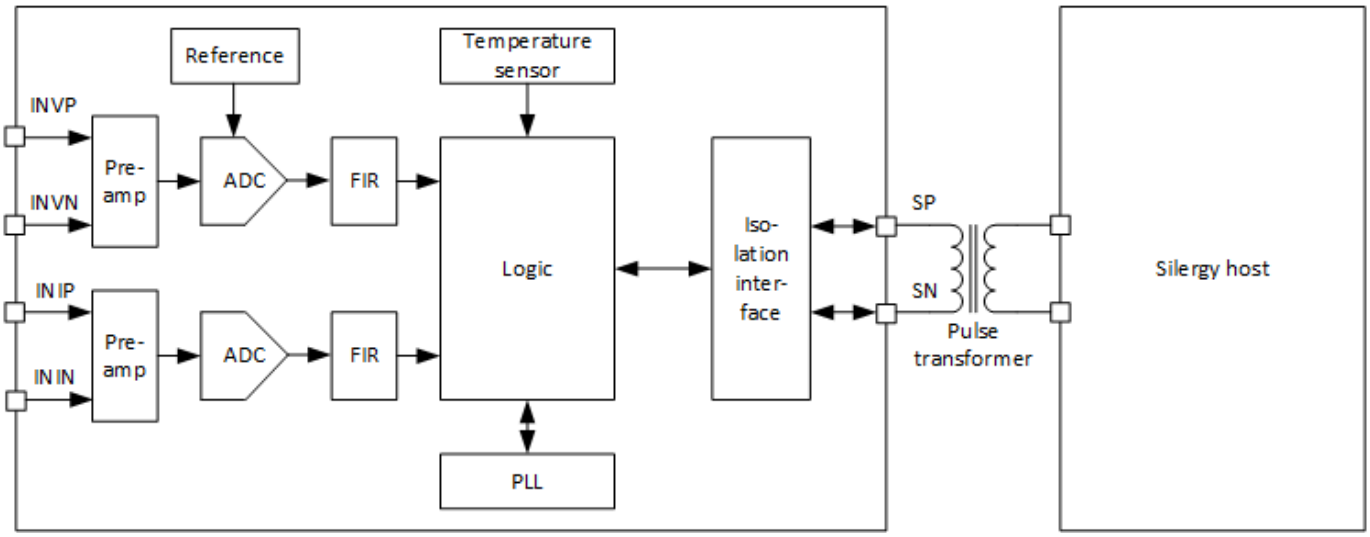
General Description

The MAX71071 are dual-channel isolated analog-to-digital converters (ADCs) for use with a compatible host. The device provides current and voltage measurements to the host while the host provides control, command, and power to the MAX71071. A pulse transformer provides the isolated data, clock, and power path between the device and host, eliminating the need for additional isolation components in the measurement subsystem. These metrology ADCs operate over the industrial temperature range and come in a 10-pin µSOP package.

Benefits and Features

- Accurately Measure Voltage and Current
  - Dual 24-Bit ADC
  - 0.1% Accuracy Over 2000:1 Dynamic Range
  - Exceeds IEC 62053/ANSI C12.20 Standards
  - On-Chip Temperature Sensor Enables Localized Digital Temperature Compensation
- Galvanic Isolation Through Pulse Transformer provides Power, Bidirectional Data, and Timing Reference
  - 1.4mA Typical Consumption
  - On-Chip PLL and Power Monitoring

Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SSA}.)
Supplies and Ground Pins
V_{CC}.....-0.5V to +3.6V
V_{SS} .....-0.1V to +0.1V
Analog Input Pins
INP, INN, SP, SN .....-10mA to +10mA, -0.5V to (V_{CC} + 0.5V)
Digital Pins
TEST.....-10mA to +10mA, -0.5V to +3.6V
Operating Junction Temperature (peak, 100ms).....+140°C
Operating Junction Temperature (continuous) .....+125°C
Storage Temperature..... -45°C to +165°C
Solder Temperature (10s duration) .....+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µSOP
Junction-to-Ambient Thermal Resistance (θ_{JA})
Multilayer Board .....113.10°C/W
Single-Layer Board.....180°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	V_{CC}	V_{SS}	Bypass capacitor for supply	1.0	µF
R1, R2, R3, R4	Sensor	ND	To establish proper bias for INVN/INVP and ININ/INIP pins	1.0	kΩ

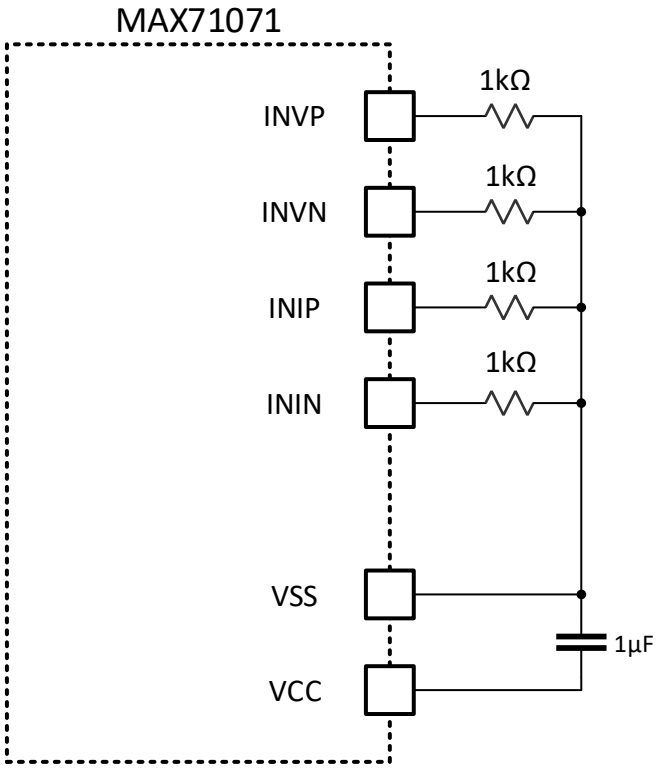


Figure 1. Recommended External Components Circuit

Recommended Operating Conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage		2.5		3.6	V
Operating Temperature Range		-40		+85	°C

Performance Specifications

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT					
V_{CC} Current, Normal Operation	V_{CC} = 3.3V, voltage ADC preamp bypassed	1.2	1.6		mA
V_{REF}					
V_{REF}(22), V_{REF} Output Voltage	T_A = +22°C	1.1925	1.195	1.1975	V
V_{REF} Power Supply Sensitivity $\Delta V_{REF}/\Delta V_{CC}$		-2.4		+2.4	mV/V
V_{NOM} Definition	$V_{NOM}(T) = V_{REF}(22) + (T - 22) \times TC_1 + (T - 22)^2 \times TC_2$ (Note 2)				V
TC_1 and TC_2 Equations		$TC_1 = 316 – TRIMT*5.94$			µV/C
		$TC_2 = -0.582 + TRIMT*(0.00132)$			µV/(C^2)
$V_{REF}(T)$ Deviation from $V_{NOM}(T)$ $[(V_{REF}(T) - V_{NOM}(T))/V_{NOM}(T)] \times [10^6/62]$	(Note 3)	-93	0	+93	ppm/°C
V_{CC} VOLTAGE MONITOR					
BNOM: Nominal Value, T_A = +22°C	V_{CC} = 3.0V		120		LSB
V_{CC} Voltage	V_{CC} = 3.0 + (BSENSE - 120) x 0.0244 (Note 4)				V
Measurement Error		-150		+150	mV
TEMPERATURE MONITOR					
T_{NOM}: Nominal Value, T_A = +22°C			945		LSB
Temperature Error	T_A = -40°C, -10°C, +55°C, +85°C (Note 3)		0		°C
TETIME: Duration of Temperature Measurement	V_{CC} = 3.0V	14	30		ms
POWER PULSE					
Power Pulse Frequency			1.638		MHz
PULSE I/O					
SP and SN Outputs V_{OH} (ONE Pulse)	I_{OH} = 1mA	V_{CC} - 0.28			V
SN and SN Outputs V_{OL} (ONE Pulse)	I_{OL} = 1mA			0.287	V

Performance Specifications (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PREAMP GAIN					
Gain = 14x		14 - 2%	14	14 + 2%	V/V
Gain = 9x		9 - 2%	9	9 + 2%	V/V
Gain = 4x		4 - 2%	4	4 + 2%	V/V
Phase Shift			1		m°
Phase Shift Variation vs. Supply	(Note 3)	-10		+10	m°/V
Phase Shift Variation vs. Temperature	(Note 3)	-0.1		+0.1	m°/°C
Input Current	Preamp gain = 4x, 9x, 14x	7.5	13	24	µA
PREAMP OFFSET					
Gain = 14x	(Note 7)	-1.7		+1.7	mV
Gain = 9x	(Note 7)	-1.9		+1.9	mV
Gain = 4x	(Note 7)	-2.25		+2.25	mV
ADC CONVERTER					
Usable Input Range (I_{NP} - I_{NN})		-250/gain		250/gain	mV_{PK}
THD (FIRST 10 HARMONICS)					
Preamp Gain = 1x	V_{IN} = 65Hz, 64kpts FFT, Blackman-Harris window		85		dB
250mV_{PK}/Preamp Gain, Preamp Gain = 4x, 9x, 14x	V_{IN} = 65Hz, 64kpts FFT, Blackman-Harris window		85		dB
20mVPK/Preamp Gain, Preamp Gain = 4x, 9x, 14x	VIN = 65Hz, 64kpts FFT, Blackman-Harris window		85		dB
Input Impedance	Preamp bypassed (Note 6)	20		40	kΩ
	Preamp = 4x	6.5	12	18	
	Preamp = 9x	3.5	6.3	9.1	
	Preamp = 14x	2.3	4.3	6.3	
LSB SIZE					
Preamp Gain = 14x	FIR length = 100		22.9		nV/LSB
Preamp Gain = 9x	FIR length = 100		35.5		nV/LSB
Preamp Gain = 4x	FIR length = 100		79.9		nV/LSB
Digital Full Scale *L* = FIR Length	FIR length = 100	±1,000,000			LSB
ADC Gain Error vs. % Power Supply Variation	V_{IN} = 250mV_{PK}, 55Hz			120	ppm/%
Current Channel Gain Variation	V_{IN} = 250mV_{PK}, 55Hz (Note 3)			90	ppm/%
Input Offset, Preamp Bypassed				-4	mV

Note 2: This relationship describes the nominal behavior of V_{REF} at different temperatures.

Note 3: Guaranteed by design, not production tested.

Note 4: This is a definition, and it is not a measured quantity.

Note 5: N/A

Note 6: For Preamp gain = 4x, 9x, and 14x, an internal amplifier with both input and feedback resistors is used in front of the ADC. External source impedance can degrade the gain significantly by adding resistance to the input resistor.
For bypassed preamp (gain = 1), the ADC is directly connected to the input, and only the interaction of the internal impedance with the source impedance will decrease the signal amplitude, with no change in gain.

Note 7: This is the offset of the preamp as well as of the ADC, meaning this is the total offset seen at the ADC input.

Pin Configuration

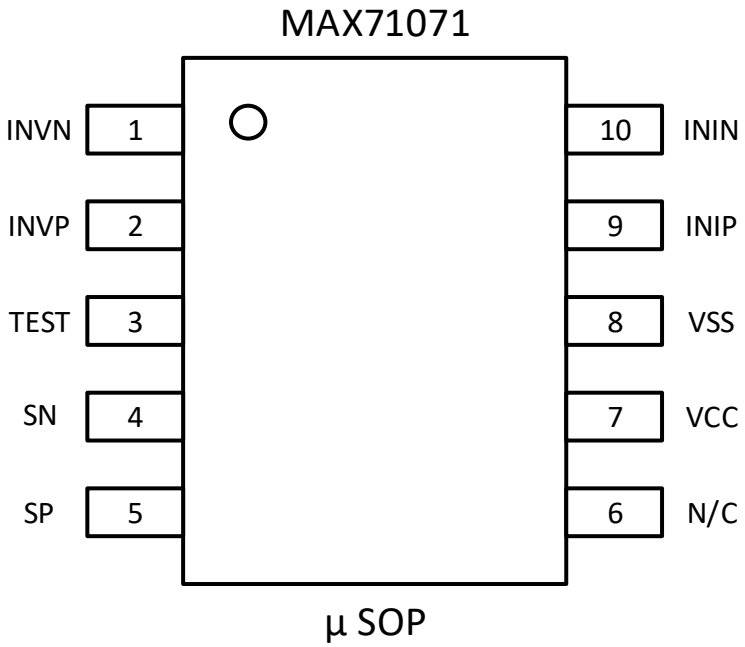


Figure 2. Pin Diagram

Pin Description

PIN	NAME	FUNCTION
1	INVN	Voltage Channel Negative Input
2	INVP	Voltage Channel Positive Input
3	TEST	Test Mode Enable. Must be grounded in normal operation.
4	SN	Transformer Negative
5	SP	Transformer Positive
6	N.C.	Not Connected
7	V_{CC}	Power Bypass. Connect 1µF capacitor to ground.
8	V_{SS}	Ground.
9	INIP	Current Channel Positive Input
10	ININ	Current Channel Negative Input

Detailed Description

The MAX71071 are dual-channel isolated metrology analog-to-digital converters (ADCs) that are compatible with MAX71xxx MAX78615 hosts. The device digitizes a current signal from a shunt type current sensor and/or a voltage signal from a resistor-divider. The two input channels of the MAX71071 are identical except that the voltage channel contains an option to bypass the preamp.

The device continuously sends ADC data to the host. The host can request the device to return certain ancillary data such as the temperature monitor output. The MAX71071 communicate with the host through a pulse transformer to provide isolation from the high-voltage power domain.

The MAX71071 include a rectifier, two staring preamp/ADC channels, bandgap, temperature monitor, PLL, and BIAS block.

Rectifier

The active rectifier in the device rectifies the power pulses received from the host through the pulse transformer to create the V_{CC} voltage. The block also has the drivers that drive the data bits out of the MAX71071 and through the transformer.

ISO Interface

The isolated interface block receives the incoming data from the host and transmits data back to the host through the pulse transformer.

Preamp

The preamp is a low-noise differential amplifier. The INP and INN pins are the differential inputs to the preamp. It has three gain settings (4x, 9x, and 14x) The gain is controlled by the host, using two preamp gain control bits:

Bit 1	Bit 0	Gain
0	0	4
0	1	9
1	0	14
1	1	N/A

The inputs are V_{SS} referenced, and the output of the preamp connects directly to the ADC.

Bandgap

The device includes an on-chip precision bandgap volt- age reference that incorporates autozero techniques as well as production trims to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient that is compensated in firmware by the host.

Temperature Monitor

The temperature monitor block performs a temperature and a supply measurement whenever the MAX71071 receives an instruction from the host requesting for STEMP or BSENSE. This request causes the MAX71071 to return STEMP or BSENSE from the previous measurement and to initiate a new measurement for both. The temperature can be determined from the STEMP reading as follows:

$T = 22.85 + STEMP*0.344 + (STEMP^2)*1.95*10^{-5}$

Temperature Compensation

The host can implement temperature compensation for each connected MAX71071 based on the temperature reported by each MAX71071 and its fuse settings. Linear (TC1) and quadratic (TC2) coefficients can be obtained as follows:

$TC_1 = 316 – TRIMT*5.94$ µV/C

$TC_2 = -0.582 + TRIMT*(0.00132)$ µV/(C^2)

See section *Application Information* on how to read TRIMT.

PLL

The PLL locks to the incoming power pulses to create reference clocks for the ADC and communications interface to the host. The PLL is typically stable after power pulses have been applied for 5ms.

Pulse I/O

The pulse I/O block in the MAX71071 receives the incoming data from the MAX71xxx host and transmits the data back to the host. The integrated output is applied to the input of a comparator, and the comparator output is captured by a flip-flop at the end of the integration time.

ADC

Two proven Teridian delta-sigma ADCs digitize the voltage and current-sense voltages.

Application Information

Trim Fuse Information

To establish the temperature coefficient for the purpose of temperature compensation, the host IC reads the *TRIMT* value, using read code 0b001 and TMUX[2:0] setting = 0b00x. *TRIMT* is an 8-bit unsigned integer.

Device temperature, supply voltage, and other parameters can be read using the settings in the table below.

RD_ CODE2	***RD_ CODE1***	***RD_ CODE0***	***TMUX2***	***TMUX1***	***TMUX0***	**Function**
0	0	0	X	X	X	ZERO command
0	0	1	0	0	X	Read TRIMBGA, TRIMT
0	0	1	0	1	X	Read BG_STEP, IBIAS, TEMP_MON
0	0	1	1	0	X	Read TRIMBGB, TRIMBGD
0	0	1	1	1	X	Read Device ID, TRIMBGC
0	1	0	0	0	X	Read STEMP
0	1	0	0	1	X	Read VSENSE
0	1	0	1	0	X	Read VERSION
0	1	0	1	1	X	MAX71071 sends 0xD9BA test pattern
0	1	1	0	1	1	RESET command
1	1	0	X	X	X	Illegal code

Functional Diagram

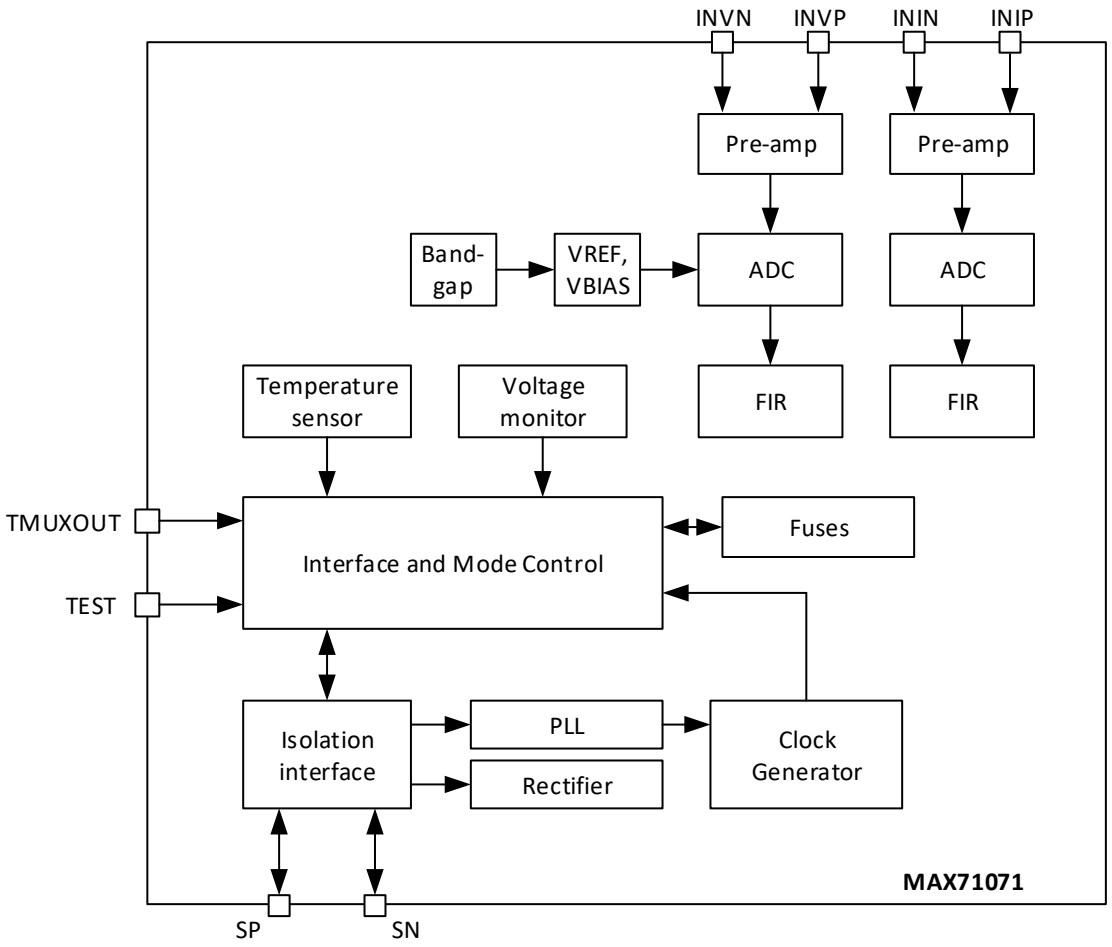


Figure3. Functional Block Diagram

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX71071+	-40°C to +85°C	10 µSOP
MAX71071+T	-40°C to +85°C	10 µSOP

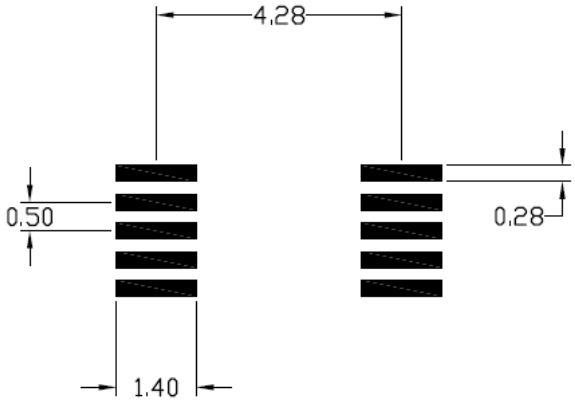
+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Package Information

Package outline information is appended to this document. Land patterns (footprints) are shown below.



NOTES:
1. ALL DIMENSIONS IN MM.
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/2014	Initial release	—
1	1/2015	Updated the *Benefits and Features* section	1
2	4/2016	Rebranding only	All
3	6/2019	Added data for pre-amp offset Added compensated tolerance for VREF over temperature Added notes 6 and 7 Added typical time for PLL to stabilize Added formula for temperature reading and compensation Added legal disclaimer Removed references to MAX71071H	4 4 5 6 6 10 all
4	4/2020	Corrected Figure 1 (removed reference to MAX71071H) Added TC_1 and TC_2 equations in electrical specifications, corrected voltage levels for Pulse I/O Added table with trim fuse information Added land pattern (PCB footprint) Corrected package drawing	2 3 7 9 12

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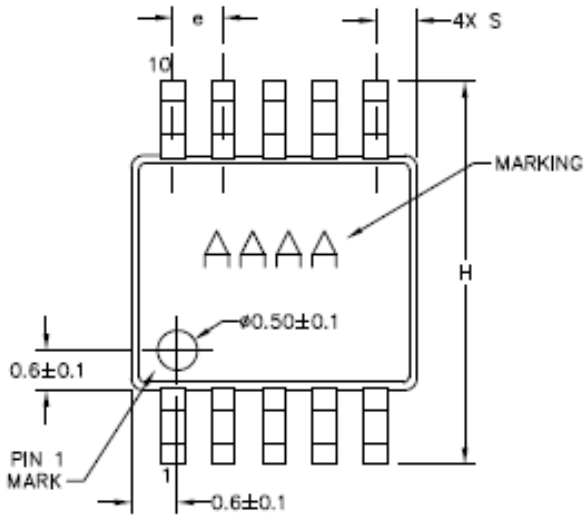
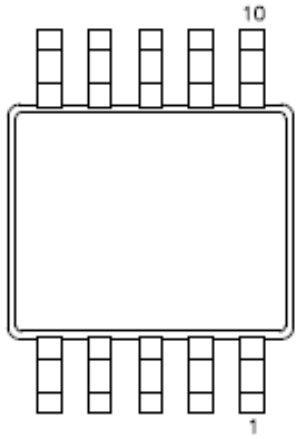
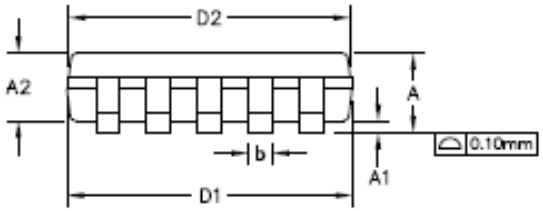


TOP VIEW

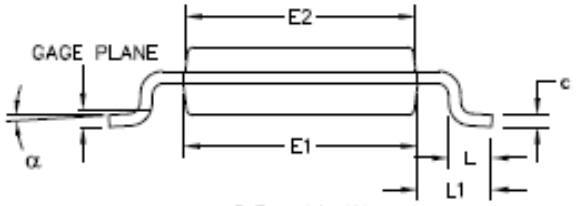


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10–2; U10CN–1; U10+5; U10M–5; U10–2C; U10–6C				



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION BA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–