MAX71313L/MAX71314L

ZON M1L/M1
Single-Phase Electricity Meter SoC

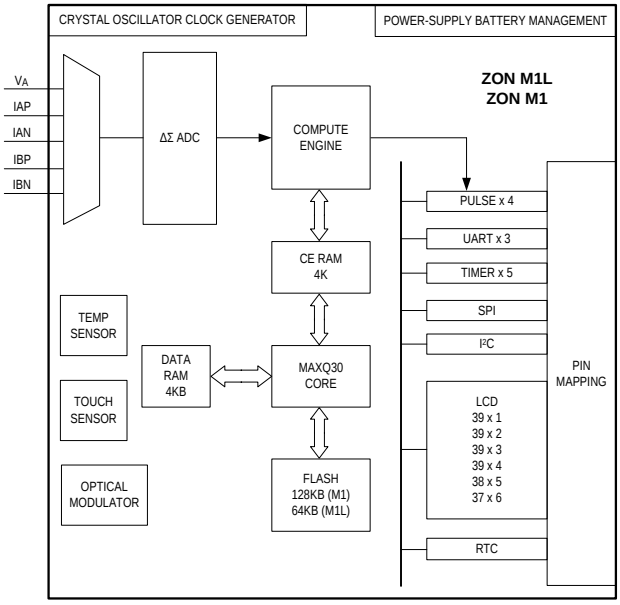
General Description

The ZON™ M1L (MAX71313L) and M1 (MAX71314L) electricity meter systems-on-chip (SoC) integrate dual 32-bit processors for demanding single-phase metering applications with 128KB or 64KB flash, 8KB RAM, and a single-cycle 32 x 32 + 64 multiplier. A low-power metering mode allows metering in the presence of neutral disconnect tampering. The low-power, dedicated compute engine (CE) handles high-rate metrology processing and a 32-bit MAXQ30 MPU core handles other application functions including communications and display control.

Features and Benef ts

- Single ADC Offers High-Accuracy Performance and Cost-Effective Solution
  - Supports Up to 5 Multiplexed Inputs
  - 0.1% (typ) Wh Accuracy over 2000:1 Current Range
- Dual-Core Architecture Improves System Performance
  - Dedicated 32-bit DSP Core for High-Rate Metrology Processing
  - MAXQ30 32-Bit RISC MPU, 10 MIPS (at 10MHz)
- Highly Integrated Product Features and Flexible Peripherals Support Broad Application Needs
  - 128KB (M1) or 64KB (M1L) f ash, 8KB SRAM
  - Supports Current Transformers or Shunts for Current Measurement
  - RTC with Hardware Temperature Compensation
  - Digital Temperature Compensation for Metrology
  - 45Hz to 65Hz Line Frequency Range
  - Phase Compensation (10)
  - Four Pulse Outputs
  - LCD Controller Supports Up to 39 Segment Drivers and Up to Six Common Planes
  - Two PWM Channels with Programmable Frequency, Duty Cycle, Ramp Time
  - Five General-Purpose Timers
  - Touch Switch Input
  - SPI (Master and Slave)
  - I2C (Master and Slave)
  - 3x UARTs (One with Optical Encoder)
- Small 64-Pin LQFP Package Saves Board Space
- Low-Power Operation Extends Battery Life
  - Enables Metering Mode Operation During Neutral Disconnect Tampering
  - 5.6 mA Consumption at 3.3V in Typical Metering Mode
  - 1.6 mA Typical Current Consumption at 3.3V in Low-Power Metering Mode
  - 1.75µA Typical Sleep Mode Current

Block Diagram



Ordering Information/Selector Guide ***and*** *Typical Operating Circuit* ***appears at end of data sheet.***

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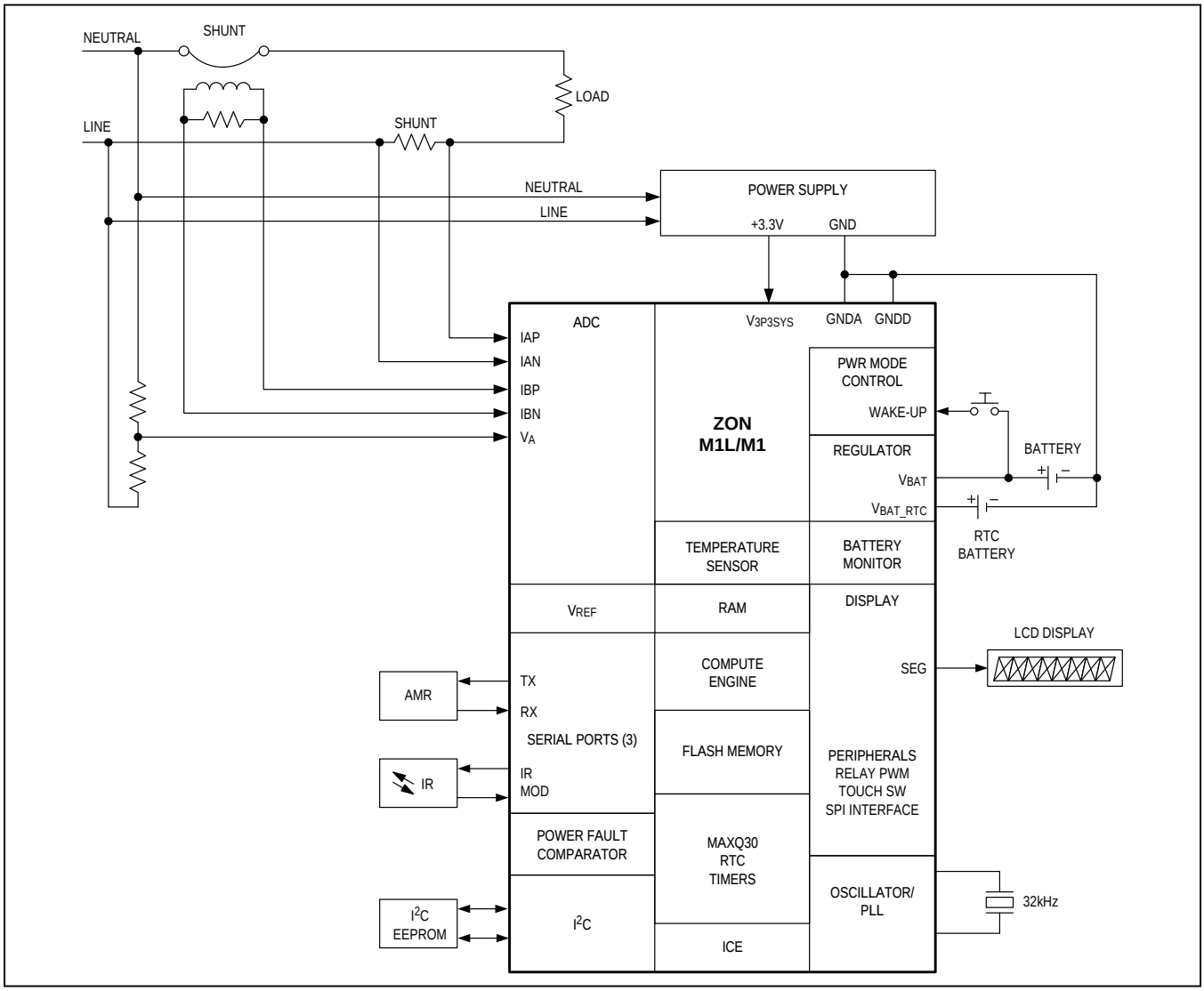
Rev 2; 4/16

Typical Operating Circuit



Absolute Maximum Ratings

(All voltages with respect to GNDD.)

Temperature and ESD Stress

Voltage and Current Supplies and Ground Pins

Operating Junction Temperature (peak, 100ms).....+140°C
V_{3P3SYS} ..... -0.5 to +3.6V
Operating Junction Temperature (continuous).....+125°C

Crystal Pins

Storage Temperature Range ..... -45°C to +165°C
XIN, XOUT.....(-10mA to +10mA), (-0.5V to +3.0V)
ESD Stress on All Pins.....±4kV, HBM

Digital Pins

Lead Temperature (soldering, 10s) .....+300°C
Inputs..... (-10mA to +10mA), (-0.5V to +3.6V, MSN/BRN mode)
Soldering Temperature (reflow) .....+250°C
Inputs..... (-10mA to +10mA), (-0.5V to +3.6V , SLP mode)
Outputs.....(-8mA to +8mA), (-0.5V to (V_{3P3D} + 0.5V))

Package Thermal Characteristics (Note 1)

LQFP

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....55.50°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....23.50°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Recommended Operating Conditions

(GNDA and GNDD must be connected.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V3P3SYS Supply Voltage—Precision Metering Operation (Mission mode)	V_{BAT} = 0V to 3.8V V_{RTC} = 0V to 3.8V	3.0		3.6	V
V_{BAT} Voltage—Brownout and Low Power Metering Modes (In these modes, V_{3P3SYS} is below the V3OK comparator threshold. Either V_{3P3SYS} or V_{RTC} must be high enough to power the RTC module)	V_{3P3SYS} < PFV2p8 and V_{RTC}, V_{3P3SYS} (max) > 2.0V	2.5		3.8	V
V_{RTC} Voltage	V_{3P3SYS} < 2.0V	2.0		3.8	V
Operating Temperature		-40		+85	°C

Electrical Characteristics

(V_{3P3SYS} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	$V_{3P3PSYS}$		3.0		3.6	V
Supply Voltage, Backup Battery	V_{BAT}		2.5		3.8	V
Supply Voltage, RTC Battery	V_{BAT_RTC}		2.0		3.8	V
Supply Current	I_{DD1}	(Note 3)		7.1	8.2	mA
	I_{DD2}	(Note 4)		6.9	8	
	I_{DD3}	(Note 5)		1.5	2	
Dynamic Current		V_{3P3SYS} = 3.3V metrology enabled, ADC operating full-speed (f_{MPUCLK} at 10MHz - f_{MPUCLK} at 1.25MHz)		290		µA/MHz

Electrical Characteristics (continued)

(V_{3P3SYS} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BAT} Current	I_{VBAT}	MSN mode		7	50	nA
		BRN mode		6.1	8	mA
		LPM mode		1.3	2	mA
		LCD_ONLY mode (DAC off)		2.5	10	µA
		LCD_ONLY mode (DAC on)		15	100	µA
		SLP mode		0	0.3	µA
V_{BAT_RTC} Current	I_{VBAT_RTC}	MSN mode		7	25	nA
		BRN mode		3.5	5.5	µA
		LCD_ONLY mode		1.2	3	µA
		SLP mode		1.6	3.2	µA
CRYSTAL OSCILLATOR						
RTC Oscillator Frequency	f_{RTC}			32.768		kHz
Peak Output Source Current	I_{XOUT}		-3.5		-0.4	µA
Maximum Crystal Power					-1	µW
Frequency Variation with Voltage		T_A = +25°C, V_{3P3SYS} = 0V, V_{BAT_RTC} = 2.0V to 3.8V		0.03		PPM
LOGIC LEVELS						
Digital High-Level Input Voltage	V_{IH}		+2.0		5.5	V
Digital Low-Level Input Voltage	V_{IL}		-0.3		+0.6	V
Input Leakage Current			-1		+1	µA
Input Pullup Current, GPIO	I_{IL}	V_{IN} = 0V	40		160	µA
Input Pullup Current, RSTN	I_{IL}	V_{IN} = 0V	5		160	µA
Input Pulldown Current, JTAG_E		V_{IN} = V_{3P3SYS}	-160		-30	µA
Digital High-Level Output Voltage	V_{OH}	I_{LOAD} = -1mA	V_{3P3D} - 0.4		V_{3P3D}	V
		I_{LOAD} = -5mA (Note 6)	V_{3P3D} - 0.6		V_{3P3D}	V
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = 1mA	0		0.4	V
		I_{LOAD} = 15mA	0		0.85	V
BATTERY MONITOR						
Measurement Error		V_{BAT} = 2.0V, TEMP_PWR = 1		-0.2		%
		V_{BAT} = 3.8V, TEMP_PWR = 1		-0.1		
		V_{BAT_RTC} = 2.0V, TEMP_PWR = 0		-0.3		
TEMPERATURE MONITOR						
Temperature Error		T_A = +22°C		±3.6		°C
Relative Temperature Error		-40°C < T_A < +85°C, 3.0V < V_{3P3SYS} < 3.6V	-1.75		+1.75	°C
LCD						
V_{LCD} Current		V_{LCD} = 3.3V (DAC Off)		1.4	4.0	µA

Electrical Characteristics (continued)

(V_{3P3SYS} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF}						
Nominal Reference Voltage	V_{REF}	T_A = +22°C	1.226	1.228	1.230	V
Variation with Power Supply		V_{3P3SYS} = 3.0V to 3.6V	-1.5		+1.5	mV/V
Deviation from Predicted Variation with Temperature			-40		+40	ppm/°C
ADC						
Usable Input Range		All channels (IA preamp off)	-250		+250	mV peak
		Preamp gain = 4 (IA only)	-62.5		+62.5	
		Preamp gain = 8 (IA only)	-31.25		+31.25	
Input Impedance		f_{IN} = 65Hz, (IA - preamp off)	60		120	kΩ
		f_{IN} = 65Hz, preamp gain = 4 (IA only)	2.5		10	
		f_{IN} = 65Hz, preamp gain = 8 (IA only)	2.5		10	
LSB Size		FIR_LEN = 11		296		nV/LSB
		FIR_LEN = 15		125		
Digital Full Scale		FIR_LEN = 11		±1105920		LSB
		FIR_LEN = 15		±2621440		
Input Offset Voltage			-10		+10	mV
THD, Voltage Channel		No preamp		-91		dB
THD, Current Channel		No preamp		-91		dB
		Preamp gain = 8		-75		
Current Channel Preamp Gain		Preamp gain = 4	3.9	4.0	4.1	V/V
		Preamp gain = 8	7.8	8.0	8.2	
Gain Variation with Supply Voltage		±10% variation in V_{3P3}	-50		+40	ppm/%
Gain Variation with Temperature		T_A = -40°C to +85°C (Note 7)	-55		+55	ppm/°C
Current Channel Phase Shift		T_A = +25°C, V_{3P3A} = 3.0V to 3.6V; Preamp gain = 4		10.4		m°
		T_A = +25°C, V_{3P3A} = 3.0V to 3.6V; Preamp gain = 8		18.5		
Phase Shift Variation with Supply		±10% variation in V_{3P3}	-20		+20	m°
Phase Shift Variation with Temperature		-40°C to 85°C, ±10% variation in V_{3P3}	-0.1		+0.1	m°

Electrical Characteristics (continued)

(V_{3P3SYS} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR						
Nominal Frequency				24		MHz
Base Accuracy			-3		+3	%
Frequency Variation with Supply				-19.4		kHz/V

Note 2: Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 3: Supply current is the current into V_{3P3SYS}; part is out of reset, no port activity, no flash writes, measured at V_{3P3SYS} = V_{3P3A} = 3.3V, executing from flash, f_{MPUCLK} = 10MHz, metrology enabled, with ADC operating full speed.

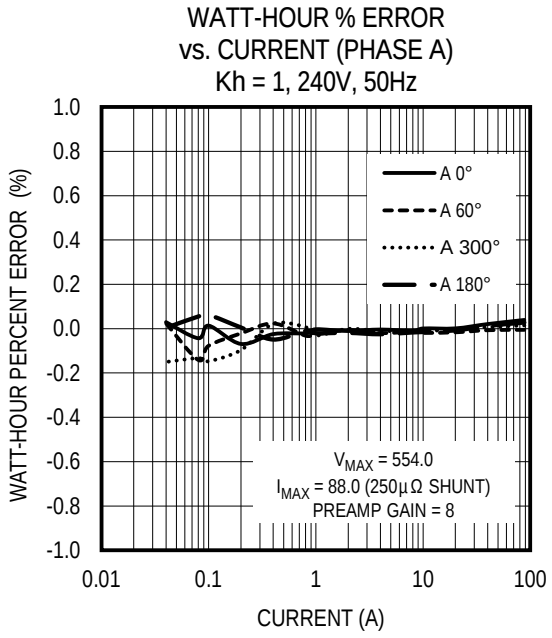
Note 4: Supply current is the current into; part is out of reset, no port activity, no flash writes, measured at V_{3P3SYS} = V_{3P3A} = 3.3V, executing from flash, f_{MPUCLK} = 10MHz, metrology enabled, with ADC operating half speed.

Note 5: Supply current is the current into V_{3P3SYS}; part is out of reset and in low-power metering mode (LPMM), no port activity, no flash writes, measured at V_{3P3SYS} = 3.3V, the MPU is executing from flash. In LPMM: MAXQ30 operating at reduced speed (f_{MPUCLK} = 245kHz), metrology enabled, with ADC operating at low speed (f_{ADCLK} = 0.98304MHz) or 1/5 of full-speed, compute engine operating at low speed (f_{CECLK} = 3.932MHz).

Note 6: The total current sourced by all DIO pins should not exceed 5mA.

Note 7: Guaranteed by design, not production tested.

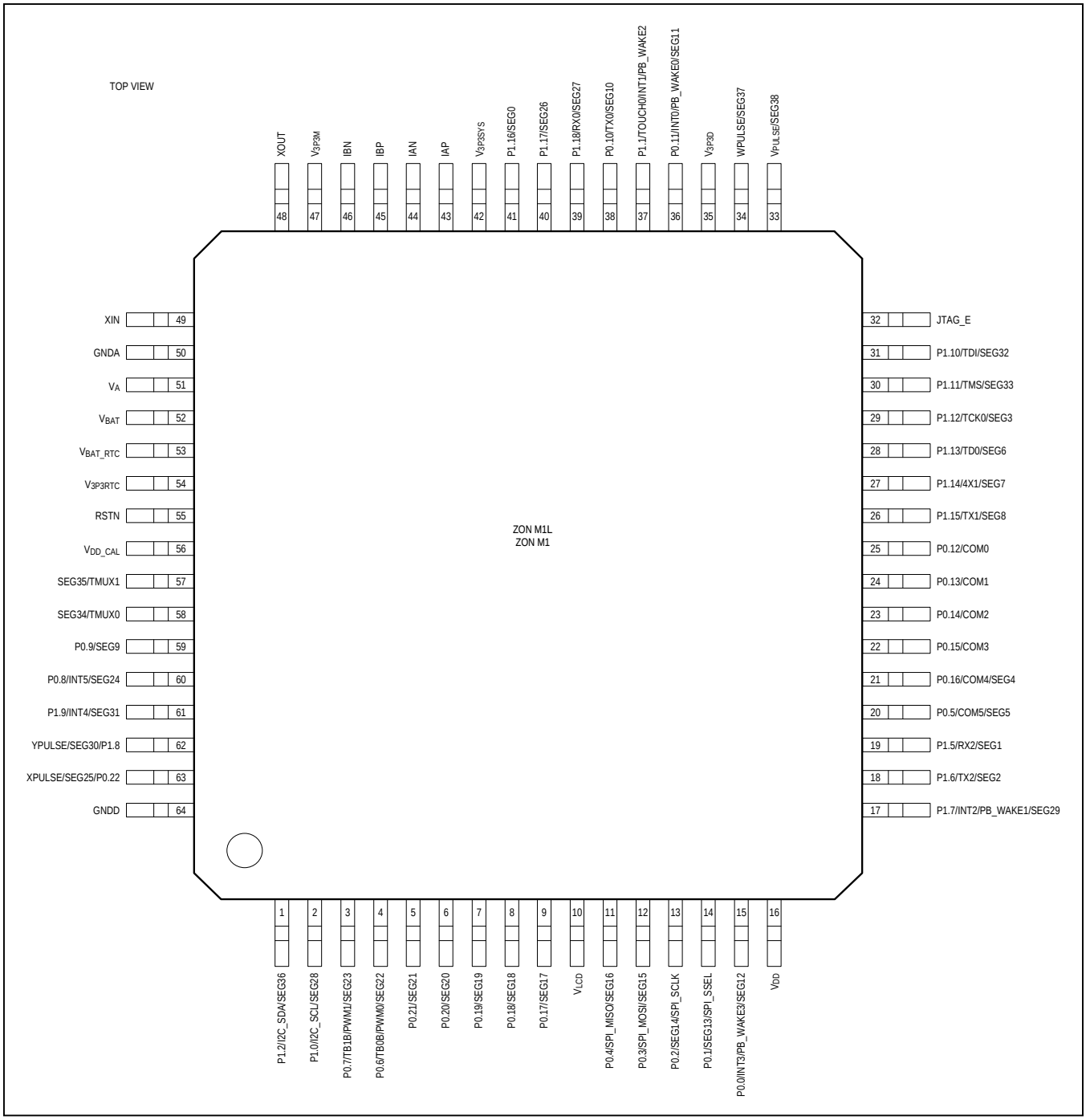
Typical Operating Characteristics



Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNIT
CV3P3D	V_{3P3D}	GNDD	Bypass capacitor for V_{3P3D} output	1.0 ±20%	µF
CV3P3SYS	V_{3P3SYS}	GNDD	Bypass capacitor for V_{3P3SYS}	≥ 1.0 ±30%	µF
CVDD	V_{DD}	GNDD	Bypass capacitor for V_{DD}	1.0 ±20%	µF
CVLCD	V_{LCD}	GNDD	Bypass capacitor for V_{LCD} pin	≥ 0.1 ±20%	µF
CV3P3RTC	V_{3P3RTC}	GNDD	Bypass capacitor for V_{3P3RTC}	1.0 ±30%	µF
CV3P3M	V_{3P3M}	GNDA	Bypass capacitor for V_{3P3M}	≥ 0.1 ±20%	µF
CVDD_CAL	V_{DD_CAL}	GNDD	Bypass capacitor for V_{DD_CAL}	≥ 0.1 ±20%	µF
XTAL	XIN	XOUT	32.768kHz tuning fork crystal—electrically similar to ECS 0.327-12.5-17X, Vishay XT26T or Suntsu SCP6–32.768kHz TR (load capacitance 12.5 pF).	32.768	kHz
CXS	XIN	GNDA	Load capacitor values for crystal depend on crystal specif cations and board parasitic capacitance. Nominal values are based on 3pF board capacitance and include an allowance for chip capacitance.	20 ±10%	pF
CXL	XOUT	GNDA		20 ±10%	pF

Pin Conf guration



Pin Description

PIN	GPIO	PIN NAME	INTERRUPT	WAKE	LCD COMMON	LCD SEGMENT	COMMENT
1	P1.2	I2C_SDA	—	—	—	36	I^2C
2	P1.0	I2C_SCL	—	—	—	28	I^2C
3	P0.7	TB1B/PWM1	—	—	—	23	TIMER1 Output
4	P0.6	TB0B/PWM0	—	—	—	22	TIMER0 Output
5	P0.21	SDIO	—	—	—	21	
6	P0.20	SDIO	—	—	—	20	
7	P0.19	SDIO	—	—	—	19	
8	P0.18	SDIO	—	—	—	18	
9	P0.17	SDIO	—	—	—	17	
10	—	V_{LCD}	—	—	—	—	Bypass Only
11	P0.4	SPI_MISO	—	—	—	16	SPI
12	P0.3	SPI_MOSI	—	—	—	15	SPI
13	P0.2	SPI_SCLK	—	—	—	14	SPI
14	P0.1	SPI_SSEL	—	—	—	13	SPI
15	P0.0	PB_WAKE3	3	PB_3	—	12	
16	—	V_{DD}	—	—	—	—	Bypass Only
17	P1.7	PB_WAKE1	2	PB_1	—	29	
18	P1.6	TX2	—	—	—	2	UART2 TX
19	P1.5	RX2	—	RU_2	—	1	UART2 RX
20	P0.5	COM5	—	—	COM5	5	
21	P0.16	COM4	—	—	C0M4	4	
22	P0.15	COM3	—	—	COM3	—	
23	P0.14	COM2	—	—	COM2	—	
24	P0.13	COM1	—	—	COM1	—	
25	P0.12	COM0	—	—	COM0	—	
26	P1.15	TX1	—	—	—	8	UART1 TX
27	P1.14	RX1	—	RU_1	—	7	UART1 RX
28	P1.13	TDO	—	—	—	6	JTAG TDO
29	P1.12	TCK	—	—	—	3	JTAG TCK
30	P1.11	TMS	—	—	—	33	JTAG TMS
31	P1.10	TDI	—	—	—	32	JTAG TDI
32	—	JTAG_E	—	—	—	—	JTAG Eanable. JTAG_E has an internal pulldown resistor.
33	—	V_{PULSE}	—	—	—	38	VARH Pulse
34	—	WPULSE	—	—	—	37	WH Pulse
35	—	V_{3P3D}	—	—	—	—	Bypass

Pin Description (continued)

PIN	GPIO	PIN NAME	INTERRUPT	WAKE	LCD COMMON	LCD SEGMENT	COMMENT
36	P0.11	PB_WAKE0	0	PB_0		11	
37	P1.1	TOUCH0	1	PB_2	—	—	
38	P0.10	TX0	—	—	—	10	UART0 TX
39	P1.18	RX0	—	RU_0	—	27	UART0 RX
40	P1.17	—	—	—	—	26	
41	P1.16	—	—	—	—	0	
42	—	V_{3P3SYS}	—	—	—	—	+3.3V Supply
43	—	IAP	—	—	—	—	ADC Input 0. Pin names ref ect assignments for 1P/2W metering. The use of the ADC inputs is determined by the CE code.
44	—	IAN	—	—	—	—	ADC Input 1. Pin names ref ect assignments for 1P/2W metering. The use of the ADC inputs is determined by the CE code.
45	—	IBP	—	—	—	—	ADC Input 2. Pin names ref ect assignments for 1P/2W metering. The use of the ADC inputs is determined by the CE code.
46	—	IBN	—	—	—	—	ADC Input 3. Pin names ref ect assignments for 1P/2W metering. The use of the ADC inputs is determined by the CE code.
47		V_{3P3M}	—	—	—	—	Bypass Only
48	—	XOUT	—	—	—	—	32kHZ Oscillator
49	—	XIN	—	—	—	—	32kHZ Oscillator
50	—	AGND	—		—	—	Analog Ground
51	—	V_A	—	—	—	—	ADC Input 4. Pin names ref ect assignments for 1P/2W metering. The use of the ADC inputs is determined by the CE code.
52	—	V_{BAT}	—	—	—	—	Primary Battery Input
53	—	V_{BAT_RTC}	—	—	—	—	RTC Battery Input
54	—	V_{3P3RTC}	—	—		—	Bypass
55	—	RSTN	—	—	—	—	
56	—	V_{DD_CAL}	—	—	—	—	Bypass Only
57	—	TMUX1	—	—	—	35	
58	—	TMUX0	—	—	—	34	
59	P0.9	SDIO	—	—	—	9	

Pin Description (continued)

PIN	GPIO	PIN NAME	INTERRUPT	WAKE	LCD COMMON	LCD SEGMENT	COMMENT
60	P0.8	SDIO	5	—	—	24	
61	P1.9	SDIO	4	—	—	31	
62	P1.8	YPULSE	—	—	—	30	GPIO function is unavailable when CE is enabled.
63	P0.22	XPULSE	—	—	—	25	GPIO function is unavailable when CE is enabled.
64	—	DGND	—	—	—	—	Digital Ground

Detailed Description

Hardware Overview

The ZON M1L/M1 single-phase electricity meter SoC incorporates a 32-bit MAXQ30 MPU core, delivering approximately one MIPS/MHz of clock (nominally, 9.83MHz); a 32-bit dedicated metrology compute engine, and a complete set of peripherals onto a single device. The ZON SoC is available in a 64-pin LQFP package.

The SoC offers a display controller that supports 6-way multiplexing of LCD segments. Up to 37 available segment pins provide up to 222 controllable display segments in the 6-way multiplexing configuration.

The SoC integrates a high-precision 22-bit delta-sigma ADC with five multiplexed inputs. For one-phase, two-wire metering applications, four inputs are configured as two differential inputs for current measurement and the fifth is configured as a single-ended input for voltage measurement. The ADC samples are processed by a fixed-point compute engine (CE). The code and data for the compute engine reside in RAM that is dual-mapped to the CE and the MAXQ30 MPU core.

The SoC clocks are usually generated from a crystal oscillator controlled by a 32,768Hz tuning-fork type crystal that is also used as the reference for the RTC. A phase-locked loop multiplies this clock to provide the 9.83MHz required by the core, the 19.66MHz required by the CE and other clocks required by the system.

In a typical application, the compute engine of the SoC processes the samples from its metrology input channels and performs calculations to measure real energy and reactive energy as well as volt-ampere hours, A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MAXQ30 MPU core, processed further and output using the peripheral devices available to the MPU.

The SoC features a real-time clock to record time of use (TOU) metering information for multirate applications and to time-stamp tamper or other events.

The SoC includes a precision voltage reference. A temperature correction mechanism guarantees conformance to accuracy standards over temperature. Temperature-dependent external components such as crystal oscillator, current transformers and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

The SoC has one pin that can be configured as a touch detect input. When configured for touch detect, this pin self-oscillates at a frequency dependent on the capacitive load on the pins. A low-power timer circuit measures the oscillation frequency and alerts the MPU when the frequency falls below a certain threshold (indicating an increase in the capacitive loading). This input can be used to wake the processor, if desired.

The SoC has three UART channels with independent baud rate generators. These UART channels can be connected to driver/receiver chips for RS232 or, with an additional GPIO pin for transmit enable, for RS422/RS485. One of the three UART channels is provided with a modulator for transmit data to support 38kHz IR communication.

The SoC includes standard peripherals for interfacing serial memory devices and complex display subsystems, among other devices. These devices include one serial peripheral interface (SPI) port and one I^2C port.

Analog Front End

The analog front end (AFE) comprises a high-resolution delta-sigma ADC that is connected to five analog input pins through a multiplexer. The analog inputs can be configured as single ended inputs to the ADC, or two inputs may be paired to provide a differential mode input.

In a single-phase (equation 0) or split phase (equation 1) meter applications, the AFE inputs are configured as shown.

- IAP and IAN provide a differential input for line current measurement. An input preamplif er can be inserted into this signal path to provide additional gain to enable use of smaller shunts.
- IBP and IAN provide a differential input for line or neutral current measurement.
- VA provides a single ended input for line voltage measurement.

Analog inputs are sampled at up to 5MHz. The samples are decimated in a FIR filter with an oversampling ratio of up to 512. Finished samples are available to the DSP section at up to 4.68 kilosamples per second per channel.

ADC pin configuration, input multiplexing, sampling rate, and decimation filter length is controlled by the CE. The decimated ADC samples are written directly into the CE's data RAM.

The ADC has an input range of ±0.25 V_{PEAK} relative to the device ground. When IAP and IAN are configured as a differential input, the differential signal can be applied to a programmable gain preamplifier with selectable gains of 4, 8, or 16.

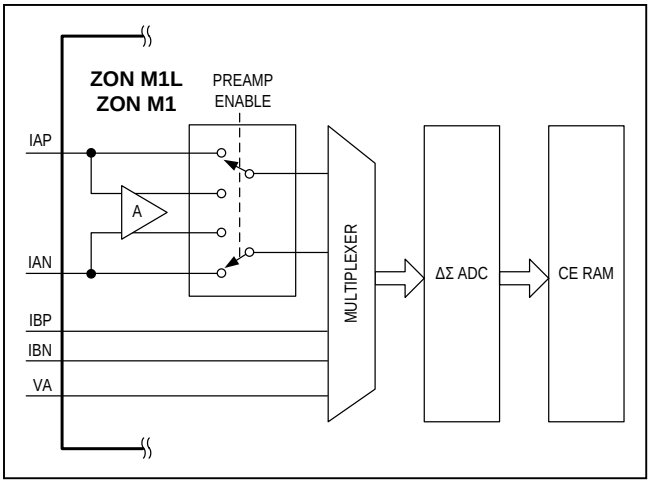


Figure 1. Analog Front-End Block Diagram

Inputs to the ADC channels must be referenced to AGND and must be scaled so that the signal is no greater than 250mV above or below AGND. For example, a system that is expected to monitor up to $300V_{RMS}$ needs to scale that voltage to no more than $250mV_{PEAK}$, and requires a voltage divider with a divide ratio of no less than:

$$\frac{300V \times \sqrt{2}}{0.25V} = 1{,}697$$

For the current channels, the maximum differential amplitude permitted on the input pins scales with the preamplifier gain value:

$$V_{PEAK} = \frac{0.250}{GAIN}$$

For example, in a design using a 120µΩ shunt targeting a $100A_{RMS}$ load, one might consider using a gain of 8, because the maximum RMS current in this arrangement is:

$$\frac{\frac{0.250V / 8}{\sqrt{2}}}{120 \times 10^{-6}\Omega} \cong \frac{22 \times 10^{-3}V}{120 \times 10^{-6}\Omega} \cong 184A$$

Digital Compute Engine (CE)

The compute engine (CE) is a dedicated 32-bit fixed-point RISC processor. It performs the signal processing necessary for energy measurement.

The CE is a programmable device, for which Silergy provides binary code modules. The flexibility of the CE code allows for adaptation of the meter to various metering requirements or sensor types without having to change hardware. It is possible to store more than one CE code image in flash and load the CE image dynamically during meter operation. The CE calculations and processes can include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Combination of intermediate energy results according to the implemented meter equation 90° phase shifter (for VAR calculations)
- Pulse generation
- Measurement of the input signal frequency (for frequency and phase information)
- Monitoring of the input signal amplitude (for sag detection)
- Scaling of the processed samples based on calibration coeff cients
- Scaling of samples based on MPU temperature compensation information
- Extraction, suppression, or f ltering of harmonics for special functions
- DC removal
- Variable gain compensation
- Variable phase compensation

CE Calculations

During each CE code pass, the CE calculates and updates certain instantaneous measurement values. At the end of each accumulation interval, the CE calculates and updates fundamental energy measurement variables.

The specific calculations performed by the CE depend upon the specific CE code used in an application. Typical CE outputs include:

$$WSUM = \sum_{n=0}^{n=nsamples-1} v(n) \times i(n), \text{energy accumulation}$$

where nsamples is the number of samples in the accumulation interval.

$$VSQSUM = \sum_{n=0}^{n=nsamples-1} v(n)^2.$$

used by the MPU for V_{RMS} calculation

$$ISQSUM = \sum_{n=0}^{n=nsamples-1} i(n)^2.$$

used by the MPU for I_{RMS} calculation

VARSUM,

Line frequency calculated from line voltage

Chip temperature

For information on the specific calculations performed by a particular CE program, refer to the appropriate CE Reference Manual that can be obtained from Silergy.

Meter Equations

The CE can implement, among others, the equations listed in Table 1. The standard CE codes implement equation 0. For other configurations, contact the factory.

CE Registers

Communication between the CE and the MAXQ30 core is implemented through RAM that is accessible to both the CE and the MAXQ30 core. The CE code maps this shared RAM as a file of 32-bit registers. The CE output registers are updated by the CE following each accumulation interval. Examples for CE registers are:

- Real energy collected per phase
- Real energy combined per implemented meter equation
- Fundamental content of real energy collected per phase
- Fundamental content of real energy combined per implemented meter equation
- Reactive energy collected per phase
- Reactive energy combined per implemented meter equation
- Summed squares of currents per phase
- Summed squares of voltages per phase, including neutral current
- Mains frequency
- Wh pulse count
- VARh pulse count
- Voltage phase angle A/B and A/C

Inputs from the MAXQ30 MPU core to the CE are also provided in CE registers and comprise the following:

- CE code configuration (selection of phases to be monitored, type of pulse generation, etc.)
- Pulse rate
- Number of samples per accumulation interval
- Sag/swell thresholds and time limits
- Pulse source registers
- Magnitude and phase adjustments from calibration
- Noise cancelling

Table 1. Meter Equations

EQU	DESCRIPTION	Wh AND VARh FORMULA	
		ELEMENT 0	ELEMENT 1
0	1-element, 2-W, 1ϕ with neutral current sense	VA x IA	VA x IB
1	1-element, 3-W, 1ϕ	VA(IA-IB)/2	N/A

Note: *Other equations can be implemented, depending upon the CE code.*

A complete description of all CE registers, functionality, LSB values, and general code performance can be found in the CE Code Reference Manual for the particular CE code.

CE-MPU Signaling

The compute engine alerts the MAXQ30 core to changes in its condition over six circuits:

- **CE_BUSY:** This signal indicates that the CE is actively processing data. The trailing edge of this signal can interrupt the MAXQ30 processor for events that must be processed on each sample.
- **XFER_BUSY:** This signal indicates that the CE is updating the output region of the CE RAM with data for the MPU. This update typically includes the result of energy and squared-sample summations, and occurs after the number of samples designated in the SAMPLE field of the CECN register. This signal can interrupt the MAXQ30 processor for those events that must be processed every accumulation interval.
- **VPULSE, WPULSE, XPULSE, and YPULSE:** These output pulses can be conf gured to interrupt the MAXQ30 core. Typically, WPULSE indicates a certain amount of real energy has been accumulated, and VPULSE indicates a certain amount of reactive energy has been accumulated. YPULSE is often conf gured to indicate a loss of zero crossings on the voltage channel, and XPULSE can be conf gured for other signif cant events. Any of these signals can be routed directly to DIO pins to provide direct outputs to pulse LEDs or alert other external equipment.

Compute Engine RAM

The compute engine uses a single 2K x 16 block of RAM for both code and data storage.

CE code is written to the RAM block by the MAXQ30 processor core during system initialization. After that, the MAXQ30 core releases the compute engine to begin executing. The RAM space is shared by the MAXQ30 core, the CE and the ADC block as interleaved cycles.

Because of the time interleaving the CE data RAM can be accessed apparently simultaneously by the compute engine and the MAXQ30 core. The CE can access any location in the shared SRAM. The MAXQ30 core reads and writes the SRAM as the primary means of data communication between the two processors.

The CE deals with all data on a 64-bit or 32-bit basis and has no concept of single bytes. The shared memory controller stores 32-bit words from the CE in the same way that the MPU reads and writes such that the byte order that the MPU expects is preserved.

Real-Time Monitor

The CE hardware includes a real-time monitor (RTM) that can be configured by the MPU to monitor up to four selectable CE RAM locations at full sample rate, either for diagnostic purposes or for streaming of samples. The four monitored locations are serially output at the beginning of each CE code pass.

MAXQ30 Core

The MAXQ30 core is a 32-bit RISC core. It is unique because all instructions can be coded as a simple MOVE instruction, yielding high efficiency in both time and power.

The MAXQ30 core has the following characteristics:

- Instructions typically execute in a single cycle.
- All peripherals are f rst-class data objects.
- Flexible data pointers make block data moves simple.
- Dedicated 32 x 32 single-cycle multiplier.

Register Complement

The MAXQ30 registers are divided into system registers (called special purpose registers) and peripheral registers (called special function registers). Registers are divided into blocks of register modules that are groups of up to 32 related registers. Register modules 0–5 are dedicated to special function registers that are used for I/O operations, while registers 7–15 are dedicated to special purpose registers (system registers). Registers are first-class data objects, so peripheral objects can take part in ALU transactions, be tested for values, or any other operation that a MPU register can do in other architectures.

Memory Organization and Addressing

The MAXQ30 core is a Harvard machine. As such, it has separate code and data memory spaces. In the MAXQ30 core, each memory space can be up to 32MB in length. When accessed as code, memory is organized as 16MB x 16 bits; when accessed as data, the memory space can appear as 32MB x 8, 16MB x 16, or 8MB x 32.

Flash Memory

The ZON M1 contains 128KB, and the ZON M1L contains 64KB of on-chip flash memory that serves as program store for the MAXQ30 core. The use of flash memory as program store allows the firmware to be easily updated. Because flash write and erase operations cannot be performed while code is executing from flash, code in the utility ROM mediates all flash write and erase operations.

Because the MAXQ30 core is a Harvard architecture processor, the core cannot access as data the memory block from which code is executing. That means that user code executing in flash space cannot directly access data stored in flash memory. However, facilities are provided in the utility ROM to access data stored in flash memory.

Utility ROM

The SoC contains an 8KB ROM organized as 4k x 16 that serves as utility ROM. This block of memory resides at 0x80 0000 in code space. The utility ROM manages the following functions:

- **Boot:** Execution begins from reset at the base of the utility ROM. Under normal circumstances a jump is executed to the base of f ash memory, but under special circumstances some other code block may take the execution thread (boot loader, debug, etc.).
- **Debug:** The utility ROM contains routines that assist the built-in hardware debugger to communicate with ICE software on a PC.
- **Bootloader:** The bootloader provides in-system programming facilities. Integrated debug environment software with the appropriate drivers can invoke the bootloader directly to write code blocks to the flash memory.
- **Utility functions:** Functions such as flash programming and block moves are provided in the utility ROM to assist user software.
- Test: Functions used to perform unit test of the SoC device are included in the utility ROM.

RAM

The SoC contains a total of 8KB of RAM (not including the 96 bytes of RAM dedicated for the debug function). Of this total, 4KB is dedicated to the MAXQ30 core for its internal operation, including stack space. This RAM block is configured as nonvolatile memory and is maintained in the absence of primary power by the V_{BAT} power supply (or V_{BAT_RTC}, should the primary V_{BAT} supply fail). The other 4KB block is dedicated for CE code and data RAM and can be accessed at will by the compute engine and

the MAXQ30 core at will through interleaved access. It is not backed by the VBAT supply and loses its contents when primary power is removed or when the processor enters SLEEP mode.

Internal data memory starts at address 0x00 0000 in data space and is contiguous through 0x00 0FFF (byte addresses). It is implemented as static RAM, and all accesses to internal memory require only one clock cycle. Data memory mapping and access control are handled by a memory management unit (MMU). The MMU is responsible for mapping the data memory at the appropriate place in code or data space. When accessed as data, the data RAM can be written and read as bytes, words or long words.

Shared RAM

One RAM block is shared between the MAXQ30 MPU core and the compute engine. The 4KB block mapped to MAXQ30 data space from byte addresses 0x00 0C00 to 0x00 13FF is also mapped as CE code/data RAM at word addresses 0x0000 to 0x0BFF.

Accesses to shared RAM are interleaved between the MAXQ30 core and the compute engine. From a programmer's perspective, it appears that each core has exclusive access to the memory: memory access by one core does not cause wait states to be added to execution in the other core. Programmers must take care that writes to the shared memory by one core does not cause defective computations in the other core.

Interrupts and Exceptions

The MAXQ30 MPU core processor supports multiple interrupts that transfer control to fixed vectors. Those vectors reside in the base page of memory.

The interrupts are presented in a natural priority order; that is, the PF interrupt is the highest priority interrupt. Priorities can be changed by modifying the interrupt priority register.

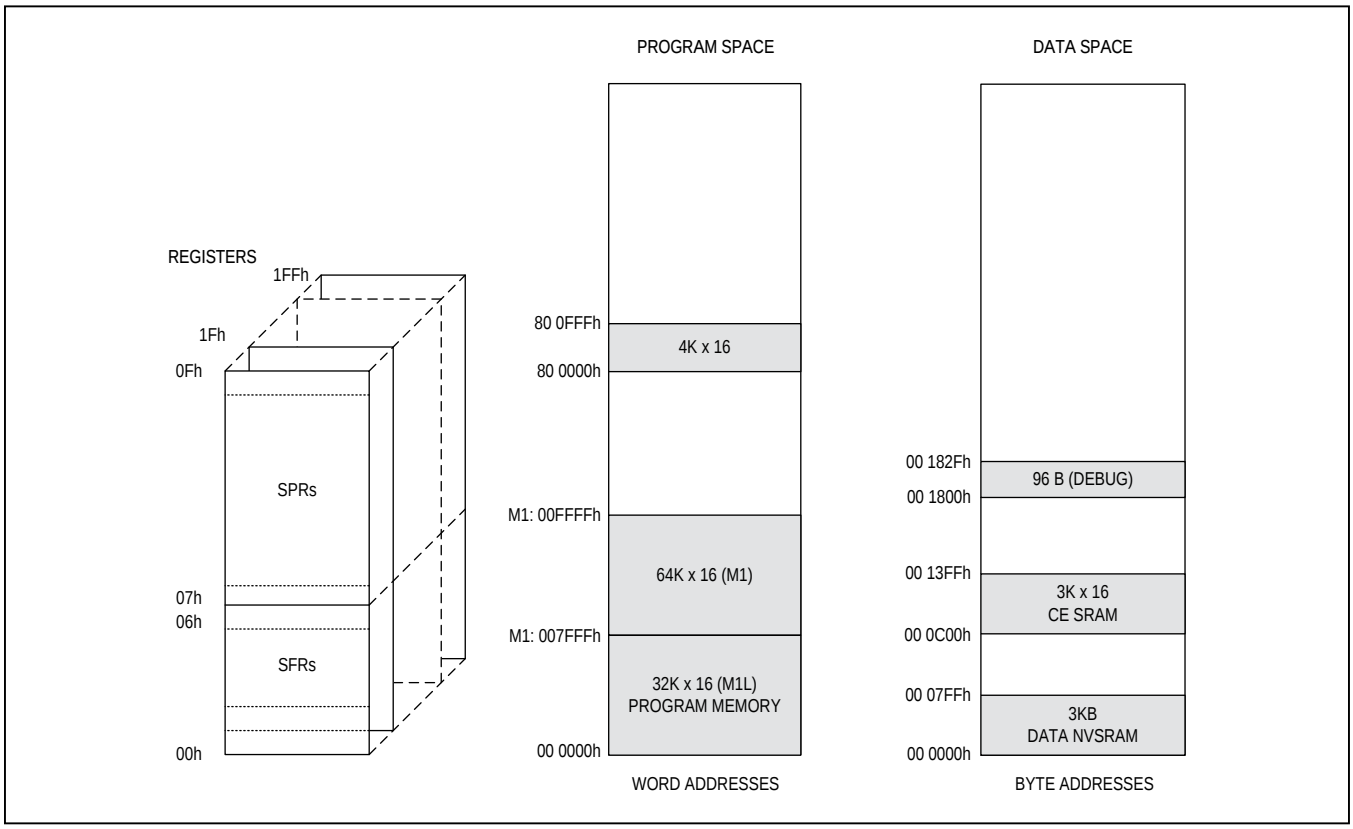


Figure 2. Memory Map

Table 2. Memory Map

MPU ADDRESS	NAME	DESCRIPTION
CODE SPACE (WORD ADDRESSES)		
0x00 0000	FLASH	64K x 16 (ZON M1), 32K x 16 (ZON M1L) f ash program memory
0x80 0000	UROM	4K x 16 utility ROM
DATA SPACE (WORD ADDRESSES)		
0x00 0000	DRAM	2K x 16 static, non-volatile RAM for MCU data
0x00 0C00	CERAM	2K x 16 shared memory for CE data
0x00 1800	DBRAM	48 x16 MAXQ30 debug RAM

Debug

The MAXQ30 MPU core has an integrated debugger that allows real-time debugging of the code running on the MAXQ30 MPU core. The debugger contains a hardware component that connects to the JTAG port, and a software component that is contained in the utility ROM. The debugger supports multiple breakpoints, register inspection and modification, RAM dump and modify, and other functions.

Power

The SoC requires a single 3.3V supply for operation. In most cases, two battery supplies are attached to the device as well: a battery that provides operational power when primary power fails, and a second battery that maintains internal RAM and clock facilities. How these supplies interact and what blocks are powered at what times is covered in this section.

Power Pins

There are three power supply input pins:

V_{3P3SYS}: This is the primary digital power input for the device.

V_{BAT}: This is the primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.

V_{BATRTC}: This pin provides the RTC and nonvolatile memory backup power.

Five pins are used to provide a bypass points for internal power rails. These pins are not used to connect external power sources or loads.

- V_{3P3D}
- V_{LCD}
- V_{3P3RTC}
- V_{DDCAL}
- V_{3P3M}

These power rails are described with more detail in the following sections.

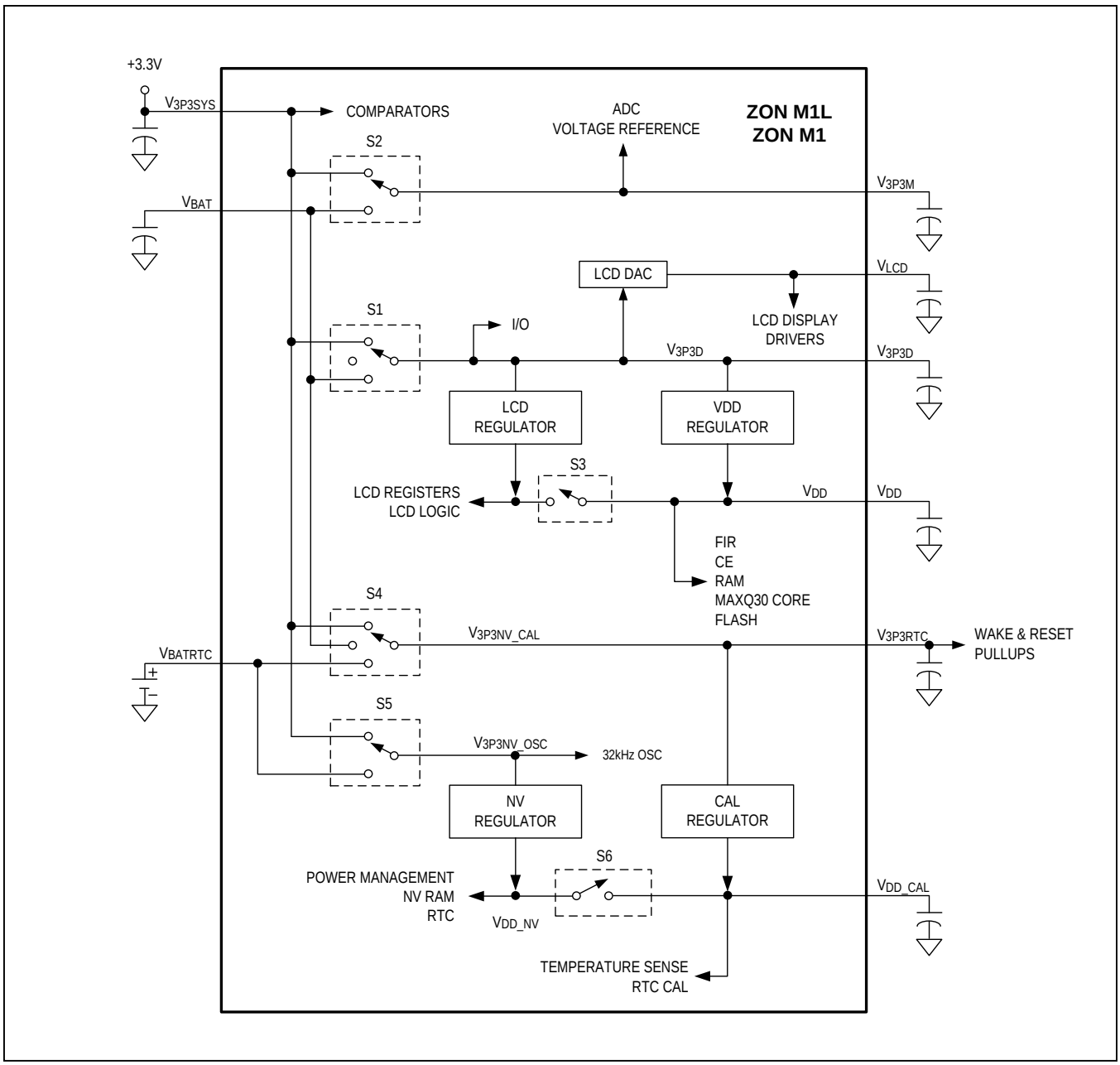


Figure 3. Power Supply

Power Domains

There are eight internal power supply domains that are powered from different power input pins depending upon the operational mode of the device:

- **V_{3P3M}:** This is the power supply for the analog front end, including the ADC, bandgap reference, and bandgap buffer. It may be supplied from either V_{3P3SYS} or V_{BAT}.
- **V3P3D:** This is the primary internal digital supply. It may be supplied from either V_{3P3SYS} or V_{BAT}.
- **V_{DD}:** V_{DD} is the digital supply rail for the MPU, CE, flash memory, and RAM, except for the NV RAM. It is powered through an internal regulator from V_{3P3D}.
- **V_{DD_LCD}:** V_{DD_LCD} powers the LCD registers and logic, and can be sourced from V_{DD} or directly from V_{3P3D} through an internal regulator.
- **V_{3P3NV_CAL}**: Powers the PLL, temperature sensor oscillator and can also power V_{DD_CAL} through a regulator. It can be sourced from V_{3P3SYS}, V_{BAT}, or V_{BAT_RTC}.
- **V_{3P3NV_OSC}:** Powers the 32kHz crystal oscillator and powers the V_{DD_NV} domain through an internal regulator. It is powered from either V_{3P3SYS} or V_{BAT_RTC}.
- **V_{DD_NV}:** Powers the power management unit, nonvolatile RAM and RTC. It can be powered from V_{3P3NV_CAL} or V_{3P3NV_OSC}.
- **V_{DD_CAL}:** Provides power to the RTC calibration logic and temperature sensor. It is powered from V_{3P3NV_CAL} through an internal regulator.

Four internal voltage regulators and six internal power switches control the power distribution system. Some of the switches are controlled by software and others by internal circuitry that senses the voltage on the external pins and makes automatic decisions about the appropriate configuration. Also internally, there are a set of power busses: four primary busses that provide power to various parts of the device logic, two busses dedicated to the LCD functions and one dedicated to the ADC section.

The switches perform the following functions:

S1: Controlled by hardware. This switch selects the source for I/O voltages and the V_{3P3D} circuit. The switch is controlled by internal logic that monitors V_{3P3SYS}. If V_{3P3SYS} falls below the threshold level, the system enters BROWNOUT mode and switches S1 to take power from V_{BAT}. The system is also alerted that it has entered BROWNOUT mode, and it is the responsibility of operating firmware to perform the operations necessary to enter LCD ONLY or SLEEP modes to reduce power consumption from the battery. In these last modes, the switch is placed in the neutral position, effectively powering down the IO, V_{3P3D}, and core logic.

S2: Controlled by hardware. This switch selects the source for V_{3P3M}, which powers the ADC and voltage reference. When V_{3P3SYS} is below the threshold level and both SLEEP and LPM_MODE bits are set, this switch is placed in the V_{BAT} position to power the ADC from the VBAT input. When the LPM_MODE bit is cleared and the SLEEP mode bit is set, the switch is placed to the disconnect position if V_{3PESYS} is below the threshold level. When V_{3P3SYS} is above the threshold level, V_{3P3M} is always powered from V_{3P3SYS}.

S3: Controlled by firmware. Under normal operation, S4 is closed and the LCD operating power is provided by the primary regulator (V_{DD}). When firmware places the system in LCD ONLY mode, S3 is open and LCD power is taken from its dedicated regulator.

S4: Controlled by hardware. This switch selects the power source for the V_{3P3NV_CAL} domain. If V_{3P3SYS} is good, it is selected as the nonvolatile domain source; otherwise, if V_{BAT} is good, it is selected as the nonvolatile domain source; otherwise, V_{BATRTC} is used. This provides power to the PLL and, after regulation, to the temperature sensor and to the RTC calibration logic.

S5: Controlled by hardware. This switch selects either the V_{3P3SYS} or the V_{BATRTC} source to power the 32kHz crystal oscillator and the NV regulator, which powers the NVRAM, RTC, and the power management logic. It is configured automatically based on the level of V_{3P3SYS}.

S6: Controlled by firmware. In all modes except SLEEP mode, this switch is closed, connecting the NV bus and the calibration power bus. When firmware places the device in SLEEP mode, S8 is open, isolating the calibration power bus and ensuring lowest possible power.

Operating Modes

The SoC has five operating modes. Some mode transitions are under hardware control while others are invoked by software.

- **Mission mode:** This is the normal operating mode. The SoC is in mission mode when the primary power supply is in specif cation. All current is supplied through the V_{3P3SYS} pin. Comparators monitor the voltage level on the V_{3P3SYS} pin. If the voltage level falls below the set threshold, the part automatically switches to brownout mode.

- **Brownout mode:** When V_{3P3SYS} fails the source for V_{3P3D}, which supplies main power for the I/O and other circuits, is automatically switched to the V_{BAT} input. No power is supplied to the V_{3P3M} domain. The core continues to operate at full speed until firmware switches to another mode.
- **LCD:** The LCD mode can be commanded by the MPU by first setting the LCD_ONLY control bit and then setting the SLEEP control bit. In LCD mode the core is halted, the core voltage regulator is disabled, and the LCD operates independent of software control, taking power from V_{BAT}. The device may exit the LCD only mode to either mission mode or brownout mode on an enabled wake event. The MPU can command the part to enter LCD mode at any time. If an enabled wake event is present when LCD mode is commanded, the device enters LCD mode and immediately begins a wake sequence.
- **SLEEP:** Sleep mode shuts down power to all logic blocks except the RTC and nonvolatile memory blocks. The device exits sleep mode when an enabled wake event is detected. Sleep mode can be commanded at any time by software, but if an enabled wake condition exists when the device is placed into sleep mode, the device immediately begins a wake sequence upon entering sleep mode.
- **LPM (Low-Power Metering):** Operating in LPM mode allows the device to perform measurements even when the main power (V_{3P3SYS}) is not at a valid level. This mode is entered when both LPM_MODE and SLEEP bits are set, and is typically entered from brownout mode. In LPM_MODE all power domains remain on. The V_{3P3M} domain will be powered from either V_{3P3SYS} or from V_{BAT}, depending on whether V_{3P3SYS} is above or below the operating threshold. The watchdog timer interval is increased from 1.5s to 6s. The MPU, CE, and analog front end can continue to operate normally. In a typical application, the software conserves power by reducing the MPU and CE clock speed and loading reduced functionality CE code that measures only primary current. If the neutral connection to the meter has been disconnected, there is no line voltage measurement and no system 3.3V power. The application can configure the CE to make a periodic line current measurement and use the current to calculate an imputed energy consumption using the nominal line voltage.

If V_{3P3SYS} fails and the firmware does not put the part into SLEEP mode before the V_{BAT} falls below the emergency shutoff threshold the device registers a BADVDD condition. When the device is operating on battery power the software should monitor the voltage status to detect this condition (BADVDD) and if it occurs, should perform a safe shutdown and enter sleep mode. Otherwise, the device is forced into sleep mode and the event is flagged so that it can be detected when the device wakes.

Table 3 shows what blocks are powered in each mode and the power source for each.

Table 3. Power Sources for Operating Modes

OPERATING MODE	POWER SOURCE			
	MPU, CE, AND FLASH	LCD	ANALOG FRONT END	RTC AND NONVOLATILE RAM
Mission	V_{3P3SYS}	V_{3P3SYS}	V_{3P3SYS}	V_{3P3SYS}
Brownout	V_{BAT}	V_{BAT}	Off	V_{BAT_RTC}
LPM	V_{3P3SYS} or V_{BAT}	V_{3P3SYS} or V_{BAT}	V_{3P3SYS} or V_{BAT}	V_{3P3SYS} or V_{BAT_RTC}
LCD_ONLY	Off	V_{BAT}	Off	V_{BAT_RTC}
Sleep	Off	Off	Off	V_{BAT_RTC}

On-Chip Resources

Oscillators

The SoC contains three oscillators:

- An internal 24MHz oscillator that starts immediately upon power-up.
- A crystal oscillator that uses a 32,768Hz tuning-fork crystal as its time base. When the device is operating from the crystal oscillator, an internal PLL multiplies the reference frequency to the various clocks required in the device.
- An internal 32,768Hz backup oscillator in case of crystal oscillator failure.

On-chip timing is normally derived from the 32,768Hz oscillator. In the event of oscillator failure, the RTC clock source switches to the internal backup oscillator, and the MPU and CE clocks are derived from the 24MHz oscillator.

Timers

The SoC contains five timer channels. Each timer channel can be configured as a counter, a timer or a PWM modulator. Additionally the timers can perform count capture and compare functions. They can be used for timing, pulse generation, pulse width modulation, pulse timing, or many other uses. Inside the timer logic, multiple sources can be selected to generate an interrupt to the MAXQ30 core.

The timers have the following features:

- **MPU interrupts:** The timers can interrupt the MPU on overf ow or when the timer matches some preset value.
- **Pulse measurement:** The timers can be triggered by an external pulse.
- **Pulse width modulation:** The timers can be used to generate a PWM signal with selectable characteristics.
- **Counters:** The timers can be configured to count the number of external pulse edges.

When configured as timers, the clocks are derived from the system clock. A prescaler system allows the system clock to be scaled by up to 1,024 before being used as the timer clock.

UARTs

The SoC contains three UART channels. All channels are directly controlled by the MAXQ30 core and feature independent baud rate generators.

Each UART features:

- Four modes of operation: one synchronous, three asynchronous
- Dedicated baud rate generators per UART
- Double-buffered transmitter and receiver
- Odd, even, or no parity
- 1, 1½, or 2 stop bits
- Maskable interrupts for receive buffer full or transmit buffer empty

Optical Modulator

UART0 is provided with an optical modulator. When the optical modulator is enabled, the transmit data from the UART is modulated with a carrier frequency (usually 38kHz, but configurable). For optical reception of a modulated signal, an IR remote receiver should be interfaced to the UART RX pin.

LCD Controller

The SoC includes an LCD controller that supports up to six common planes and up to 39 segments. It can control bare glass LCD displays natively operating up to 3.3V. The LCD controller supports many operating modes, including:

- Static, with up to 39 segments
- Two common planes with up to 39 segment circuits for a total of 78 segments operating at ½ bias
- Three common planes with up to 39 segment circuits for a total of 117 segments operating at ½ or ⅓ bias
- Four common planes with up to 39 segment circuits for a total of 156 segments operating at ⅓ bias
- Five common planes with up to 38 segment circuits for a total of 190 segments operating at ⅓ bias
- Six common planes with up to 37 segment circuits for a total of 222 segments operating at ⅓ bias

Additionally, the LCD controller has test features that allow all segments to be turned on or off without disturbing LCD data, a reset feature that quickly clears all LCD data, and a built-in DAC for contrast adjustment.

LCD Special Modes

The LCD controller is capable of much more than just displaying the contents of the LCD display registers. Special LCD modes include blinking up to twelve segments (two segment circuits on each of six common circuits), alternate page configurations so that one page can be updated while the other is being displayed, and all segments on/all segments off for test purposes.

I²C Interface

The SoC includes an I²C peripheral that can act as an I²C master or slave.

The I²C bus is a bidirectional two-wire serial bus interface. It has the following characteristics:

- Information is transferred over a serial data circuit (SDA) and serial clock circuit (SCL).
- The peripheral can operate in either a master mode or a slave mode.
- The peripheral supports either standard (7-bit) addressing or extended (10-bit) addressing.
- The peripheral operates in three modes to support multiple transfer rates.
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1Mbps
- The peripheral contains an on-chip filter to reject spikes on the data circuit.

SPI

The serial peripheral interface (SPI) provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface provides access to a four-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is up to the system reference clock frequency for master mode. For slave mode, the maximum frequency is a function on the I/O driver, character length, and the system clock.

The main element in the SPI module is the block containing the shift register, the transmit FIFO and the receive FIFO. The shift register is double buffered and serves as temporary data storage. The receive FIFO holds received data from the network. The transmit FIFO contains data ready to be transmitted out.

The SPIB SFR provides access for both transmit and receive data. Reads are directed to the read FIFO. Writes are directed to the shift register automatically if the transmit FIFO is empty; otherwise, write operations store data into the transmit FIFO.

The four interface signals used by the SPI are MISO, MOSI, SCLK, and SSEL:

MISO (Master In/Slave Out). This signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most significant bit first. The slave device places the MISO pin in an input state with a weak pull-up when it is not selected.

MOSI (Master Out/Slave In). This signal is an output from a master device and an input to the slave devices. It is used to serially transfer data from the master to the selected slave. Data is transferred most significant bit first.

SCLK (SPI Clock). This serial clock is an output from the master device and an input to the slave devices. It is used to synchronize the transfer of data between the master and the slave on the data bus.

SSEL (Slave Select). The slave select signal enables a SPI slave when activated by a master device. The slave can be configured to select the active state of SSEL. When the master asserts SSEL it is signaling the beginning of an SPI transfer. SSEL should remain asserted for the duration of the transfer.

Touch Sensors

The SoC contains a capacitive touch switch input. This input is designed to operate with a wide range of quiescent capacitance values and should be generally immune from most noise sources.

The touch switch uses a free-running oscillator with the frequency of the oscillator determined by the capacitance at the pin. Placing a finger near the touch plate connected to the pin changes the capacitance at the pin, which changes the oscillator frequency. This shift in frequency is detected by internal logic and can be used to signal an event to the processor.

Multiply-Accumulate Unit

The SoC provides a 32 x 32 fixed-point multiply-accumulate unit to assist in mathematical operations. The multiplier provides a 64-bit result in a single cycle, and sums the product to a 64-bit accumulator in the same cycle. The multiplier is ready for another operation two cycles later. If the MAXQ30 core is running at 10MHz, the multiplier can perform five million 32 x 32 multiply cycles per second, in theory (in practice, the throughput is slowed by the requirement of loading and unloading the multiplier registers).

Real-Time Clock

The SoC's real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. The RTC includes:

- 32-bit seconds register
- Eight-bit subseconds register
- 32-bit alarm register
- Wake MPU from sleep mode on a variety of events
- Temperature measurement
- Third-order (cubic) temperature compensation hardware
- Battery condition monitor

The RTC block resides across three power domains. The real-time clock itself and the oscillator that drives it must reside in a nonvolatile power domain since the RTC cannot be allowed to lose time when power fails. The wake controller also resides in this power domain so that it can wake the MPU even when all other power sources are shut off.

Other RTC logic, such as the temperature measurement and temperature compensation logic, resides in an on-demand power domain. The operation of this logic section depends upon the operating mode of the SoC.

When the device is in either the mission or the brownout mode, this domain is always powered. When the programmable RTC measurement timer expires, the chip temperature is measured and the RTC temperature compensation adjusts to reflect the last temperature measurement. For details of the RTC temperature compensation, refer to the ZON M1 Hardware Reference Manual.

When the device is in LCD or sleep modes, the on-demand domain is normally powered off. When the RTC measurement timer expires, this domain powers up, and the device temperature is measured. If the temperature change has exceeded a programmed difference from the previous measurement, the hardware updates the saved temperature measurement, updates the oscillator temperature compensation, and then powers off the on-demand domain.

The final power domain is the mission mode domain. It has power only when the MPU is actually active. This domain contains the MPU facing registers and

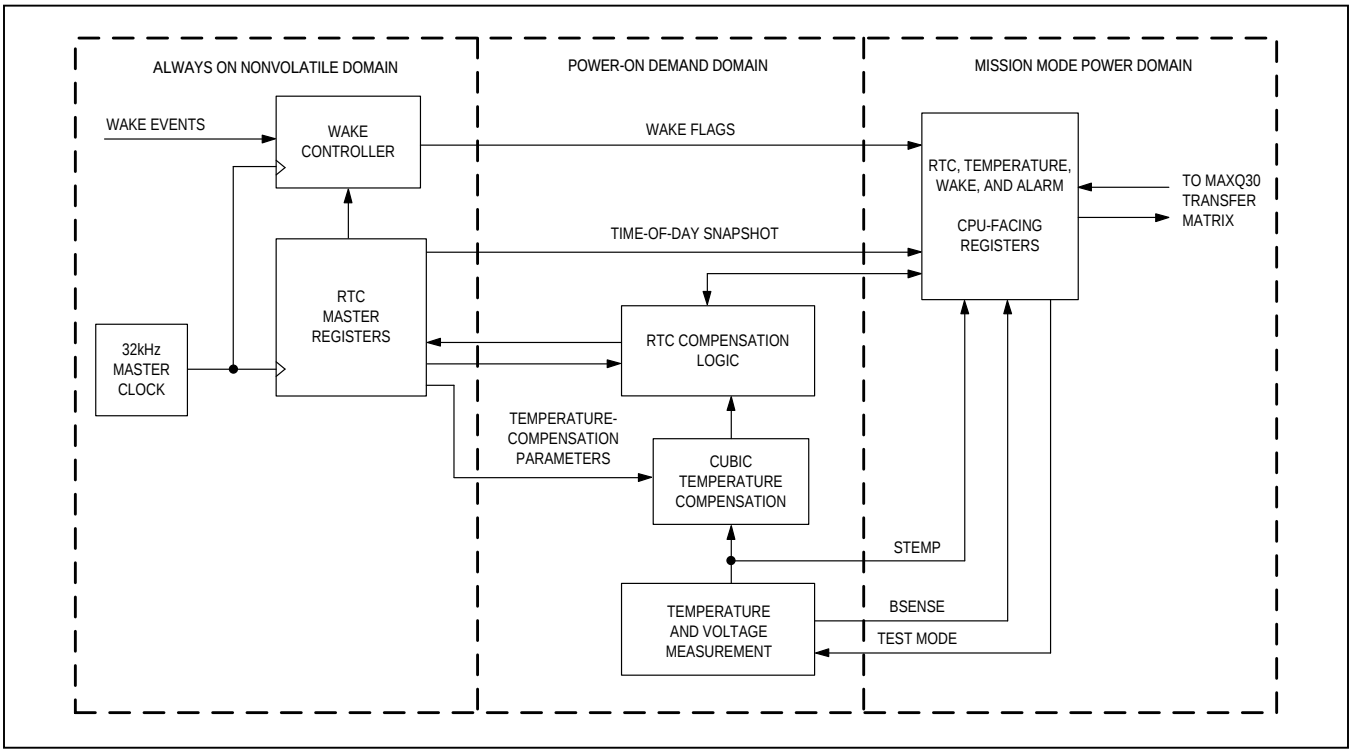


Figure 4. Real-Time Clock Block Diagram

associated interface logic. By keeping this domain off unless the MPU is active battery power is saved.

Digital I/O

The SoC contains a number of pins that can be configured as digital I/O, either as peripheral pins or as direct-write general-purpose I/O. When assigned to a peripheral, these pins are automatically configured for the selected peripheral. When assigned for general-purpose I/O, the user can select from a number of different configurations.

DIO pins are organized as two 32-bit ports, port 0 and port 1. Each bit is individually configurable for input, output or bidirectional modes. All 32 bits of either port are not implemented in the ZON M1L/M1. Refer to the pin description table for details.

External Interrupts

Six of the DIO pins can be configured as external interrupts. All are edge triggered, with the active edge selectable.

Hardware Watchdog Timer

There are two watchdog timers in the SoC: fixed-duration (always runs and is always enabled) and software-enabled.

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (kB)	DATA MEMORY (kB)	PIN-PACKAGE
MAX71313LECB+ (ZON M1L)	-40°C to +85°C	+3.0 to +3.6	64	8	64 LQFP
MAX71313LECB+T (ZON M1L)	-40°C to +85°C	+3.0 to +3.6	64	8	64 LQFP
MAX71314LECB+ (ZON M1)	-40°C to +85°C	+3.0 to +3.6	128	8	64 LQFP
MAX71314LECB+T (ZON M1)	-40°C to +85°C	+3.0 to +3.6	128	8	64 LQFP

+Denotes a lead(PB)-free/RoHS-compliant package.

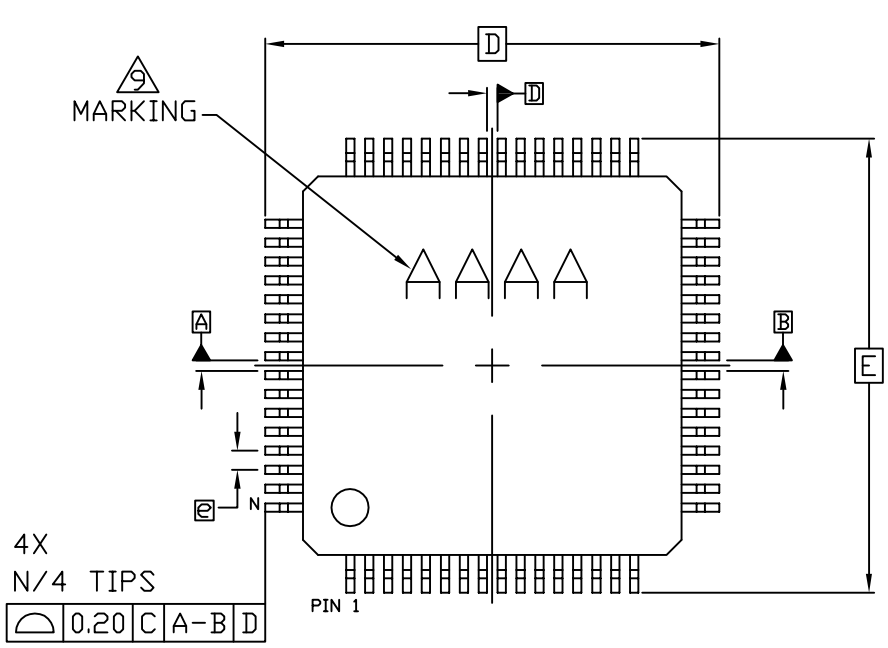
T = *Tape and reel.*

Package Information

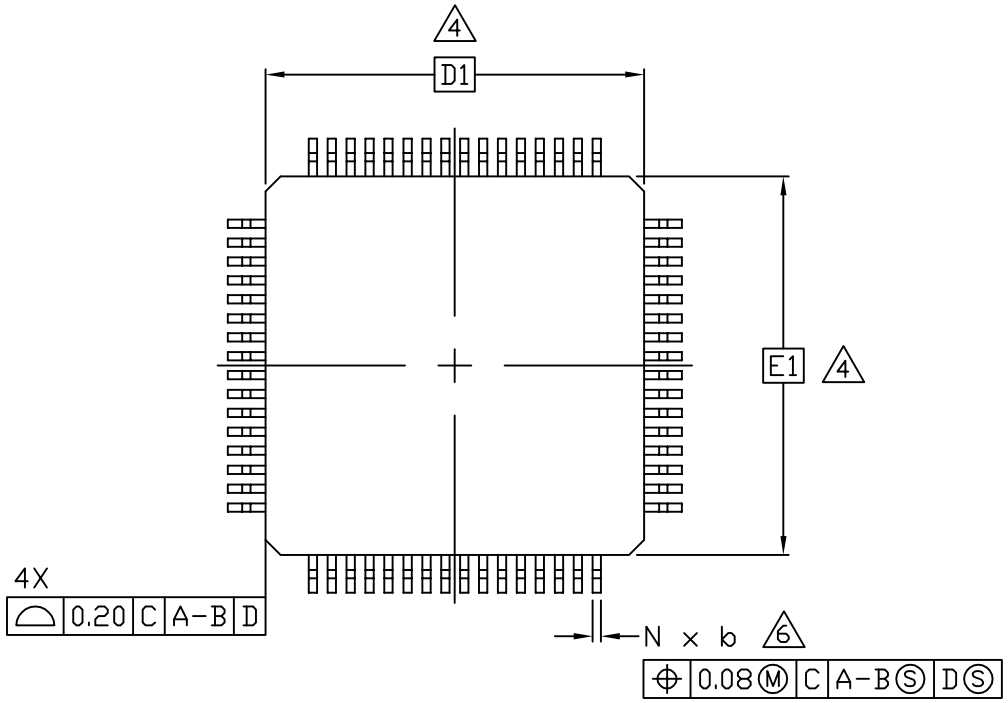
Package outline information and land patterns (footprints) are appended to this document.

Revision History

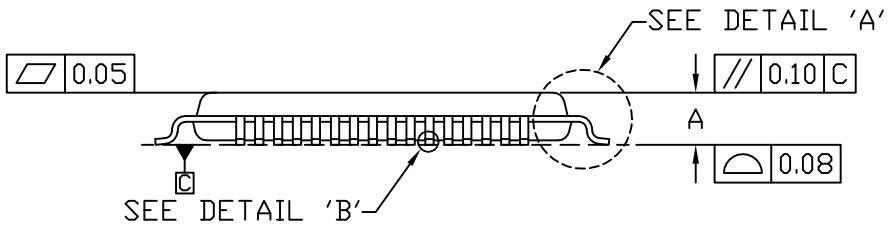
REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	11/14	Removed future product references	24
2	4/16	Rebranding only	



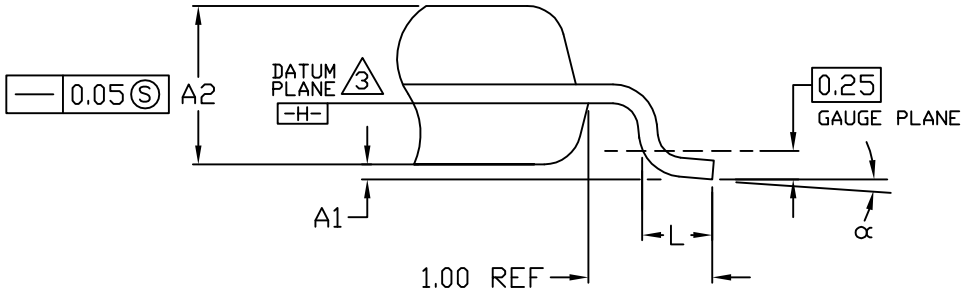
TOP VIEW



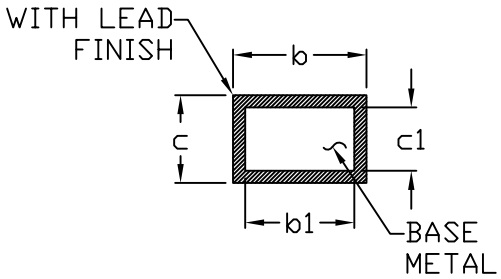
BOTTOM VIEW



SIDE VIEW



DETAIL "A"



LEAD TIP DETAIL

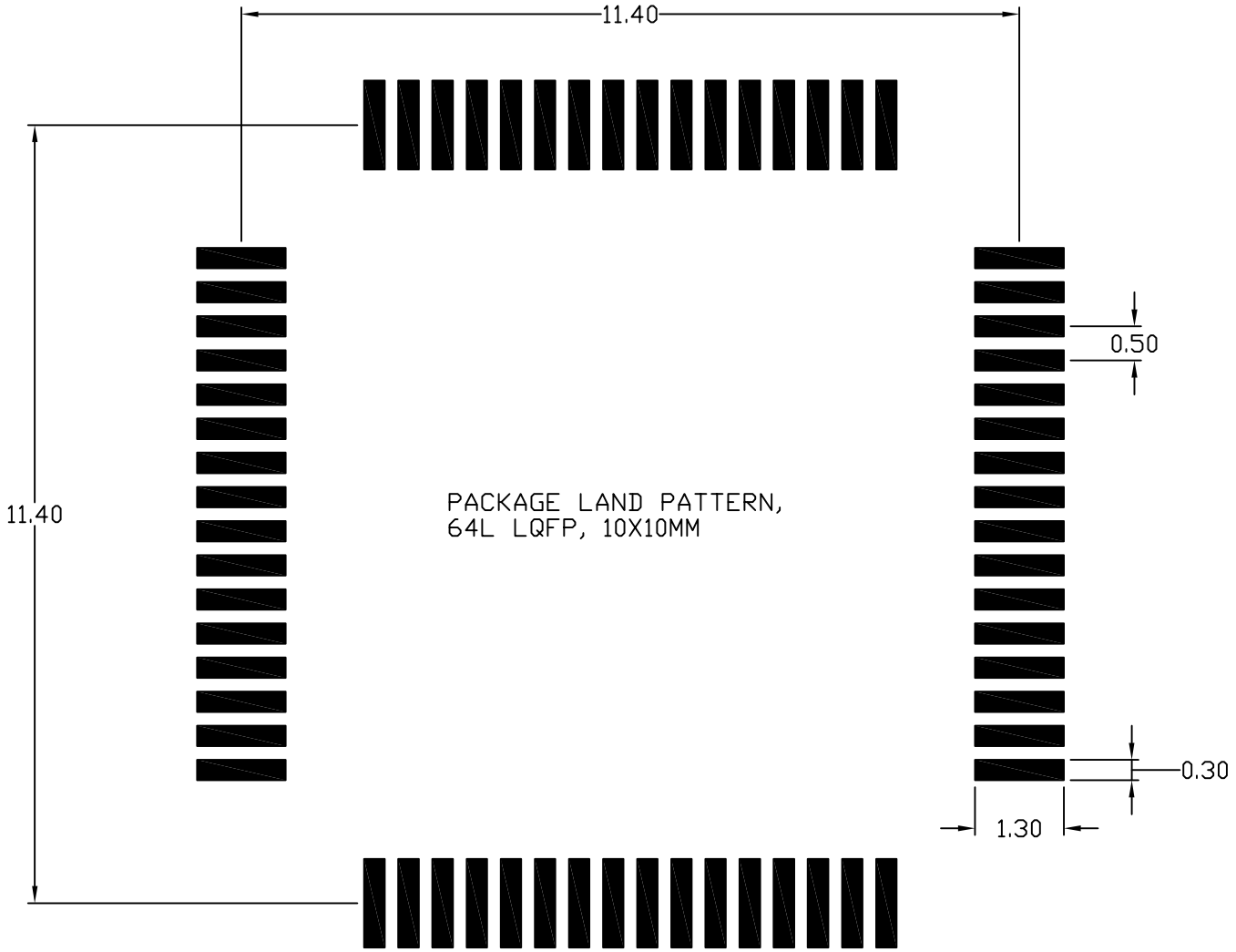
DETAIL 'B'

64L LQFP, 10X10MM

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
3. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026, VARIATION BCD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. "N" IS THE TOTAL NUMBER OF TERMINALS.

JEDEC VARIATION			
	BCD		
	64 LEAD		
	MIN	NOM	MAX
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
D	12.00 BSC.		
D1	10.00 BSC.		
E	12.00 BSC.		
E1	10.00 BSC.		
e	0.50 BSC.		
L	0.45	0.60	0.75
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	---	0.20
c1	0.09	---	0.16
α	0°	---	7°



NOTES:

1. ALL DIMENSIONS IN MM
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.