MAX71314/MAX71315 Single-Phase Electricity Meter SOC

General Description

The MAX71314/MAX71315 integrate dual 32-bit processors for demanding single-phase metering applications with 256kB flash (MAX71315) or 128kB flash (MAX71314), 12kB RAM, and a single-cycle 32 x 32 + 64 multiplier. The user processor (MPU) is a 32-bit MAXQ®30 core. The metrology compute engine (CE) is a 32-bit processor dedicated to computing the metering parameters from voltage and current samples.

Features and Benefits

- Four Independent Metrology Channels
- 0.1% Accuracy Over 5000:1 Current Range with Integrated Metrology ADCs
- Two Remote ADC Interfaces
- Support Current Transformers, Rogowski Coils, and Shunts
- Four Pulse Outputs from the CE
- Digital Temperature Compensation for Metrology
- 45Hz to 65Hz Line Frequency Range with the Same Calibration
- Phase Compensation (±10°)
- 256kB Flash, 12kB SRAM (MAX71315)
- 128kB Flash, 12kB SRAM (MAX71314)
- Single-Cycle 32 x 32 + 64 Multiply-Accumulate Unit
- Low-Power 5ksps ADC for Environmental Monitoring
- RTC with Temperature Compensation
- On-Chip Digital Temperature Sensor
- LCD Controller Supporting Up to Eight Common Planes
- Two PWM Relay Control Channels with Programmable Frequency, Duty Cycle, and Ramp Time
- Two Touch Switch Inputs
- 12.5mA Typical Consumption at 3.3V and 10MHz in Active Mode
- 1.75µA Sleep Mode
- SPI (Master and Slave), Master I^2C, 4 x UARTs
- Two Smart Card Ports
- 38kHz IR Encoder/Decoder
- Up to 10 MIPS (at 10MHz)
- 100-Pin LQFP

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX71314.related**.*

***Ordering Information** appears at end of data sheet.*

19-6883; Rev 0; 12/13

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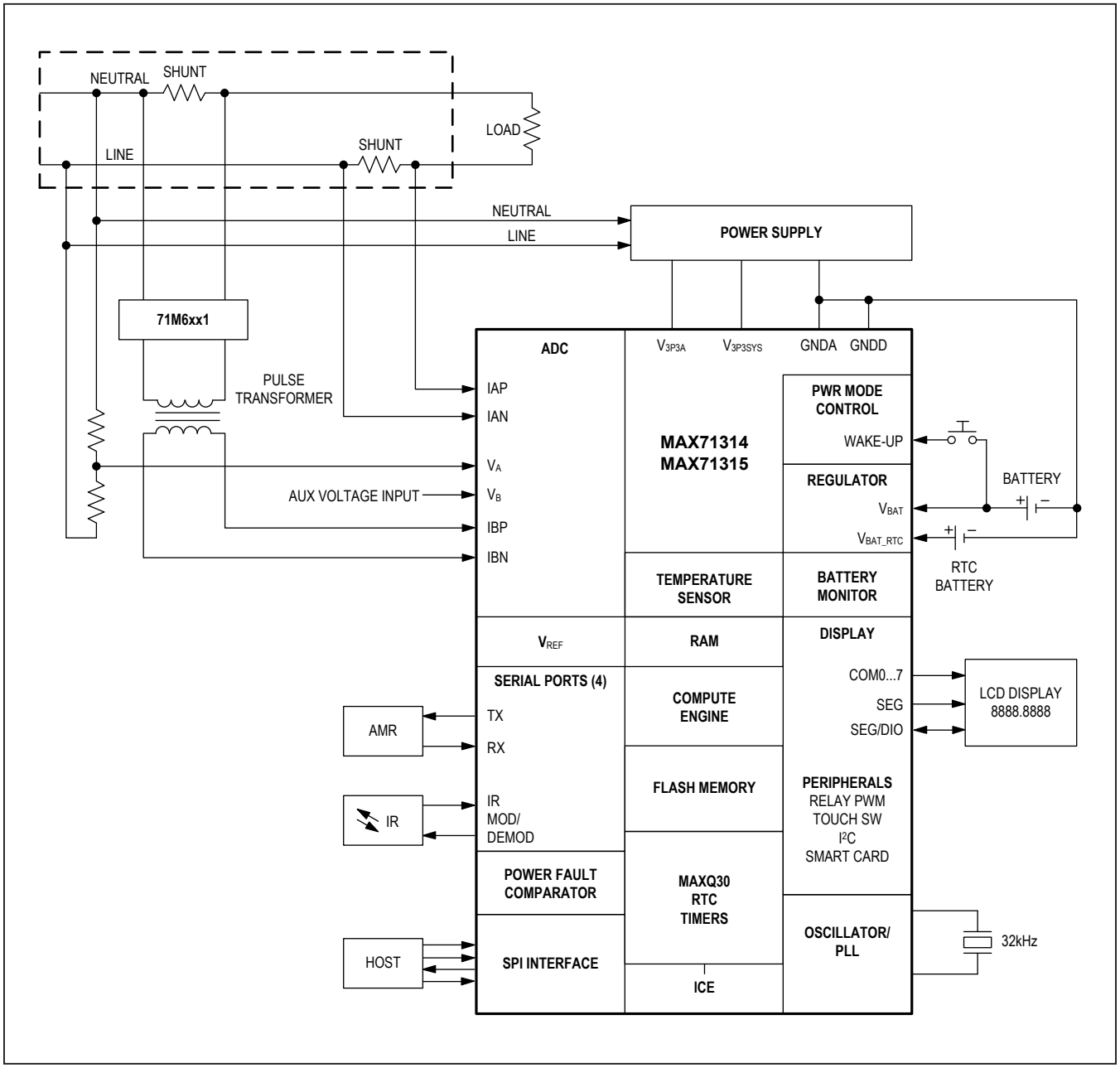
Typical Operating Circuit



Absolute Maximum Ratings

Voltage, Current Supplies, and Ground Pins:
V_{3P3SYS} .....-0.5 to +3.6V
Crystal Pins:
XIN, XOUT.....(-10mA to +10mA), (-0.5V to +3.0V)
Digital Pins:
Inputs (MSN/BRN Mode)... (-10mA to +10mA), (-0.5V to +6V)
Inputs (SLP Mode)..... (-10mA to +10mA), (-0.5V to V_{3P3SYS} + 0.5V)
Outputs ..... (-8mA to +8mA), (-0.5V to (V_{3P3SYS} + 0.5V))

Temperature and ESD Stress
Operating Junction Temperature (peak, 100ms).....+140°C
Operating Junction Temperature (continuous).....+125°C
Storage Temperature Range..... -45°C to +165°C
ESD Stress on All Pins.....±4kV, HBM
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+250°C

Package Thermal Characteristics (Note 1)

LQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....47.88°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....10.90°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{3P3SYS} = V_{3P3A} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{3P3SYS}		3.0		3.6	V
Supply Voltage, Backup Battery	V_{BAT}		2.5		3.8	V
Supply Voltage, RTC Battery	V_{BAT_RTC}		2.0		3.8	V
Supply Current	I_{DD1}	(Note 3)		12.5	20.0	mA
Supply Current	I_{DD2}	(Note 4)		11.0	17.0	mA
Dynamic Current		V_{3P3SYS} = V_{3P3A} = 3.3V, metrology enabled, ADC operating full speed, ($I_{CPUCLK=10MHz}$ - $I_{CPUCLK=1.25MHz}$)/4.3		356		µA/MHz
V_{BAT} Current	I_{VBAT}	MSN mode	-100		+600	nA
		BRN mode		8.5	16.0	mA
		SLP mode		2	360	nA

Electrical Characteristics (continued)

(V_{3P3SYS} = V_{3P3A} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BAT_RTC} Current	I_{VBAT_RTC}	MSN mode, *TEMP_PWR = 1*		±100		nA
		BRN mode, *TEMP_PWR = 1*		1		µA
		SLP mode		1.75	36.00	µA
CRYSTAL OSCILLATOR						
RTC Oscillator Frequency	f_{RTC}			32.768		kHz
Peak Output Source Current	I_{XOUT}		0.4		3.5	µA
Maximum Output Voltage					1.5	V
Maximum Crystal Power					1	µW
Frequency Variation with Voltage		T_A = +25°C, V_{3P3SYS} = 0V, V_{BAT_RTC} = 2.0V to 3.8V		0.86		ppm
LOGIC LEVELS						
Digital High-Level Input Voltage	V_{IH}		+2.0			V
Digital Low-Level Input Voltage	V_{IL}				+0.6	V
Input Leakage Current			-1.3		+1.3	µA
Input Pullup Current, RSTN		V_{IN} = 0V	5		160	µA
Input Pulldown Current, JTAG_E		V_{IN} = V_{3P3SYS}	30		160	µA
Digital High-Level Output Voltage	V_{OH}	I_{LOAD} = 5mA	V_{3P3D} - 0.4			V
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = -1mA			0.4	V
		I_{LOAD} = -5mA			0.85	V
BATTERY MONITOR						
Measurement Error		V_{BAT} = 2.0V to 3.8V, sensing either V_{BAT} or V_{BAT_RTC}			4	%

Electrical Characteristics (continued)

(V_{3P3SYS} = V_{3P3A} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE MONITOR						
Temperature Error		T_A = +22°C		±3.6		°C
Relative Temperature Error		-40°C < T < +85°C, 3.0V < V_{3P3A} < 3.6V	-1.75		+1.75	°C
LCD						
V_{LCD} Current		V_{LCD} = 3.3V			4	µA
V_{REF}						
Nominal Reference Voltage	V_{REF}	T_A = +22°C	1.226	1.228	1.230	V
Variation with Power Supply		V_{3P3A} = 3.0V to 3.6V	-1.5		+1.5	mV/V
Deviation from Predicted Variation with Temperature			-40		+40	ppm/°C
ADC						
Usable Input Range		Preamp off	-250		+250	mV peak
		Preamp gain = 4	-26.5		+26.5	
		Preamp gain = 8	-13		+13	
		Preamp gain = 16	-6.5		+6.5	
Input Impedance		f_{IN} = 65Hz, preamp off	140		450	kΩ
		f_{IN} = 65Hz, preamp gain = 4	2.5		10.0	
		f_{IN} = 65Hz, preamp gain = 8	2.5		10.0	
		f_{IN} = 65Hz, preamp gain = 16	2.5		10.0	
LSB Size		FIR_LEN = 15		97		nV/LSB
Digital Full Scale		FIR_LEN = 15		±3375000		LSB
Input Offset Voltage			-10		+10	mV
THD, Voltage Channel				-85		dB

Electrical Characteristics (continued)

(V_{3P3SYS} = V_{3P3A} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THD, Current Channel		No preamp		-87		dB
		Preamp gain = 8		-85		dB
Current Channel Preamp Gain		Preamp gain = 4	3.9	4.0	4.1	V/V
		Preamp gain = 8	7.8	8.0	8.2	
		Preamp gain = 16	15.6	16.0	16.4	
Gain Variation with Supply Voltage			-40		+40	ppm/%
Gain Variation with Temperature		(Note 5)	-55		+55	ppm /°C
Current Channel Phase Shift		+25°C, V_{3P3A} = 3.0V to 3.6V		6		m°
Phase Shift Variation with Supply		(Note 5)	-20		+20	m°/V
Phase Shift Variation with Temperature		(Note 5)	-0.1		+0.1	m°/°C
INTERNAL OSCILLATOR						
Nominal Frequency				24		MHz
Base Accuracy			-2		+2	%
Frequency Variation with Supply				-7.21		kHz/V

Note 2: Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 3: Supply current is the combined current into V_{3P3SYS} and V_{3P3A}; part is out of reset, no port activity, no flash writes, measured at V_{3P3SYS} =V3P3A =3.3V, executing from flash, CPUCLK = 10MHz, metrology enabled, with ADC operating full speed.

Note 4: Supply current is the combined current into V_{3P3SYS} and V_{3P3A}; part is out of reset, no port activity, no flash writes, measured at V_{3P3SYS} = V_{3P3A} = 3.3V, executing from flash, CPUCLK = 10MHz, metrology enabled, with ADC operating half speed.

Note 5: Guaranteed by design, not production tested.

Functional Block Diagram

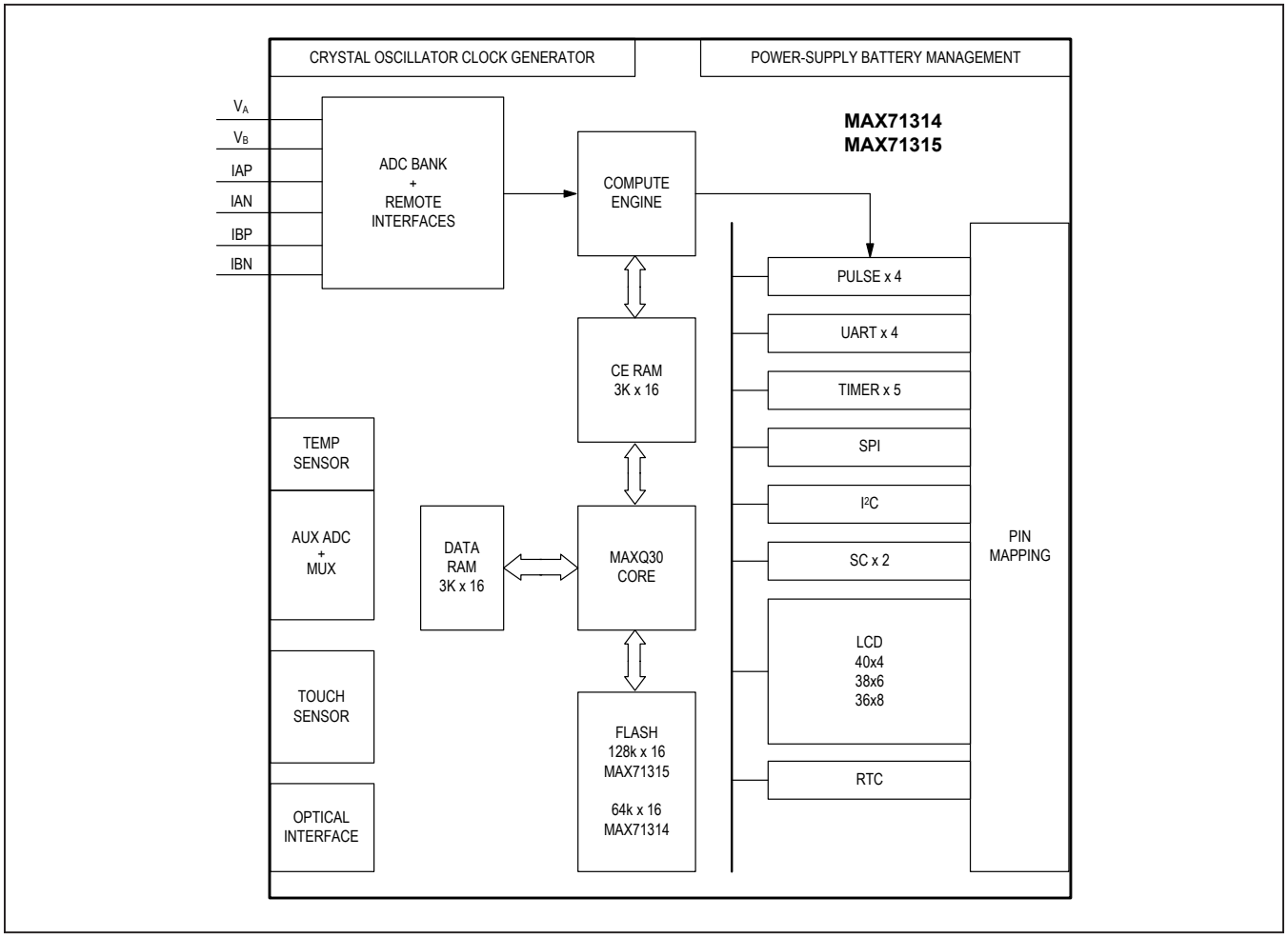
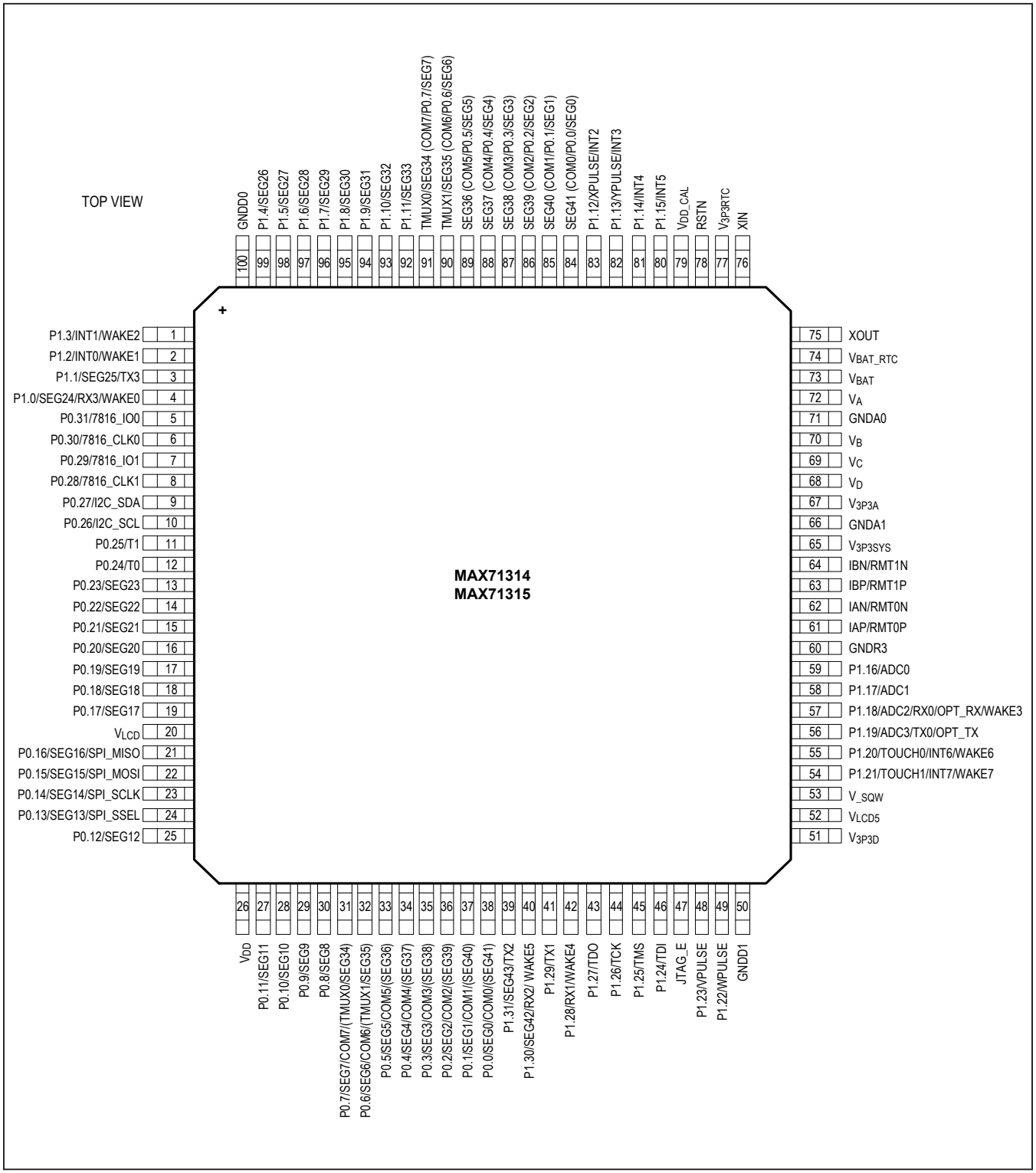


Table 1. Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C2	V_{3P3D}	GNDD	Bypass capacitor for 3.3V output	0.1 ± 20%	µF
CSYS	V_{3P3SYS}	GNDD	Bypass capacitor for V_{3P3SYS}	≥ 1.0 ± 30%	µF
CVDD	V_{DD}	GNDD	Bypass capacitor for V_{DD}	0.1 ± 20%	µF
CVLCD	V_{LCD}	GNDD	Bypass capacitor for V_{LCD} pin (when charge pump is used)	≥ 0.1 ± 20%	µF
XTAL	XIN	XOUT	32.768kHz tuning-fork crystal, electrically similar to: ECS .327-12.5-17X, Vishay XT26T, or Suntsu SCP6-32.768kHz TR (load capacitance 12.5pF).	32.768	kHz
CXS	XIN	GNDA	Load capacitor values for crystal depends on crystal specifications and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance.	22 ± 10%	pF
CXL	XOUT	GNDA		22 ± 10%	pF

Pin Configuration



Pin Description (Sorted by Pin Number)

PIN	NAME	FUNCTION	PRIORITY
1	P1.3/INT1/WAKE2	GPIO Port 1 Bit 3; External Interrupt 1; CPU Wake Input 2	Dedicated GPIO bit; interrupt and wake functions independently enabled.
2	P1.2/INT0/WAKE1	GPIO Port 1 Bit 2; External Interrupt 0; CPU Wake Input 1	Dedicated GPIO bit; interrupt and wake functions independently enabled.
3	P1.1/SEG25/TX3	GPIO Port 1 Bit 1; LCD Segment 25; UART 3 Transmit Data	LCD GPIO UART
4	P1.0/SEG24/RX3/WAKE0	GPIO Port 1 Bit 0; LCD Segment 24; UART 3 Receive Data; CPU Wake Input 0	LCD GPIO, UART receive
5	P0.31/7816_IO0	GPIO Port 0 Bit 31; ISO UART 0 Data In/Out	ISO UART (if enabled) GPIO
6	P0.30/7816_CLK0	GPIO Port 0 Bit 30; ISO UART 0 Clock	ISO UART (if enabled) GPIO
7	PP0.29/7816_IO1	GPIO Port 0 Bit 29; ISO UART 1 Data In/Out	ISO UART (if enabled) GPIO
8	P0.28/7816_IO_CLK1	GPIO Port 0 Bit 28; ISO UART 1 Clock	ISO UART (if enabled) GPIO
9	P0.27/I2C_SDA	GPIO Port 0 Bit 27; I^2C SDA	I^2C port (if enabled) GPIO
10	P0.26/I2C_SCL	GPIO Port 0 Bit 26; I^2C SCL	I^2C port (if enabled) GPIO
11	P0.25/T1	GPIO Port 0 Bit 25; Timer 1 Output	PWM output function (if configured) GPIO
12	P0.24/T0	GPIO Port 0 Bit 24; Timer 0 Output	PWM output function (if configured) GPIO
13	P0.23/SEG23	GPIO Port 0 Bit 23; LCD Segment 23	LCD GPIO
14	P0.22/SEG22	GPIO Port 0 Bit 22; LCD Segment 22	LCD GPIO
15	P0.21/SEG21	GPIO Port 0 Bit 21; LCD Segment 21	LCD GPIO
16	P0.20/SEG20	GPIO Port 0 Bit 20; LCD Segment 20	LCD GPIO
17	P0.19/SEG19	GPIO Port 0 Bit 19; LCD Segment 19	LCD GPIO
18	P0.18/SEG18	GPIO Port 0 Bit 18; LCD Segment 18	LCD GPIO
19	P0.17/SEG17	GPIO Port 0 Bit 17; LCD Segment 17	LCD GPIO
20	V_{LCD}	LCD Supply Voltage	—
21	P0.16/SEG16/SPI_MISO	GPIO Port 0 Bit 16; LCD Segment 16; SPI_MISO	LCD SPI port (if enabled) GPIO

Pin Description (Sorted by Pin Number) (continued)

PIN	NAME	FUNCTION	PRIORITY
22	P0.15/SEG15/SPI_MOSI	GPIO Port 0 Bit 15; LCD Segment 15; SPI_MOSI	LCD SPI port (if enabled) GPIO
23	P0.14/SEG14/SPI_SCLK	GPIO Port 0 Bit 14; LCD Segment 14; SPI_SCLK	LCD SPI port (if enabled) GPIO
24	P0.13/SEG13/SPI_SSEL	GPIO Port 0 Bit 13; LCD Segment 13; SPI_SSEL	LCD SPI port (if enabled) GPIO
25	P0.12/SEG12	GPIO Port 0 Bit 12; LCD Segment 12	LCD GPIO
26	V_{DD}	—	—
27	P0.11/SEG11	GPIO Port 0 Bit 11; LCD Segment 11	LCD GPIO
28	P0.10/SEG10	GPIO Port 0 Bit 10; LCD Segment 10	LCD GPIO
29	P0.9/SEG9	GPIO Port 0 Bit 9; LCD Segment 9	LCD GPIO
30	P0.8/SEG8	GPIO Port 0 Bit 8; LCD Segment 8	LCD GPIO
31	P0.7/SEG7/COM7/(TMUX0/SEG34)	GPIO Port 0 Bit 7; LCD Segment 7; LCD Common 7 (Mirrored Segment 34)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
32	P0.6/SEG6/COM6/(TMUX1/SEG35)	GPIO Port 0 Bit 6; LCD Segment 6; LCD Common 6 (Mirrored Segment 35)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
33	P0.5/SEG5/COM5/(SEG36)	GPIO Port 0 Bit 5; LCD Segment 5; LCD Common 5 (Mirrored Segment 36)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
34	P0.4/SEG4/COM4/(SEG37)	GPIO Port 0 Bit 4; LCD Segment 4; LCD Common 4 (Mirrored Segment 37)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
35	P0.3/SEG3/COM3/(SEG38)	GPIO Port 0 Bit 3; LCD Segment 3; LCD Common 3 (Mirrored Segment 38)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO

Pin Description (Sorted by Pin Number) (continued)

PIN	NAME	FUNCTION	PRIORITY
36	P0.2/SEG2/COM2/(SEG39)	GPIO Port 0 Bit 2; LCD Segment 2; LCD Common 2 (Mirrored Segment 39)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
37	P0.1/SEG1/COM1/(SEG40)	GPIO Port 0 Bit 1; LCD Segment 1; LCD Common 1 (Mirrored Segment 40)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
38	P0.0/SEG0/COM0/(SEG41)	GPIO Port 0 Bit 0; LCD Segment 0; LCD Common 0 (Mirrored Segment 41)	Mirrored function (if enabled) LCD common (if enabled) LCD segment GPIO
39	P1.31/SEG43/TX2	GPIO Port 1 Bit 31; LCD Segment 43; UART 2 Transmit Data	LCD segment UART (If enabled in LCD assignment register) GPIO
40	P1.30/SEG42/RX2/WAKE5	GPIO Port 1 Bit 30; LCD Segment 42; UART 2 Receive Data; CPU Wake Input 5	LCD segment GPIO UART input and CPU wake input are available in parallel with GPIO functions, if enabled.
41	P1.29/TX1	GPIO Port 1 Bit 29; UART 1 Transmit Data	UART (If enabled in LCD assignment register) GPIO
42	P1.28/RX1/WAKE4	GPIO Port 1 Bit 28; UART 1 Receive Data; CPU Wake Input 4	Dedicated GPIO bit; UART and wake functions independently enabled.
43	P1.27/TDO	GPIO Port 1 Bit 27; JTAG TDO	JTAG (if enabled with JTAG_E pin) GPIO
44	P1.26/TCK	GPIO Port 1 Bit 26; JTAG TCK	JTAG (if enabled with JTAG_E pin) GPIO
45	P1.25/TMS	GPIO Port 1 Bit 25; JTAG TMS	JTAG (if enabled with JTAG_E pin) GPIO
46	P1.24/TDI	GPIO Port 1 Bit 24; JTAG TDI	JTAG (if enabled with JTAG_E pin) GPIO
47	JTAG_E	JTAG Port Enable	—
48	P1/23/VPULSE	GPIO Port 1 Bit 23	VPULSE output (if enabled) GPIO
49	P1/22/WPULSE	GPIO Port 1 Bit 22	WPULSE output (if enabled) GPIO
50	GNDD	Digital Ground	—
51	V_{3P3D}	Power Output for External Digital Devices	—
52	V_{LCD5}	Input from External LCD Charge Pump	—
53	$V_{\_SQW}$	Square-Wave Output for LCD Charge Pump	—

Pin Description (Sorted by Pin Number) (continued)

PIN	NAME	FUNCTION	PRIORITY
54	P1.21/TOUCH1/INT7/ WAKE7	GPIO Port 1 Bit 21; Touch Input 1; External Interrupt 7; CPU Wake Input 7	Touch input (if enabled) GPIO; external interrupts are available when GPIO is selected.
55	P1.20/TOUCH01/INT7/ WAKE6	GPIO Port 1 Bit 20; Touch Input 0; External Interrupt 6; CPU Wake Input 6	Touch input (if enabled) GPIO; external interrupts are available when GPIO is selected.
56	P1.19/ADC3/TX0/OPT_TX	GPIO Port 1 Bit 19; AUX ADC Input 3; UART 0 Transmit Data; Optical Transmit	AUX ADC (if selected) UART 0 (optionally modulated for optical transmission) GPIO.
57	P1.18/ADC2/RX0/OPT_RX/ WAKE3	GPIO Port 1 Bit 18; AUX ADC Input 2; UART 0 Receive Data; Optical Receive/ CPU Wake Input 3	AUX ADC (if selected) GPIO The optical receiver is enabled if the AUX ADC input is enabled, the demodulation filter is active and the UART receiver is enabled.
58	P1.17/ADC1	GPIO Port 1 Bit 17; AUX ADC Input 1	AUX ADC (if selected) GPIO
59	P1.16/ADC0	GPIO Port 1 Bit 16; AUX ADC Input 0	AUX ADC (if selected) GPIO
60	GNDR	Ground for Remote ADC Channels	—
61	IAP/RMT0P	Current Input A, Noninverting input; Remote Interface 0 Positive Pole	RMT0P (if enabled) IAP
62	IAN/RMT0N	Current input A, Inverting Input; Remote Interface 0 Negative Pole	RMT0N (if enabled) IAN
63	IBP/RMT1P	Current input B, Noninverting Input; Remote Interface 1 Positive Pole)	RMT1P (if enabled) IBP
64	IBN/RMT1N	Current input B, Inverting Input; Remote Interface 1 Negative Pole	RMT1N (if enabled) IBN
65	V_{3P3SYS}	Main Power Input (3.3V)	—
66	GNDA	Analog Ground	—
67	V_{3P3A}	3.3V Analog Input	—
68	V_D	Additional Voltage Input for Metrology ADC	—
69	V_C	Additional Voltage Input for Metrology ADC	—
70	V_B	Additional Voltage in Input for Metrology ADC	—
71	GNDA	Analog Ground	—
72	V_A	Voltage Sensor Input A	—
73	V_{BAT}	Primary Backup Battery Input	—
74	V_{BAT_RTC}	RTC Backup Battery Input	—
75	XOUT	32kHz Crystal Amplifier Output	—

Pin Description (Sorted by Pin Number) (continued)

PIN	NAME	FUNCTION	PRIORITY
76	XIN	32kHz Crystal Amplifier Input	—
77	V_{3P3RTC}	—	—
78	RSTN	Active-Low Reset Input	—
79	V_{DD_CAL}	—	—
80	P1.15/INT5	GPIO Port 1 Bit 15; External Interrupt 5	Dedicated GPIO bit; interrupt function independently enabled.
81	P1.14/INT4	GPIO Port 1 Bit 14; External Interrupt 4	Dedicated GPIO bit; interrupt function independently enabled.
82	P1.13/YPULSE/INT3	GPIO Port 1 Bit 13; YPULSE; External Interrupt 3	YPULSE output (if enabled) GPIO The external interrupt function operates whether or not the pulse output is enabled
83	P1.12/XPULSE/INT2	GPIO Port 1 Bit 12; XPULSE; External Interrupt 2	XPULSE output (if enabled) GPIO The external interrupt function operates whether or not the pulse output is enabled
84	SEG41 (COM0/P0.0/SEG0)	LCD Segment 41 (Mirrored LCD Common 0; GPIO Port 0 Bit 0; LCD Segment 0)	Mirrored function (if enabled) LCD segment
85	SEG40 (COM1/P0.1/SEG1)	LCD Segment 40 (Mirrored LCD Common 1; GPIO Port 0 Bit 1; LCD Segment 1)	Mirrored function (if enabled) LCD segment
86	SEG39 (COM2/P0.2/SEG2)	LCD Segment 39 (Mirrored LCD Common 2; GPIO Port 0 Bit 2; LCD Segment 2)	Mirrored function (if enabled) LCD segment
87	SEG38 (COM3/P0.1/SEG3)	LCD Segment 38 (Mirrored LCD Common 3; GPIO Port 0 Bit 3; LCD Segment 3)	Mirrored function (if enabled) LCD segment
88	SEG37 (COM4/P0.4/SEG4)	LCD Segment 37 (Mirrored LCD Common 4; GPIO Port 0 Bit 4; LCD Segment 4)	Mirrored function (if enabled) LCD segment
89	SEG36 (COM5/P0.5/SEG5)	LCD Segment 36 (Mirrored LCD common 5; GPIO Port 0 Bit 5; LCD Segment 5)	Mirrored function (if enabled) LCD segment
90	TMUX1/SEG35/ (COM6/P0.6/SEG6)	TMUX1; LCD Segment 35 (Mirrored LCD Common 6; GPIO Port 0 Bit 6; LCD Segment 6)	Mirrored function (if enabled) LCD segment TMUX1
91	TMUX0/SEG34/ (COM7/P0.7/SEG7)	TMUX0; LCD Segment 34 (Mirrored LCD Common 7; GPIO Port 0 Bit 7; LCD Segment 7)	Mirrored function (if enabled) LCD segment TMUX0
92	P1.11/SEG33	GPIO Port 1 Bit 11; LCD Segment 33	LCD GPIO
93	P1.10/SEG32	GPIO Port 1 Bit 10; LCD Segment 32	LCD GPIO
94	P1.9/SEG31	GPIO Port 1 Bit 9; LCD Segment 31	LCD GPIO

Pin Description (Sorted by Pin Number) (continued)

PIN	NAME	FUNCTION	PRIORITY
95	P1.8/SEG30	GPIO Port 1 Bit 8; LCD Segment 30	LCD GPIO
96	P1.7/SEG29	GPIO Port 1 Bit 7; LCD Segment 29	LCD GPIO
97	P1.6/SEG28	GPIO Port 1 Bit 6; LCD Segment 28	LCD GPIO
98	P1.5/SEG27	GPIO Port 1 Bit 5; LCD Segment 27	LCD GPIO
99	P1.4/SEG26	GPIO Port 1 Bit 4; LCD Segment 26	LCD GPIO
100	GNDD	Digital Ground	—

Pin Description (Sorted by Function)

FUNCTION	PIN	DESCRIPTION
POWER		
V_{3P3SYS}	65	3.3V Power Input for Digital Circuits
V_{3P3A}	67	3.3V Power Input for Analog Circuits
V_{BAT}	73	Power Input for Primary Backup Battery. This battery supplies all digital circuits in brownout mode and LCD only mode.
V_{BAT_RTC}	74	Power Input for RTC Backup Battery. This battery supplies the RTC block and the calibration block (temperature sensor and associated circuitry) even when primary V_{BAT} and V_{3P3SYS} supplies are unavailable.
V_{3P3D}	51	Provides a Bypass Point to the Internal 3.3V Bus
V_{DD}	26	Provides a Bypass Point to the Internal Regulated (1.8V) Core Supply Bus
V_{3P3RTC}	77	Provides a Bypass Point to the Real-Time clock Power Bus
V_{DD_CAL}	79	Provides a Bypass Point to the RTC Calibration Power Bus
GNDA	66, 71	Analog Ground. Should be at the same potential as digital ground. Typically, analog and digital grounds connect together at a single point.
GNDD	50, 100	Digital Ground
GNDR	60	Remote Ground. This is the ground return for the remote sensor interfaces and is provided separately due to high currents that can flow in this circuit.
CLOCK		
XOUT	75	Crystal Amplifier Output Pin. Connect to a 32,768Hz tuning-fork crystal.
XIN	76	Crystal Amplifier Input Pin. Connect to a 32,768Hz tuning-fork crystal.
ANALOG		
IAP	61	Main Current Channel Noninverting Analog Input
IAN	62	Main Current Channel Inverting Analog Input
IBP	63	Neutral Current Channel Noninverting Analog Input
IBN	64	Neutral Current Channel Inverting Analog Input

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
V_A	72	Primary Voltage Channel Analog Input (Single-Ended)
V_B	70	Secondary Voltage Channel Analog Input (Single-Ended)
V_C	69	Additional Voltage Input to Metrology Channel (Single-Ended)
V_D	68	Additional Voltage Input to Metrology Channel (Single-Ended)
RMT0P	61	Main Current Channel Remote Input, Positive Pole
RMT0N	62	Main Current Channel Remote Input, Negative Pole
RMT1P	63	Neutral Current Channel Remote Input, Positive Pole
RMT1N	64	Neutral Current Channel Remote Input, Negative Pole
ADC0	59	Auxiliary ADC Input Channel 0
ADC1	58	Auxiliary ADC Input Channel 1
ADC2	57	Auxiliary ADC Input Channel 2
ADC3	56	Auxiliary ADC Input Channel 3
SYSTEM		
JTAG TDO	43	JTAG Test Data Out
JTAG TCK	44	JTAG Test Clock
JTAG TMS	45	JTAG Test Mode Select
JTAG TDI	46	JTAG Test Data In
JTAG_E	47	JTAG Port Enable. External circuitry must pull this pin high at power-up to enable the JTAG port. When not using the JTAG port (as when the product is deployed), JTAG_E should be pulled low so the JTAG pins can be used for other purposes.
RSTN	78	Reset. This active-low signal resets the CPU core forcing restart to the utility ROM. If JTAG_E is not active (JTAG_E is low), most MAXQ peripherals and registers are reset to their default value. This pin must be pulled up under all operating conditions.
TMUX0	91	Test Multiplexer 0 Output. The test multiplexer can be configured to present several internal signals to the TMUX0 pin.
TMUX1	90	Test Multiplexer 1 Output. The test multiplexer can be configured to present several internal signals to the TMUX1 pin.
GPIO		
P0.0	38	General-Purpose I/O Port 0 Bit 0. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.1	37	General-Purpose I/O Port 0 Bit 1. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.2	36	General-Purpose I/O Port 0 Bit 2. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.3	35	General-Purpose I/O Port 0 Bit 3. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.4	34	General-Purpose I/O Port 0 Bit 4. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
P0.5	33	General-Purpose I/O Port 0 Bit 5. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.6	32	General-Purpose I/O Port 0 Bit 6. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.7	31	General-Purpose I/O Port 0 Bit 7. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.8	30	General-Purpose I/O Port 0 Bit 8. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.9	29	General-Purpose I/O Port 0 Bit 9. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.10	28	General-Purpose I/O Port 0 Bit 10. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.11	27	General-Purpose I/O Port 0 Bit 11. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.12	25	General-Purpose I/O Port 0 Bit 12. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.13	24	General-Purpose I/O Port 0 Bit 13. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.14	23	General-Purpose I/O Port 0 Bit 14. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.15	22	General-Purpose I/O Port 0 Bit 15. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.16	21	General-Purpose I/O Port 0 Bit 16. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.17	19	General-Purpose I/O Port 0 Bit 17. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.18	18	General-Purpose I/O Port 0 Bit 18. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.19	17	General-Purpose I/O Port 0 Bit 19. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.20	16	General-Purpose I/O Port 0 Bit 20. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.21	15	General-Purpose I/O Port 0 Bit 21. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.22	14	General-Purpose I/O Port 0 Bit 22. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.23	13	General-Purpose I/O Port 0 Bit 23. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.24	12	General-Purpose I/O Port 0 Bit 24. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.25	11	General-Purpose I/O Port 0 Bit 25. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
P0.26	10	General-Purpose I/O Port 0 Bit 26. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.27	9	General-Purpose I/O Port 0 Bit 27. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.28	8	General-Purpose I/O Port 0 Bit 28. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.29	7	General-Purpose I/O Port 0 Bit 29. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.30	6	General-Purpose I/O Port 0 Bit 30. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P0.31	5	General-Purpose I/O Port 0 Bit 31. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.0	4	General-Purpose I/O Port 1 Bit 0. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.1	3	General-Purpose I/O Port 1 Bit 1. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.2	2	General-Purpose I/O Port 1 Bit 2. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.3	1	General-Purpose I/O Port 1 Bit 3. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.4	99	General-Purpose I/O Port 1 Bit 4. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.5	98	General-Purpose I/O Port 1 Bit 5. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.6	97	General-Purpose I/O Port 1 Bit 6. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.7	96	General-Purpose I/O Port 1 Bit 7. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.8	95	General-Purpose I/O Port 1 Bit 8. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.9	94	General-Purpose I/O Port 1 Bit 9. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.10	93	General-Purpose I/O Port 1 Bit 10. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.11	92	General-Purpose I/O Port 1 Bit 11. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.12	83	General-Purpose I/O Port 1 Bit 12. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.13	82	General-Purpose I/O Port 1 Bit 13. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.14	81	General-Purpose I/O Port 1 Bit 14. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
P1.15	80	General-Purpose I/O Port 1 Bit 15. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.16	59	General-Purpose I/O Port 1 Bit 16. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.17	58	General-Purpose I/O Port 1 Bit 17. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.18	57	General-Purpose I/O Port 1 Bit 18. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.19	56	General-Purpose I/O Port 1 Bit 19. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.20	55	General-Purpose I/O Port 1 Bit 20. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.21	54	General-Purpose I/O Port 1 Bit 21. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.22	49	General-Purpose I/O Port 1 Bit 22. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.23	48	General-Purpose I/O Port 1 Bit 23. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.24	46	General-Purpose I/O Port 1 Bit 24. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.25	45	General-Purpose I/O Port 1 Bit 25. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.26	44	General-Purpose I/O Port 1 Bit 26. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.27	43	General-Purpose I/O Port 1 Bit 27. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.28	42	General-Purpose I/O Port 1 Bit 28. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.29	41	General-Purpose I/O Port 1 Bit 29. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.30	40	General-Purpose I/O Port 1 Bit 30. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
P1.31	39	General-Purpose I/O Port 1 Bit 31. This pin can be configured as input, totem-pole output, or open-drain output with or without a weak pullup.
LCD		
COM0	38	LCD Backplane Output 0
COM1	37	LCD Backplane Output 1
COM2	36	LCD Backplane Output 2
COM3	35	LCD Backplane Output 3
COM4	34	LCD Backplane Output 4
COM5	33	LCD Backplane Output 5

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
COM6	32	LCD Backplane Output 6
COM7	31	LCD Backplane Output 7
SEG0	38	LCD Segment Output 0
SEG1	37	LCD Segment Output 1
SEG2	36	LCD Segment Output 2
SEG3	35	LCD Segment Output 3
SEG4	34	LCD Segment Output 4
SEG5	33	LCD Segment Output 5
SEG6	32	LCD Segment Output 6
SEG7	31	LCD Segment Output 7
SEG8	30	LCD Segment Output 8
SEG9	29	LCD Segment Output 9
SEG10	28	LCD Segment Output 0
SEG11	27	LCD Segment Output 11
SEG12	25	LCD Segment Output 12
SEG13	24	LCD Segment Output 13
SEG14	23	LCD Segment Output 14
SEG15	22	LCD Segment Output 15
SEG16	21	LCD Segment Output 16
SEG17	19	LCD Segment Output 17
SEG18	18	LCD Segment Output 18
SEG19	17	LCD Segment Output 19
SEG20	16	LCD Segment Output 20
SEG21	15	LCD Segment Output 21
SEG22	14	LCD Segment Output 22
SEG23	13	LCD Segment Output 23
SEG24	4	LCD Segment Output 24
SEG25	3	LCD Segment Output 25
SEG26	99	LCD Segment Output 26
SEG27	98	LCD Segment Output 27
SEG28	97	LCD Segment Output 28
SEG29	96	LCD Segment Output 29
SEG30	95	LCD Segment Output 30
SEG31	94	LCD Segment Output 31
SEG32	93	LCD Segment Output 32
SEG33	92	LCD Segment Output 33

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
SEG34	91	LCD Segment Output 34
SEG35	90	LCD Segment Output 35
SEG36	89	LCD Segment Output 36
SEG37	88	LCD Segment Output 37
SEG38	87	LCD Segment Output 38
SEG39	86	LCD Segment Output 39
SEG40	85	LCD Segment Output 40
SEG41	84	LCD Segment Output 41
SEG42	40	LCD Segment Output 42
SEG43	39	LCD Segment Output 43
V_{LCD}	20	LCD Contrast DAC Output. User should connect a 0.1µF bypass capacitor to this pin.
V_{LCD5}	52	Input for Boosted LCD Voltage. Provides an alternate input for the LCD contrast DAC.
V_{SQW}	53	Square Wave to Drive a Charge Pump to Generate Boosted LCD Voltage. Can be disabled by software.
EXTERNAL INTERRUPTS		
INT0	2	External Interrupt 0 Input. External interrupts can be individually enabled or masked.
INT1	1	External Interrupt 1 Input. External interrupts can be individually enabled or masked.
INT2	83	External Interrupt 2 Input. External interrupts can be individually enabled or masked.
INT3	82	External Interrupt 3 Input. External interrupts can be individually enabled or masked.
INT4	81	External Interrupt 4 Input. External interrupts can be individually enabled or masked.
INT5	80	External Interrupt 5 Input. External interrupts can be individually enabled or masked.
INT6	55	External Interrupt 6 Input. External interrupts can be individually enabled or masked.
INT7	54	External Interrupt 7 Input. External interrupts can be individually enabled or masked.
WAKE		
WAKE0	4	External CPU Wake Input 0. An edge on this input can be configured to wake the CPU from sleep mode.
WAKE1	2	External CPU Wake Input 1. A level on this input can be configured to wake the CPU from sleep mode.
WAKE2	1	External CPU wake input 2. A level on this input can be configured to wake the CPU from sleep mode.
WAKE3	57	External CPU Wake Input 3. An edge on this input can be configured to wake the CPU from sleep mode.
WAKE4	42	External CPU Wake Input 4. An edge on this input can be configured to wake the CPU from sleep mode.
WAKE5	40	External CPU Wake Input 5. An edge on this input can be configured to wake the CPU from sleep mode.
WAKE6	55	External CPU Wake Input 6. A level on this input can be configured to wake the CPU from sleep mode.
WAKE7	54	External CPU Wake Input 7. A level on this input can be configured to wake the CPU from sleep mode.

Pin Description (Sorted by Function) (continued)

FUNCTION	PIN	DESCRIPTION
UART		
TX0	56	UART 0 Transmit Data
RX0	57	UART 0 Receive Data
TX1	41	UART 1 Transmit Data
RX1	42	UART 1 Receive Data
TX2	39	UART 2 Transmit Data
RX2	40	UART 2 Receive Data
TX3	3	UART 3 Transmit Data
RX3	4	UART 3 Receive Data
SMART CARD		
7816_IO0	5	ISO UART 0 Input/Output
7816_CLK0	6	ISO UART 0 Clock
7816_IO1	7	ISO UART 1 Input/Output
7816_CLK1	8	ISO UART 1 Clock
I^2C		
I2C_SDA	9	I^2C Port Serial Data
I2C_SCL	10	I^2C Port Serial Clock
TIMER		
T0	12	Timer B Channel 0 PWM Output
T1	11	Timer B Channel 1 PWM Output
SPI		
SPI_MISO	21	SPI Port Master In, Slave Out
SPI_MOSI	22	SPI Port Master Out, Slave In
SPI_SCLK	23	SPI Port Serial Clock
SPI_SSEL	24	SPI Port Slave Select
PULSE		
WPULSE	49	Pulse Output, Real Energy
VPULSE	48	Pulse Output, Reactive Energy
XPULSE	83	Pulse Output, Auxiliary Pulse X
YPULSE	82	Pulse Output, Auxiliary Pulse Y
TOUCH SWITCH		
TOUCH0	55	Touch Switch Channel 0 Sensor Input
TOUCH1	54	Touch Switch Channel 1 Sensor Input
OPTICAL INTERFACE		
OPT_RX	57	Optical Demodulator Receiver Input
OPT_TX	56	Optical Modulator Transmitter Output

Detailed Description

Hardware Overview

The MAX71314/MAX71315 single-phase electricity meter SOCs incorporate a 32-bit MAXQ30 microcontroller core, delivering approximately one MIPS/MHz of clock (nominally, 9.83MHz); a 32-bit dedicated metrology compute engine; interfaces for remote sensors, and a complete set of peripherals onto a single device. The devices are available in a 100-pin LQFP package.

The devices offer a display controller that supports 8-way multiplexing of LCD segments. Up to 36 available segment pins provide up to 288 controllable display segments in the 8-way multiplexing configuration. Measurement results can be displayed on an LCD, either 3.3V glass commonly used in low-temperature environments, or 5V glass used in more demanding environments using an external 5V power supply. An oscillator pin allows the use of an external charge pump to create the 5V LCD voltage. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs.

The devices integrate four high-precision 24-bit delta-sigma ADCs for measuring two current channels (differential inputs) and two voltage channels (single-ended inputs). A fixed-point compute engine (CE) processes the ADC samples. The code for the CE resides in RAM and is shared with the MAXQ30 CPU core.

One of the four converters (ADC3) can also be configured to accept up to three multiplexed inputs of interest, enabling the application to monitor wide dynamic range environmental signals. These environmental signals can include a magnetic field generated by a strong permanent magnet, or a varying AC field induced by nearby power lines.

The devices also contain two remote interfaces capable of supporting up to four metrology channels. Typically, these channels are assigned to measure the primary parameters of interest, such as line voltage, line current, and neutral current, plus any other analog signal of interest. The remote channels are self-contained and provide inherent isolation to protect the devices from line potentials. In the current channels, you can select any sensor including current transformers, shunts, or Rogowski coils.

The devices include a separate ADC subsystem (the auxiliary ADC) to monitor slow-moving environmental conditions. This ADC samples at a 5kHz rate and can be multiplexed between any of four pins.

The devices are clocked by one 32,768Hz tuning-fork-type crystal that is used as a reference for the RTC. A phase-locked loop multiplies this clock to provide the 9.83MHz required by the core, the 19.66MHz required by the CE, and other clocks required by the system.

In a typical application, the CE of the devices processes the samples from its metrology input channels and performs calculations to measure real energy and reactive energy, as well as volt-ampere hours, A2h, and V2h for four-quadrant metering. These measurements are then accessed by the MAXQ30 CPU core, processed further, and output using the peripheral devices available to the MPU.

The devices feature a real-time clock to record time-of-use (TOU) metering information for multirate applications, and to time-stamp tamper or other events.

The devices include a precision voltage reference. A temperature-correction mechanism guarantees conformance to accuracy standards over temperature. Temperature-dependent external components such as crystal oscillator, current transformers and their corresponding signal-conditioning circuits, can be characterized, with their correction factors programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

The devices have two pins that are configurable as touch-detect inputs. When configured for touch detect, the pins self-oscillate at a frequency dependent on the capacitive load on the pins. A low-power timer circuit measures the oscillation frequency and alerts the CPU when the frequency falls below a certain threshold (indicating an increase in the capacitive loading). If desired, these inputs can wake the processor.

The devices have four UART channels with independent baud-rate generators. These UART channels can connect to driver/receiver chips for RS-232 or, with an additional GPIO pin for transmit enable, for RS-422/RS-485. One of the four UART channels can be dedicated for infrared I/O. In this configuration, transmitted data combines with a carrier signal so that the modulated carrier can be applied to an IR transmitter; the received modulated carrier is applied to a filter to extract the modulation waveform before being applied to the UART input.

The devices include two ports for smart cards for pre-pay metering applications. In many applications, the pins can connect directly to the smart card sockets. It is also possible to use external transceivers to achieve full ISO 7816 compliance.

The devices include standard peripherals for interfacing serial memory devices and complex display subsystems, among other devices. These devices include one SPI port and one Inter-IC Communication (I^2C) port.

Analog Front-End

The devices contain four delta-sigma ADC channels, three of which monitor line voltage, line current, and neutral current. The fourth channel is configurable as an additional voltage input, a magnetic tamper monitor, or a temperature-measurement channel. Two ADCs contain preamplifiers that provide a gain of 1, 4, 8, or 16, as required.

Analog inputs sample at up to 5MHz. The samples decimate in a FIR filter with an oversampling ratio of up to 512. Finished samples are available to the DSP section at up to 10.92ksps per channel.

Inputs to the ADC channels must be referenced to AGND and must be scaled so that the signal is no greater than 250mV above or below AGND. For example, a system that is expected to monitor up to 300V RMS would need to scale that voltage to no more than 250mV peak, and would require a voltage-divider with a divide ratio of no less than:

$$\frac{300V \times \sqrt{2}}{0.25V} = 1{,}697$$

For the current channels, the maximum differential amplitude permitted on the input pins scales with the pre-amplifier gain value:

$$V_{PEAK} = \frac{0.250V}{GAIN}$$

For example, in a design using a 120µΩ shunt targeting a 100A RMS load, one might consider using a gain of 8 because the maximum RMS current in this arrangement is:

$$\frac{\frac{0.250V / 8}{\sqrt{2}}}{120x10^{-6}} \cong \frac{22x10^{-3}V}{120x10^{-6}} \cong 184A$$

Remote Interfaces

The two current input channels are configurable for remote interfaces.

The devices support both 71M6000 series single-channel remote interfaces and MAX7107x 2-channel remote interfaces. In a typical configuration, one might use a MAX7107x isolated interface to connect to a line voltage sensor and a line current sensor, and a 71M6000 type isolated interface to connect to a neutral current sensor. In this configuration, all interfaces have galvanic isolation from line potentials.

The remote interfaces provide power to the remotes by sending current pulses across an isolation transformer. The data output from the isolated remotes is decimated by the FIR filter and stored in RAM where it can be accessed and processed by the CE.

Compute Engine (CE)

The two current input channels are configurable for remote interfaces.

The devices support both 71M6000 series single-channel remote interfaces and MAX7107x 2-channel remote interfaces. In a typical configuration, one might use a MAX7107x isolated interface to connect to a line voltage sensor and a line current sensor, and a 71M6000 type isolated interface to connect to a neutral current sensor. In this configuration, all interfaces have galvanic isolation from line potentials.

The remote interfaces provide power to the remotes by sending current pulses across an isolation transformer. The data output from the isolated remotes is decimated by the FIR filter and stored in RAM where it can be accessed and processed by the CE.

Meter Equations

The CE can implement, among others, the equations listed in Table 2. The devices' standard CE codes implement equation 0. For other configurations, contact the factory.

Pulse Generators

The devices' pulse generator hardware supports the primary pulses (VPULSE and WPULSE) and the secondary pulse outputs (XPULSE and YPULSE).

During each CE code pass, the hardware stores exported sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate all the pulse generator outputs at the beginning of its code pass and to rely on hardware to spread them evenly over the sample frame. The FIFO resets at the beginning of each sample frame.

Table 2. Meter Equations

EQU	DESCRIPTION	Wh AND VARh FORMULA	
		ELEMENT 0	ELEMENT 1
0	1-element, 2-W, 1ϕ with neutral current sense	VA · IA	VA · IB
1	1-element, 3-W, 1ϕ	VA(IA-IB)/2	N/A
2	2-element, 3-W, 1ϕ	VA · IA	VB · IB

The pulse generator outputs are available as alternate functions on P1.12, P1.13, P1.22, and P1.23.

The devices provide four pulse generators (VPULSE, WPULSE, XPULSE, and YPULSE), as well as hardware support for the VPULSE and WPULSE pulse generators. The XPULSE and YPULSE generators are used by standard CE code to output CE status indicators, such as sag detection, to the GPIO pins. All pulses are configurable to generate interrupts to the MPU.

The polarity of the pulses can be inverted with PLS_INV. When this bit is set, the pulses are active high, rather than the more usual active low. PLS_INV inverts all the pulse outputs.

XPULSE and YPULSE

Pulses generated by the CE can be exported to the XPULSE and YPULSE pulse outputs. Generally, the XPULSE and YPULSE outputs are updated once on each pass of the CE code.

Standard CE code permits the signaling of a sag event for the YPULSE output. The XPULSE output indicates zero crossings of the main voltage, which can be used to synchronize PLC modems or other equipment.

VPULSE and WPULSE

During each CE code pass, the hardware stores exported WPULSE AND VPULSE sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate the VPULSE and WPULSE outputs at the beginning of its code pass and to rely on hardware to spread them over the sample frame. The FIFO resets at the beginning of each sample frame.

The clock provided to the VPULSE and WPULSE generators is 9.82MHz. Thus, the minimum resolution for the generator is 101.8ns.

MAXQ Core

The devices use a MAXQ30 32-bit CPU core as the administrative processor.

The MAXQ30 core is a 32-bit RISC core. It is unique because all instructions can be coded as a simple MOVE instruction, yielding high efficiency in both time and power.

The MAXQ core has the following characteristics:

- Instructions typically execute in a single cycle
- All peripherals are first-class data objects
- Flexible data pointers make block data moves simple
- Dedicated 32 x 32 single-cycle multiplier

You can find information on the MAXQ architecture and its benefits at **www.maximintegrated.com/app-notes/index.mvp/id/4811**.

Register Complement

The MAXQ30 core supports 512 32-bit registers. Not all these register addresses are used in any particular core implementation. Registers are divided into two blocks: system registers (called special-purpose registers, consisting of accumulators, memory pointers, and other core registers) and peripheral registers (called special-function registers).

The 512 registers are divided into blocks of register modules. A register module is a group of up to 32 related registers. The MAXQ30 architecture supports up to 16 register modules. Register modules 0–5 are dedicated to special-function registers (peripherals), while registers 7–15 are dedicated to special-purpose registers (system registers).

Memory Organization and Addressing

The MAXQ core is a Harvard machine. As such, it has separate code and data memory spaces. In the MAXQ30 core, each memory space is 32MB in length. When accessed as code, memory is organized as 16MB x 16 bits; when accessed as data, the memory space can appear as 32MB x 8, 16MB x 16, or 8MB x 32. See Figure 1.

I/O is typically performed using registers. The MAXQ architecture supports up to 512 registers in 16 register modules. Each register can be up to 32 bits in length. Registers are first-class data objects, so peripheral objects can take part in ALU transactions, be tested for values, or any other operation that a CPU register can do in other architectures. See Table 3.

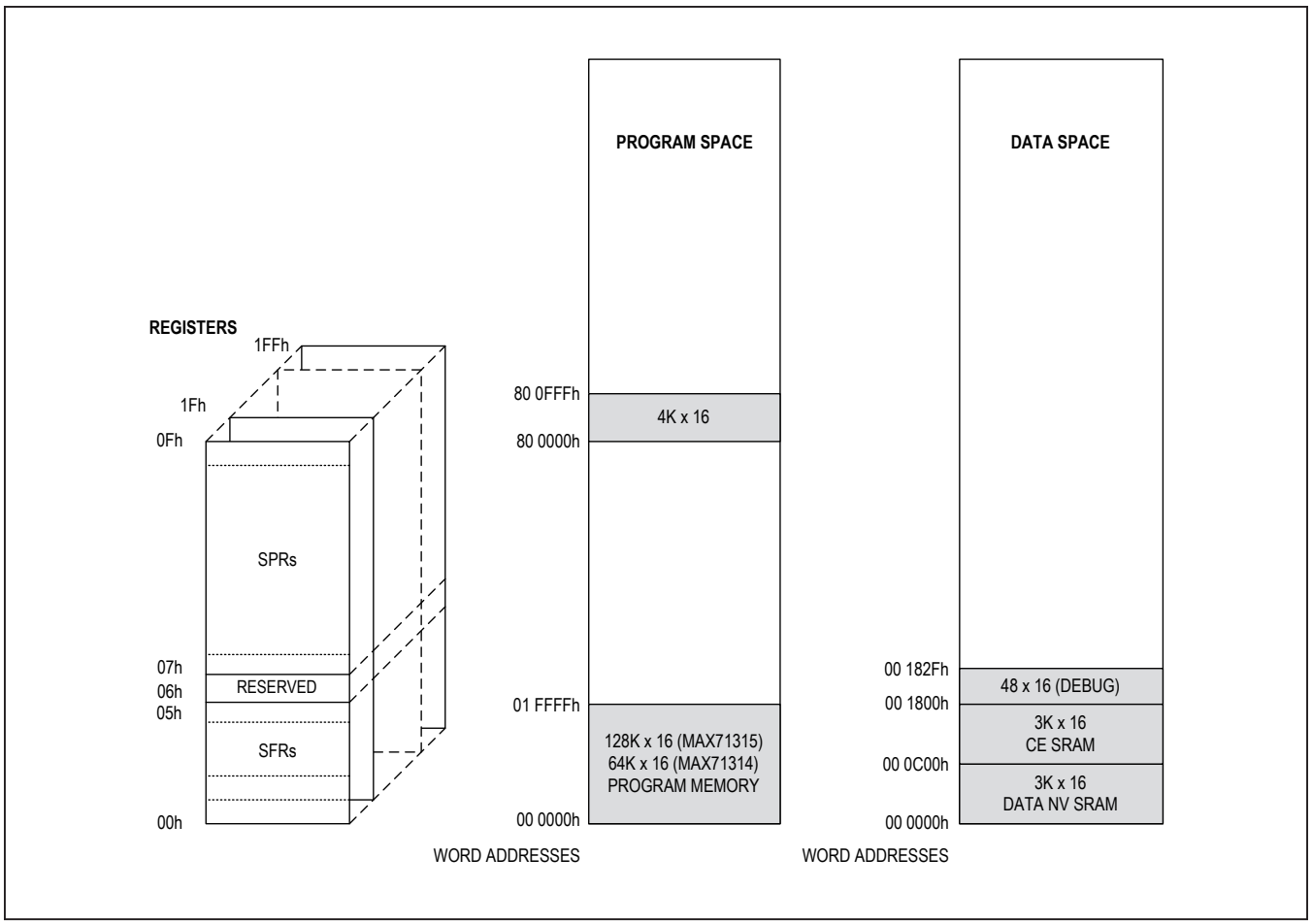


Figure 1. MAX71314/MAX71315 Memory Map

Table 3. Memory Map

MPU ADDRESS	NAME	DESCRIPTION
CODE SPACE (WORD ADDRESSES)		
0x00 0000	FLASH	128K x 16 (MAX71315) or 64K x 16 (MAX71314) flash program memory
0x80 0000	UROM	4K x 16 utility ROM
DATA SPACE (WORD ADDRESSES)		
0x00 0000	DRAM	3K x 16 static, nonvolatile RAM for MCU data
0x00 0C00	CERAM	3K x 16 shared memory for CE data
0x00 1800	DBRAM	48 x16 MAXQ debug RAM

Flash Memory

The MAX71314 contains 128Kb and the MAX71315 contains 256kB of on-chip flash memory that serves as program store for the MAXQ30 core. The use of flash memory as program store allows the firmware to be easily updated. Because flash write and erase operations cannot be performed while code is executing from flash, code in the utility ROM mediates all flash write and erase operations.

Because the MAXQ30 core is a Harvard architecture processor, the core cannot access as data the memory block from which code is executing. This means that user code executing in flash space cannot directly access data stored in flash memory. However, facilities provided in the utility ROM allow access to data stored in flash memory.

When the flow of execution is transferred from one memory block to another (e.g., when a call is made from a program running in flash space to a function in the utility ROM), the MAXQ30 core automatically remaps the data space. This means the memory block currently used as code space does not appear as data space, permitting the memory space previously used as code space to be remapped as data space. In this way, user code can access constant data stored in flash as data.

The sequence for accessing data stored in flash memory is as follows:

- Place the address of the data to be read in a data pointer register
- Call a routine in the utility ROM to read the memory from flash (utility ROM can do this since utility ROM and flash are separate memory blocks)
- The utility ROM routine reads the memory location the data pointer designates
- The routine returns. The flash data is available in the accumulator.

Additionally, a program running in flash space can write a code sequence to data RAM, branch to the routine in data RAM, and that code can access flash since RAM and flash are separate memory blocks. See Table 4.

Utility ROM

The devices contain an 8kB ROM organized as 4k x 16, which provides boot services and utility functions to the application program running in flash. This block of memory resides at 0x80 0000 in code space. The utility ROM manages the following functions:

- **Boot:** Execution begins from reset at the base of the utility ROM. Under normal circumstances, a jump is executed to the base of flash memory, but under special circumstances, some other code block can take the execution thread (e.g., boot loader, debug, etc.).
- **Debug:** The utility ROM contains routines that assist the built-in hardware debugger to communicate with ICE software on a PC.
- **Bootloader:** The bootloader provides in-system programming facilities. Integrated debug-environment software with the appropriate drivers can invoke the bootloader directly to write code blocks to the flash memory.
- **Utility Functions:** Functions such as flash programming and block moves are provided in the utility ROM to assist user software.
- **Test:** Functions used to perform unit test of the devices are included in the utility ROM.

RAM

The devices contain a total of 12kB of RAM (not including the 96 bytes of RAM dedicated for the debug function). Of this total, 6kB is dedicated to the MAXQ core for its internal operation. This RAM block is configured as nonvolatile memory and is maintained in the absence of primary power by the V_{BAT} power supply (or V_{BAT_RTC}, should the primary V_{BAT} supply fail). The other 6kB block is dedicated for CE code and data RAM and is accessible at will by the CE and accessible at will by the MAXQ30 core through interleaved access; it is not backed by the V_{BAT}.

Internal data memory starts at address 0x00 0000 in data space and is contiguous through 0x00 17FF (byte addresses). Implemented as static RAM, all accesses to internal memory require only one clock cycle.

Table 4. Memory Mapping

WHEN RUNNING IN	AT ADDRESSES	FLASH APPEARS AS DATA AT	RAM APPEARS AS DATA AT	UTILITY ROM APPEARS AS DATA AT
Flash	0x00 0000 to 0x01 FFFF	—	0x00 0000	0x80 0000
Data RAM	0xA0 0000 to 0xA0 17FF	0x00 0000	—	0x80 0000
Utility ROM	0x80 0000 to 0x80 0FFF	0x80 0000	0x00 0000	—

Interrupts and Exceptions

The MAXQ processor supports multiple interrupts that transfer control to fixed vectors. Note that the interrupts have a natural priority order given by their location in memory (e.g., the PF interrupt is the highest priority interrupt in the natural priority order because it is the interrupt vector with the lowest address). Change priorities by modifying the interrupt priority register. See Table 5.

Debug

The MAXQ core has an integrated debugger that allows real-time debugging of the code running on the MAXQ core. The debugger contains a hardware component that connects to the JTAG port, and a software component that is contained in the utility ROM. The debugger supports multiple breakpoints, register inspection and modification, RAM dump and modify, and other functions.

Table 5. Exception Vector Table

MPU ADDRESS	NAME	DESCRIPTION
0x00 0000	MAIN	This is the main entry point. The utility ROM executes a jump to this address after performing device initialization and checking for loader mode or debug mode.
0x00 0008	PF	Power-Fail Warning. Activated when V_{3P3A} falls below the power-fail threshold.
0x00 0010	EI	External Interrupt. Activated when any enabled external interrupt pin becomes active. Software in the interrupt service routine must poll the available interrupt sources to determine which of the external interrupt sources caused the interrupt.
0x00 0018	CE	Compute Engine. Activated to alert the MAXQ30 core when the CE has completed an accumulation cycle.
0x00 0020	I2C	I^2C. Activated when the I^2C peripheral detects an event (e.g., START completed, STOP completed, transmit buffer empty, receive character available, or timeout fault).
0x00 0028	SPI	SPI. Activated when the SPI peripheral has clocked in/out one character.
0x00 0030	UART	UART. Activated when the UART has an exception condition (e.g., receive character available, transmit buffer empty, parity fault, or framing error).
0x00 0038	ISO0	ISO UART 0. Activated whenever an exception condition is detected on the smart card channel 0.
0x00 0040	ISO1	ISO UART 1. Activated whenever an exception condition is detected on the smart card channel 1.
0x00 0048	WDT	Watchdog Timer. Activated when the watchdog timer is about to reset the device. This interrupt provides the MAXQ30 an opportunity either to reset the watchdog timer or to save status before the watchdog resets the core.
0x00 0050	TB	Timer B. Activated when an interrupt condition occurs on any timer channel. Interrupts can be an expiration of the timer or can indicate that a measurement is complete in pulse-width measurement mode.
0x00 0058	TRIM	Trim Check
0x00 0060	RTC	Real-Time Clock. Activated when any interrupt source in the RTC block is activated, including alarm, voltage status, or temperature range.
0x00 0068	DEMOD	38kHz Demodulator Interrupt. If enabled, this interrupt becomes active when the 38kHz modulator is enabled and the demodulator senses a 38kHz signal in its passband.
0x00 0070	TOUCH	Touch Switch Interrupt. If enabled, this interrupt becomes active when either of the touch switch inputs is activated.
0x00 0078	—	Reserved
0x00 0080	—	Reserved
0x00 0088	TRAP	General Interrupt Trap. Activated whenever an interrupt not covered by any other condition occurs.

Power

The devices require a single 3.3V supply for operation. Optionally, up to two battery supplies can be attached to the MAXQ71315, as well as a first battery of sufficient capacity to provide operational power when primary power fails, and a second battery of lower capacity that maintains internal RAM and clock facilities in the event both primary power and the first battery fail. How these supplies interact and what blocks are powered at what times are covered in this section. See Figure 2.

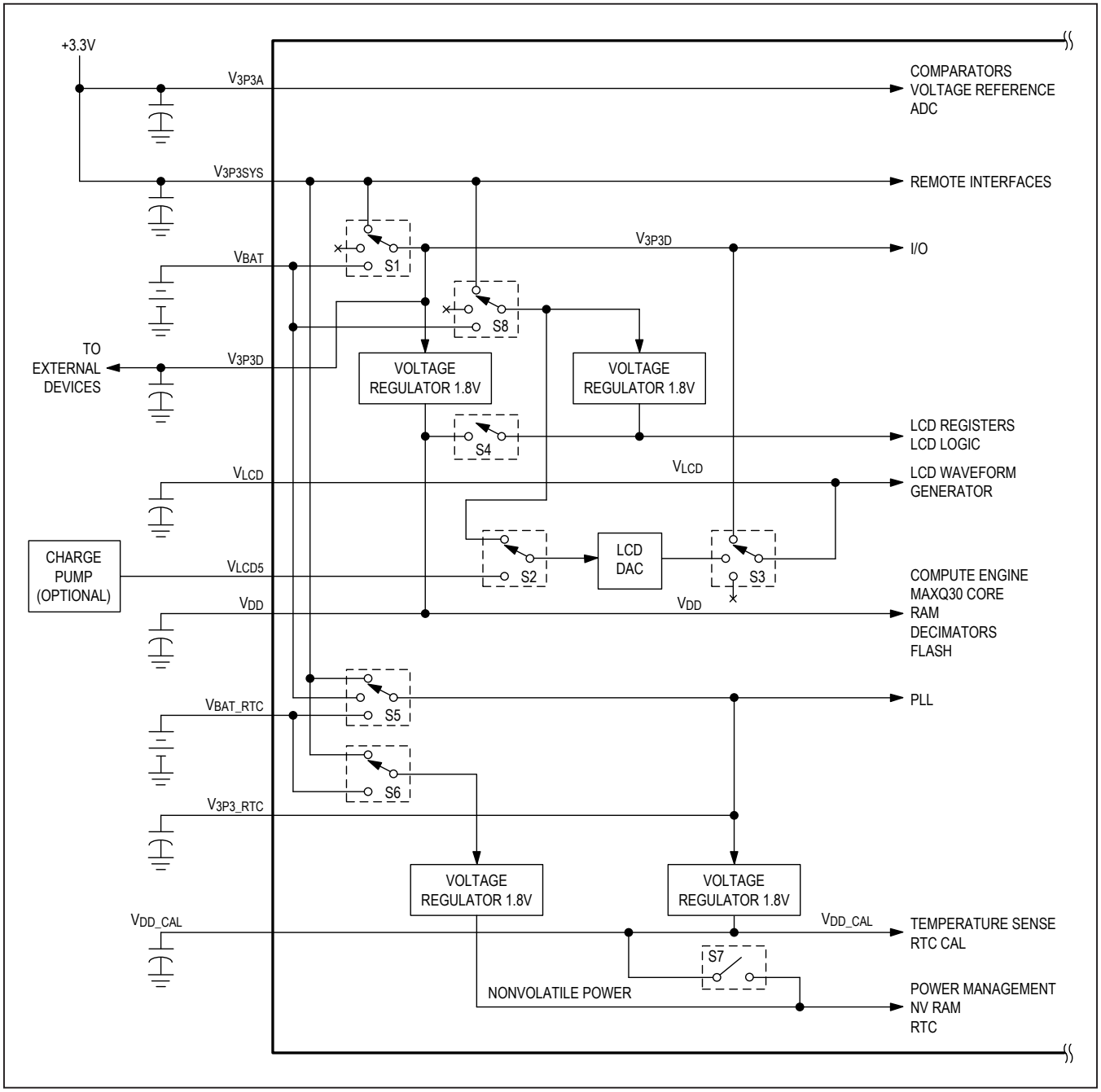


Figure 2. Internal Power Distribution

Operational Modes

The devices support four operational modes:

1) **Mission Mode:** The devices are in mission mode when the primary power supply is in specification. Primary power is supplied through the V_{3P3SYS} and V_{3P3A} pins. Comparators on the V_{3P3SYS} pin monitor the voltage level on this bus. If the level falls below a set threshold, the part automatically switches to brownout mode.
2) **Brownout Mode:** In brownout mode, V_{3P3SYS} has failed and main power for the I/O and other circuits automatically switches to the V_{BAT} input. Since there is no path for power to flow from V_{BAT} to the metrology blocks, these blocks are effectively turned off. The core continues to operate at full speed until firmware switches to another mode.
3) **LCD Only:** In LCD-only mode, the core is halted and the core voltage regulator is disabled, and the LCD operates independent of software control. The LCD can take its power from either V_{BAT}, the V_{LCD5} pin (from an external charge pump), or from an external V_{LCD} supply, depending on the LCD configuration.
4) **Sleep:** Sleep mode shuts down power to all logic blocks except the RTC and nonvolatile memory blocks.

There are 10 pins that are used to provide power or to provide a bypass point for internal power nodes:

1) **V_{3P3A}:** This is the primary analog power input for the device. It provides power to the ADC blocks, the voltage comparator blocks, and to the bandgap voltage reference and its output buffer. This block is not directly backed up by any on-chip battery.
2) **V_{3P3SYS}:** This is the primary digital power input for the device. It is typically connected to the same supply as V_{3P3A}, but separately bypassed.
3) **V_{BAT}:** The primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.
4) **V_{3P3D}:** The output from an internal switch that selects either V_{3P3SYS} (if the primary supply is above threshold) or V_{BAT} (if the primary supply is below threshold). It should always be bypassed, but can also be used to provide power to low-power external devices such as serial memory during brownout conditions.
5) **V_{LCD}:** Usually, this is a bypass point for the LCD supply. Frequently the supply is the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply, directly. This pin can also be used as an input to provide an external V_{LCD}.
6) **V_{LCD5}:** An input from a charge pump if operation with 5V-compatible LCD glass is desired. In one LCD mode, a square wave is available to drive a charge pump so that only an external RC circuit and two diodes are required to provide a 5V supply.
7) **V_{BAT_RTC}:** This pin provides the RTC and nonvolatile memory backup power. It is frequently connected to a lithium battery to maintain the RTC and NV memory elements.
8) **V_{3P3RTC}:** The bypass for the nonvolatile power bus.
9) **V_{DD_CAL}:** The bypass point for the internal calibration power bus.
10) **V_{DD}:** The bypass point for the internal regulated core power supply.

Internally, there are four voltage regulators and eight power switches that control the power distribution system. Some of the switches are controlled by software and the others are controlled by internal logic that senses the voltage on the external pins and makes automatic decisions about the appropriate configuration. Also internally, there are a set of power busses: four primary busses that provide power to various parts of the device logic, two busses dedicated to the LCD functions, and two dedicated to the ADC section and to the remote interfaces.

The switches perform the following functions:

- **S1:** Controlled by Hardware. This switch selects the source for I/O voltages and the V_{3P3D} circuit. S1 is controlled by internal logic that monitors V_{3P3SYS}. If V_{3P3SYS} falls below the threshold level, the system enters brownout mode and switches S1 to take power from V_{BAT}. The system is also alerted that it has entered brownout mode, and it is the responsibility of operating firmware to perform the operations necessary to enter LCD-only or sleep modes to reduce power consumption from the battery. In these last modes, the switch is placed in the neutral position, effectively powering down the I/O, V_{3P3D}, and core logic.
- **S2:** Controlled by Firmware. This switch selects LCD boost mode. Under normal circumstances, the switch connects the LCD DAC to the V_{3P3D} bus, providing the LCD with 3.3V power that can drive low-voltage (3V) LCD glass. Firmware can configure this switch to change the LCD system to boost mode, connecting the input of the LCD DAC to the V_{LCD5} pin. An external charge pump or other power supply can place up to 5V on this pin to allow the DAC to drive standard voltage (5V) glass.

- **S3:** Controlled by Firmware. This switch selects the source for the LCD supply voltage, V_{LCD}. Under normal circumstances, the switch selects the LCD DAC to drive V_{LCD}. However, firmware can force LCD power to be taken directly from the V_{3P3D} rail, or it can disable internal power entirely. In this last case, V_{LCD} is used as an input from an external voltage source. Again, the LCD DAC is bypassed; the external circuit is, in this case, responsible for controlling the LCD voltage and the contrast of the display.
- **S4:** Controlled by Firmware. Under normal operation, S4 is closed and the LCD operating power is provided by the primary regulator (V_{DD}). When firmware places the system in LCD-only mode, S4 is open and LCD power is taken from its dedicated regulator.
- **S5:** Controlled by Hardware. This switch selects the power source for the V_{DD_CAL} domain. If V_{3P3SYS} is good, it is selected as the nonvolatile domain source; otherwise, if V_{BAT} is good, it is selected as the nonvolatile domain source; otherwise, V_{BAT_RTC} is used. This provides power to the PLL and, after regulation, to the temperature sensor and to the RTC calibration logic.
- **S6:** Controlled by Hardware. This switch selects either the V_{3P3SYS} or the V_{BAT_RTC} source to power the RTC, the NV RAM, and the power-management logic. S6 configures automatically based on the level of V_{3P3SYS}.
- **S7:** Controlled by Firmware. In all modes except sleep mode, this switch is closed, connecting the NV bus and the calibration power bus. When firmware places the device in sleep mode, S8 is open, isolating the calibration power bus and ensuring the lowest possible power.
- **S8:** Controlled by Hardware. When V_{3P3SYS} is available and the device is operating in LCD-only mode, this switch connects the LCD logic voltage regulator to the V_{3P3SYS} bus. When V_{3P3SYS} fails, the switch connects the voltage regulator to the V_{BAT} bus. When firmware places the device into sleep mode, this switch and the main power switch (S1) are in their neutral positions, with power removed from both primary power regulators.

Oscillators

The devices contain a crystal oscillator that uses a 32,768Hz tuning-fork crystal as its time base. An internal PLL multiplies the reference frequency to the various clocks required in the device.

Timers

The devices contain five timer channels. Each timer channel is configurable as a counter, a timer, or a PWM modulator. Additionally, the timers can perform count capture and compare functions. They can be used for timing, pulse generation, pulse-width modulation (PWM), pulse timing, or many other uses. Inside the timer logic, multiple sources can be selected to generate an interrupt to the MAXQ30 core.

The timers have the following features:

- CPU Interrupts: The timers can interrupt the CPU on overflow, or when the timer matches some preset value
- Pulse Measurement: The timers can be triggered by an external pulse
- Pulse-Width Modulation: The timers can be used to generate a PWM signal with selectable characteristics
- Counters: The timers can be configured to count the number of external pulse edges

When configured as timers, the clocks are derived from the system clock. A prescaler system allows the system clock to be scaled by up to 1,024 before being used as the timer clock.

UARTs

The devices contain four UART channels. All channels are directly controlled by the MAXQ30 core and feature independent baud-rate generators.

UART 3 is unique in that it contains an option to modulate its output with a high-frequency carrier (nominally 38kHz), and contains a photodiode amplifier and detector that allows the channel to sense high-frequency carrier and demodulate serial data contained on the carrier.

Each UART features:

- Four modes of operation, one synchronous and three asynchronous
- Dedicated baud-rate generators per UART
- Double-buffered transmitter and receiver
- Odd, even, or no parity
- 1, 1.5, or 2 stop bits
- Maskable interrupts for receive buffer full or transmit buffer empty

Optical UART

One of the four UART channels contains an optical interface module. When engaged, the transmit data from the UART is modulated with a carrier frequency (usually 38kHz, but configurable) and receive data is taken from an optical demodulator module.

The optical modulator is engaged by firmware. When engaged, the optical modulator takes the logical sum of the TSD bit and the modulation frequency. In this way, the modulation frequency is only passed to the TXD pin during the space time of the serial bit stream. The OFS bit selects whether the mark level is a logical 1 or a logical 0 to accommodate the requirements of external hardware.

On the receive side, a PIN photodiode amplifier and demodulator are inserted into the receive data path. See Figure 3.

The output of the photodiode amplifier is applied to a first-order delta-sigma modulator. From there, the modulator output is decimated and the finished samples are filtered, squared, and smoothed. The output of the smoothing filter is a representation of the level of in-band energy present in the optical signal. This signal is applied to a limiting amplifier with a small amount of hysteresis, and its output should be a close representation of the original modulating signal.

In the illustration shown in Figure 4, the modulated carrier is transmitted cleanly by the IRED, but by the time the photodiode receives the signal it has been mixed with noise and flicker due to ambient fluorescent lighting driven by electronic ballast mechanisms. The signal processing removes the noise and recovers a usable signal.

LCD Controller

The devices include an LCD controller that supports up to eight common planes and up to 44 segments. You can attach bare LCD glass natively operating up to 3.3V, or with an external boost circuit, up to 5V. The LCD controller supports many operating modes, including:

- Static, with up to 43 segments
- Two common planes with up to 42 segment circuits, for a total of 84 segments operating at 1/2 bias

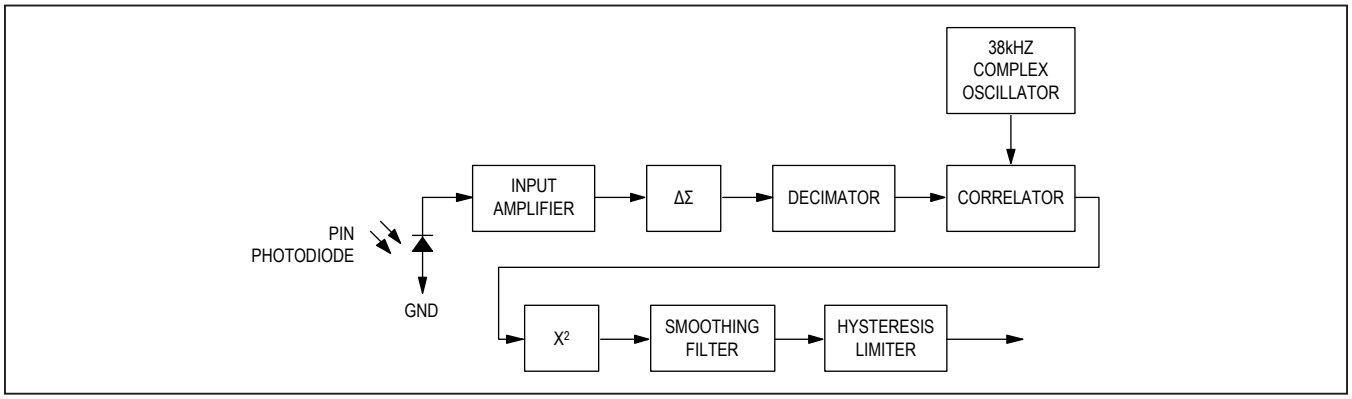


Figure 3. Optical Demodulation Block

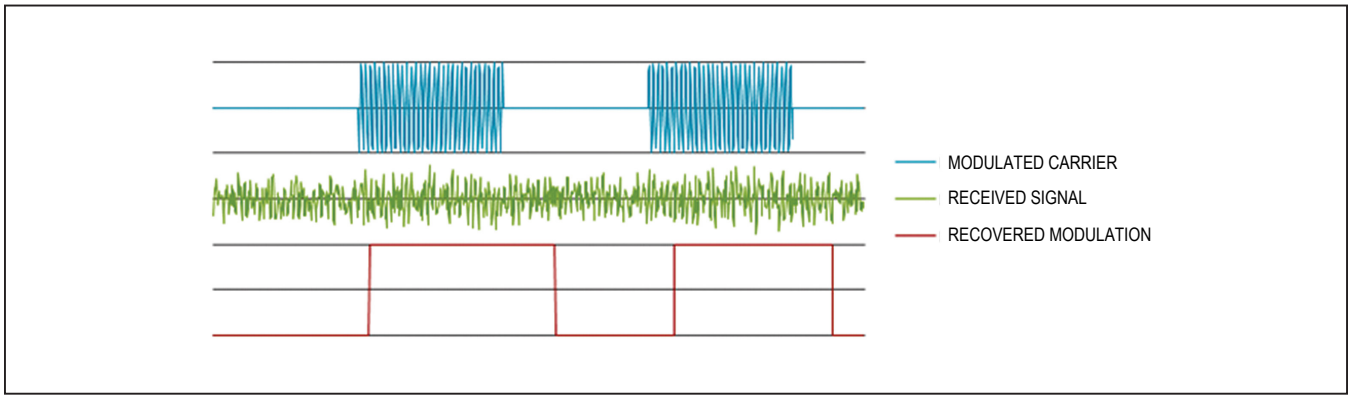


Figure 4. Optical Demodulator Performance

- Three common planes with up to 41 segment circuits, for a total of 123 segments operating at 1/2 or 1/3 bias
- Four common planes with up to 40 segment circuits, for a total of 160 segments operating at 1/3 bias
- Five common planes with up to 39 segment circuits, for a total of 195 segments operating at 1/3 bias
- Six common planes with up to 38 segment circuits, for a total of 228 segments operating at 1/3 bias
- Eight common planes with up to 36 segment circuits, for a total of 288 segments operating at 1/3 bias

Additionally, the LCD controller has test features that allow all segments to be turned on or off without disturbing LCD data, a reset feature that quickly clears all LCD data, and a built-in DAC for contrast adjustment.

V_{LCD}

Setting the LCD voltage (the V_{LCD} pin) is critical to successfully using the LCD controller. Among other characteristics, the V_{LCD} level controls the contrast of the display.

The LCD glass has a recommended operating voltage, frequently 3V or 5V. The specified operating voltage assumes a typical set of LCD waveforms. For example, a 3V LCD glass operating at 1/3 bias expects to see voltages at 0V, 1V, 2V, and 3V, with a total differential peak-to-peak voltage of 6V maximum (that is, backplane at 0V and segment at 3V, followed by backplane at 3V and segment at 0V).

In the devices, four V_{LCD} sources can be selected that make use of the internal resources of the device. The selection is made by writing the LCD_VMODE field in the LCDMODE register.

LCD Special Modes

The LCD controller is capable of much more than just displaying the contents of the LCD display registers. Special LCD modes include blinking up to 16 segments (two segment circuits on each of eight common circuits), alternating page configurations so that one page can be updated while the other is being displayed, and all segments on/all segments off for test purposes. A pin-mirroring scheme eases board routing when limited routing resources are available.

I²C Interface

The devices include an I²C peripheral that can act as an I²C master or slave.

The I²C bus is a bidirectional 2-wire serial bus interface, with the following characteristics:

- Information that is transferred over a serial-data circuit (SDA) and serial-clock circuit (SCL)
- Peripheral that can operate in either a master mode or a slave mode
- Peripheral that operates in three modes to support multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1Mbps
- Peripheral that contains an on-chip filter to reject spikes on the data circuit

Serial Peripheral Interface (SPI)

The SPI provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple-master or multiple-slave system. The interface provides access to a 4-wire, full-duplex serial bus, and can be operated either in master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is up to the system-reference clock frequency for master mode. For slave mode, the maximum frequency is a function on the I/O driver, character length, and system clock.

The main element in the SPI module is the block containing the shift register, transmit FIFO, and receive FIFO. The shift register is double-buffered and serves as temporary data storage. The receive FIFO holds received data from the network. The transmit FIFO contains data ready to be transmitted out.

The SPIB SFR provides access for both transmit and receive data. Reads are directed to the read FIFO. Writes are directed to the shift register automatically if the transmit FIFO is empty; otherwise, write operations store data into the transmit FIFO.

The four interface signals used by the SPI are MISO, MOSI, SCLK, and SSEL:

1) **MISO (Master In/Slave Out):** This signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most significant bit first. The slave device places the MISO pin in an input state with a weak pullup when not selected.
2) **MOSI (Master Out/Slave In):** This signal is an output from a master device and an input to the slave devices. It is used to serially transfer data from the master to the selected slave. Data is transferred most significant bit first.

3) **SCLK (SPI Clock):** This serial clock is an output from the master device and an input to the slave devices. It is used to synchronize the transfer of data between the master and the slave on the data bus.
4) **SSEL (Slave Select):** The slave select signal enables an SPI slave when activated by a master device. The slave is configurable to select the active state of SSEL. When the master asserts SSEL, it is signaling the beginning of an SPI transfer. SSEL should remain asserted for the duration of the transfer. Normally, this signal has no function in master mode and its port pin can be used as a general-purpose I/O. However, the SSEL can optionally be used as a mode fault detection in master mode.

ISO UART

The devices contain two smart card-compatible UART channels for connection to a smart card interface. The ISO UART provides a bidirectional I/O circuit and a separate clock circuit.

The ISO UART has the following features:

- Supports half-duplex asynchronous transmission
- Programmable baud rate
- Eight-character FIFO with parity detect/transmit
- Error management for T = 0 protocol (stream)
- Extra guard time between characters on transmit

The ISO UART I/O signal provides a half-duplex asynchronous data channel between the ISO UART controller and an external smart card interface IC, and defines the elementary time unit (ETU) for data timing. The external smart card interface IC supplies the data and clock connections to the smart card. To ensure synchronization between the smart card interface IC and the ISO UART controller, the clocks for both should be derived from the same base source.

Touch Sensors

The devices contain two capacitive touch switch inputs. These inputs are designed to operate with a wide range of quiescent capacitance values and should be generally immune from most noise sources.

The touch switches use a free-running oscillator with the frequency of the oscillator determined by the capacitance of a touch plate. When a conductive object is brought near to the touch plate, the oscillator frequency changes. This shift in frequency is detected by internal logic and can be used to signal an event to the processor.

The power consumption of the touch switch hardware is low enough to run on backup batteries, so the touch switch can be left enabled even when the device is in LCD_ONLY mode. The touch interrupt can be configured to wake the processor.

Auxiliary ADC

In addition to the metrology channels, the devices contain a 10-bit auxiliary ADC. This block can be used for a variety of purposes, and is used to condition optical receiver input, among other things.

The auxiliary ADC is a 10-bit ΔΣ converter operating at a modulator rate of 5MHz and a fixed oversampling rate that provides a final conversion rate of 4,800 samples per second.

Four pins can be configured to be used as AUX ADC inputs (see Table 6).

CRC

The devices contain a CRC generator for computing check words for most popular communication protocols. It generates a 16-bit CRC with a polynomial of 0x1021 ($x^{16} + x^{12} + x^5 + 1$), or a 32-bit CRC with a polynomial of 0x04C11DB7 ($x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$).

Multiply-Accumulate Unit

The devices provide a 32 x 32 fixed-point, multiply-accumulate unit to assist in mathematical operations. The multiplier provides a 64-bit result in a single cycle, and sums the product to a 64-bit accumulator in the same cycle. The multiplier is ready for another operation two cycles later. If the MAXQ30 core is running at 10MHz, the multiplier can perform five million 32 x 32 multiply cycles per second, in theory (in practice, the throughput is slowed by the requirement of loading and unloading the multiplier registers).

Table 6. Auxiliary ADC Input Pins

AUX ADC INPUT	PIN	ALTERNATE FUNCTION
0	59	GPIO Port 1 Bit 16
1	58	GPIO Port 1 Bit 17
2	57	GPIO Port 1 Bit 18, UART0 RxD, Optical Receive, CPU Wake Input 3
3	56	GPIO Port 1 Bit 19, UART0 TxD, Optical Transmit

Table 7. Auxiliary ADC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
AUXILIARY ADC					
Resolution			10		Bits
ADC Clock Frequency	f_{ACLK}	0.1		5.0	MHz
Integral Nonlinearity	INL		±2		LSB
Differential Nonlinearity	DNL		±1		LSB
Conversion Time		1024			ACLK
Input Voltage Range	V_{AN}	V_{GND} - 0.3		V_{3P3SYS} + 0.3	µA/ MHz

Metrology ADC Control

The metrology ADC channels operate essentially autonomously, depositing samples into RAM belonging to the CE and alerting the CE that a cycle is required to accumulate the new samples. However, the metrology subsystem must be configured to operate properly.

Metrology Overview

The devices contain two separate metrology subsystems. The first subsystem is a set of four DC modulators and associated decimation filters. These four modulators are typically configured to monitor line current, neutral current and line current, with the fourth modulator responsible for monitoring other conditions, such as a second voltage channel, temperature or a magnetic sensor for tamper detection. The second subsystem is a pair of remote interfaces that interface to Maxim R6000 remote sensors. These remote sensors can be configured to measure line and neutral current using current shunts rather than transformers or Rogowski coils, with isolation in both the measurement channels and the power circuit provided by inexpensive pulse transformers. See Figure 5.

The analog section of the devices consists of four analog-to-digital converters:

1) **ADC0:** Dedicated to current channel A (line current). An optional preamplifier can be inserted into the circuit for additional gain.
2) **ADC1:** Dedicated to current channel B (neutral current). An optional preamplifier can be inserted into the circuit for additional gain.
3) **ADC2:** Dedicated to voltage channel A (line voltage).
4) **ADC3:** Can be dedicated to any of three inputs, or configured to multiplex between the three inputs. The three inputs are V_B, V_C, V_D.

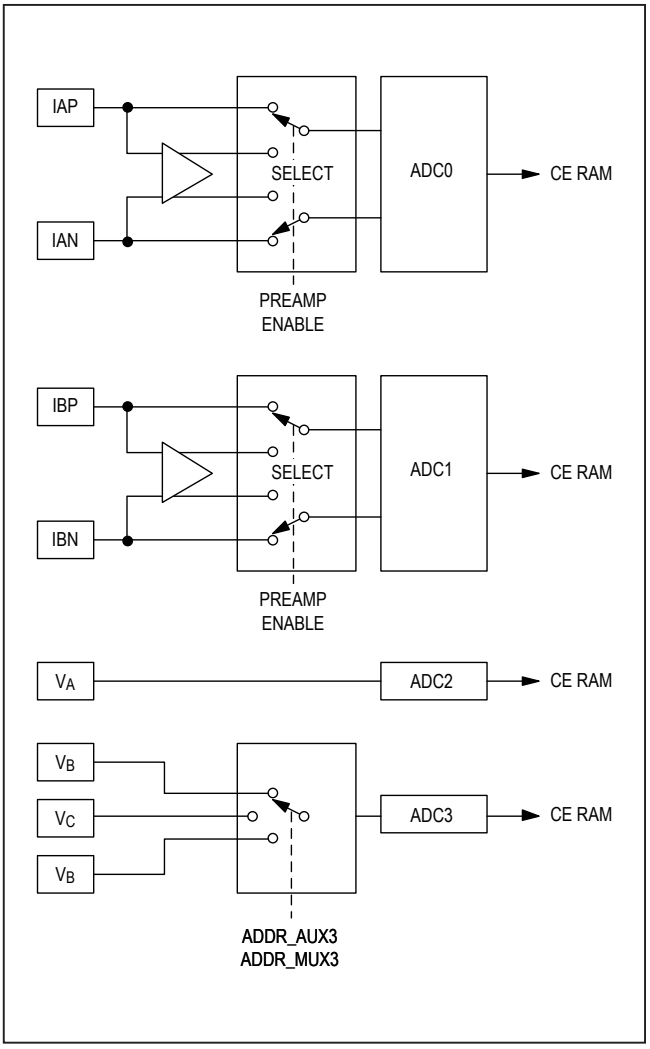


Figure 5. Metrology Channels

Remote Channels

The devices support the use of two remote interfaces for isolating the current channels. There are two generic types of remote interface supported, one is the 71M6000 series single-channel isolated remote interface, and the other is the MAX7107X 2-channel isolated remote interface. Both types of remote interface ICs use a pulse transformer to provide power to the device and to communicate ADC data and status information back to the device.

The pulse transformer effectively isolates the remote sensor interface and its attached sensors that typically operate at line potential (the hot side) from the MAX71314/MAX71315 microcontroller (the cold side). The devices provide a pulse stream that traverses the transformer and is rectified by the remote interface to provide power. The devices also transmit control data in the forward direction (MAX71314/MAX71315 to remote), and the remote interface provides a stream of ADC data, as well status information, in the reverse direction (remote to MAX71314/MAX71315.)

Real-Time Clock

The devices' real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. See Figure 6.

The RTC includes:

- 32-bit seconds register
- 8-bit sub-seconds register
- 32-bit alarm register
- Wake CPU from sleep mode on a variety of events
- Temperature measurement
- 3rd-order (cubic) temperature-compensation hardware
- Battery condition monitor

The RTC block resides across three power domains. Obviously, the real-time clock itself and the oscillator that drives it must reside in a nonvolatile power domain since the RTC cannot be allowed to lose time when power fails! The wake controller also resides in this power domain so it can wake the CPU even when all other power sources are off.

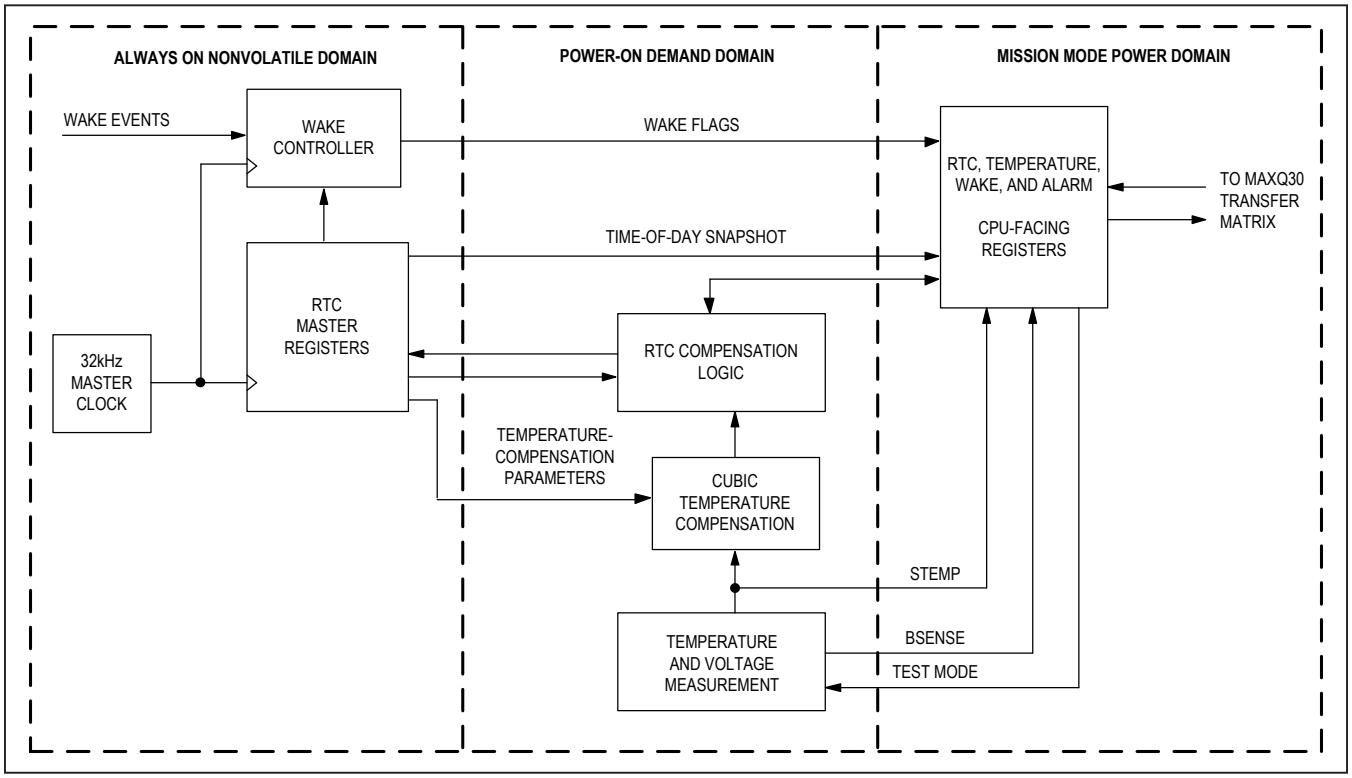


Figure 6. Real-Time Clock Block Diagram

Other RTC logic, such as the temperature-measurement and temperature-compensation logic, resides in an on-demand power domain. Chip logic can turn this power domain on and off as required, so from time to time the nonvolatile domain can turn on power to the on-demand domain, perform a compensation cycle, and then turn off power.

The final power domain is the mission mode domain. It has power only when the CPU is actually active. This domain contains the CPU-facing registers and associated interface logic. By keeping this domain off, unless the CPU is active, battery power is saved.

Digital I/O

The devices contain a number of pins that are configurable as digital I/O, either as peripheral pins or as direct-write general-purpose I/O. When assigned to a peripheral, these pins are automatically configured for the selected peripheral. When assigned for general-purpose I/O, the user can select from a number of different configurations.

In the devices, GPIO pins are organized as two 32-bit ports (port 0 and port 1). Each bit is individually configurable for input, output, or bidirectional modes.

GPIO Interrupts

Port 0 bits 7:0 also support external interrupts. All external interrupts in the devices are edge triggered, with the active edge configurable.

To enable external interrupts, set the bits in the EIE register that correspond to the pins you wish to cause an interrupt. You can also set the bits in the EIES register to select the active edge by writing a 0 to enable the rising edge or a 1 to enable the falling edge.

When the selected edge occurs on a pin configured for an interrupt, and if the interrupt is enabled, the corresponding bit is set in the interrupt flag register (IEF0). If interrupts are globally enabled (e.g., IGE = 1) an interrupt is generated to the MAXQ30 core.

Hardware Watchdog Timer

There are two independent watchdog timers in the devices. The first is a robust, fixed-duration watchdog timer associated with the metrology hardware, and the second is a configurable timer suitable for software watchdog purposes.

Ordering Information

PART	TEMP RANGE	OPERATING VOLTAGE	PROGRAM MEMORY	DATA MEMORY	METROLOGY CHANNELS	PIN-PACKAGE
MAX71314ECQ+*	-40°C to +85°C	+3.0V to +3.6V	128kB	12kB	4	100 LQFP, Bulk
MAX71314ECQ+T*	-40°C to +85°C	+3.0V to +3.6V	128kB	12kB	4	100 LQFP, T&R
MAX71315ECQ+	-40°C to +85°C	+3.0V to +3.6V	256kB	12kB	4	100 LQFP, Bulk
MAX71315ECQ+T	-40°C to +85°C	+3.0V to +3.6V	256kB	12kB	4	100 LQFP, T&R

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
100 LQFP	C100L+8	21-0684	90-0416

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—

