MAX71315S/MAX71316S/ MAX71335S/MAX71336S

ZON P5S/P5SL and M5S/M5SL Poly- and Single-Phase Energy Meter SoCs

General Description

The ZON™ P5S/P5SL (MAX71336S/MAX71335S) and ZON M5S/M5SL (MAX71316S/MAX71315S) are very low-power poly- and single-phase metering systems-on-chips (SoCs) that comprise a 20MHz MAXQ30 MPU core, real-time clock (RTC) with digital temperature compensation, flash memory, LCD drivers and a single-cycle 32 x 32 multiplier (MAC). Seven (ZON P5S/P5SL) or four (ZON M5S/M5SL) analog inputs with individual 24-bit delta-sigma ADCs, digital metrology temperature compensation, a precision voltage reference, a 32-bit computation engine (CE) with four pulse outputs, and security engines implementing AES and DES encryption support a wide range of smart metering applications with very few external components.

The ZON P5S/P5SL and ZON M5S/M5SL SoCs support optional interfaces to the 71M6xxx and MAX71071 series of isolated remote sensors that offer BOM cost reduction and enhanced reliability. The devices feature low-power operation in active and battery modes, 48KB RAM, and 256KB or 512KB of flash memory, programmable with code and/or data during meter operation.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI, IEC, and BIS electricity metering standards worldwide.

Applications

- Smart Meters
- Secure Meters
- Energy Monitoring

Benefits and Features

- Dual-core Architecture for Maximum Performance and Flexibility in 128-Pin LQFP
  - 32-Bit MAXQ30 MPU Core with 256/512KB Flash, 32KB Data NV-RAM (Shared with CE Data RAM), Up to 20MHz
  - 32-Bit Computing Engine (CE) with Separate 16KB Program and Data RAM, 40MHz, and Single-Cycle 64-Bit MAC
- Low Power Consumption Supports Low BOM Cost
  - Less than 13.7mA (typ) Consumption at 3.3V and 20MHz in Active Mode
  - < 3µA in RTC Compensation Mode, 2.3µA in SLP Mode
  - 2.7V to 3.6V Operating Voltage
- Advanced AFE with Exceptional Accuracy and Temperature Stability Supports a Broad Range of Applications, Including High-End Meters
  - Voltage Reference Temperature Coefficient (max) 40ppm/°C
  - RTC with Dedicated Temperature Compensation Circuit
  - On-Chip Digital Temperature Sensor and Battery Monitor
  - 24-Bit 2nd Order Delta-Digma ADCs with Differential Inputs Supporting CTs, Rogowski Coils and Both Single and Dual Input Remote Sensor Interface SoCs with Shunts (71M6xx3 or MAX71071)
  - Configurable Sampling Rate Up to 10ksps/Channel
  - ±0.1% Wh Accuracy Over 5000:1 Current Range
  - 40Hz–70Hz Line Frequency Range and Phase Compensation (±10°)
- Highly Integrated Product Features and Flexible Peripherals Support Broad Application Needs
  - Single 32kHz Crystal Provides All Operating Clocks
  - Low-Power 5ksps Auxiliary ADC for Environmental Monitoring
  - Two PWM Control Channels with Programmable Frequency, Duty Cycle, and Ramp Time
  - Two Touch Sensor Switch Inputs
  - SPI and I²C Master and Slave
  - Security Engines (3DES, AES)
  - 5 Timers
  - Single-Cycle 32 x 32 MAC Unit
  - 4x 40/6x 38/8x 36 LCDs with Autopaging
  - 5 UARTs, 1 with 38kHz IR Encoder/Decoder), Two Compliant with ISO 7816

***Ordering Information** appears at end of data sheet.*

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, send an email to support.metering@silergy.com*

Rev 3.1; 11/17

Absolute Maximum Ratings

(All voltages with respect to DGND.)

Voltage and Current Supplies and Ground Pins

V_{3P3SYS} ..... -0.5 to +3.8V

Crystal Pins

XIN, XOUT..... (-10mA to +10mA), (-0.5V to +3.0V)

Digital Pins

Inputs..... (-10mA to +10mA), (-0.5V to +6V, MSN/BRN mode)

Inputs..... (-10mA to +10mA), (-0.5V to V_{3P3SYS} + 0.5V, SLP mode)

Outputs..... (-8mA to +8mA), (-0.5V to (V_{3P3SYS} + 0.5V)

Temperature and ESD Stress

Operating Junction Temperature (peak, 100ms)..... +140°C

Operating Junction Temperature (continuous)..... +125°C

Storage Temperature Range..... -45°C to +165°C

ESD Stress on All Pins..... ±4kV, HBM

Lead Temperature (soldering, 10s)..... +300°C

Soldering Temperature (reflow)..... +250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

LQFP

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....45.6°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....16.1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Electrical and Timing Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{3P3SYS}	V_{BAT} = 0V to 3.8V, V_{BAT_RTC} = 2.0V to 3.8V	3.0		3.6	V
Supply Voltage, I/O	V_{IO}	Not in SLP or LCD modes	3.0		3.6	V
Supply Voltage, Backup Battery	V_{BAT}	V_{3P3SYS} < 2.8V and max (V_{BAT_RTC}, V_{3P3SYS}) > 2.0V	2.5		3.8	V
Supply Voltage, RTC Battery	V_{BAT_RTC}	V_{3P3SYS} < 2.0V	2.0		3.8	V
Supply Current (Note 2)	I_{DD1}	V_{3P3SYS} = 3.3V, RTM disabled, CE and ADCs enabled, ADCLK = 1		17	24	mA
Supply Current (Note 3)	I_{DD2}	V_{3P3SYS} = 3.3V, RTM disabled, CE and ADCs enabled 1, ADCLK = 2		13.7	18	mA
Supply Current (Note 6)	I_{DD3}	Normal operation, as above, except with variation of clock divider (CKCN)		12.5	17.1	mA
V_{BAT} Current	I_{VBAT}	MSN mode		±100		nA
		BRN mode, full speed (Note 7)		3.5	8.5	mA
		BRN mode, low speed (Note 8)		1.4	3.5	mA
		LCD_ONLY (Note 9)		3.2	8	µA
		SLP mode			0.4	µA
V_{BAT_RTC} Current	I_{VBAT_RTC}	MSN mode		±100		nA
		BRN mode		1.4	2.8	µA
		LCD_ONLY		1.2	8.0	µA
		SLP mode		2.3		µA

Electrical and Timing Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR FOR EXTERNAL CRYSTAL						
RTC Oscillator Frequency	f_{RTC}			32.768		kHz
Maximum Output Voltage		V_{IN} = 32.768kHz 0.2V_{P-P} sine			1.5	V
Maximum Crystal Power					1	µW
XIN to XOUT Capacitance				3		pF
CAPACITANCE TO DGND						
XIN		XIN = 100mV_{P-P}		14		pF
XOUT		XOUT = 0V		20		
Frequency Variation with Voltage		V_{BAT_RTC} = 2.2V to 3.8V		0.96		ppm
HF Oscillator Frequency	f_{HF}			117.96		MHz
INTERNAL OSCILLATOR						
Backup Oscillator Frequency	f_{BU}	Crystal oscillator disabled	23.45	24	24.53	MHz
LOGIC LEVELS						
Digital High-Level Input Voltage	V_{IH}		2		5.5	V
Digital Low-Level Input Voltage	V_{IL}		-0.3		+0.6	V
Other Digital Inputs	I_{IL}	J_{TAG_E} = 3.3V	-1	0	+1	µA
Input Pulldown Current $\overline{RST}$, JTAG_E	I_{IH}	V_{IN} = V_{3P3D}	10		100	µA
Other Digital Inputs	I_{IH}	V_{IN} = V_{3P3D}	-1	0	+1	
Digital High-Level Output Voltage	V_{OH}	I_{LOAD} = 1mA	V_{3P3D} - 0.4		V_{IO}	V
		I_{LOAD} = 5mA	V_{3P3D} - 0.6		V_{IO}	V
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = 1mA	0		0.4	V
		I_{LOAD} = 15mA	0		0.8	V
VSTAT LEVELS						
Analog Supply Threshold	V_{3AOK}			2.8		V
Digital Supply Threshold	V_{3OK}			2.5		V
Core Regulator Threshold	V_{3P3DOK}			2.3		V
Core Threshold	V_{DDOK}			1.6		V
BATTERY MONITOR						
Measurement Error		Sensing on V_{BAT} or V_{BAT_RTC}, 2.0V to 3.8V 2.0V			4	%
TEMPERATURE MONITOR						
Temperature Error		T_A = +22°C		3.6		%

Electrical and Timing Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE						
Nominal Reference Voltage	V_{REF}	T_A = +22°C, V_{3P3A} = 3.3V	1.226	1.228	1.230	V
Variation with Power Supply		V_{3P3A} = 3.0V to 3.6V	-1.5		+1.5	mV/V
Deviation from Predicted Variation with Temperature		V_{3P3A} = 3.0V to 3.6V	-40		+40	ppm/°C
ADC (METROLOGY)						
Usable Input Range		Preamp disabled	-250		+250	mV peak
Input Impedance		f_{IN} = 65Hz, preamp disabled	140		450	kΩ
Input Impedance		f_{IN} = 65Hz, preamp enabled	2.5		10	kΩ
LSB Size		FIR_LEN = 15		97		µV/LSB
Digital Full Scale		FIR_LEN = 15		±3375000		LSB
Input Offset Voltage			-10		+10	mV
THD				-87		dB
AUXILIARY ADC						
Resolution				10		Bits
ADC Clock Frequency	f_{ACLK}			5.0		MHz
Integral Nonlinearity	INL			±2		LSB
Differential Nonlinearity	DNL			±1		LSB
Input Impedance				667		kΩ
Conversion Time				1024		Cycles
SPI PORT						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CPUCLK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CPUCLK}/4$	MHz
SCLK Output Pulse-Width High/ Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - 35			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$ - 35			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - 35			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		35			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Input Pulse-Width High/ Low	t_{SCH}, t_{SCL}			t_{SCK} /2		ns
SSEL Active to First Shift Edge	t_{SSE}			50		ns

Electrical and Timing Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		35			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		35			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				70	ns
SCLK Inactive to SSEL Rising	t_{SD}		35			ns

Note 2: Supply current is the combined current into V_{3P3SYS} and V_{3P3A}; device is out of reset, no port activity, no flash writes measured at V_{3P3SYS} = V_{3P3A} = 3.3V, executing from flash, f_{CPUCLK} = 20MHz, metrology enabled, with ADC operating at full speed.

Note 3: Supply current is the combined current into V_{3P3SYS} and V_{3P3A}; device is out of reset, no port activity, no flash writes, measured at V_{3P3SYS} = V_{3P3A} = 3.3V, executing from flash, f_{CPUCLK} = 20MHz, metrology enabled, with ADC at operating half speed.

Note 4: Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 5: Guaranteed by design, not production tested.

Note 6: Same conditions as in Note 2, but f_{CPUCLK} = 20MHz/8.

Note 7: BRN current with PLL at 30MHz and f_{CPUCLK} = 5MHz.

Note 8: Same conditions as in Note 7, but f_{CPUCLK} = 1.23MHz.

Note 9: Transitional currents above stated maximum currents can occur when V_{3P3SYS}/V_{3P3A} are ramped up or down.

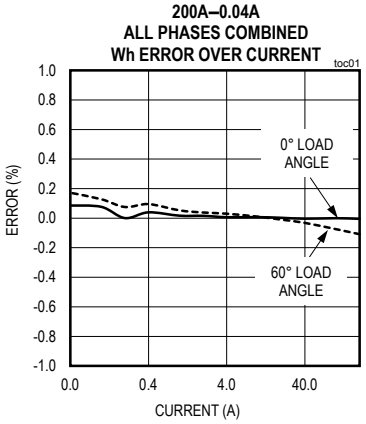
Recommended External Components

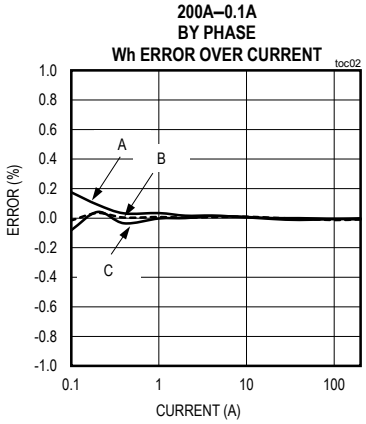
NAME	FROM	TO	FUNCTION	VALUE	UNIT
C2	V_{3P3D}	DGND	Bypass capacitor for 3.3V output	≥ 10	µF
CSYS	V_{3P3SYS}	DGND	Bypass capacitor for V_{3P3SYS}	≥ 1.0 ±20%	µF
CVDD	V_{DD}	DGND	Bypass capacitor for V_{DD}	0.1 ±20%	µF
CVLCD	V_{LCD}	DGND	Bypass capacitor for V_{LCD5} pin (when a charge pump is used)	≥ 0.1 ±20%	µF
XTAL	X_{IN}	XOUT	32.768 kHz crystal. Electrically similar to ECS .327-12.5-17X, Vishay XT26T or Suntsu SCP6–32.768kHz TR (load capacitance 12.5pF).	32.768	kHz
CXS	X_{IN}	AGND	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance.	20 ±10%	pF
CXL	X_{OUT}	AGND		20 ±10%	pF
C3	V_{3P3_RTC}	DGND	Bypass capacitor for V_{3P3_RTC} output	≥ 1.0	µF

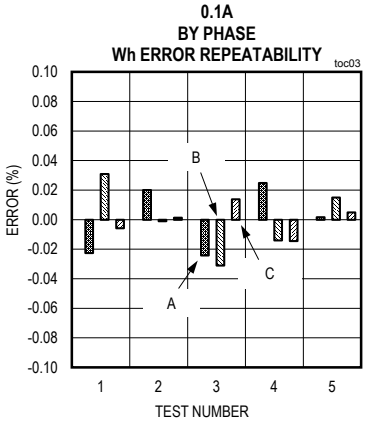
Note: *Values for recommended bypass capacitors are given as a general guideline and depend on the specific application. Contact Silergy Technology for details on the recommended component value.*

Typical Operating Characteristics

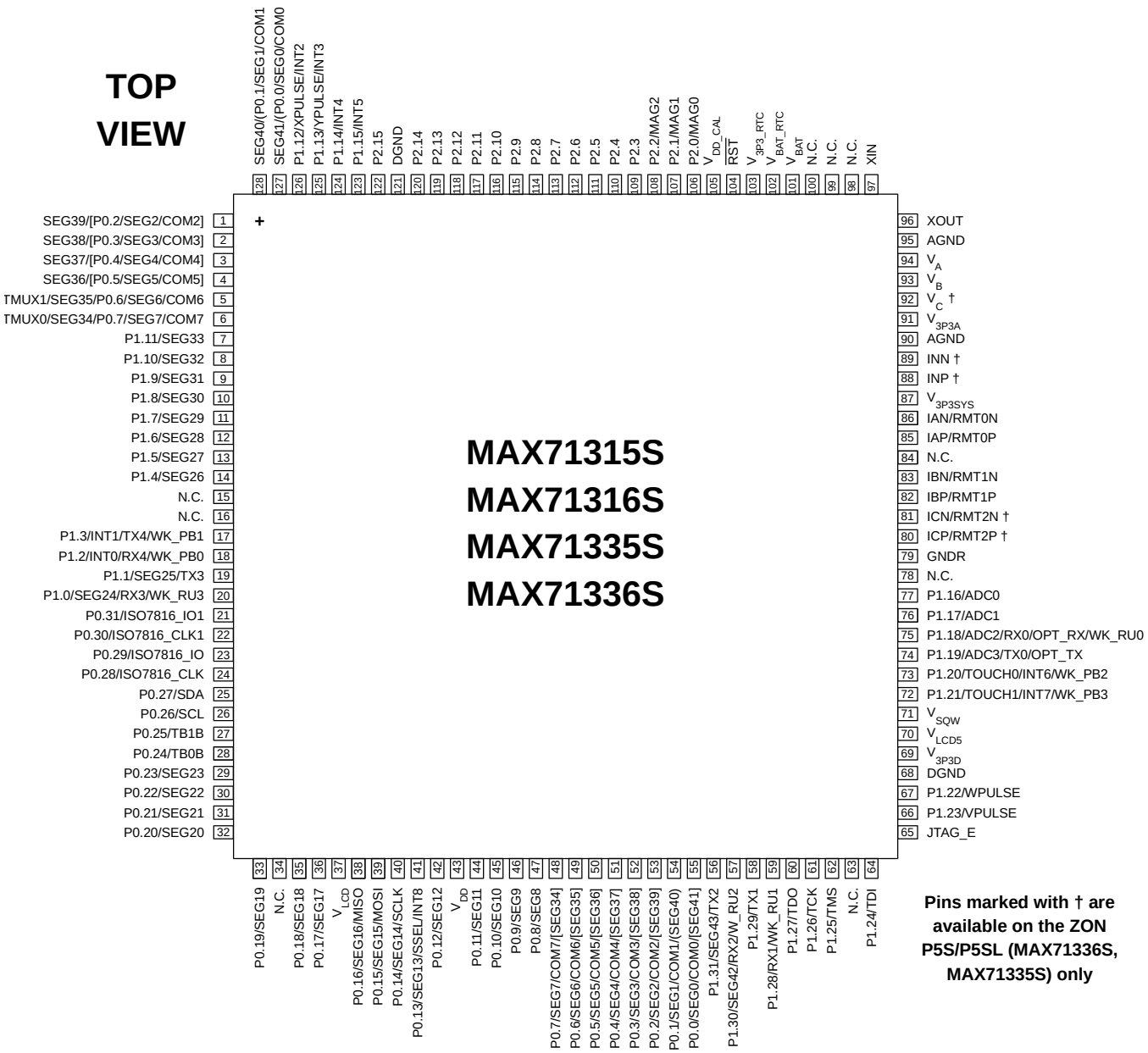
(V_{3P3SYS} = V_{3P3A} = 3.3V, room temperature, DC supply. The measurements use billing grade CTs and meter calibration systems operating at mains voltages under realistic conditions.)







Pin Configuration



Pins marked with † are available on the ZON P5S/P5SL (MAX71336S, MAX71335S) only

Pin Description

PIN	NAME	FUNCTION
1	SEG39/[P0.2/SEG2/COM2]*	LCD Segment 39 When the MIRROR bit is set, the pin is configurable as GPIO port P0.2, LCD segment 2, or LCD common 2.
2	SEG38/[P0.3/SEG3/COM3]*	LCD Segment 38 When the MIRROR bit is set, the pin is configurable as GPIO port P0.3, LCD segment 3, or LCD common 3.
3	SEG37/[P0.4/SEG4/COM4]*	LCD Segment 37 When the MIRROR bit is set, the pin is configurable as GPIO port P0.4, LCD segment 4, or LCD common 4.
4	SEG36/[P0.5/SEG5/COM5]*	LCD Segment 36 When the MIRROR bit is set, the pin is configurable as GPIO port P0.5, LCD segment 5, or LCD common 5.
5	TMUX1/SEG35/[P0.6/SEG6/COM6]*	Configurable as test multiplexer output or LCD segment 35. When the MIRROR bit is set, the pin is configurable as GPIO port P0.6, LCD segment 6, or LCD common 6.
6	TMUX0/SEG34/[P0.7/SEG7/COM7]*	Configurable as test multiplexer output or LCD segment 34. When the MIRROR bit is set, the pin is configurable as GPIO port P0.7, LCD segment 7, or LCD common 7.
7	P1.11/SEG33	Configurable as GPIO port P1.11 or LCD segment 33.
8	P1.10/SEG32	Configurable as GPIO port P1.10 or LCD segment 32.
9	P1.9/SEG31	Configurable as GPIO port P1.9 or LCD segment 31.
10	P1.8/SEG30	Configurable as GPIO port P1.8 or LCD segment 30.
11	P1.7/SEG29	Configurable as GPIO port P1.7 or LCD segment 29.
12	P1.6/SEG28	Configurable as GPIO port P1.6 or LCD segment 28.
13	P1.5/SEG27	Configurable as GPIO port P1.5 or LCD segment 27.
14	P1.4/SEG26	Configurable as GPIO port P1.4 or LCD segment 26.
15, 16, 34, 63, 78, 84, 98–100	N.C.	No Connection. Do not connect anything to these pins.
80–83, 92 (on ZON M5S/M5SL only)		
17	P1.3/INT1/TX4/WK_PB1	Configurable as GPIO port P1.3, external interrupt 1 input, PB1 wakeup input (WAKE2), or UART4 TX.
18	P1.2/INT0/RX4/WK_PB0	Configurable as GPIO port P1.2, external interrupt 0 input, PB0 wakeup input (WAKE1), or UART4 RX.
19	P1.1/SEG25/TX3	Configurable as GPIO port P1.1, LCD segment 25, or UART3 TX.
20	P1.0/SEG24/RX3/WK_RU3	Configurable as GPIO port P1.0, LCD segment 24, or UART3 RX input with wake capability (WAKE0).

Pin Description (continued)

PIN	NAME	FUNCTION
21	P0.31/ISO7816_IO1	Configurable as GPIO port P0.31 or ISO7816 Smart Card pin IO1.
22	P0.30/ISO7816_CLK1	Configurable as GPIO port P0.30 or ISO7816 Smart Card pin CLK1.
23	P0.29/ISO7816_IO	Configurable as GPIO port P0.29 or ISO7816 Smart Card pin IO.
24	P0.28/ISO7816_CLK	Configurable as GPIO port P0.28 or ISO7816 Smart Card pin CLK.
25	P0.27/SDA	Configurable as GPIO port P0.27 or I2C SDA signal.
26	P0.26/SCL	Configurable as GPIO port P0.26 or I2C SCL signal.
27	P0.25/TB1B	Configurable as GPIO port P0.26 or timer 1 B output.
28	P0.24/TB0B	Configurable as GPIO port P0.24 or timer 0 B output.
29	P0.23/SEG23	Configurable as GPIO port P0.23 or LCD segment 23.
30	P0.22/SEG22	Configurable as GPIO port P0.22 or LCD segment 22.
31	P0.21/SEG21	Configurable as GPIO port P0.21 or LCD segment 21.
32	P0.20/SEG20	Configurable as GPIO port P0.20 or LCD segment 20.
33	P0.19/SEG19	Configurable as GPIO port P0.19 or LCD segment 19.
35	P0.18/SEG18	Configurable as GPIO port P0.18 or LCD segment 18.
36	P0.17/SEG17	Configurable as GPIO port P0.17 or LCD segment 17.
37	V_{LCD}	Bypass point for the LCD supply. Typically, the supply is the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply, directly. V_{LCD} can also be used as an input to provide an external voltage to the LCD system. A 0.1µF capacitor to DGND should be connected to V_{LCD}.
38	P0.16/SEG16/MISO	Configurable as GPIO port P0.16, LCD segment 16, or SPI MISO signal.
39	P0.15/SEG15/MOSI	Configurable as GPIO port P0.15, LCD segment 15, or SPI MOSI signal.
40	P0.14/SEG14/SCLK	Configurable as GPIO port P0.14, LCD segment 14, or SPI SCLK signal.
41	P0.13/SEG13/ SSEL/INT8	Configurable as GPIO port P0.13, LCD segment 13, SPI SSEL signal, or external interrupt 8 input.
42	P0.12/SEG12	Configurable as GPIO port P0.12 or LCD segment 12.
43	V_{DD}	Bypass Point for the Internal V_{DD} Voltage. A 0.1µF capacitor to DGND should be connected to V_{DD}.
44	P0.11/SEG11	Configurable as GPIO port P0.11 or LCD segment 11.
45	P0.10/SEG10	Configurable as GPIO port P0.10 or LCD segment 10.
46	P0.9/SEG9	Configurable as GPIO port P0.9 or LCD segment 9.
47	P0.8/SEG8	Configurable as GPIO port P0.8 or LCD segment 8.
48	P0.7/SEG7/COM7/ (SEG34)*	Configurable as GPIO port P0.7, LCD segment 7, common 7.
		When the MIRROR bit is set, the pin functions as LCD segment 34.
49	P0.6/SEG6/COM6/ (SEG35)*	Configurable as GPIO port P0.6, LCD segment 6, common 6.
		When the MIRROR bit is set, the pin functions as LCD segment 35.
50	P0.5/SEG5/COM5/ (SEG36)*	Configurable as GPIO port P0.5, LCD segment 5, common 5.
		When the MIRROR bit is set, the pin functions as LCD segment 36.
51	P0.4/SEG4/COM4/ (SEG37)*	Configurable as GPIO port P0.4, LCD segment 4, common 4.
		When the MIRROR bit is set, the pin functions as LCD segment 37.

Pin Description (continued)

PIN	NAME	FUNCTION
52	P0.3/SEG3/COM3/ (SEG38)*	Configurable as GPIO port P0.3, LCD segment 3, common 3.
		When the MIRROR bit is set, the pin functions as LCD segment 38.
53	P0.2/SEG2/COM2/ (SEG39)*	Configurable as GPIO port P0.2, LCD segment 2, common 2.
		When the MIRROR bit is set, the pin functions as LCD segment 39.
54	P0.1/SEG1/COM1/ (SEG40)*	Configurable as GPIO port P0.1, LCD segment 1, common 1.
		When the MIRROR bit is set, the pin functions as LCD segment 40.
55	P0.0/SEG0/COM0/ (SEG41)*	Configurable as GPIO port P0.0, LCD segment 0, common 0.
		When the MIRROR bit is set, the pin functions as LCD segment 41.
56	P1.31/SEG43/TX2	Configurable as GPIO port P1.31, LCD segment 43, or UART2 TX signal.
57	P1.30/SEG42/RX2/ WK_RU2	Configurable as GPIO port P1.30, LCD segment 42, UART2 RX input with wake capability (WAKE7).
58	P1.29/TX1	Configurable as GPIO port P1.29 or UART1 TX signal.
59	P1.28/RX1/WK_RU1	Configurable as GPIO port P1.28, UART1 RX input with wake capability (WAKE6).
60	P1.27/TDO	GPIO Port P1.27. When JTAG_E is pulled high this pin carries the JTAG TDO signal.
61	P1.26/TCK	GPIO Port P1.26. When JTAG_E is pulled high this pin carries the JTAG TCK signal.
62	P1.25/TMS	GPIO Port P1.25. When JTAG_E is pulled high this pin carries the JTAG TMS signal.
64	P1.24/TDI	GPIO Port P1.24. When JTAG_E is pulled high this pin carries the JTAG TDI signal.
65	JTAG_E	Enables the JTAG port when pulled high. Should be pulled down during normal operation.
66	P1.23/RPULSE	Configurable as GPIO port P1.23 or VARh pulse output.
67	P1.22/WPULSE	Configurable as GPIO port P1.22 or Wh pulse output.
68, 121	DGND	Digital Ground
69	V_{3P3D}	Auxiliary Voltage V_{3P3D} Output. A 0.1µF capacitor to DGND should be connected to V_{3P3D}.
70	V_{LCD5}	The Supply Point for the LCD System. If operation with 5V-compatible LCD glass is desired. A 0.1µF capacitor to DGND should be connected to V_{LCD5} when a charge pump is used.
71	V_{SQW}	The Square Wave Output. This pin can be used to implement a charge pump for generating a 5V supply for the LCD system.
72	P1.21/TOUCH1/ INT7/WK_PB3	Configurable as GPIO port P1.21, touch pad input 1, external interrupt 7 input, or PB3 wakeup input (WAKE4).
73	P1.20/TOUCH0/ INT6/WK_PB2	Configurable as GPIO port P1.20, touch pad input 0, external interrupt 6 input, or PB2 wakeup input (WAKE5).
74	P1.19/ADC3/ TX0/OPT_TX	Configurable as GPIO port P1.19, auxiliary ADC3 input, UART0 TX signal, or TX signal for the optical port.
75	P1.18/ADC2/ RX0/WK_RU0	Configurable as GPIO port P1.18, auxiliary ADC2 input, UART0 RX input with wake capability (WAKE3), or RX signal for the optical port.
76	P1.17/ADC1	Configurable as GPIO port P1.17, or auxiliary ADC1 input.
77	P1.16/ADC0	Configurable as GPIO port P1.16, or auxiliary ADC0 input.

Pin Description (continued)

PIN	NAME	FUNCTION
79	GNDR	Return for Remote Drivers. Must be connected to DGND.
80	ICP/RMT2P†	Positive Input to the ADC for Current in Phase C. When a remote sensor is used, the pulse transformer is connected to this pin. Only available on the ZON P5S/P5SL.
81	ICN/RMT2N†	Negative Input to the ADC for Current in Phase C. When a remote sensor is used, the pulse transformer is connected to this pin. Only available on the ZON P5S/P5SL.
82	IBP/RMT1P	Positive Input the ADC for Current in Phase B. When a remote sensor is used, the pulse transformer is connected to this pin.
83	IBN/RMT1N	Negative Input to the ADC for Current in Phase B. When a remote sensor is used, the pulse transformer is connected to this pin.
85	IAP/RMT0P†	Positive Input to the ADC for Current in Phase A. When a remote sensor is used, the pulse transformer is connected to this pin. Only available on the ZON P5S/P5SL.
86	IAN/RMT0N†	Negative Input to the ADC for Current in Phase A. When a remote sensor is used, the pulse transformer is connected to this pin. Only available on the ZON P5S/P5SL.
87	V_{3P3SYS}	Positive Supply Voltage for the Digital Circuits in the SoC. The 3.0VDC to 3.6VDC supply voltage is connected here.
88	INP	Positive Input to the ADC for the Neutral Current. Only available on ZON P5S/P5SL.
89	INN	Negative Input to the ADC for the Neutral Current. Only available on ZON P5S/P5SL.
90, 95	AGND	Analog Ground Reference
91	V_{3P3A}	Positive Supply Voltage for the Analog Circuits in the SoC. The 3.0VDC to 3.6VDC supply voltage is connected here.
92	Vc†, (N.C. on ZON M5S/ M5SL)	Input to the ADC for Voltage in Phase C. Only available on ZON P5S/P5SL.
93	V_B	Input to the ADC for Voltage in Phase B
94	V_A	Input to the ADC for Voltage in Phase A
96	XOUT	Crystal Oscillator Output. A 32kHz crystal is connected between XOUT and XIN.
97	XIN	Crystal Oscillator Input
101	V_{BAT}	Positive Supply Voltage for the Operation of the SoC in BRN Mode. Typically, a battery with voltage from 2.5VDC to 3.8VDC is connected here.
102	V_{BAT_RTC}	Positive Supply Voltage for the Operation of the SoC in SLP Mode. Typically, a battery with voltage from 2.0VDC to 3.8VDC is connected here.
103	V_{3P3_RTC}	The Bypass Point for the Nonvolatile Power Bus. A 0.1µF capacitor to DGND should be connected to V_{3P3_RTC}.
104	$\overline{RST}$	Low-Active Reset Input. A soft pullup to V_{3P3_RTC} should be provided for this pin.
105	V_{DD_CAL}	The Bypass Point for the Internal Calibration Power Bus. A 0.1µF capacitor to DGND should be connected to V_{DD_CAL}.
106	P2.0/MAG0	Configurable as P2.0 or input 5 for the general-purpose ADC.
107	P2.1/MAG1	Configurable as P2.1 or input 6 for the general-purpose ADC.
108	P2.2/MAG2	Configurable as P2.2 or input 7 for the general-purpose ADC.
109	P2.3	GPIO Port P2.3
110	P2.4	GPIO Port P2.4

Pin Description (continued)

PIN	NAME	FUNCTION
111	P2.5	GPIO Port P2.5
112	P2.6	GPIO Port P2.6
113	P2.7	GPIO Port P2.7
114	P2.8	GPIO Port P2.8
115	P2.9	GPIO Port P2.9
116	P2.10	GPIO Port P2.10
117	P2.11	GPIO Port P2.11
118	P2.12	GPIO Port P2.12
119	P2.13	GPIO Port P2.13
120	P2.14	GPIO Port P2.14
122	P2.15	GPIO Port P2.15
123	P1.15/INT5	Configurable as GPIO port P1.15 or external interrupt 5 input.
124	P1.14/INT4	Configurable as GPIO port P1.14 or external interrupt 4 input.
125	P1.13/YPULSE/INT3	Configurable as GPIO port P1.13, Y pulse output from the CE, or external interrupt 3 input.
126	P1.12/XPULSE/INT2	Configurable as GPIO port P1.12, X pulse output from the CE, or external interrupt 2 input.
127	SEG41/(P0.0/SEG0/ COM0)*	LCD Segment 41
		When the MIRROR bit is set, the pin can be configured as GPIO port P0.0, LCD segment 0, or LCD common 0.
128	SEG40/ (P0.1/SEG1/COM1)*	LCD Segment 40
		When the MIRROR bit is set, the pin can be configured as GPIO port P0.1, LCD segment 1, or LCD common 1.

**Pins are controlled by the so-called MIRROR bit: By setting the MIRROR bit in the LCDCTL register the LCD segment pins on the south side of the SoC are swapped with LCD segment pins on the north side of the chip. Pin functions in parentheses denote functions activated when the MIRROR bit is true. See the section on Special LCD Modes for details.*

†*Pins are available on the P5S/P5SL devices only. These pins have no connection on the M5S/M5SL devices.*

Detailed Description

Hardware Description

This data sheet covers the MAX71335S (256KB) and MAX71336S (512KB) polyphase energy measurement systems-on-chip (SoCs) and the MAX71315S (256KB) and MAX71316S (512KB) single-phase energy measurement systems-on-chip.

The MAX71335S/MAX71336S in conjunction with the 71M6xx3 or MAX71071 SoCs make it possible to use three inexpensive shunt current sensors plus one optional neutral current sensor (shunt or CT) to create polyphase energy meters with excellent performance. The MAX71335S/MAX71336S SoCs also support current transformers (CT) and Rogowski coils.

The block diagram of the device is shown in Figure 1.

The MAX71316S/MAX71315S can be used to implement a variety of single-phase or dual-phase energy meters:

- One MAX71316S/MAX71315S SoC with two 71M6xx3 or MAX71071 SoCs and two inexpensive shunt sensors implements a two-phase electricity meter for equation 1 (ANSI split phase) or equation 2.
- One MAX71316S/MAX71315S SoC with two CTs or Rogowski coils implements a two-phase electricity meter for equation 1 (ANSI split phase) or equation 2.
- One MAX71316S/MAX71315S SoC combined with one inexpensive shunt sensor and a CT implement a single-phase electricity meter for equation 0, using the CT for neutral current monitoring and tamper detection.
- One MAX71316S/MAX71315S SoC with one 71M6xx3 or MAX71071 SoCs and two inexpensive shunt sensor implements a single-phase electricity meter for equation 0, using the second shunt sensor for neutral current monitoring and tamper detection.

All ZON P5S/P5SL and M5S/M5SL SoCs incorporate a 32-bit MAXQ30 microcontroller core, delivering approximately one MIPS/MHz of clock (nominally, 19.66MHz); a 32-bit dedicated metrology compute engine; an interface for external sensor controllers and a complete set of peripherals onto a single device. The devices are available in a 128-pin LQFP package.

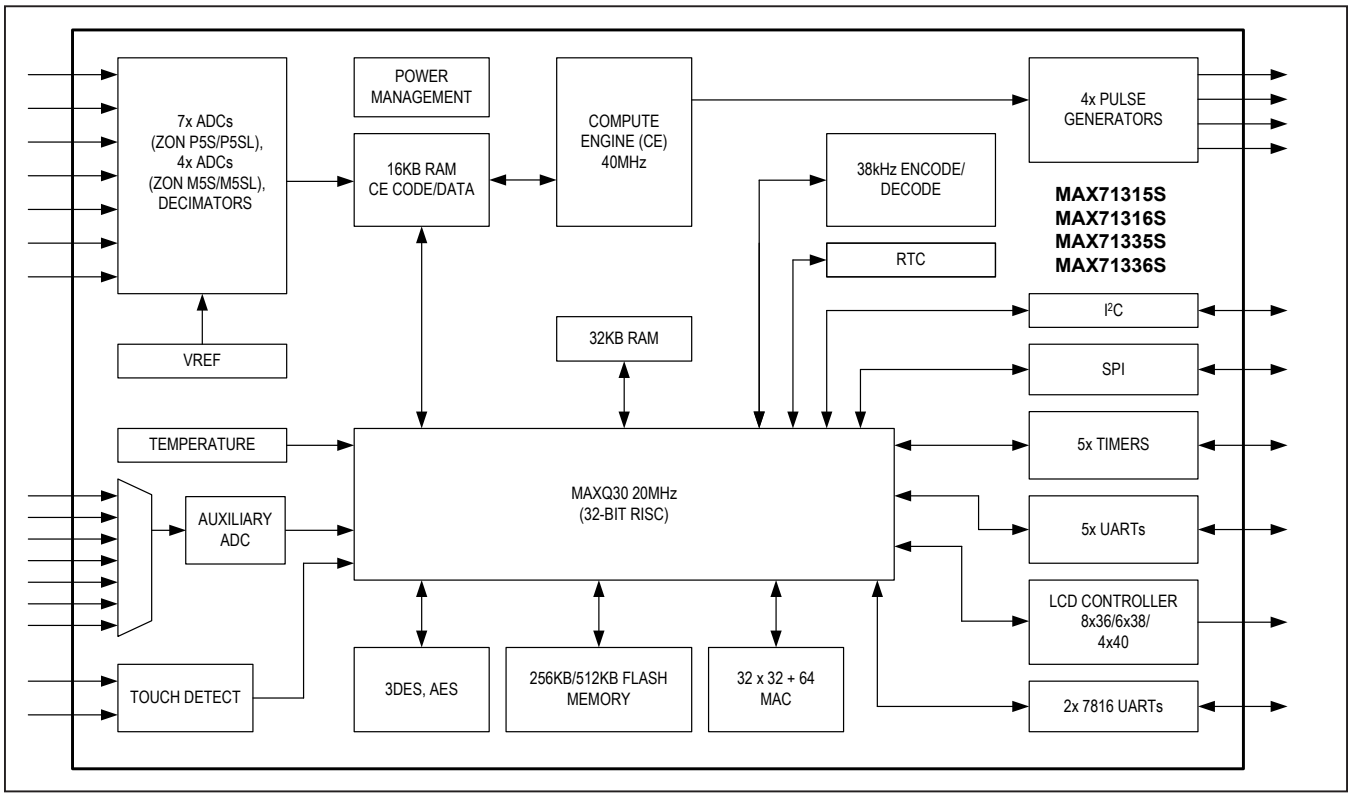


Figure 1. Functional Diagram

The ZON P5S/P5SL and M5S/M5SL SoCs offer a display controller that supports 8-way multiplexing of LCD segments. Up to 36 available segment pins provide up to 288 controllable display segments in the 8-way multiplexing configuration.

The ZON P5S/P5SL contains interfaces capable of supporting up to seven metrology channels. Typically, these channels are assigned to measure the primary parameters of interest: line voltages, line currents and neutral current. Three of the analog channels can be used in remote mode and can provide inherent isolation to protect the ZON P5S/P5SL from line potentials. In the current channels, any sensor including current transformers, shunts or Rogowski coils can be selected.

Similarly, the ZON M5S/M5SL contains interfaces capable of supporting up to four metrology channels. Typically, these channels are assigned to measure line voltages, line currents and neutral current. Two of the analog channels can be used in remote mode and can provide inherent isolation to protect the ZON M5S/M5SL from line potentials. For the current channels, any sensor including current transformers, shunts or Rogowski coils can be selected.

The ADC samples are processed by a fixed-point compute engine (CE). The code for the CE resides in RAM that is shared with the MAXQ30 MPU core.

The ZON P5S/P5SL and M5S/M5SL SoCs include a separate ADC subsystem to monitor slow-moving environmental conditions. This ΔΣ ADC is clocked at a fixed rate of 4.9152MHz and can be multiplexed among four pins.

The ZON P5S/P5SL and M5S/M5SL SoCs are clocked by one external 32,768Hz tuning-fork type crystal that is used as a reference for the RTC. A PLL multiplies this clock by 3600 to provide a 117.9648MHz master clock that is divided to the 19.6608MHz required by the MAXQ30 MPU core, the 39.32MHz required by the CE and other clocks required by the system.

In a typical application, the CE of the ZON P5S/P5SL or M5S/M5SL SoCs processes the samples from its metrology input channels and performs calculations to measure real energy and reactive energy as well as volt-ampere hours, A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MAXQ30 MPU core, processed further, and output using the peripheral devices available to the MPU.

The ZON P5S/P5SL and M5S/M5SL SoCs feature a real-time clock to record time of use (TOU) metering information for multirate applications and to time-stamp tamper or other events. Measurement results can be displayed on an LCD: either 3.3V glass commonly used in low-temperature environments or 5V glass used in more demanding environments, using an external 5V power supply. An oscillator pin is provided to allow the use of an external charge pump to create the 5V LCD voltage. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs.

The ZON P5S/P5SL and M5S/M5SL SoCs include a precision voltage reference. A temperature correction mechanism guarantees conformance to accuracy standards over temperature. Temperature-dependent external components such as current transformers and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

The ZON P5S/P5SL and M5S/M5SL SoCs support the use of remote interfaces for isolating the current and/or voltage channels. Two types of remote interfaces are supported: the 71M6xxx single-channel isolated remote interface and the MAX71071 two-channel isolated remote interface. Both types of remote interface SoCs use a pulse transformer to provide power to the device and to communicate ADC data and status information back to the ZON P5S/P5SL or M5S/M5SL SoCs.

For details on the P5S/P5SL and M5S/M5SL SoC hardware, register locations, register details, etc., refer to the ZON P5S/P5SL and M5S/M5SL HRM (Hardware Reference Manual).

Analog Front End (AFE)

The ZON P5S/P5SL SoCs contain seven delta-sigma ADC channels with associated decimation filters for monitoring line voltages, line currents, and neutral current. Four channels contain a preamplifier that provides a gain of one, four, eight, or sixteen as required. The assignment of ADC channels is as follows:

- ADC0: Dedicated to current channel A (line current). An optional preamplifier can be inserted into the circuit.
- ADC1: Dedicated to current channel B (line current). An optional preamplifier can be inserted into the circuit.
- ADC2: Dedicated to current channel C (line current). An optional preamplifier can be inserted into the circuit.
- ADC3: Dedicated to current channel D (neutral current). An optional preamplifier can be inserted into the circuit.
- ADC5: Dedicated to voltage channel A.
- ADC6: Dedicated to voltage channel B.
- ADC7: Dedicated to voltage channel C.

The ZON M5S/M5SL SoCs contain four delta-sigma ADC channels with associated decimation filters for monitoring line voltages, line currents and neutral current. Two channels contain a preamplifier that provides a gain of one, four, eight, or sixteen as required. The assignment of ADC channels is as follows:

- ADC0: Dedicated to current channel A (line current). An optional preamplifier can be inserted into the circuit for additional gain.
- ADC1: Dedicated to current channel B (line current). An optional preamplifier can be inserted into the circuit for additional gain.
- ADC5: Dedicated to voltage channel A.
- ADC6: Dedicated to voltage channel B.

Analog inputs are sampled at up to 1.66MHz. The samples are decimated in a FIR filter with an oversampling ratio of up to 512. Finished samples are available to the CE at up to 10.92ksps per channel.

Inputs to the AFE must be referenced to AGND and must be scaled so that the signal is no greater than 250mV above or below AGND. For example, a system that is expected to monitor up to $300V_{RMS}$ would need to scale that voltage to no more than 250mV peak, and would require a voltage divider with a divide ratio of no less than:

$$\frac{300\times\sqrt{2}}{0.25} = 1{,}697$$

Similar calculations must be made for the current channels.

The metrology ADC channels operate essentially autonomously, depositing samples into RAM belonging to the CE and alerting the CE that a cycle is required to accumulate the new samples. The metrology subsystem must be configured, however, to operate properly.

Remote Interfaces

A low-cost pulse transformer effectively isolates the remote sensor interface and its attached sensors that typically operate at line potential (the hot side) from the ZON P5S/P5SL or M5S/M5SL SoCs (the cold side). The ZON P5S/P5SL and M5S/M5SL SoCs provide a pulse stream that traverses the transformer and is rectified by the remote interface to provide power. The ZON P5S/P5SL and M5S/M5SL SoCs also transmit control data in the forward direction (ZON P5S/P5SL or M5S/M5SL SoC to remote), and the remote interface provides a stream of ADC data as well status information in the reverse direction (remote to ZON P5S/P5SL or M5S/M5SL SoC).

For the ZON P5S/P5SL SoCs, three of the analog input channels can be configured for remote interfaces, whereas the ZON M5S/M5SL SoC supports two remote interfaces. The ZON P5S/P5SL or M5S/M5SL SoCs support various remote technologies: one channel can be connected to a one-channel remote interface (e.g., the 71M6103), and a second channel can be connected to a two-channel remote interface (MAX71071). The remote interfaces provide power to the remotes by sending current pulses across an isolation transformer. The data output from the 71M6xxx-type isolated remotes is decimated by FIR filters and stored in RAM where it can be accessed and processed by the CE.

Digital Computation Engine (CE)

The compute engine is a dedicated 32-bit DSP operating at a 40MHz clock frequency. With binary code modules provided by Silergy, it performs the signal processing necessary to accurately measure energy. The CE calculations and processes can include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time)
- 90° phase shifter (for VARh calculations)
- Pulse generation
- Measurement of the input signal frequency (for frequency and phase information)
- Monitoring of the input signal amplitude (for sag and swell detection)
- Scaling of the processed samples based on calibration coefficients
- Scaling of samples based on MPU temperature compensation information
- Extraction, suppression or filtering of harmonics for special functions
- Variable gain compensation
- Variable phase compensation

The CE uses a single 8K x 16 block of RAM for both code and data storage. A single-cycle 64-bit multiply-accumulate (MAC) operation is supported.

CE code is written to the RAM block by the MAXQ30 MPU core during system initialization. After that, the MAXQ30 MPU core releases the CE to begin executing. The MAXQ30 MPU core, the CE and the ADC block share the CE data RAM space with interleaved cycles.

Because of the time interleaving the CE data RAM can be accessed apparently simultaneously by the CE and the MAXQ30 MPU core. The CE can access any location in the shared SRAM. The MAXQ30 MPU core reads and writes the SRAM as the primary means of data communication between the two processor cores.

The CE deals with all data on a 64-bit or 32-bit basis and has no concept of single bytes. The shared memory controller stores 32-bit words from the CE in the same way that the MPU reads and writes such that the byte order that the MPU expects is preserved.

The CE data RAM can be accessed by the FIR block, the RTM, the CE, and the MPU. Assigned time slots are reserved for MPU and metering, so that memory accesses to shared RAM do not collide. FIR data is written one clock cycle after the FIR completes its calculation. RTM data is read from the locations specified by registers RTM0, RTM1, RTM2, and RTM3 in the scheduled time slots to avoid collision with MPU accesses.

Before starting the CE the MPU has to establish the proper environment for the CE by enabling the ADC, setting the ADC clock, analog gain selections, FIR lengths, time slots, pulse settings, and accumulation intervals to their proper values. The environment required for a particular CE code is documented in the CE code Reference Manual for the CE code used.

At startup, the MAXQ30 MPU core writes the calibration coefficients and other parameter to CE RAM where they are read and used by the CE.

Typical CE Codes can implement the equations listed in Table 1. The ZON P5S/P5SL standard poly-phase CE codes implement only equation 5. The ZON M5S/M5SL standard single-phase CE codes implement only equations 0, 1, and 2. For other configurations, contact the factory.

The CE hardware includes a real-time monitor (RTM) that can be configured by the MPU to monitor four selectable CE RAM locations at full sample rate, either for diagnostic purposes or for streaming of samples. The four monitored locations are serially output at the beginning of each CE code pass. The RTM output is clocked at the ADC clock rate. Each RTM word is clocked out in 35 cycles and contains a leading flag bit.

The pulse generator hardware of the ZON P5S/P5SL and M5S/M5SL SoCs supports the primary pulses RPULSE and WPULSE and the secondary pulse outputs XPULSE and YPULSE.

During each CE code pass, the hardware stores exported sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate all of the pulse generator outputs at the beginning of its code pass and to rely on hardware to spread them evenly over the sample frame. The FIFO is reset at the beginning of each sample frame.

The pulse generator outputs are available as alternate functions on P1.12, P1.13, P1.22, and P1.23.

The ZON P5S/P5SL and M5S/M5SL SoCs provide four pulse generators, RPULSE, WPULSE, XPULSE, and YPULSE, as well as hardware support for the RPULSE and WPULSE pulse generators. The XPULSE and YPULSE generators are used by standard CE code to output CE status indicators, for example the status of the sag detection, to GPIO pins. All pulses can be configured to generate interrupts to the MPU.

The polarity of the pulses can be inverted with PLS_INV. When this bit is set, the pulses are active high, rather than the more usual active low. PLS_INV inverts all the pulse outputs.

Pulses generated by the CE can be exported to the XPULSE and YPULSE pulse outputs. Generally, the XPULSE and YPULSE outputs are updated once on each pass of the CE code, resulting in a maximum pulse frequency that is equivalent to the ADC sample frequency.

Standard CE code permits the signaling of a sag event for the YPULSE output. The XPULSE output is used to indicate zero crossings of the mains voltage that can be used to synchronize PLC modems or other equipment.

For details on CE operation, register locations, register details, LSB values, code features, etc., refer to the ZON P5S/P5SL CE or ZON M5S/M5SL Reference Manual.

Table 1. CE Equations

EQU	CALCULATION METHOD FOR Wh AND VARh	DESCRIPTION
0	VA x IA	(1 element, 2W)
1	VA x (IA - IB)/2	(2 element, 3W)
2	VA x IA + VB x IB	(2 element, 3W, 3φ Delta)
3	VA x (IA - IB)/2 + VC x IC	(2 element, 4W 3φ Delta)
4	VA x (IA - IB)/2 + VB x (IC - IB)/2	(2 element, 4W 3φ Wye)
5	VA x IA + VB x IB + VC x IC	(3 element, 4W 3φ Wye)

CE—MAXQ30 Communication

The CE alerts the MAXQ30 MPU core to changes in its condition over six hardware circuits:

CE_BUSY: This signal indicates that the CE is actively processing data. The trailing edge of this signal can interrupt the MAXQ30 MPU core for events that must be processed on each sample.

XFER_BUSY: This signal indicates that the CE is updating the output region of the CE RAM with data for the MPU. This update typically includes the result of energy and squared-sample summations, and occurs after the number of samples designated in the SAMPLE field of the CECN register. This signal can interrupt the MAXQ30 MPU core for those events that must be processed every accumulation interval.

RPULSE, WPULSE, XPULSE, and YPULSE: These output pulses can be configured to interrupt the MAXQ30 MPU core. Typically, WPULSE indicates a certain amount of real energy has been accumulated, and RPULSE indicates a certain amount of reactive energy has been accumulated. YPULSE is often configured to indicate a loss of zero crossings on the voltage channel, and XPULSE can be configured for other significant events. Any of these signals can be routed directly to DIO pins to provide direct outputs to pulse LEDs or alert other external equipment.

MAXQ30 MPU Core

The MAXQ30 MPU implements a 32-bit RISC core. It is unique because all instructions can be coded as a simple MOVE instruction, yielding high efficiency in both time and power. The MAXQ30MPU core has the following characteristics:

- Instructions typically execute in a single cycle
- All peripherals are first-class data objects
- Flexible data pointers make block data moves simple
- Dedicated 32x32 single-cycle multiplier

MAXQ30 Register Complement

The MAXQ30 MPU core supports a total of 512 32-bit registers, not all of which are used for the ZON P5S/P5SL or M5S/M5SL. Registers are divided into system registers (called Special Purpose registers or SPRs) and peripheral registers (called Special Function registers or SFRs).

The 512 registers are divided into blocks of register modules. A register module is a group of up to 32 related registers. The MAXQ30 architecture supports up to 16 register modules. Register modules 0–5 are dedicated to Special Function registers and dedicated to controlling peripherals, while registers 7–15 are dedicated to Special Purpose registers and dedicated to controlling system functions.

All registers are described in detail in the ZON P5S/P5SL and ZON M5S/M5SL HRM (Hardware Reference Manual). In demo code and in the HRM, register locations are sometimes called out using a hexadecimal address, for example 0x154. In this format, 4 is the module number, and 0x15 is the register address.

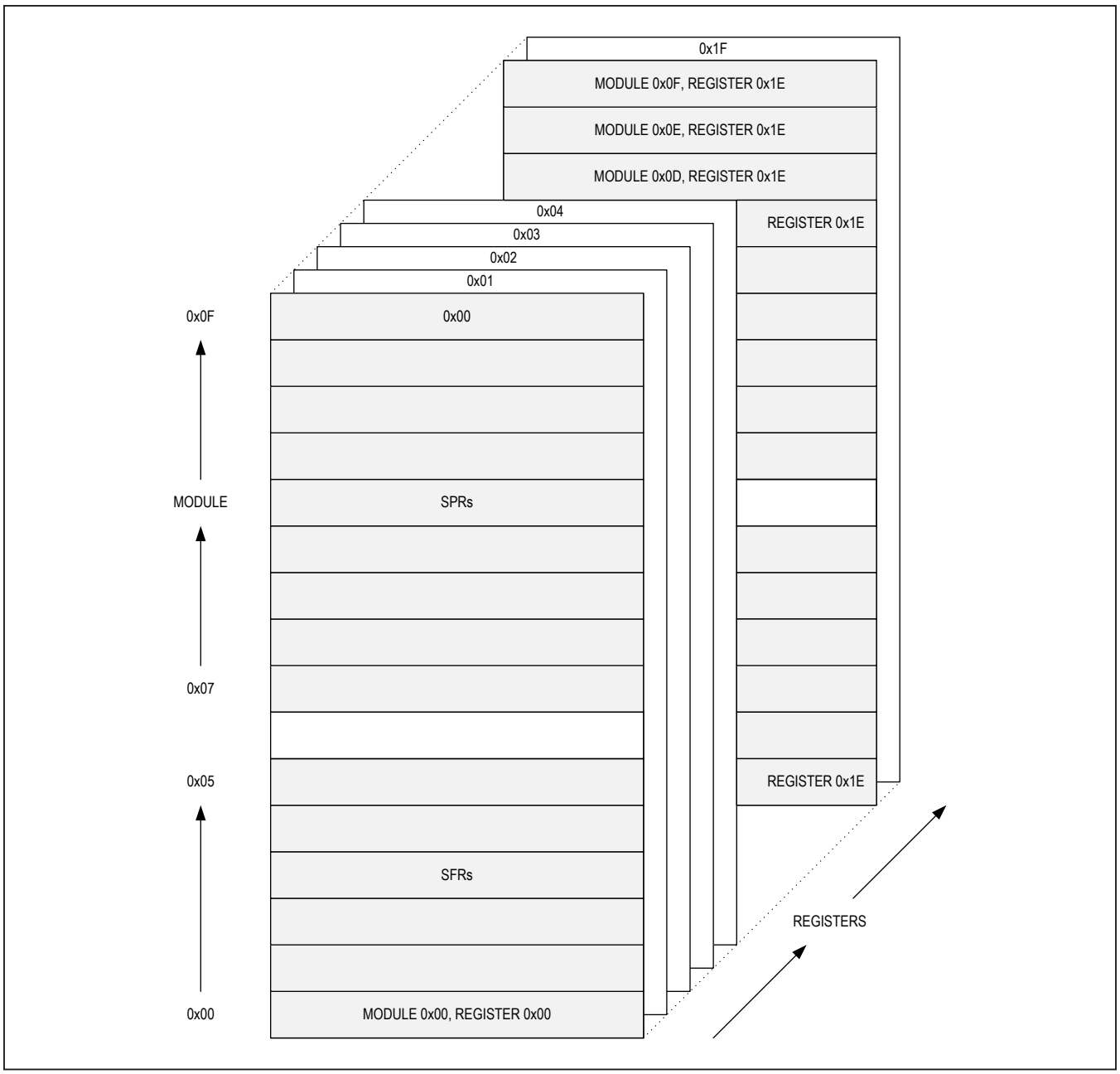


Figure 2. Map of SPRs and SFRs

System Registers (SFRs)

All system registers are described in detail in the ZON P5S/P5SL and M5S/M5SL HRM (Hardware Reference Manual). Table 2 contains the addresses for the Special Function registers.

Table 2. Special Function Registers

REGISTER INDEX	MODULE INDEX					
	M0 (0x00)	M1 (0x01)	M2 (0x02)	M3 (0x03)	M4 (0x04)	M5 (0x05)
0x00	I2C0CN	PO0	MCNT	SCON0	MUXCN	RCTI
0x01	I2C0INT	PO1	MA	SBUF0	RMTCN	LCDIND ADDR
0x02	I2C0ST	EIF0	MB	SCON1	RMTCMD	LCDIND DATA
0x03	I2C0DATA	TB0CN	—	SBUF1	ADCN	TSW0CMP
0x04	I2C0MCN	TB1CN	MC0	SCON2	ADCFG	TSW0CN
0x05	SPICN	TB2CN	MC1	SBUF2	UCNT1	TSW0CNT
0x06	SPIST	TB3CN	UCNT0	SCON3	UTR1	TSW1CMP
0x07	SPIB	TB4CN	UTR0	SBUF3	CEPCN	TSW1CN
0x08	I2C0RX	PI0	UST0	DEMCN	UST1	TSW1CNT
0x09	I2C0RXCFG	PI1	UCK0	DEMSAMP	UCK1	TMUXSEL
0x0A	I2C0TX	EIE0	UGT0	SMD0	UGT1	RTCSEC
0x0B	I2C0TXCFG	EIES0	MC0R	PRL0	CECN	RTCSUB
0x0C	I2C0SLA	PO2	MC1R	SMD1	CEI	RTCCAL
0x0D	I2C0CKH	PI2	UDESD	PRL1	RMTDATA	RTCALARM
0x0E	I2C0CKL	PD2	UDESC	SMD2	RMTERR	TEMPCNTL
0x0F	I2C0HSCK	TB0V	—	PR2	ADCLK	RTCWAKE
0x10	I2C0TO	PD0	AESC	SMD3	RMTTMP2	TEMP
0x11	I2C0FIFO	PD1	CRCNT	PRL3	FIRLEN	TEMPALRM
0x12	SPICF	TB0R	CRC1	DEMTHR0	SDLY	TCAB
0x13	SPICK	TB0C	CRC2	DEMTR1	VDLY	TCCD
0x14	SYSCN	TB1V	—	DEMINT	VZERO	WAKEFROM
0x15	—	TB1R	—	SCON4	RTM0	RTCCONT
0x16	—	TB1C	—	SBUF4	RTM1	TMPPEEK1
0x17	—	TB2V	—	SMD4	RTM2	TMPPEEK2
0x18	ICDT0	TB2R	—	PRL4	RTM3	TMPPEEK3
0x19	ICDT1	TB2C	—	ADCN	RMTTMP	TMPPEEK4
0x1A	ICDC	TB3V	—	ADST	RMTCTL0	LCDMAP0
0x1B	ICDF	TB3R	—	ADDATA	RMTCTL1	LCDMAP0
0x1C	ICDB	TB3C	—	—	RMTCTL2	LCDMAP1
0x1D	ICDA	TB4V	—	—	RMTCTL3	
0x1E	ICDD	TB4R	FCNTL	TM2	RMTSTA	LCDMO
0x1F	TM	TB4C	FDATA	TM3	RMTRG	LCDCTL

Memory Organization and Addressing

The MAXQ30 MPU core implements a machine with Harvard architecture. As such, it has separate code and data memory spaces. In the MAXQ30 MPU core, each memory space is 32MB in length. When accessed as code, memory is organized as 16MB x 16 bits; when accessed as data, the memory space can appear as 32MB x 8, 16MB x 16, or 8MB x 32.

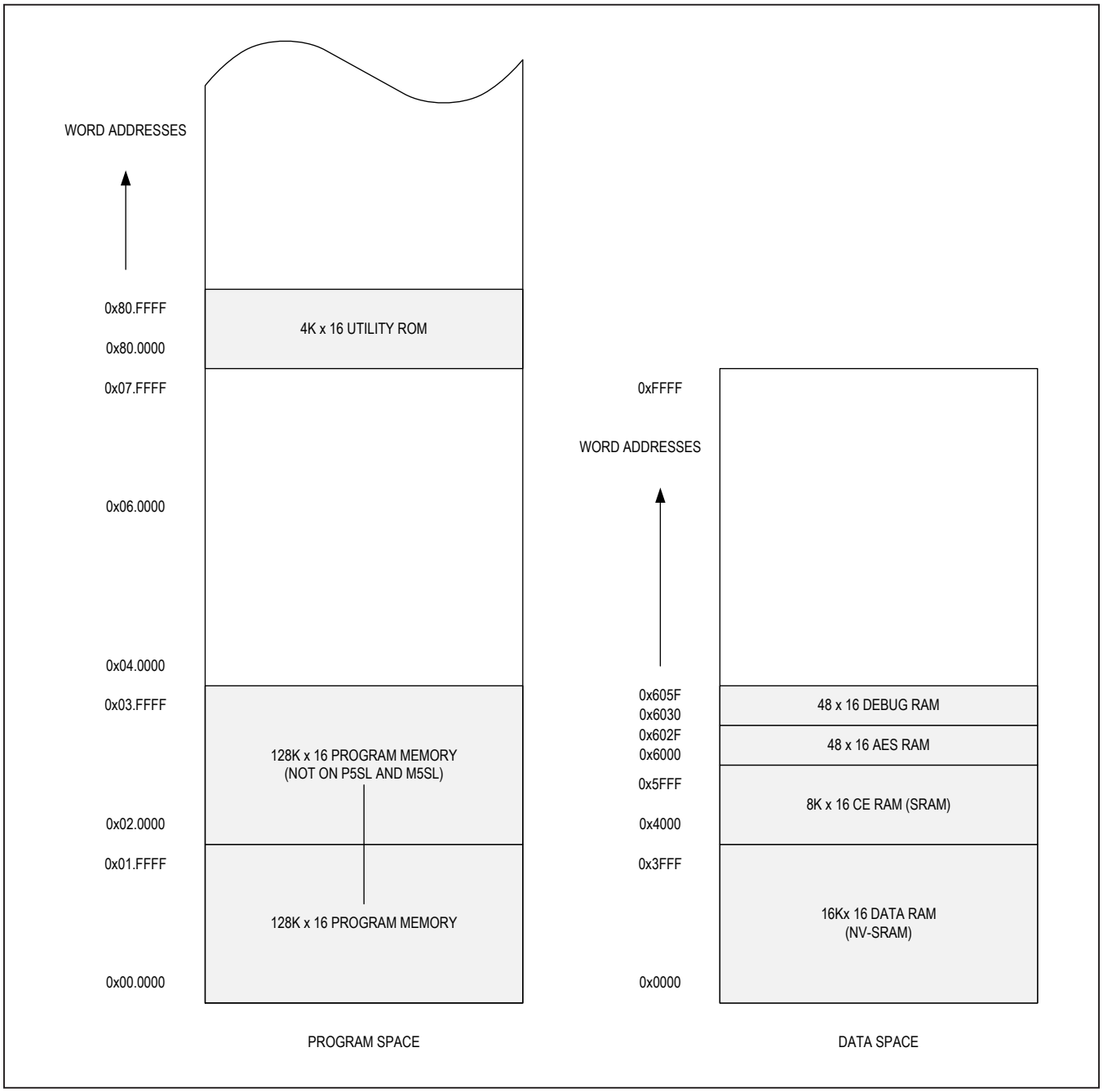


Figure 3. Memory Map

I/O is typically performed through the use of registers. Each register can be up to 32 bits in length. Registers are first-class data objects, so peripheral objects can take part in ALU transactions, be tested for values, or any other operation that a MPU register can do in other architectures.

Debug Support

Debugging in the MAXQ30 environment is a joint operation between the hardware and firmware.

The MAXQ30 MPU core has an integrated debugger that allows real-time debugging of the code running on the MAXQ30 MPU core. The debugger contains a hardware component that connects to the JTAG port, and a software component that is contained in the utility ROM. The debugger supports single-stepping, multiple breakpoints, register inspection and modification, RAM dump and modify, and other functions. The debugger is tightly integrated with the JTAG module so that software running on a host computer can control all aspects of system execution.

When a breakpoint is encountered, or when a single-step is executed the MAXQ30 MPU core pushes the current context to the stack and branches to 0x80 0010. This address is in the utility ROM, and the code there communicates with the debug host over the JTAG port. Commands supported by the debug code in the utility ROM include dump memory, modify RAM, read and modify registers, set, clear and inspect breakpoints and other commands. When the RUN command is executed, the code restores the context of the running program and returns.

The details of the communications protocols between the debug host and the MAXQ30 MPU core are typically handled by the provided debug drivers.

Interrupts and Exceptions

The MAXQ30 MPU core supports multiple interrupts that transfer control to fixed vectors. Those vectors reside in the base page of memory, at the locations in Table 4.

Table 3. Memory Map

START ADDRESS	END ADDRESS	NAME	DESCRIPTION
CODE SPACE (WORD ADDRESSES)			
0x00 0000	0x01 FFFF	FLASH	128K x 16 flash program memory (ZON P5S/P5SL and M5S/M5SL)
0x02 0000	0x03 FFFF	FLASH	128K x 16 flash program memory (ZON P5S and M5S)
0x80 0000	0x80 FFFF	UROM	4K x 16 utility ROM
DATA SPACE (WORD ADDRESSES)			
0x00000	0x03FFF	DRAM	16K x 16 static, nonvolatile RAM for MAXQ30 MPU data. The CE has no access to this area.
0x04000	0x05FFF	CERAM	8K x 16 memory for CE data and code. This area is accessible to the MAXQ30 MPU core. MPU location 0x04 0000 is mapped to CE address 0x0000, MPU location 0x05 FFFF is mapped to CE address 0x02 FFFF.
0x06000	0x0602F	DBRAM	48 x 16 AES RAM
0x06030	0x0605F	DBRAM	48 x 16 MAXQ30 debug RAM

Table 4. Exception Vectors

MPU ADDRESS	NAME	DESCRIPTION
0x00 0000	ISP	Initial supervisor stack pointer. Read by the utility ROM and used to initialize the stack pointer before branch to the user memory.
0x00 0004	IPC	Initial program counter. Read by the utility ROM and contains the MAIN entry point for user code.
0x000008	PF	Power-fail warning. Activated when V_{3P3A} falls below the power-fail threshold.
0x00 0010	EI	External interrupts. Activated when any enabled external interrupt pin becomes active. Software in the interrupt service routine must poll the available interrupt sources to determine which of the external interrupt sources caused the interrupt.
0x000018	CE	Compute engine. Activated to alert the MAXQ30 MPU core when the Compute Engine has completed an accumulation cycle.
0x000020	I^2C	I^2C. Activated when the I^2C peripheral detects an event: START completed, STOP completed, transmit buffer empty, receive character available or timeout fault.
0x000028	SPI	SPI. Activated when the SPI peripheral has clocked in/out one character.
0x00 0030	UART	UART. Activated when the UART has an exception condition: receive character available, transmit buffer empty, parity fault or framing error.
0x000038	ISO0	ISO UART 0. Activated whenever an exception condition is detected on the ISO7816 UART channel 0.
0x00 0040	ISO1	ISO UART 1. Activated whenever an exception condition is detected on the ISO7816 UART channel 1.
0x000048	WDT	Watchdog timer. Activated when the watchdog timer is about to reset the device. This interrupt provides the MAXQ30 an opportunity to either reset the watchdog timer or to save status before the watchdog resets the core.
0x00 0050	TB	Timer B. Activated when an interrupt condition occurs on the general timer B channel. Interrupts can be an expiration of the timer or can indicate that a measurement is complete in pulse-width measurement mode.
0x000058	TRIM	Trim check
0x00 0060	RTC	Real-time clock. Activated when any interrupt source in the RTC block is activated, including alarm, voltage status, or temperature range.
0x000068	—	Demod
0x00 0070	—	RTC
0x000078	—	Security functions (AES/DES encryption)
0x00 0080	—	Remote interrupt
0x000088	TRAP	General interrupt trap. Activated whenever an interrupt not covered by any other condition occurs.

Flash Memory

The ZON P5S/P5SL and M5S/M5SL SoCs contain 256/512KB of on-chip flash memory that serves as program store for the MAXQ30 MPU core. The use of flash memory as program store allows the firmware to be easily updated. The utility ROM performs all flash write and erase operations.

Because the MAXQ30 MPU core is based on the Harvard architecture, the core cannot access as data the memory block from which it is executing. That means that user code executing in flash space cannot directly access data stored in flash memory. However, facilities are provided in the utility ROM to access data stored in flash memory.

When execution is transferred from one memory block to another, (e.g., when a call is made from a program running in flash space to a function in the utility ROM), the MAXQ30 MPU core automatically remaps the data space so that the memory block being used as code space does not appear as data space.

The sequence for accessing data stored in flash memory is this:

- Place the address of the data to be read in a data pointer register.
- Call a routine in the utility ROM to read the memory from flash (utility ROM can do this since utility ROM and flash are separate memory blocks).
- The utility ROM routine reads the memory location the data pointer designates.
- The routine returns. The flash data is available in the accumulator.

Additionally, a program running in flash space can write a code sequence to data RAM, branch to the routine in data RAM, and that code can access flash since RAM and flash are separate memory blocks. Table 5 shows where the various memory spaces appear in code space and data space.

A scramble feature for the flash contents is available. Typically, an individual descramble key is programmed into the info-block of the SoC for a series of SoCs (e.g., a certain meter model) and then locked against modification. The binary code for this meter is post-processed by the meter manufacturer with the corresponding scramble key after compilation. Since the code does not properly operate on generic parts that are not equipped with the matching descramble key, code copied from a protected meter cannot be reused in generic parts.

Utility ROM

The ZON P5S/P5SL and M5S/M5SL SoCs contain an 8KB ROM organized as 4k x 16 that serves as utility ROM. This block of memory resides at 0x80 0000 in code space. The utility ROM manages the following functions:

Boot: Execution begins from reset at the base of the utility ROM. Under normal circumstances, a jump is executed to the base of flash memory. Under special circumstances, some other code block can take the execution thread (boot loader, debug, etc.).

Debug: The utility ROM contains routines that assist the built-in hardware debugger to communicate with ICE software on a PC.

Bootloader: The bootloader provides in-system programming facilities. Integrated debug environment software with the appropriate drivers can invoke the bootloader directly to write code blocks to the flash memory.

Utility functions: Functions such as flash programming and block moves are provided in the Utility ROM to assist user software.

Test: Functions used to perform unit test of the ZON P5S/P5SL and M5S/M5SL device are included in the utility ROM.

Table 5. Memory Spaces

WHEN RUNNING IN	AT ADDRESSES	FLASH DATA APPEARS AT	RAM APPEARS AS DATA AT	UTILITY ROM APPEARS AS DATA AT
Flash	0x00 0000–0x07 FFFF	—	0x00 0000	0x80 0000
Data RAM	0xA0 0000–0xA0 17FF	0x00 0000	—	0x80 0000
Utility ROM	0x80 0000–0x80 0FFF	0x80 0000	0x00 0000	—

Boot Sequence

At power-up, the MAXQ30 MPU core begins executing the utility ROM boot code at location 0x80 0000. Broadly, the device performs the following actions before branching to user code:

- Determine if the loader has requested control. The loader is invoked by setting a bit in a register through the JTAG interface. If this bit is set, the Utility ROM does not jump to user code, but begins running the loader.
- If the loader is not to be invoked, the utility ROM reads the 32-bit value at byte address 0x00 0000 and loads this value into the stack pointer.
- The utility ROM then reads the 32-bit value at byte address 0x00 0004 and loads that value into the PC register, effectively performing a jump to the address.

User code must contain code at addresses 0x00 0000 and 0x00 0004 that corresponds to the desired stack location and the main entry point, respectively.

Binary Loader

The utility ROM includes a binary loader module that can be used to load, verify, dump and erase the code image in flash memory. In general, it is unnecessary for a developer to directly interact with the loader. Development software and associated drivers communicate directly with the loader and provide a simplified interface to the developer.

Details on the loader commands and on the utility ROM in general can be found in the P5S HRM (Hardware Reference Manual).

RAM

MAXQ30 RAM

The MAXQ30 MPU core can access a total of 24KB x 16 of RAM (not including the 96 bytes of RAM dedicated for the debug function). Of this total, 16KB x 16 are dedicated to the MAXQ30 MPU core for its internal operation. This RAM block is configured as nonvolatile memory and is maintained in the absence of primary power by the nonvolatile power supply. The other 8KB block is dedicated for both CE code and data RAM and can be accessed at will by the CE and the MAXQ30 MPU core through interleaved access. It is not backed by the nonvolatile supply and loses its contents when primary power is removed.

Internal data memory starts at address 0x00 0000 in data space and is contiguous through 0x00 3FFF (word addresses). It is implemented as static RAM, and all accesses to internal memory require only one clock cycle.

Data memory mapping and access control are handled by a memory management unit (MMU). The MMU is responsible for mapping the data memory at the appropriate place in code or data space. When accessed as data, the data RAM can be written and read as bytes, words, or long words.

Shared RAM

One RAM block is shared between the MAXQ30 MPU core and the CE. The 16KB block mapped to MAXQ30 data space from addresses 0x4000 to 0x5FFF is also mapped as CE code/data RAM at word addresses 0x0000 to 0x1FFF.

Access to shared RAM is interleaved between the MAXQ30 MPU core and the CE. From a programmer's perspective, it appears that each core has exclusive access to the memory: memory access by one core does not cause wait states to be added to execution in the other core. Programmers must take care that write operations to the shared memory by one core do not adversely impact ongoing computations in the other core.

Power System

Power Sources

The ZON P5S/P5SL and M5S/M5SL SoCs require a single 3.3V supply for operation. In most cases, two battery supplies are attached to the device as well: a battery that provides operational power when primary power fails, and a second battery that maintains internal RAM and clock facilities.

Operational Modes

The ZON P5S/P5SL and M5S/M5SL SoCs support four operational modes:

Mission mode (MSN): The device is in MSN mode when the primary power supply is in specification. Primary power is supplied through the V_{3P3SYS} and V_{3P3A} pins. Comparators on the V_{3P3SYS} pin monitor the voltage level on the supply. If the level falls below a set threshold, the part automatically switches to BRN mode.

Brownout mode (BRN): In brownout mode, main power for the I/O and other circuits is automatically switched to the V_{BAT} input. The metrology blocks are effectively turned off. In BRN mode, the MAXQ30 MPU core continues to operate at full speed until firmware can switch to another mode such as LCD or SLP mode.

LCD only mode (LCD): In this mode the MAXQ30 MPU core is halted and the LCD operates independently from software control. The LCD can take its power from either V_{BAT}, the V_{LCD5} pin (from an external source such as a charge pump) or from an external V_{LCD} supply, depending on the LCD configuration.

Sleep mode (SLP): This mode shuts down all logic blocks except the RTC, the 32kHz oscillator, and nonvolatile memory blocks.

There are ten pins that are used to provide power or to provide a bypass point for internal power nodes:

V_{3P3A}: This is the primary analog power input for the device. It provides power to the ADC blocks, the voltage comparator blocks, and the bandgap voltage reference and its output buffer. This block is not directly backed up by any on chip battery.

V_{3P3SYS}: This is the primary digital power input for the device. It is typically connected to the same supply as V_{3P3A}, but separately bypassed.

V_{BAT}: This is the primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.

V_{3P3D}: The output from an internal switch that selects either V_{3P3SYS} (if the primary supply is above threshold) or V_{BAT} (if the primary supply is below threshold). It should always be bypassed, but can also be used to provide power to low-power external devices, such as serial memory, during brownout conditions.

V_{LCD}: Usually, this is a bypass point for the LCD supply. Frequently, the supply is the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply directly. This pin can also be used as an input to provide an external V_{LCD}.

V_{LCD5}: An input from a charge pump if operation with 5V-compatible LCD glass is desired. In one LCD mode, a square wave is available to drive a charge pump so that only an external RC circuit and two diodes are required to provide a 5V supply.

V_{BAT_RTC}: This pin provides the RTC and nonvolatile memory backup power. It is frequently connected to a lithium battery to maintain the RTC and NV memory elements.

V_{3P3_RTC}: This is the bypass for the nonvolatile power bus.

V_{DDCAL}: This is the bypass point for the internal calibration power bus.

V_{DD}: This is the bypass point for the internal logic supply voltage.

Power Status Register

The power status that the device finds itself in is reflected in the VSTAT field of the RTCI register.

VSTAT: This field reflects the current status of the supply voltage level comparators.

When the value of VSTAT changes, the RTC_I_VS bit is set. If the RTC_M_VS bit is also set (and interrupts are enabled globally), the MPU is interrupted. In this way, the MPU is notified both when power is failing and when power is restored.

Clock System

ZON P5S/P5SL and M5S/M5SL are normally clocked by an external 32,768Hz watch crystal that serves as the sole time base for the device. An internal PLL multiplies the reference frequency by 3600 to generate the 117.9648MHz master clock. A prescaler with multiple taps is used to generate the clock for the various on-chip peripherals and subsystems.

The device includes internal backup oscillators. A failure detection block ensures that, upon loss of the 32kHz crystal, two internal oscillators provide the device a backup clock:

- The 24MHz oscillator is trimmed and its design ensures stability over temperature.
- The 32kHz oscillator. This oscillator ensures continued operation of the RTC (at lower accuracy) and of all circuits depending on the 32kHz frequency.

Table 6. VSTAT Values

VSTAT VALUE	MEANING
0b00000	Power is good, all systems can function.
0b00001	Metrology is inaccurate, but all digital functions can operate. V_{3AOK} status bit is active.
0b00011	Low-power warning. Power supply is below detection threshold, but digital operation is still reliable. Code should begin taking steps to conserve power. V_{3OK} and V_{3AOK} status bits are active.
0b00111	Final power warning to MAXQ30 MPU. The V_{DD} regulator is at the limit of regulation and regulated power will begin to sag from this point. The MAXQ30 MPU must set the SLP bit shortly. No flash memory writes from this point. V_{3AOK}, V_{3OK}, and V_{3P3DOK} status bits are active.
0b01111	V_{DD} out of range. The MAXQ30 MPU never sees this value. The power management system declares BADVDD if this state is reached before the MAXQ30 MPU sets the SLP mode. V_{3AOK}, V_{3OK}, V_{3P3DOK}, and V_{DDOK} status bits are active.

The SoC starts up with the 24MHz oscillator. Once the PLL driven by the 32kHz oscillator is stabilized all internal clocks are derived from the 117.9648MHz master clock. If the 32kHz oscillator does not start up, the internal 24MHz oscillator stays active.

The clock rate for the MAXQ30 MPU core and the peripherals is selectable through the CD field in the CKCN register. Table 7 shows the selectable clock rates.

An additional stop mode for the MAXQ30 code and associated peripherals in also featured. By setting the STOP bit in the CKCN register, the MAXQ30 clock is halted. The normal operation can be resumed upon a power-on or reset. The STOP mode can be exited utilizing digital I/O properly configured.

The CE operates at a fixed clock rate of 1/6 of the PLL master clock or 19,660,800Hz. The main ADC clock setting is selectable through the ADCLK register. Table 8 shows the selectable clock rates.

On-Chip Resources

Timers

The ZON P5S/P5SL and M5S/M5SL SoCs contain five timer channels. Each timer channel is a MAXQ30 type B timer, which is an advanced timer design that can be configured as a counter, timer or PWM modulator, and can perform capture and compare functions. The timers can be used for general timing, pulse generation, time measurement, pulse width modulation, pulse timing, and more. Inside the timer logic, multiple sources can be selected to generate an interrupt to the MAXQ30 MPU core.

The timers have the following features:

MPU interrupts: the timers can interrupt the MPU on overflow or when the timer matches some preset value.

Pulse measurement: the timers can be triggered by an external pulse.

Pulse-width modulation: The timers can be used to generate a PWM signal with selectable characteristics.

Counters: The timers can be configured to count the number of external pulse edges.

When configured as timers, the clocks are derived from the system clock. A prescaler system allows the system clock to be scaled by up to 1,024 before being used as the timer clock.

The timers can be operated in autoreload mode, capture mode, or up/down count autoreload mode. They can also have a PWM output function where the output signal is provided to the P1.16 and P1.17 pins that can be configured for PWM output. For the PWM mode, the submodes RESET, SET, and TOGGLE are available.

UARTs

The ZON P5S/P5SL and M5S/M5SL SoCs contain seven UART channels. All channels are directly controlled by the MAXQ30 MPU core and feature independent baud rate generators. These baud rate generators are independent from any timer, and are independent from each other.

UART0 is unique in that it contains an option to modulate its output with a high-frequency carrier (nominally 38kHz) and contains a photodiode amplifier and detector that allows the channel to sense high-frequency carrier and demodulate serial data contained on the carrier.

Each UART features:

- Double-buffered transmitter and receiver
- Odd, even, or no parity
- 1, 1½, or 2 stop bits
- Maskable interrupts for receive buffer full or transmit buffer empty

The UART modes of operation are summarized in Table 9.

Table 7. Selectable Clock Rates

CD[1:0] SETTING	DIVIDER SELECTION	CLOCK FREQUENCY (MHz)
00	1/6	19.6608
01	1/12	9.8304
10	1/24	4.9152
11	1/48	2.4576

Table 8. ADC Clock Selection

ADCLK[1:0] SETTING	CLOCK FREQUECNY (MHz)
00	Reserved
01	2.4576
10	4.9152
11	Reserved

Table 9. UART Modes of Operation

SM0:SM1	MODE	FUNCTION	BAUD CLOCK	LENGTH	FRAMING	9th BIT
00	0	Synchronous	4 of 12 clocks	8	None	None
01	1	Asynchronous	BRG	8	1 start, 1 stop	None
10	2	Asynchronous	32 or 64 clocks	9	1 start, 1 stop	0, 1, parity
11	3	Asynchronous	BRG	9	1 start, 1 stop	0, 1, parity

The UART has a control register (SCON) and a transmit/receive register (SBUF). The SBUF register provides access to both transmit and receive registers, where a read is directed to the receive buffer and a write is directed to the transmit buffer. There is a holding buffer that allows the UART to receive an incoming word before software has read the previous one.

LCD System

The ZON P5S/P5SL and M5S/M5SL SoCs include an LCD controller that supports up to eight common planes and up to 44 segments. You can attach bare LCD glass natively operating up to 3.3V, or with an external boost circuit, up to 5V. The LCD controller supports many operating modes, including:

- Static, with up to 44 segments
- Two common planes with up to 42 segment circuits for a total of 84 segments operating at 1/2 bias
- Three common planes with up to 41 segment circuits for a total of 123 segments operating at 1/2 or 1/3 bias
- Four common planes with up to forty segment circuits for a total of 160 segments operating at 1/3 bias
- Five common planes with up to 39 segment circuits for a total of 195 segments operating at 1/3 bias
- Six common planes with up to 38 segment circuits for a total of 228 segments operating at 1/3 bias
- Eight common planes with up to 36 segment circuits for a total of 288 segments operating at 1/3 bias

Additionally, the LCD controller has test features that allow all segments to be turned on or off without disturbing LCD data, a reset feature that quickly clears all LCD data, and a built-in DAC for contrast adjustment. Two segment circuits (SEG22 and SEG23) can be configured to blink. Blinking is defined as causing any segment that is set on to alternate between the on and off states. Blinking works in any LCD mode and at either pattern frequency.

Each pin that serves as an LCD segment or common output must be configured in the LCDMAP registers. There are two such registers: LCDMAP0 and LCDMAP1. They control the assignments of segments to pins.

When a pin is configured for LCD, its alternate function is completely disabled. Alternately, if a pin is configured for an alternate function (such as GPIO or a peripheral function), the contents of the LCD data register associated with that segment have no effect.

The LCD data is accessed through an indirect register mechanism. Two registers are used: the LCDINDADDR register is used to point to a particular LCD data element, and the LCDINDDATA register is used to access the data element for read or write. Each LCD data element is 32 bits wide, and represents the eight possible backplane assignments for four of the LCD segment pins. Because there are 44 possible segment pins and up to eight time slots, there are 44 bytes of LCD data arranged as eleven 32-bit words.

Table 10. UART Modes of Operation

ELEMENT	PIN NUMBER MIRROR		REGISTER	BIT	ELEMENT	PIN NUMBER MIRROR		REGISTER	BIT
	0	1				0	1		
SEG0/COM0	55	127	LCDMAP1	0	SEG22	30	30	LCDMAP1	22
SEG1/COM1	54	128	LCDMAP1	1	SEG23	29	29	LCDMAP1	23
SEG2/COM2	53	1	LCDMAP1	2	SEG24	20	20	LCDMAP1	24
SEG3/COM3	52	2	LCDMAP1	3	SEG25	19	19	LCDMAP1	25
SEG4/COM4	51	3	LCDMAP1	4	SEG26	14	14	LCDMAP1	26
SEG5/COM5	50	4	LCDMAP1	5	SEG27	13	13	LCDMAP1	27
SEG6/COM6	49	5	LCDMAP1	6	SEG28	12	12	LCDMAP1	28
SEG7/COM7	48	6	LCDMAP1	7	SEG29	11	11	LCDMAP1	29
SEG8	47	47	LCDMAP1	8	SEG30	10	10	LCDMAP1	30
SEG9	46	46	LCDMAP1	9	SEG31	9	9	LCDMAP1	31
SEG10	45	45	LCDMAP1	10	SEG32	8	8	LCDMAP0	0
SEG11	44	44	LCDMAP1	11	SEG33	7	7	LCDMAP0	1
SEG12	42	42	LCDMAP1	12	SEG34	6	6	LCDMAP0	2
SEG13	41	41	LCDMAP1	13	SEG35	5	5	LCDMAP0	3
SEG14	40	40	LCDMAP1	14	SEG36	4	4	LCDMAP0	4
SEG15	39	39	LCDMAP1	15	SEG37	3	3	LCDMAP0	5
SEG16	38	38	LCDMAP1	16	SEG38	2	2	LCDMAP0	6
SEG17	36	36	LCDMAP1	17	SEG39	1	1	LCDMAP0	7
SEG18	35	35	LCDMAP1	18	SEG40	128	128	LCDMAP0	8
SEG19	33	33	LCDMAP1	19	SEG41	127	127	LCDMAP0	9
SEG20	32	32	LCDMAP1	20	SEG42	57	57	LCDMAP0	10
SEG21	31	31	LCDMAP1	21	SEG43	56	56	LCDMAP0	11

Table 11. LCD Control

LCDINDADDR	BYTE 3 (MSB)	BYTE 2	BYTE 1	BYTE 0 (LSB)
0	SEG0	SEG1	SEG2	SEG3
1	SEG4	SEG5	SEG6	SEG7
2	SEG8	SEG9	SEG10	SEG11
3	SEG12	SEG13	SEG14	SEG15
4	SEG16	SEG17	SEG18	SEG19
5	SEG20	SEG21	SEG22	SEG23
6	SEG24	SEG25	SEG26	SEG27
7	SEG28	SEG29	SEG30	SEG31
8	SEG32	SEG33	SEG34	SEG35
9	SEG36	SEG37	SEG38	SEG39
10	SEG40	SEG41	SEG42	SEG43

For example, to set the state of SEG0, the MPU writes 0x00 to LCDINDADDR and then writes bits 31:24 of LCDINDDATA. Each bit of the SEGxx field controls the state of the SEG pin relative to one of the eight common planes according to Table 12.

For segment pins not configured for LCD output (LCDMAP = 0) the indirect data in the SEGxx field configures the pin for digital I/O. You can use the LCDINDDATA bits to directly control the I/O state of the pins, or software can set SEGxx for pins that are not being used for the LCD display to 0x04. This defers control of the pin to the I/O logic of the MAXQ30 MPU core.

For example, pin 38 is configurable as LCD segment 16, GPIO0.16, or MISO for the SPI port. If the LCDMAP bit for this pin is set, then the LCD function is selected and neither the MAXQ GPIO nor the SPI peripheral can affect the state of the pin. If the LCDMAP bit for this pin is clear, then the pin is configured according to bits 2:0 of the SEGxx field in the LCDINDDATA RAM array. If bit 2 of the SEGxx field is set, then control of the pin is passed to the MAXQ30 port logic. In this case, if the SPI peripheral is enabled the pin serves as SPI MISO; if the SPI peripheral is disabled, then MAXQ30 GPIO logic controls the pin.

The LCD controller can operate in any one of eight multiplex and bias modes, as controlled by the LCD_MODE field.

The final factor to be considered when configuring the LCD waveforms is the LCD clock frequency. In general, you should choose the lowest frequency that gives good results with your chosen LCD glass: the power consumption of an LCD system is almost directly proportional to the operating frequency. The scan frequency is selected by the LCD_CLK field in the LCDMODE register.

By default, the LCD_CLK field is set to 64Hz, which is sufficient for most applications. For some displays, in particular, displays with high multiplex rates (eight-way multiplexing, for example), a higher clock frequency might be necessary.

The LCD voltage (V_{LCD}) is critical to successfully using the LCD controller. Broadly, the V_{LCD} level controls the contrast of the display.

The LCD glass has a recommended operating voltage, frequently 3V or 5V. The specified operating voltage assumes a typical set of LCD waveforms: a 3V LCD glass expects to see voltages at 0V, 1V, 2V, and 3V with

Table 12. LCD Common Control

BIT	LCDMAP = 0	LCDMAP = 1
SEGxx.7	N/A	LCD segment value relative to COM7
SEGxx.6	N/A	LCD segment value relative to COM6
SEGxx.5	N/A	LCD segment value relative to COM5
SEGxx.4	N/A	LCD segment value relative to COM4
SEGxx.3	N/A	LCD segment value relative to COM3
SEGxx.2	MAXQ30 control	LCD segment value relative to COM2
SEGxx.1	Pin direction (0 = input, 1 = output)	LCD segment value relative to COM1
SEGxx.0	Pin input or output value	LCD segment value relative to COM0

Table 13. LCD Controller Operation

LCD_MODE[2:0]	NUMBER OF STATES	BIAS
0	4	1/3
1	3	1/3
2	2	1/2
3	3	1/2
4	Static	—
5	5	1/3
6	6	1/3
7	8	1/3

Table 14. LCD Clock Selection

LCD_CLK[1:0]	LCD CLOCK FREQUENCY (Hz)
0	64
1	128
2	256
3	512

a total differential peak-to-peak voltage of 6V maximum (that is, backplane at 0V and segment at 3V, followed by backplane at 3V and segment at 0V). Four V_{LCD} sources can be selected that make use of the internal resources of the device. The selection is made by writing the LCD_VMODE field in the LCDMODE register. Here are the available choices:

LCD_VMODE = 0b00 (V_{LCD} = 3.3V): In this mode, V_{LCD} is connected to V_{3P3SYS} in MSN mode and to V_{BAT} in LCD only mode. The LCD DAC is bypassed, meaning there is no contrast adjustment available.

LCD_VMODE = 0b01 (V_{LCD} from LCD DAC): In mode 1, V_{LCD} is the output of the LCD DAC. The input of the LCD DAC is V_{3P3SYS} in MSN mode and V_{BAT} in LCD ONLY mode. The DAC scales its input based on the digital code written to the LCD_DAC field of the LCDCTL register. Generally, V_{DACOUT} = V_{DACIN} x (LCD_DAC[4:0]/31). User software can configure the contrast of the display be writing a value to the LCD_DAC register.

LCD_VMODE = 0b10 (V_{LCD} boost): In mode 2, V_{LCD} is once again the output of the LCD DAC, but the input of the LCD DAC is taken from the V_{LCD5} pin. The V_{LCD5} pin is typically sourced from an external charge pump. The device provides a pin that supplies a continuous square wave at 32kHz. The V_{SQW} pin is enabled by setting the V_SQ_EN bit in the LCDCTL register. Using this circuit, the device can use 5V as well as 3V glass.

LCD_VMODE = 0b11 (V_{LCD} external): In this final mode, V_{LCD} is disconnected from any internal source. The V_{LCD} pin is connected directly to the LCD waveform generator. This allows the application circuit to generate its own V_{LCD} voltage and provide it to the waveform generator. In this mode, it is the responsibility of external circuitry to regulate the LCD voltage for optimum LCD contrast.

In addition to blinking, the LCD display can be configured to display two different sets of information sequentially, alternating between the two sets without intervention of the MAXQ30 MPU core.

There are two pages of eleven 32-bit words that make up the data storage for the LCD controller. By default, only the first of these two pages is used. But by setting the PAGE_RW bit in the LCDCTL register all subsequent reads and writes to the LCDINDDATA register will go to the second of the data pages.

User software, then, can write data for display to the main page of the LCD controller, and while the LCD controller is using that page for display, user software can write data to the second page of the LCD controller. When ready, user software can write a 1 to the PAGE_SET bit in the LCDCTL register to cause the LCD controller to begin displaying data from the second page. While the second page is being displayed, the main page can be updated; when ready, the main page can be brought into view by clearing the PAGE_SET bit.

To automatically switch between the main and secondary pages, set the PAGE_TIME bit in the LCDCTL register. Now, the display alternates between the main and secondary pages at a time determined by the PAGE_TIME_SET field in the LCDCTL register. No further intervention by the MAXQ30 MPU core is required until data on one or the other pages needs to be updated.

By default, the pages alternate between the main and secondary pages at four seconds per page. Other rates can be selected by setting the PAGE_TIME_SET field in the LCDCTL register.

Bits in the LCDMODE register support the following special LCD modes:

- When the LCD_ON bit is set in the LCDMODE register, all segments are unconditionally turned on. Note that this setting does not disturb the information in the LCD data registers. Software can set this bit to test segments and then clear it to restore the previous display.
- When the LCD_OFF bit is set in the LCDMODE register, all segments are unconditionally turned off. Note that this setting does not disturb the information in the LCD data registers. Software can set this bit to test segments and then clear it to restore the previous display.
- Setting the LCD_RST bit in the LCDMODE register clears all data from the LCD controller—all segment data and all configuration information. All pins are returned to their alternate functions. The LCD_RST bit itself is cleared automatically.

A quick way to configure all of the segment pins that can also be configured as common pins is to configure the segments in LCDMAP0/1 and then set the LCD_ALLCOM bit in the LCDMODE register. All eight pins, if they are configured for LCD use in LCDMAP, are assigned as common pins. Common pins that are not used in the current multiplex scheme (as defined in LCD_MODE) receive an idle signal.

Table 15. LCD Page Timing Control

PAGE_TIME_SET[1:0]	HOLD TIME (s)
0	4
1	8
2	16
3	32

To make PCB routing easier, it is possible to mirror some of the pins associated with the LCD controller to the opposite side of the chip. If pin 1 is at the northwest corner of the MAX71335S/MAX71336S, then the common circuits emerge on the south side. This may or may not be a convenient location. By setting the MIRROR bit in the LCDCTL register, those pins are swapped with LCD segment pins on the north side of the chip.

Optical UART

The ZON P5S/P5SL and M5S/M5SL SoCs contain an optical interface module that can be assigned to UART0. When engaged, the transmit data from the UART is modulated with a carrier frequency (usually 38kHz, but configurable) and receive data is taken from an optical demodulator module.

On the receive side, a PIN photodiode amplifier can be connected to the OPT_RX input at pin 75 and a demodulator can be inserted into the receive data path.

Optical Modulator

The optical modulator is available on UART0. If enabled, the output of timer 0 is logically summed with the UART transmit data output before being presented to the transmit data pin.

The modulator is enabled by setting the EIR bit in the SMD0 register. When this bit is set, a SPACE condition is represented as a modulated output, and a MARK condition can be a logic-low or logic-high, depending on the setting of the OFS bit in the SMD0 register.

In virtually all IR transmitter configurations, the desire is to modulate the output during SPACE and to emit no IR during a MARK condition. This is because that traditional asynchronous communications idles in a MARK condition, and it is desirable to emit no radiation in the idle state. Consequently, all IR modes transmit IR during a SPACE condition.

OFS = 1 should be used for connecting an LED directly to the port pin. In this configuration, the cathode of the LED is connected to the port pin and the anode of the LED to 3.3V through an appropriate current limiting resistor. Since the current sink capability of the port pin is sufficient to drive high-efficiency IRED devices this is the least expensive way to implement the IR transmitter.

If more output power is required, an NPN driver can be used to buffer the port output. In this case, the OFS register is set to 0 and the base of an NPN transistor is driven from the port pin. The LED is in the collector circuit, again with the appropriate current limiting resistor.

Timer channel 0 controls the modulation frequency. Software must configure the timer to operate at twice the expected modulation frequency since the timer output is squared by one additional flip-flop stage.

Table 16. Optical Modular Control

UART OUTPUT	EIR	OFS	PIN OUTPUT
0	0	X	0
1	0	X	1
0	1	0	Modulated
1	1	0	1
0	1	1	Modulated
1	1	1	0

Optical Demodulator

The optical demodulator uses the multiplexer, the modulator and decimator blocks of the auxiliary ADC. When the optical demodulator is active, the auxiliary ADC is unavailable. The optical receive input is selected by setting the AUX_ADC_SEL bits in the LCDCTL register to 3 and by clearing the DEM_AUX_B bit.

The signal from the auxiliary ADC is first decimated, and the decimator output is mixed with a local oscillator operating at 38kHz. The correlation output of the mixer is then filtered and passed to a discriminator with variable hysteresis limits. The output of the discriminator is then passed to UART0. UART0 can also be supplied directly from the RX0 pin by setting DEMOD_DIS bit to 1. See the description of the auxiliary ADC for details.

I^2C Interface

The ZON P5S/P5SL and M5S/M5SL SoCs include an I^2C peripheral that can act as an I^2C master or slave.

The I^2C bus is a bidirectional two-wire serial bus interface. It has the following characteristics:

- Information is transferred over a serial data circuit (SDA) and serial clock circuit (SCL)
- The peripheral can operate in either a master mode or a slave mode
- The peripheral supports either standard (7-bit) addressing or extended (10-bit) addressing
- The peripheral operates in three modes to support multiple transfer rates
- Standard mode: 100kbps
- Fast mode: 400kbps
- Fast mode plus: 1Mbps
- The peripheral contains an on-chip filter to reject spikes on the data circuit.

- The I2C port of the device offers the following features:
  - Single-master, multimaster, or slave operation
  - Clock stretching
  - Timeout detection
  - Separate transmit FIFO (TX_FIFO) and receive FIFO (RX_FIFO) with selectable thresholds
  - Automatic response to general call address (0000 0000) used for broadcasting
  - Interactive receive mode
  - Direct control of SCL and SDA signals
  - Interrupt on errors

SPI Port

The serial peripheral interface (SPI) provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface provides access to a four-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is up to the system reference clock frequency for master mode. For slave mode, the maximum frequency is a function on the I/O driver, character length, and the system clock.

The main element in the SPI module is the block containing the shift register, the transmit FIFO and the receive FIFO. The shift register is double buffered and serves as temporary data storage. The receive FIFO holds received data from the network. The transmit FIFO contains data ready to be transmitted out.

The SPIB SFR provides access for both transmit and receive data. Reads are directed to the read FIFO. Writes are directed to the shift register automatically if the transmit FIFO is empty; otherwise, write operations store data into the transmit FIFO.

The four interface signals used by the SPI are:

MISO: Master in/slave out. This signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most significant bit first. The slave device places the MISO pin in an input state with a weak pullup when it is not selected.

MOSI: Master out /slave in. This signal is an output from a master device and an input to the slave devices. It is used to serially transfer data from the master to the selected slave. Data is transferred most significant bit first.

SCLK: SPI clock. This serial clock is an output from the master device and an input to the slave devices. It is used to synchronize the transfer of data between the master and the slave on the data bus.

SSEL: Slave select. The slave select signal enables a SPI slave when activated by a master device. The slave can be configured to select the active state of SSEL. When the master asserts SSEL it is signaling the beginning of an SPI transfer. SSEL should remain asserted for the duration of the transfer. Normally, this signal has no function in master mode and its port pin can be used as a general purpose I/O. However, the SSEL can optionally be used as a mode fault detection in master mode.

The SPI peripheral is enabled by setting the SPI enable bit (SPIEN in the SPICN register). The master mode bit (MSTM in the SPICN register) selects the operating mode, either master or slave, and the source of the SCLK signal.

The slave select SSEL input of a slave device must be externally asserted by a master before the master device can exchange data with the slave device. The active state of SSEL is determined by the slave active select bit (SAS in the SPICF register). If SAS is cleared, SSEL is active low and must be held low for the duration of the transaction. If SAS is set, SSEL is active high and must be held high for the duration of the transaction. De-asserting the SSEL signal during a transfer cycle aborts the transaction.

The SPI transfer format is determined by the SPI clock polarity bit (CKPOL) and the clock phase bit (CKPHA). CKPOL selects an active polarity of SCLK. CKPHA selects which edge of the clock – the leading or trailing edge – is used to clock data into the shift register. Together, the clock polarity bit and the clock phase bit provide the flexibility for direct interfacing of most existing synchronous serial peripheral devices.

The SPI specification describes four data transfer modes:

Mode 0 (CKPOL = 0, CKPHA = 0): The SCLK circuit idles in the low state. Data is transferred on the leading edge of the clock (the rising edge.) Data is allowed to change on the falling edge of the clock (the trailing edge). Since the first clock edge transfers data, data must be set up prior to the first clock edge (typically coincident with the assertion of the SSEL signal).

Mode 1 (CKPOL = 0, CKPHA = 1): The SCLK circuit idles in the low state. Data is transferred on the trailing edge of the clock (the falling edge.) Data is allowed to change on the rising edge of the clock (the leading edge). Since the first clock edge does not transfer data, data can be set up on the leading edge of the clock.

Mode 2 (CKPOL = 1, CKPHA = 0): The SCLK circuit idles in the high state. Data is transferred on the leading edge of the clock (the falling edge). Data is allowed to change on the rising edge of the clock (the trailing edge). Since the first clock edge transfers data, data must be set up prior to the first clock edge (typically coincident with the assertion of the SSEL signal).

Mode 3 (CKPOL = 1, CKPHA = 1): The SCLK circuit idles in the high state. Data is transferred on the trailing edge of the clock (the rising edge). Data is allowed to change on the falling edge of the clock (the leading edge). Since the first clock edge does not transfer data, data can be set up on the leading edge of the clock.

Note that it is not advisable to change the SPI operation mode or configuration when the SPI peripheral is in operation. Software should disable the SPI peripheral (clear SPIEN) before changing the mode of operation (CKPOL, CKPHA, CHR, MSTM, and SAS). Unpredictable behavior results if the SPI operation mode is changed while the SPI peripheral is enabled.

Set the SPI peripheral in master mode when the microcontroller needs to manage an external peripheral or memory device. The master establishes the transfer rules and the transfer rate.

Only an SPI master device can initiate a data transfer. Master transfer starts when the SPI master writes to SPI buffer register (SPIB). The SPI master immediately shifts out the data serially on the MOSI pin, most significant bit first, while driving the serial clock on SCLK. New data is simultaneously gated in on the MISO pin into the least significant bit of the shift register.

The data transfer rate for the network is determined by the divider ratio set in the SPI clock register (SPICK).

In master mode, the SSEL pin of the master defaults to general-purpose I/O pin. However, the SSEL can be used for mode fault detection input if the mode fault enable bit (MODFE in the SPICF register) is set. When the SPI is configured as a master and the SSEL pin is used as mode fault detection input, a mode fault condition occurs if an active signal is detected on SSEL. This indicates that some other device on the network is attempting to be a master.

The active state of the SSEL pin is defined by the slave active select (SAS) bit. When MODFE is set and SAS is cleared, an active low signal on SSEL triggers a mode fault. If MODFE is set to 1 and SAS is set, an active high signal on SSEL indicates a mode fault condition. Either way, the master device senses the error and immediately disables the SPI device to avoid bus contentions.

The mode fault error is usually caused by two SPI devices attempting to function as master at the same time. In the case where more than one device is configured as master at the same time, the resulting bus contention can cause permanent damage to push-pull CMOS drivers. Mode fault error detection is provided to protect to the device by disabling the bus drivers. When a mode fault is detected, the following actions are taken immediately:

- The MSTM bit is forced to 0 to reconfigure the SPI device as a slave.
- The SPIEN bit is forced to 0 to disable the SPI device.
- The mode fault bit (MODF) status flag is set. When set, the MODF bit can generate an interrupt if the Mode Fault Interrupt Enable bit (MODFIE) is set to 1.

The application software must correct the system conflicts before resuming normal operation. The MODF flag is set automatically by hardware, but it must be cleared by software or a reset once set. Setting the MODF bit to a 1 by software causes an interrupt if enabled.

To avoid unintentional mode fault error, software should check the status of SSEL prior to enabling the SPI peripheral as master. Otherwise, if the SSEL signal is in the active state, a mode fault error occurs, disabling the SPI peripheral and clearing master mode.

Note that the mode fault mechanism does not provide full protection from bus contention for multiple master systems. For example, if two devices are configured as master at the same time, the mode fault detect circuitry does not help to protect either device driver unless one of them selects the other as slave by asserting its SSEL signal. Also, if a master activates more than one slave (due, for example, to a software fault) and those devices try to simultaneously drive their output pins, bus contention can occur without generating a mode fault error.

Select slave mode when another device is configured as the master and the role of the device is as a peripheral to another device. The SPI is in slave mode when the MSTM bit is cleared. In slave mode, the SPI controller is dependent on the SCLK sourced from the master to control the data transfer.

The slave select (SSEL) input of a slave device must be externally asserted by a master before data exchange can take place. SSEL must be asserted before the data transaction begins and must remain asserted for the duration of the transaction. If data is to be transmitted by the slave device, it must be written to its shift register before the beginning of a transfer cycle, otherwise, the character already in the slave's shift register is transferred. For the slave device, a transfer begins with the first clock edge or the active SSEL edge, dependent on the state of CKPHA.

The active edge of SSEL is determined by the slave active select bit (SAS in the SPICF register). When SAS is cleared the falling edge of SSEL edge is the active edge. If SAS is set, the rising edge of SSEL is the active edge.

The SPI master transfers data to a slave on the MOSI pin, most significant bit first, and the selected slave device simultaneously transfers the contents of its shift register to the master on the MISO pin, also most significant bit first. Data received from the master replaces data in the slave's shift register at the completion of a transfer. Just as in the master mode, received data is loaded into the receive FIFO and the SPI receive interrupt flag is set at the end of the transfer. The setting of the SPIRXI flag can cause an interrupt if enabled.

When SSEL is not asserted, the slave device ignores the SCLK clock and the shift register is disabled. In this condition, the device is idle, no data is shifted out from the shift register and no data is sampled from the MOSI pin. The MISO pin is placed in input mode with a weak pullup to allow other devices on the bus to drive the bus. Deasserting the SSEL signal by the master during a transfer indicates that the current process is aborted, and causes the slave logic and its bit counter to be reset, no data is loaded to the receive FIFO.

In slave mode, the clock divide ratio bits in the SPI clock register (SPICK) have no function. However, the transfer format and the character length selection for the slave device should match the selection of the master for proper communication.

For master mode operation, the data rate is determined by the clock divide ratio specified in the SPI clock register (SPICK). The SPI module supports 256 different clock divide ratios for serial clock generation.

For a standard system frequency of 19.6608MHz, the fastest SPI data rate is 19.6608Mbps and the slowest data rate is 19.6608MHz/(2 x 256) = 38.4kbps.

If the SPI peripheral is configured as a slave, it receives the SPI clock on the SCLK pin from the master device. The setting of the SPICK register has no effect on the data rate of the network. The maximum slave SCLK must be less than:

$$\text{Slave SCLK (max)} = L_{CHAR} \times f_{CPU}/3$$

In this equation, L_{CHAR} is the character length. If the MPU is running at the standard system frequency of 19.6608MHz, the maximum supported slave clock is 52.4288MHz for eight-bit transfers and 104.8576MHz for sixteen-bit transfers.

The character length bit (CHR in the SPICN register) specifies either a 8-bit or 16-bit data character for a transfer cycle. When CHR is clear, the character length is 8 bits; when CHR is set, the character length is 16 bits.

The FIFO depth depends on the value of CHR. The FIFO is 64 bits, so it can accommodate 8 characters of 8-bit character length before overrun (CHR = 0), or 4 characters of 16-bit character length before overrun (CHR = 1).

The SPI buffer register (SPIB) is sixteen bits wide to accommodate sixteen bit characters. When operating in eight-bit character width mode (CHR = 0) software must write to the lower eight bits and read from the lower eight bits. The upper byte is not used when CHR = 0.

At the end of a character transfer, the received data is loaded into the receive FIFO for reading by the MAXQ30 MPU core and the SPI receive interrupt (SPIRXI) is set. This generates an interrupt if the SPI Receive FIFO interrupt enable bit (SPIRXIE) is set. Software can retrieve the received character by reading from SPIB. If no more characters are available in the receive FIFO, the SPIRXI flag is automatically cleared. If there are more characters available, the SPIRXI flag remains set.

The SPI port supports the following features related to receive operation:

- Indication of the number of characters received
- FIFO half-full and full flags with interrupt generation
- FIFO overrun flag with interrupt generation
- FIFO reset function

Software writes data to be transmitted to the SPI data buffer register (SPIB). If the shift register is empty, data is written directly to the shift register. Once the shift register is busy transmitting data, additional writes to the SPIB register is transferred into the transmit FIFO.

The transmit FIFO full flag (SPITXFI) is set when the transmit FIFO is full. This generates an interrupt if the SPI transmit FIFO full interrupt enable bit (SPITXFIE) is also set. The SPITXFI flag automatically clears when data is loaded from the transmit FIFO into the shift register.

The SPI port supports the following features related to transmit operation:

- Transmit FIFO overrun flag with interrupt generation
- FIFO transmit interrupt
- FIFO empty flag with interrupt generation
- FIFO clear register

After the SPI controller loads the last data byte from the transmit FIFO to the shift register the transmit FIFO empty

flag (SPITXEI) is set. This generates an interrupt if the SPI transmit FIFO empty interrupt enable bit (SPITXEIE) is set. The SPITXEI flag is automatically cleared when the transmit FIFO is no longer empty (that is, software provides more transmit data) or by software writing 0 to the SPITXEI flag. Since the SPITXEI flag is set when the last character is loaded into the shift register, it does not indicate that the SPI buffer is empty; there is still one more character to shift out. To ensure that the SPI buffer is empty, software should monitor the SPITXI flag.

ISO UART

The ZON P5S/P5SL and M5S/M5SL SoCs contain two ISO7816 compatible UART channels for connection to a smart card interface. The ISO UART provides a bidirectional I/O circuit and a separate clock circuit. The ISO UART has the following features:

- Supports half-duplex asynchronous transmission
- Programmable baud rate
- Eight-character FIFO with parity detect/transmit
- Error management for T = 0 protocol (stream)
- Extra guard time between characters on transmit

Temperature Sensor

The device contains a temperature sensor that is characterized at the factory at +21.24°C. The value of the temperature sensor at this temperature is stored in a reserved area of the device.

The final value in the accumulator is the temperature sensor value at +21.24°C. Since the raw temperature sensor returns a value in its STEMP register that is proportional to absolute temperature, one can use this value to determine the proportionality constant for the temperature sensor.

The STEMP value is a two's complement value; values less than zero reflect temperatures below +21.24°C.

Touch Sensor Inputs

General Description

The ZON P5S/P5SL and M5S/M5SL SoCs contain two capacitive touch switch inputs. These inputs are designed to operate with a wide range of quiescent capacitance values and are generally immune from most noise sources.

As a finger approaches the touch plate, the capacitance of the touch plate increases, and the frequency decreases. In some cases, the change in capacitance (and frequency) can be as much as two orders of magnitude. Note that the touch plate itself is never actually touched. The plate is covered by a dielectric (e.g., plastic) and the finger touches only the exterior of the dielectric. This makes the switch more of a proximity switch than a touch switch.

Digital logic is used to sense the change in frequency. To do this, the touch switch oscillator is gated on for a known period of time, and the pulses from the oscillator clock a ripple counter. As the capacitance increases, the frequency of the oscillator decreases and the count recorded also decreases.

Because the system must sense the decrease in the count, a reference count is needed to determine when the frequency falls below some threshold, and so to determine when a finger is near the touch sensor. This reference count is stored in a compare register loaded by software running on the MAXQ30 MPU core. A digital comparator determines whether the count is above or below the compare register threshold and emits an interrupt if the count is below the threshold.

A block of logic clocked by the 32kHz RTC oscillator manages the touch switch process. The state machine runs every 250ms. This is sufficient to manage a touch switch, but would be too slow for (for example) a typewriter keyboard. By performing a scan so slowly, energy is saved.

Before the touch switch is used, the compare register must be calibrated. To do this, the MAXQ30 MPU core enables the touch switch and reads the count register after the first measurement cycle without a finger near the touch plate. The MPU then reduces this value by some amount (possibly through one shift right to reduce the value by half) and store that reduced value into the compare register. From that point, an interrupt to the host occurs only when the count register contains a value less than the compare register.

A two-bit period value is included in the IP block. This value selects one of several sample periods for the oscillator.

Table 17. Touch Sensor Sample Rate Control

PERIOD VALUE	SAMPLE PERIOD
0	2 (61µs)
1	4 (122µs)
2	8 (244µs)
3	16 (488µs)

The sample period is variable to account for different touch plate arrangements that can have more or less capacitance than the nominal value.

The enable input enables the state machine logic to operate. When enable is inactive, gate is held low, clear is held active and read is held inactive. When enable is active, the state machine logic runs every 8192 of the 32kHz clock cycles.

The overflow indication informs the host MPU that an overflow event has occurred. Under an overflow condition, the count does not accurately reflect whether a touch event has occurred. The host should recalibrate the system with a shorter sample period.

The touch switch can interrupt and wake the MAXQ30 MPU as well. The CMPIE bit in the TSWxCN register must be set to enable the interrupt and establish the CMPI bit as a wake source.

Hardware Considerations

The touch sensor is actually a capacitance sensor. That means the sensor responds to any change in capacitance, whether it is from a finger or from any other source. It is important that the conductors from the sensor pin to the sensor plate be kept short and direct and generally far away from other conductors.

Another consideration is the nominal capacitance of the circuit. Broadly speaking, the smaller the stray capacitance can be, the more sensitive and more accurate the touch sensor is. If the nominal stray capacitance is (for example) 1000pF, and the change due to a finger presence is 200pF, it is much more difficult to sense this reliably then if the nominal stray capacitance is, say, 10pF.

A final consideration is oscillator drift due to elements unrelated to the plate capacitance. The oscillator is relatively stable but will still have some variation due to temperature and supply voltage variations. It may be prudent to recalibrate the sensor from time to time.

Auxiliary ADC

In addition to the metrology channels, the ZON P5S/P5SL and M5S/M5SL SoCs contain a 10-bit auxiliary ADC with seven multiplexed inputs. This block is also used for to condition the optical receiver input. Figure 4 shows a block diagram of the auxiliary ADC system.

The auxiliary ADC is a ten-bit ΔΣ converter operating at a modulator rate of 5MHz and a fixed oversampling rate that provides a final conversion rate of 4,800 samples per second.

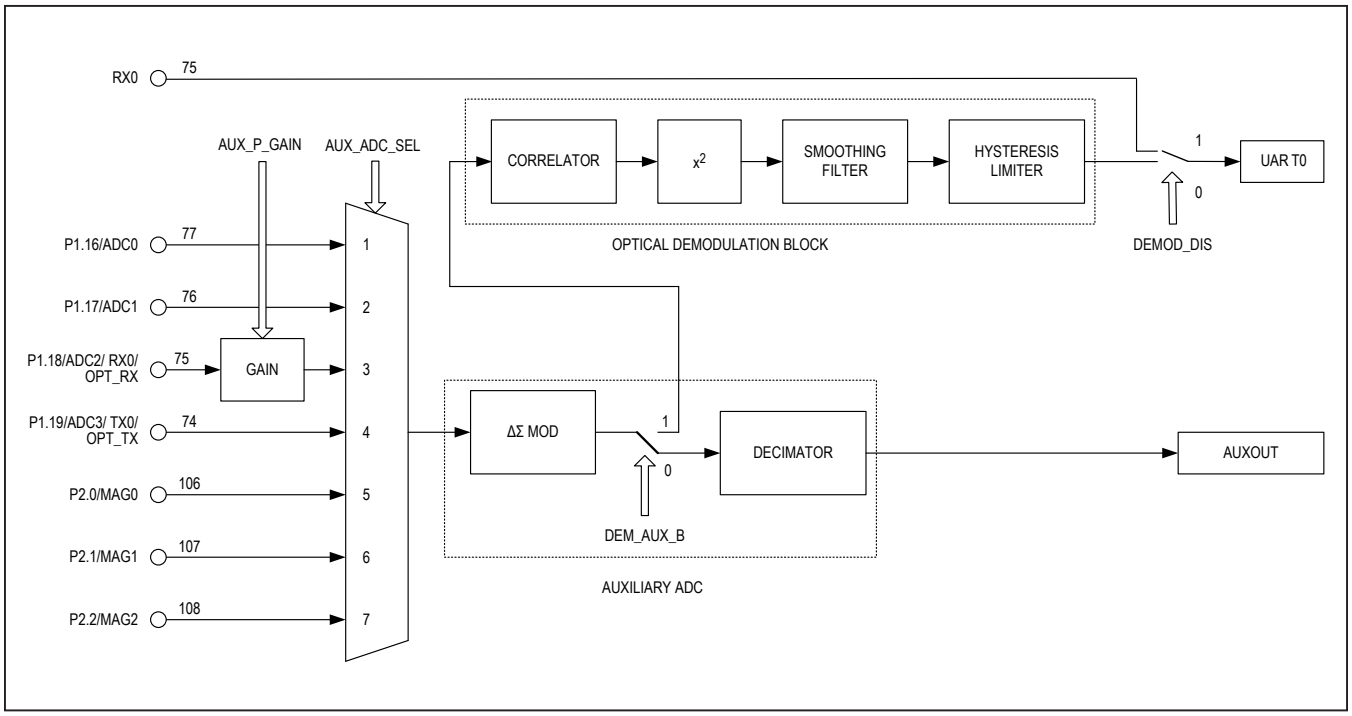


Figure 4. Auxiliary ADC and Optical Demodulation Block

Seven pins can be configured to be used as auxiliary ADC inputs, and one pin at a time is selected with a multiplexer that is controlled with the AUX_ADC_SEL bits in the LCDCTL register. Table 18 shows the allocation of ADC inputs to device pins and the AUX_ADC_SEL field.

Writing the value 1-6 into the AUX_ADC_SEL field selects the indicated pin as the ADC input. Any value other than 1–6 disables all ADC inputs, and all of the pins revert to their alternate functions. For AUX_ADC_SEL = 3, a gain of 5, 10, 20, or 40 can be selected with the AUX_P_GAIN bits.

Configuring the AUX ADC

If the optical demodulator is not in use, software should clear the DEM_AUX_B bit. When the optical demodulator is used this bit must be set. Clearing the DEM_AUX_B bit routes the incoming modulator bits to a sinc3 filter, the output of which is the finished samples that can be read from the AADCDATA register.

Using the AUX ADC

Bit 5 in the RTMCN register selects the clock for the auxiliary ADC. In addition, bit 0 in the DEMINT register has to be set. A conversion of the auxiliary ADC is started by setting bit 0 in the AADCST register. The most recent finished sample is available in the DEMSAMP register. The AUXDONE bit in the DEMCN register indicates that a sample is available in the AUXOUT[20:0] bits of the DEMSAMP register. To use the AUXDONE bit, software must clear the bit after each sample. Software cannot set this bit. Only the ADC hardware can set the bit when a new sample has arrived.

CRC Generator

The MAX71335S/MAX71336S contains a CRC generator for computing check words for most popular communication protocols. It generates 16-bit CRC with a polynomial of 0x1021 (x16 + x12 + x5 + 1) or a 32-bit CRC with a polynomial of 0x04C11DB7 (x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1).

There are three registers that pertain to the CRC generator. The CRCNT register provides control to the CRC generator peripheral, and the CRC1 and CRC2 registers provide the input and output ports for the CRC generator.

A configuration bit selects either byte or word interface mode for reads from and writes to the CRC generator peripheral.

32 x 32 Multiplier-Accumulator (MAC)

The ZON P5S/P5SL and M5S/M5SL SoCs provide a 32 x 32 fixed-point multiply-accumulate (MAC) unit to assist in mathematical operations. The multiplier provides a 64-bit result and sums the product to a 64-bit accumulator in the same cycle. The multiplier is ready for another operation two cycles later. If the MAXQ30 MPU core is running at 20MHz, the multiplier can perform 10,000,000 32 x 32 multiply cycles per second, in theory (in practice, the throughput will be slowed by the requirement of loading and unloading the multiplier registers.). The multiplier contains two input registers and two sets of two output registers.

The multiplier also contains a control register that configures the multiplier for various purposes. It manages the following functions and features:

Signed-unsigned multiplication: 32-bit unsigned values or 2's complement values

Multiply-accumulate enable: Selects either multiply plus accumulate operation or multiply only operation

Multiply-accumulate negate: Negates the result of the multiply operation before being added to the accumulator

Operand count select: A multiply-accumulate operation can occur after either operand has been loaded

Square function enable: In this mode, any write to either input register triggers a multiply operation using the register that was written as both the multiplier and the multiplicand, effectively squaring the value written

Clear data operation: Clears all registers and flags

Overflow Flag

Multiplier and accumulation results are available in the cycle after the last operand is written. However, the results are available for a second multiply-accumulate cycle only

Table 18. Allocation of ADC Inputs

AUX ADC INPUT	PIN	AUX_ADC _SEL[2:0]	ALTERNATE PIN FUNCTION(S)
—	—	0	—
0	77	1	GPIO Port 1 Bit 16
1	76	2	GPIO Port 1 Bit 17
2	75	3	GPIO Port 1 Bit 18, UART0 RxD Optical Receive (RX), Wake Input 3
3	74	4	GPIO Port 1 Bit 19, UART0 TxD Optical Transmit (TX)
4	106	5	GPIO Port 2 Bit 0
5	107	6	GPIO Port 2 Bit 1
6	108	7	GPIO Port 2 Bit 2

in the following cycle. That means it is possible to overrun the multiply-accumulate unit if successive single-operand operations or square operations are performed without intervening delay cycles (two-operand operations are not restricted in this way).

Real-Time Clock

RTC General Description

The ZON P5S/P5SL and M5S/M5SL SoCs real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. The RTC includes:

- 32-bit seconds register
- Eight-bit subseconds register
- 32-bit alarm register
- Circuits that wake the MPU from SLP mode on a variety of events
- Temperature measurement
- Third-order (cubic) temperature compensation hardware
- Battery condition monitor

The RTC block resides across three power domains. The real-time clock itself and the oscillator that drives it reside in a nonvolatile power domain since the RTC cannot be allowed to lose time when power fails. The wake controller also resides in this power domain so that it can wake the MPU even when all other power sources are shut off.

Other RTC logic, such as the temperature measurement and temperature compensation logic, resides in an on-demand power domain. Chip logic can turn this power domain on and off as required, so from time to time the nonvolatile domain can turn on power to the on-demand domain, perform a compensation cycle, and then turn off power.

The final power domain is the MSN mode domain. It has power only when the MPU is actually active. This domain contains the MPU facing registers and associated interface logic. By keeping this domain off unless the MPU is active battery power is saved.

RTC Temperature Compensation

The real-time clock contains a temperature compensation mechanism that is automatically applied to the clock oscillator. Details on temperature compensation can be found in the *Applications* section of this data sheet.

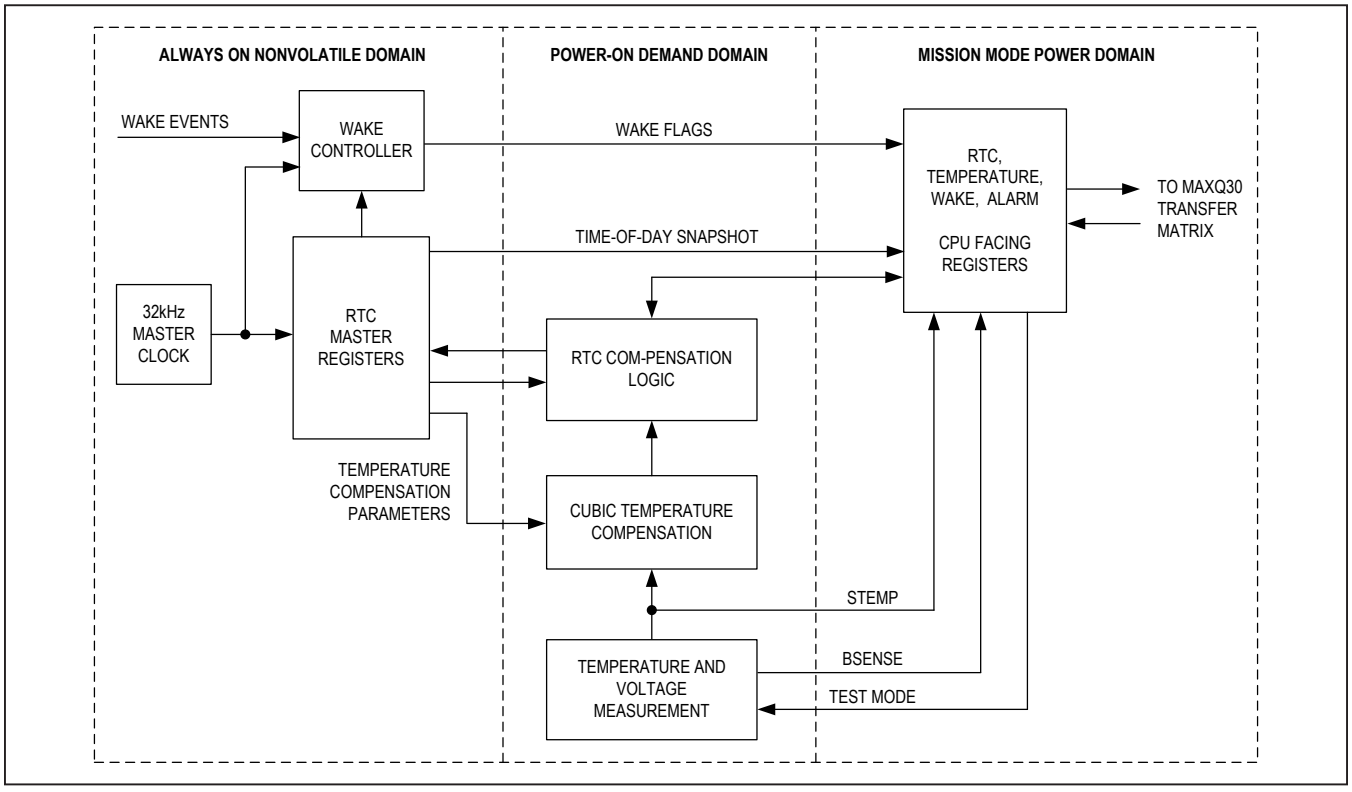


Figure 5. RTC Power Domains

Digital I/O (GPIO)

GPIO General Description

The ZON P5S/P5SL and M5S/M5SL SoCs contain a number of pins that can be configured as digital I/O, either as peripheral pins or as direct-write general-purpose I/O. When assigned to a peripheral, these pins are automatically configured for the selected peripheral. When assigned for general-purpose I/O, the user can select from a number of different configurations.

GPIO pins are organized as two 32-bit ports, port 0 and port 1, and a 16-bit port 2. Each bit is individually configurable for input, output or bidirectional modes. Each port contains three 32-bit registers: two control the state of the pin, and a third reflects the logic level on each of the physical pins associated with the port.

GPIO Interrupts

Port 0 bits 7:0 also support external interrupts. All external interrupts of the device are edge triggered, and the active edge is configurable.

To enable external interrupts, set the bits in the EIE0 register that correspond to the pins you wish to cause an interrupt. One can also set the bits in the EIES0 register to select the active edge: write a 0 to enable the rising edge and write a 1 to enable the falling edge.

When the selected edge occurs on a pin configured for an interrupt, and if the interrupt is enabled, the corresponding bit will be set in the interrupt flag register (IEF0). If interrupts are globally enabled (that is, IGE = 1), an interrupt is generated to the MAXQ30 MPU core.

Hardware Watchdog Timer

An independent, robust, fixed-duration, watchdog timer (WDT) is included in the ZON P5S/P5SL and M5S/M5SL SoCs. It uses the RTC crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time, the WDT overflows and the part is reset as if the $\overline{RST}$ pin were pulled low, except that the I/O RAM bits are in the same state as after a wake-up from SLP or LCD modes. 4100 CK32 cycles (or 125ms) after the WDT overflow, the MPU is launched from program address 0x80 0000.

The watchdog timer is also reset when the internal signal WAKE = 0. The WDT is disabled when the JTAG_E pin is pulled high. The watchdog timer is enabled only in MSN and BRN modes.

Security Features

The ZON P5S/P5SL and M5S/M5SL SoCs provide DES, 3DES, and AES encryption engines. These facilities provide fast encryption and decryption services for either communication security or protection of data stored in external memory devices.

AES: AES is a modern block cipher that uses a 128-bit or 256-bit key and operates on a 128-bit cipher block. AES combines four logical operations that involve mixing and substitution over 14-18 rounds to convert a plain-text block to a cipher block under control of the key. At the time of this writing, AES is considered secure.

DES: DES is a block cipher, published in 1977, that although still in wide use is now largely deprecated. It has a 56-bit key and a 64 bit cipher block size. DES is provided in the MAX71335S/MAX71336S to support legacy applications; its 56-bit key is considered too short for modern cryptographic security and the US government has withdrawn the single-key version of DES as a standard as of 2005. Triple-DES (3DES), which encrypts data with three rounds of the DES algorithm using two or three 56-bit keys is still considered secure, but not as secure as AES. Both two-key and three-key 3DES are fully supported in the device.

Reset Behavior

The ZON P5S/P5SL and M5S/M5SL SoCs contain a MAXQ30 MPU. Like with most MAXQ processors, execution begins in a utility ROM located at address 0x80 0000 in code space. Starting code execution at this ROM allows the MAXQ30 MPU core to check for special modes, such as boot loader or debug mode before branching to user code located at 0x00 0000.

Table 19. GPIO Pin Control

PDx:POx	PIN FUNCTION	PIN STATE	PLX STATE
00	Input	Hi-Z, unless externally driven	Indeterminate, unless externally driven
01	Input	Weak pullup	1, unless externally driven
10	Output 0	0	0
11	Output 1	1	1

Applications

Sensor Connection Diagrams

Diagrams for typical sensor connections (CTs, remotes) are shown in the Figures 6–9.

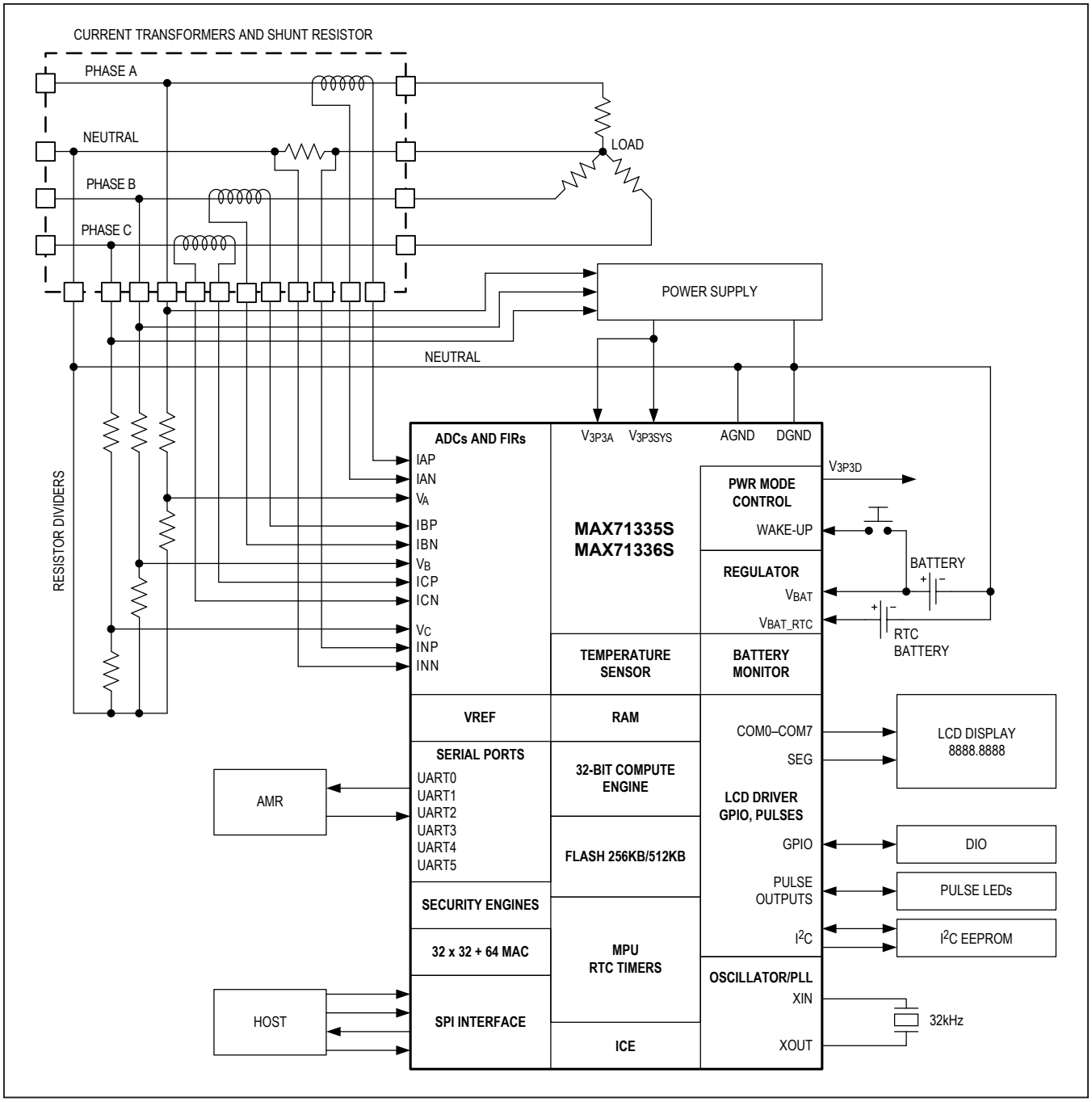


Figure 6. ZON P5S/P5SL Polyphase WYE Connection with Current Transformers

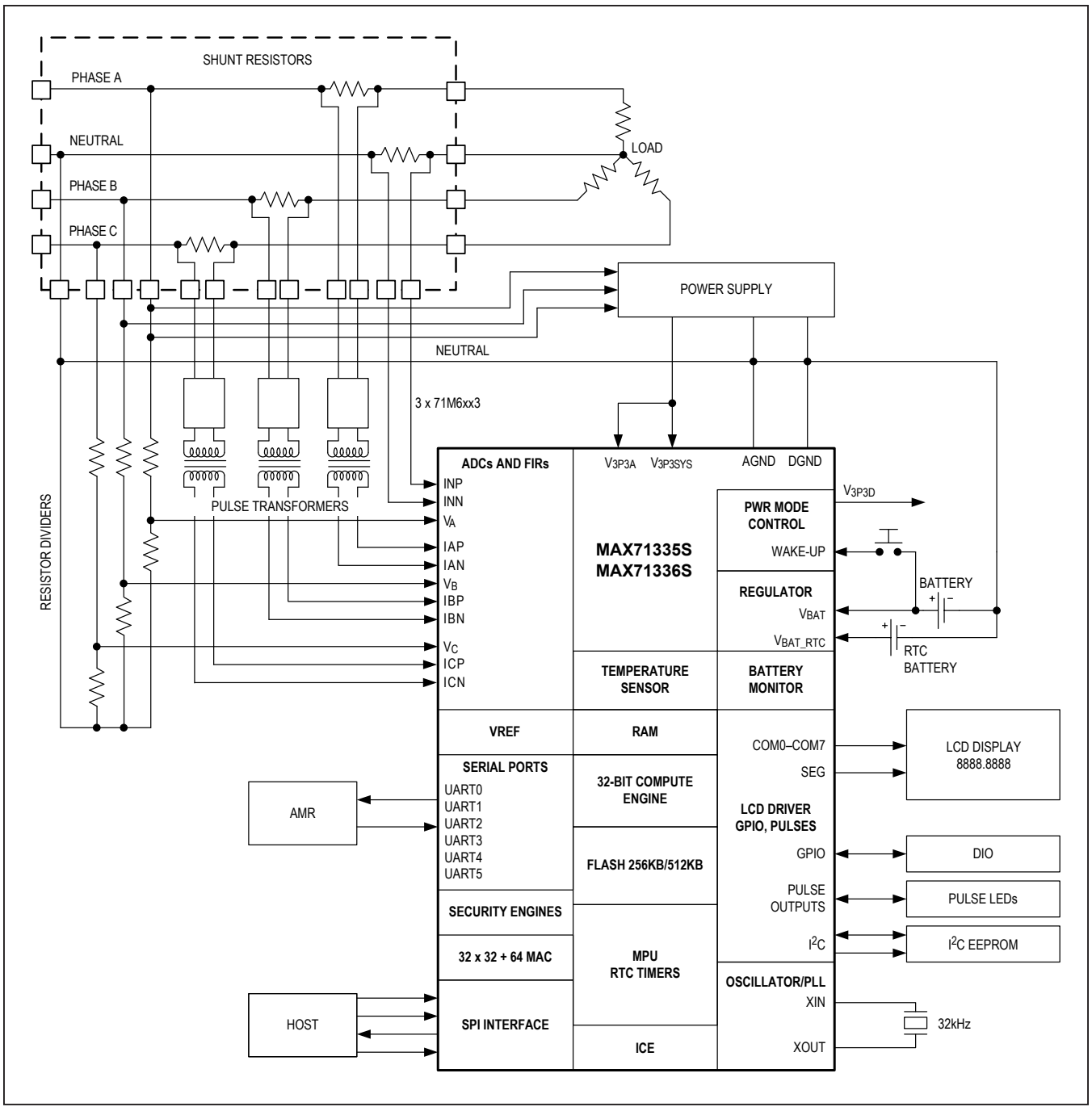


Figure 7. ZON P5S/P5SL Polyphase WYE Connection with Remotes (71M6xx3)

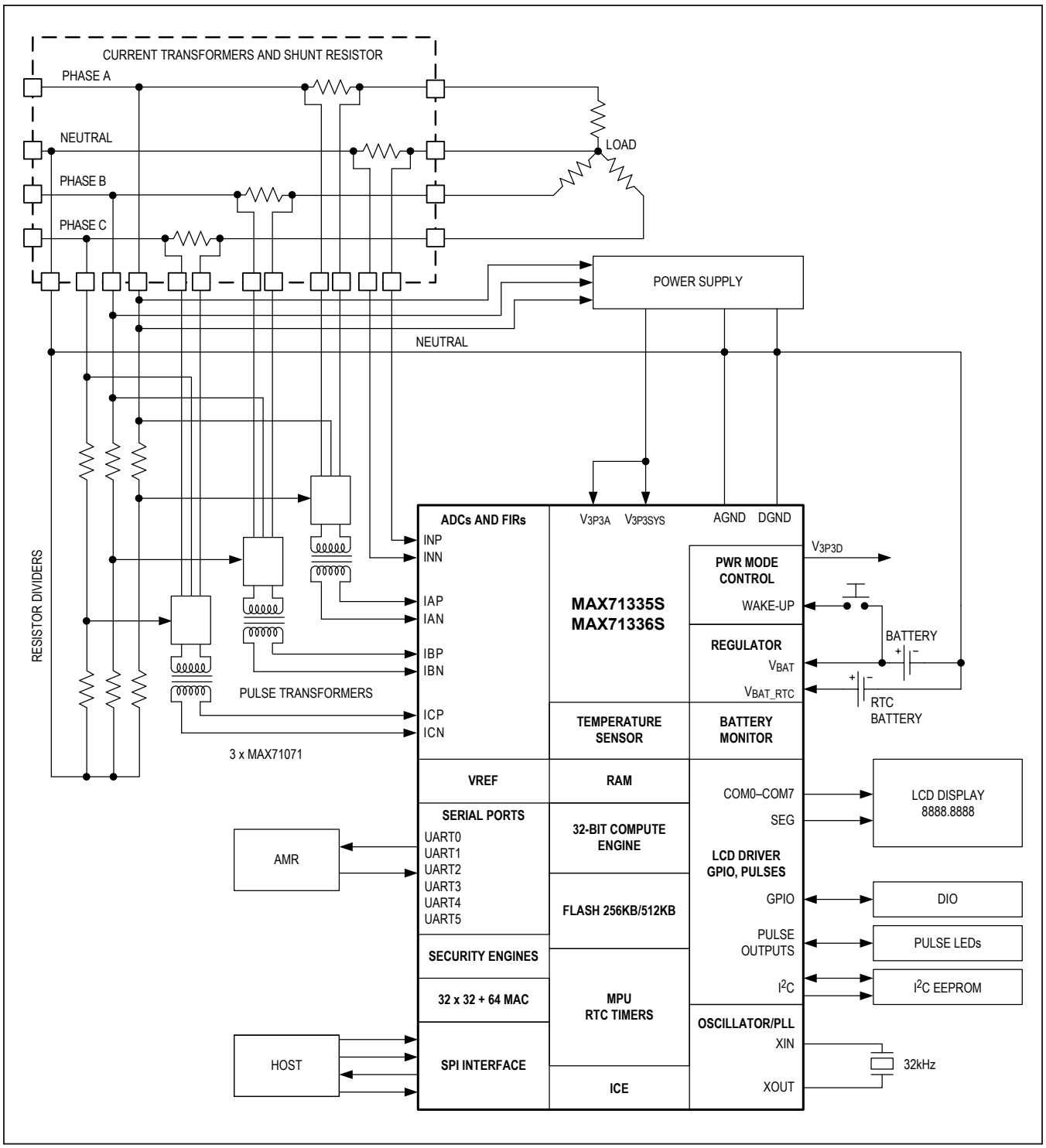


Figure 8. ZON P5S/P5SL Polyphase WYE Connection with Dual-Channel Remotes (MAX71071)

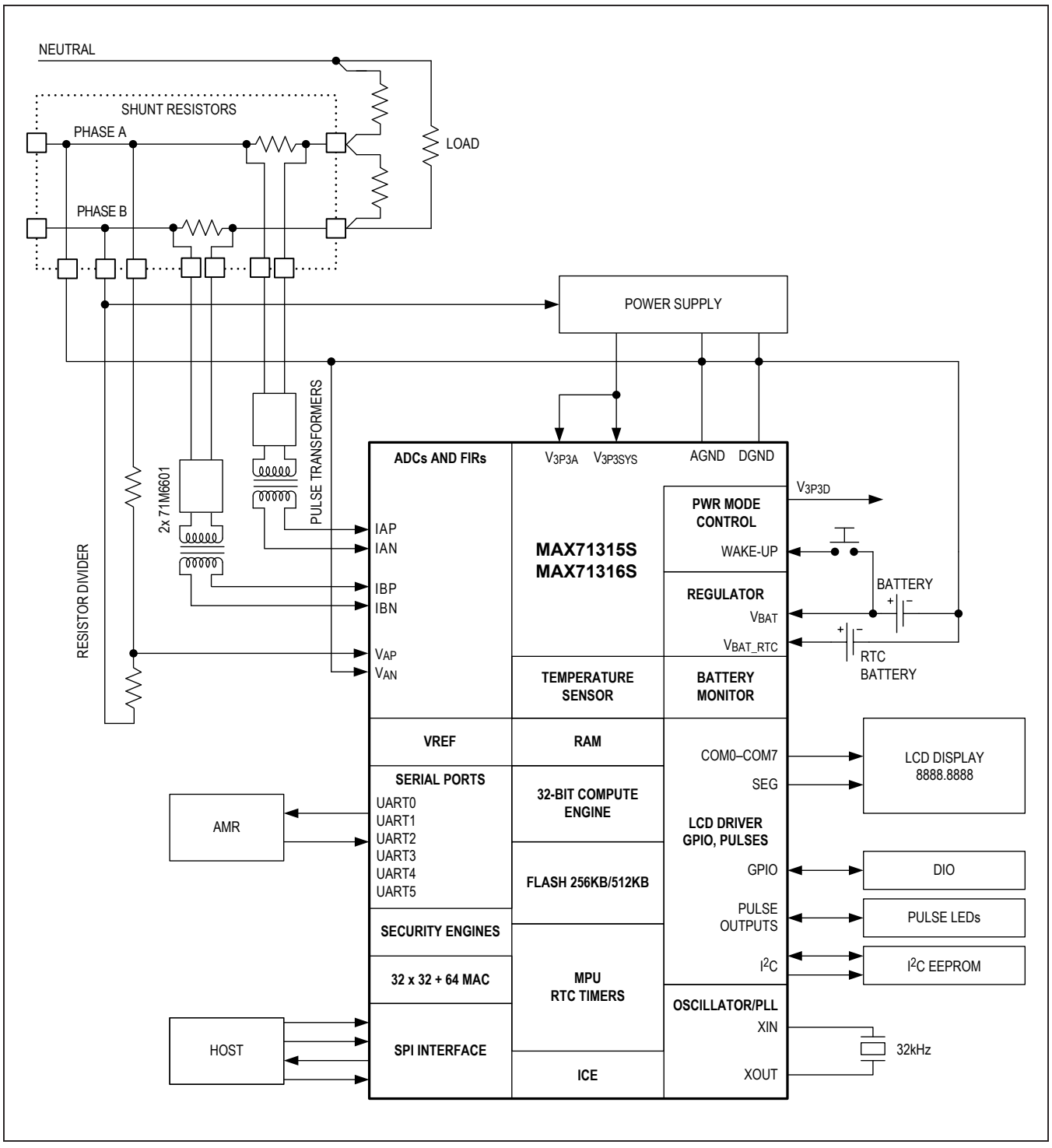


Figure 9. ZON M5S/M5SL Connection for ANSI Split-Phase with Two Remotes (71M6601)

Temperature Compensation

The ZON P5S/P5SL and M5S/M5SL SoCs support temperature compensation for both metrology and for the RTC.

Temperature Compensation for Metrology

Temperature compensation for metrology is based on the behavior of the V_{REF} reference voltage (bandgap voltage). The nominal voltage can be described with the following formula:

$V_{NOM(T)} = V_{REF(22)} + (T - 22) \times TC_1 + ((T - 22)^2) \times TC_2$

In this formula, T is the temperature in °C. The linear coefficient TC_1 and the quadratic coefficient TC_2 can be obtained from trim information of the SoC as follows:

$TC_1 = -0.00014 - 9.809 \times 10^{-6} \times TRIM\_BG\_T\ (V/°C)$

$TC_2 = -0.18 \times 10^{-6} + 12.68 \times 10^{-9} \times TRIM\_BG\_T\ (V/(°C_2))$

TRIM_BG_T is the value of the bandgap trim and is stored in the info block of the device. It can be accessed using a function in the utility ROM. Once the MPU has obtained the value for TRIM_BG_T at startup, it calculates TC_1 and TC_2 per the equations given above and copy TC_1 and TC_2 into the appropriate CE register locations where the CE can use them for internal temperature compensation. In internal temperature compensation mode, the CE autonomously controls gain adjustment registers for the metrology values based on the anticipated deviation of the bandgap voltage. It is also possible for the MPU to use the TC_1 and TC_2 coefficients in combination with system-related coefficients to implement system-wide temperature compensation. This type of compensation can adjust for sensor characteristics over temperature and other temperature-related effects. In that case, the CE is operating in external temperature compensation mode, leaving access to the gain adjustment registers to the MPU. For details on temperature compensation, refer to the ZON P5S/P5SL HRM (Hardware Reference Manual).

Temperature Compensation for the RTC

To facilitate RTC compensation for the effects of temperature on the crystal oscillator, the ZON M5S/M5SL and P5S/P5SL provide a temperature measurement circuit that is independent of the metrology ADCs, the auxiliary ADC, and the MPU. The TEMP_PER register can be used to schedule periodic automatic temperature measurements that happen even if the device is in SLP or LCD modes. The result of the last temperature measurement is contained in the STEMP register. The value is trimmed such that room temperature results in an STEMP value of zero. STEMP changes by 0.0811LSB/°C.

To improve the resolution of the RTC timekeeping, the RTC keeps time based on the 32.768 KHz crystal oscillator multiplied by a factor of six hundred (19.660800MHz). This frequency is compensated for temperature using a cubic equation. The coefficients of this equation are set in registers TC_A through TC_D to form the equation:

$$n_T = RTC_{CAL} + TC_D + \frac{TC_C}{2^{11}} \times STEMP + \frac{TC\_B}{2^{21}} \times STEMP^2 + \frac{TC\_A}{2^{31}} \times STEMP^3$$

where n_T is the number of clock cycles representing one second.

The RTC_CAL register sets the nominal frequency of the crystal. The temperature compensation represented by the cubic equation is then added to the value in RTC_CAL to determine the number of multiplied clock cycles needed to represent a single second in the RTC. The RTC_SEC register increments by one each time the number of multiplied clock cycles is equal to the value derived in the equation above. For a perfect 32.768kHz crystal, the value of RTC_CAL is 32768*600=19660800.

TC_D is the constant deviation of the crystal frequency from ideal at room temperature and can be determined by measuring the raw frequency of the crystal. TC_B is the quadratic coefficient that reflects the inverse-parabolic variation with temperature that most low-frequency tuning fork crystals have. TC_B can be obtained from the data sheet of the crystal in use. Linear (TC_C) and cubic (TC_A) coefficients are zero or near zero for most crystals.

When the device is not in SLP or LCD mode, every temperature measurement results in compensation to the RTC calibration, meaning the internal cubic equation is reevaluated. When the device is in SLP or LCD mode, to save power, any temperature measurement will only result in compensation if the temperature has changed by more than some minimum amount, defined by the TEMP_RANGE register. If the new STEMP value is less than TEMP_RANGE different from the last STEMP used to evaluate the compensation equation, then the new STEMP is discarded and no action is taken. RTC compensation is further supported by the following features:

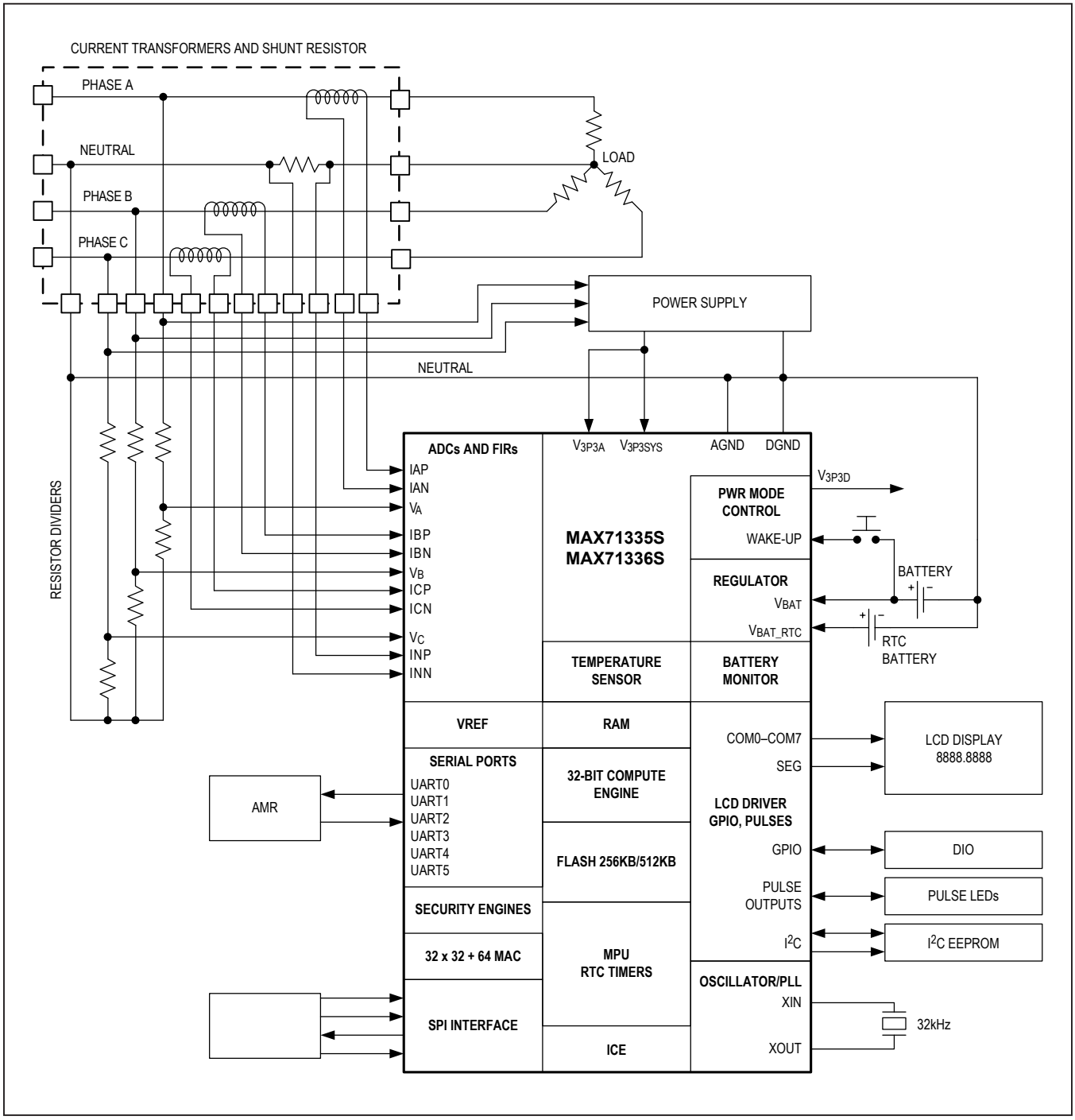
High temperature alarm limit: If the most recent temperature measurement exceeds a predefined value, the MPU is awakened if in SLP mode.

Low temperature alarm limit: If the most recent temperature measurement is less than a predefined value, the MPU is awakened if in SLP mode.

The achievable accuracy of the temperature compensation is determined by two factors:

- Accuracy of the temperature measurement
- Repeatability of the crystal characteristics (inversion temperature, quadratic coefficient)

Typical Application Circuit



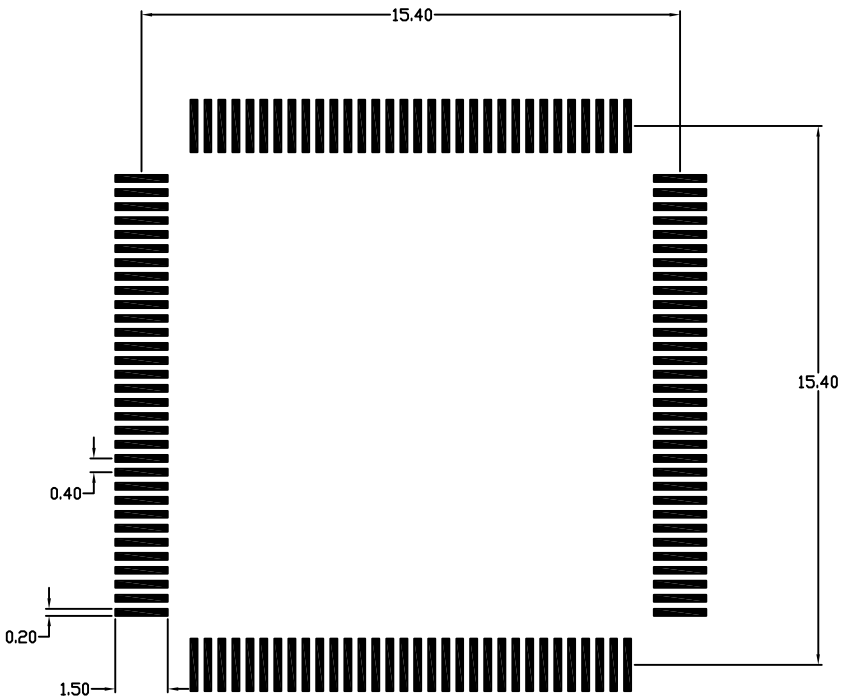
Ordering Information

PART NUMBER	PACKAGING	PROGRAM MEMORY (KB)	ADCs	TOP MARK	REMOTE ADC TRIM	EW_VSYS, EW_PB1 DEFAULTS
MAX71335SECD+	Bulk	256	7	MAX71335SECD	325ns	0,0
MAX71335SECD+T	Tape & reel	256	7	MAX71335SECD	325ns	0,0
MAX71336SECD+	Bulk	512	7	MAX71336SECD	325ns	0,0
MAX71336SECD+T	Tape & reel	512	7	MAX71336SECD	325ns	0,0
MAX71336SECD+Z	Bulk	512	7	MAX71336SECD	337ns	0,0
MAX71336SECD+ZT	Tape & reel	512	7	MAX71336SECD	337ns	0,0
MAX71336SECD+CZ	Bulk	512	7	MAX71336SECD	337ns	1,1
MAX71336SECD+CZT	Tape & reel	512	7	MAX71336SECD	337ns	1,1
MAX71315SECD+	Bulk	256	4	MAX71315SECD	325ns	0,0
MAX71315SECD+T	Tape & reel	256	4	MAX71315SECD	325ns	0,0
MAX71316SECD+	Bulk	512	4	MAX71316SECD	325ns	0,0
MAX71316SECD+T	Tape & reel	512	4	MAX71316SECD	325ns	0,0
MAX71316SECD+Z	Bulk	512	4	MAX71316SECD	337ns	0,0
MAX71316SECD+ZT	Tape & reel	512	4	MAX71316SECD	337ns	0,0
MAX71316SECD+CZ	Bulk	512	4	MAX71316SECD	337ns	1,1
MAX71316SECD+CZT	Tape & reel	512	4	MAX71316SECD	337ns	1,1

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

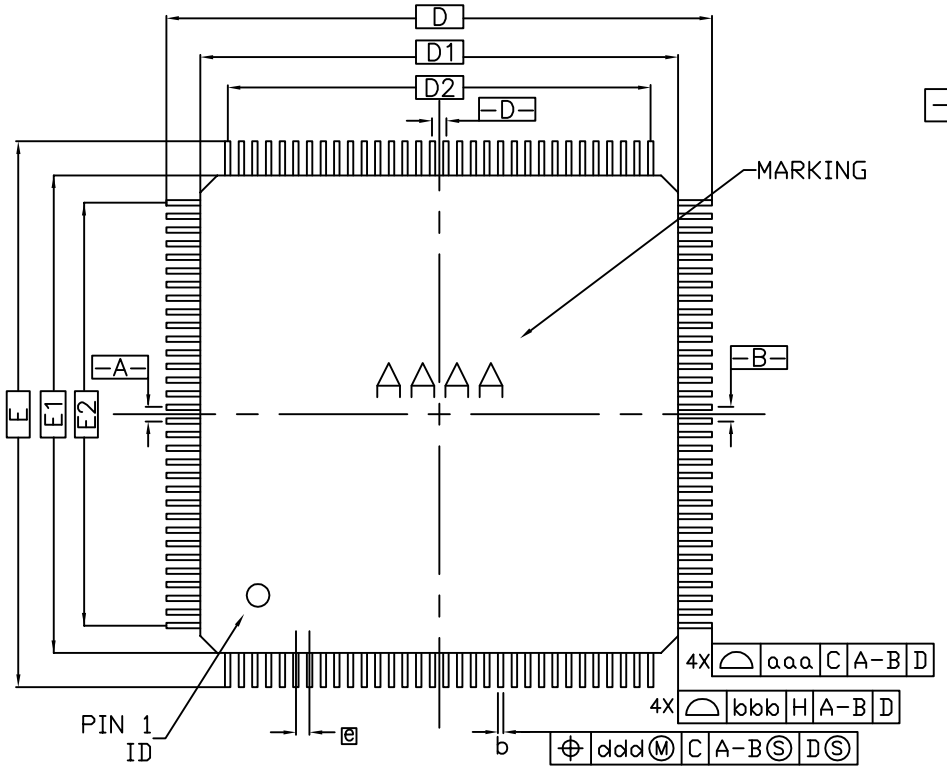
Package Information

Package outline information is appended to this document. Land patterns (footprints) are inserted below.

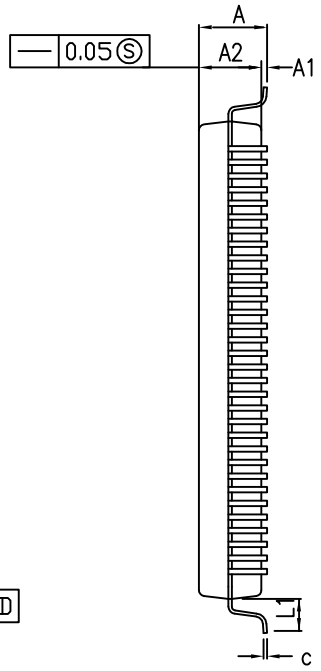


Revision History

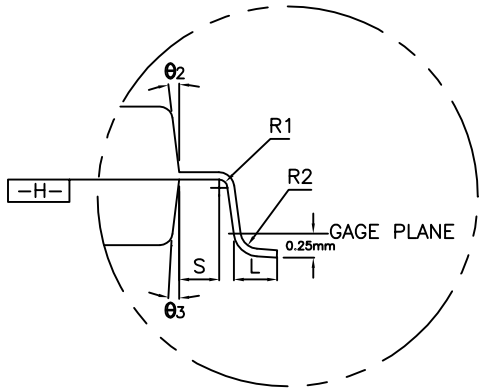
REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	7/15	Updated *Benefits and Features* section, updated supply voltage conditions, added Note 9 and VSTAT Levels section to the *Electrical and Timing Characteristics* table, updated *Recommended External Components* table, *Pin Configuration*, *Pin Description*, added parametric data, updated Figures 4, 6–9, updated the *Typical Application Circuit*, and removed future product references	1–7, 11, 13–17, 24–26, 35, 36, 39–46
2	4/16	Rebrand Only	
3	8/16	Corrected Pin Names and Top Mark	7, 8, 11, 46
3.1	11/17	Added new ordering part number options	46



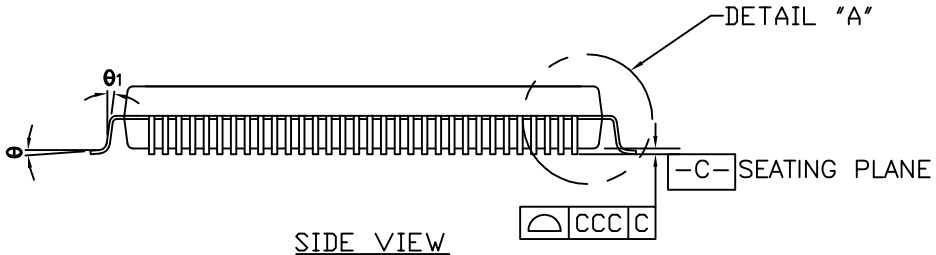
TOP VIEW



SIDE VIEW



DETAIL "A"



SIDE VIEW

-DRAWING NOT TO SCALE-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS SPECIFIED OTHERWISE.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
6. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
7. MARKING SHOWN IS PACKAGE ORIENTATION REFERENCE ONLY.
8. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
9. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40	—	1.60	—	—	.063
A_1	0.05	—	0.15	.002	—	.006
A_2	1.35	1.40	1.45	.053	.055	.057
D	16.00 BSC.			.630 BSC.		
D_1	14.00 BSC.			.551 BSC.		
E	16.00 BSC.			.630 BSC.		
E_1	14.00 BSC.			.551 BSC.		
R_2	0.08	—	0.20	.003	—	.008
R_1	0.08	—	—	.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	.004	—	.008
L	0.45	0.60	0.75	.018	.024	.030
L_1	1.00 REF			.039 REF		
S	0.20	—	—	.008	—	—
b	0.13	0.16	0.23	.005	.006	.009
e	0.40 BSC.			.016 BSC.		
D2	12.40			.488		
E2	12.40			.488		
aaa	0.20			.008		
bbb	0.20			.008		
ccc	0.08			.003		
ddd	0.07			.003		

—DRAWING NOT TO SCALE—