MAX71617/MAX71637 Smart Metering SoCs

General Description

The MAX71617 is a low-power, single-phase energy measurement system-on-chip (SoC), and the MAX71637 is a low-power polyphase energy measurement SoC. Based on an ARM Cortex®-M3 core, the devices can run modern operating systems that monitor and report energy usage and implement communications stacks. In addition to the main administrative core, the devices include a MAXQ30 CPU core to perform metering functions and a discrete compute engine for the DSP related tasks necessary for accurate energy monitoring and measurement, last cycle analysis, and FFT functions to compute the frequency spectra of the selected channel.

The DSP core provides the following energy and power measurement features in registers:

- Active energy and power per phase and sum
- Apparent energy and power per phase and sum
- Reactive energy and power per phase and sum
- Line voltage and current RMS
- Neutral current RMS
- Current vector sum, three-phase plus neutral
- Line frequency
- Fundamental frequency
- Total harmonics of active power, reactive power, voltage, and currents
- Security features

Benef ts and Features

- SoC Integration and Unique Isolation Technique Reduces BOM Cost Without Sacrificing Performance
  - Watt-Hour Accuracy of 0.1% at Up to 5,000:1 Dynamic Range
  - Sample Frequency Conf gurable; ΣΔ Sample Rate Conf gurable Up to 9.83MHz
  - Flexible Analog Input Conf guration Support Current Transformers, Shunts, or Rogowski Coils
  - 2.7V to 3.6V Operating Voltage
  - Single 32.768kHz Crystal Provides All Operating Clocks
- ARM Core M3 Application Processor Enables Rapid System Development
  - 1MB Flash
  - 64KB Code RAM
  - 64KB System RAM
  - Six UART Channels
  - Seven Timer Channels
  - I^2C Master/Slave Peripheral
  - Three SPI Peripherals
  - Smart Card Interface
- MAXQ30 Features
  - 64KB Program RAM
  - 8KB Data RAM
  - 16KB Page RAM
  - Four Meter Pulse Outputs (Configurable)
  - Two I^2C Master/Slave Peripherals
  - SPI Master/Slave Peripheral
  - 50-Segment, 6-Common LCD Interface
- Security Features Reduce or Eliminate Common Security Threats
  - Built-In Cryptographic Modules Ensure Communications Are Kept Secure
  - Tamper Detect Inputs Ensure Attempts to Breach the Case Are Recorded and Reported
  - Two Independent Cores Ensures Compliance with All Current and Future Security Requirements
- Analog Front-End
  - Seven (MAX71637) or Four (MAX71617) 24-Bit ΣΔ A/D Converters
  - Three (MAX71637) or Two (MAX71617) Voltage Inputs
  - Four (MAX71637) or Three (MAX71617) Differential Current Inputs

Applications

- Smart and Secure Single-Phase Energy Meters
- Smart and Secure Polyphase Energy Meters
- MID/WELMEC-Compliant Meters

***Ordering Information* appears at end of data sheet.**

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Rev 2; 4/16

Absolute Maximum Ratings

(Voltage on all pins with respect to GND.)
RGND and AGND.....-0.2V to +0.2V
V_{DD}.....-0.5V to +3.6V
AVDD.....-0.5V to +3.6V
RVDD.....-0.5V to +3.6V
V_{BAT}, V_{RTC}.....-0.5V to +3.8V
ADC0–ADC10.....-0.5V to (V_{AVDD} + 0.5V)
XIN, XOUT.....-0.5V to +3.0V
SEG and SEGDIO, Configured as Digital Inputs.....-0.3V to +3.6V
Digital Pins, Configured as Inputs.....-0.5V to V_{DD}
ESD Stress on All Pins.....±2kV, HBM
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

LQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....45°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....16°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Electrical Characteristics

(Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed. V_{DD} = V_{AVDD} = V_{IO} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Digital Supply Voltage	V_{DD}		V_{RST}		3.6	V
Analog Supply Voltage	V_{AVDD}		2.7		3.6	V
Supply Voltage, Remote Interfaces	V_{RVDD}		2.7		3.6	V
Supply Voltage, Backup Battery	V_{BAT}		2.0		3.8	V
Supply Voltage, RTC Battery	V_{RTC}		2.0		3.8	V
Reset Threshold	V_{RST}			1.95 ±0.05		V
Power Fail Warning Threshold	V_{PFW}			2.07 ±0.05		V
Supply Current, Digital	I_{DD1}	(Note 2)		55		mA
	I_{DD2}	(Note 3)		24		mA
Supply Current, Analog	I_{DD1}	(Note 2)		19		mA
	I_{DD2}	(Note 3)		19		mA
Stop Mode Current, Digital	I_{STOP}	V_{DD} = V_{AVDD} = 3.3V		3		mA
Stop Mode Current, Analog	I_{STOP}	V_{DD} = V_{AVDD} = 3.3V		210		µA
Dynamic Current		(Note 4)		0.98		mA/MHz
V_{BAT} Current	I_{VBAT}	MSN mode (Note 5)		±25		nA
		BRN mode (Note 6)		7		mA
		LCD_ONLY mode (Note 7)		6		µA
		SLP mode, V_{BAT} = 3.3V, V_{RTC} = 0V		2		µA
V_{RTC} Current	I_{VRTC}	MSN mode (Note 5)		±25		nA
		SLP mode, V_{BAT} = 0V, V_{RTC} = 3.3V		1.6		µA

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed. V_{DD} = V_{AVDD} = V_{IO} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR						
Oscillator Frequency	f_{RTC}			32768		Hz
Nominal Operating Frequency, Application Core				108		MHz
Nominal Operating Frequency, DSP Core				36		MHz
Nominal Operating Frequency, Compute Engine				36		MHz
Frequency Variation with Voltage		T_A = +25°C, V_{DD} = 0V, V_{RTC} = 2.0V to 3.8V		±1		ppm
Startup Time				900		ms
LOGIC LEVELS						
Digital High Level	V_{IH}	At temp corners	2.0			V
Digital Low Level	V_{IL}	At temp corners			0.8	V
Digital High Level, RSTN			$0.8V_{IO}$			V
Digital Low Level, RSTN					$0.3V_{IO}$	V
Input Hysteresis, All GPIO Pins				50		mV
Input Leakage		V_{IN} = V_{IO}	-1		+1	µA
Input Pullup Current		Pullup enabled, V_{IN} = 0V	-30.0		-1.5	µA
Digital High-Level Output Voltage	V_{OH}	6mA	V_{IO} - 0.4			V
Digital Low-Level Output Voltage	V_{OL}	6mA			0.4	V
LCD						
V_{LCD} Current		V_{LCD} = 3.3V, any multiplex mode, no output loading, LCD pins open			7	µA
V_{REF}						
Nominal Reference Voltage	V_{REF}	T_A = +22°C		1.195		V
Variation with Power Supply		V_{AVDD} = 3.0V to 3.6V		±1.5		mV/V
Deviation from Predicted Variation with Temperature				±40		ppm/°C
ADC						
Usable Input Range			-250		+250	mV peak
Input Impedance			30		50	kΩ
LSB Size		FIR_LEN = 11, 5.46kHz sample rate		92		nV/LSB
		FIR_LEN = 15		118		
Digital Full Scale		FIR_LEN = 11, 5.46kHz sample rate		±3375000		LSB
		FIR_LEN = 15		±2621440		
Input Offset			-10		+10	mV

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +22°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed. V_{DD} = V_{AVDD} = V_{IO} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THD, Voltage Channel (Note 8)		250mV$_{P-P}$			-75	dB
		20mV$_{P-P}$		-86		
THD, Current Channel (Note 8)		Preamp off, 250mV$_{P-P}$		-102	-90	dB
		Preamp off, 20mV$_{P-P}$		-87		
		Preamp on, 20mV$_{P-P}$		-84		
Current Channel 0 Preamp Gain				8.90		V/V
Gain Variation with Supply Voltage		Preamp on		±0.18		%
Gain Variation with Temperature		Preamp on	-180		+180	ppm/°C
Current Channel Phase Shift				0.03		m°
Phase Shift Variation			-100		+100	m°
Input Noise		All channels, preamp off		900		nV/√Hz
		ADC0, preamp on		100		
Crosstalk		T_A = +22°C, guaranteed by design, not production tested		-108	-97	dB
FLASH MEMORY (Note 9)						
Flash Erase Time	t_{ME}	Mass erase		20		ms
	t_{PE}	Page erase		20		ms
Flash Programming Time	t_{PROG}	Per long word		20		µs
Endurance		Number of write/erase cycles		10,000		Cycles
Data Retention		T_A = +85°C		10		Years

Note 2: Application core operating at 108MHz, metering core operating at 36MHz, instruction cache on, AES operating in 128 bit mode, one DMA channel actively copying data from application core code RAM to application core system RAM, all timers active and running (timer 0/1, timer 1/2, timer 2/4, timer 3/8, timer 4/16, timer 5/32, timer 6/64), random number generator running, application core running from flash and fetching data from flash, MAXQ30 runnning in tight loop, MAXQ30 timer operating in timer mode, all LCD segments enabled but no load on LCD pins, all ADC channels operating, RTC watchdog operating, CE running, V_{DD} = V_{AVDD} = 3.3V.

Note 3: Application core operating at 27MHz, metering core operating at 36MHz, instruction cache on, AES operating in 128 bit mode, one DMA channel actively copying data from application core code RAM to application core system RAM, all timers active and running (timer 0/1, timer 1/2, timer 2/4, timer 3/8, timer 4/16, timer 5/32, timer 6/64), random number generator running, application core running from flash and fetching data from flash, MAXQ30 running in tight loop, MAXQ30 timer operating in timer mode, all LCD segments enabled but no load on LCD pins, all ADC channels operating, RTC watchdog operating, CE running, V_{DD} = V_{AVDD} = 3.3V.

Note 4: V_{DD} = V_{AVDD} = 3.3V, ADC off, application core off, compute engine off, all peripherals off, computed at user core frequencies of 108MHz and 13.5MHz.

Note 5: $f_{APPLICATION\_CORE}$ = 108MHz; f_{DSP_CORE} = f_{CE} = 36MHz; all peripherals and security engines disabled, all GPIO pins configured for output and not externally connected. V_{DD} = V_{AVDD} = 3.3V.

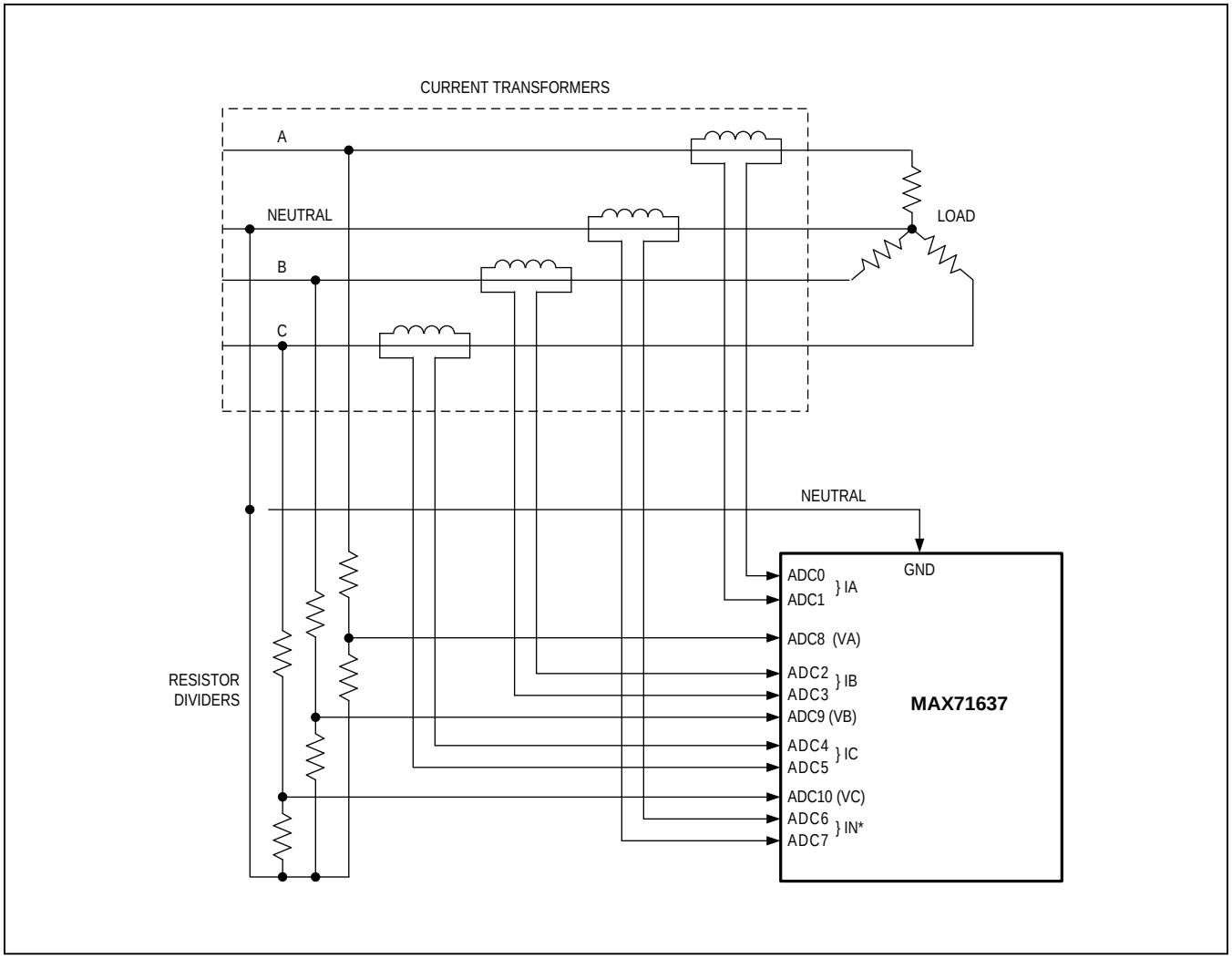
Note 6: Application core halted, metering core running at 36MHz reading data from RAM, LCD off, CE off, ADC off, peripherals off, V_{DD} = V_{AVDD} = 0V, V_{BAT} = V_{RTC} = 3.3V.

Note 7: All core regulators off, LCD operating without load, V_{BAT} = 3.3V, V_{RTC} = 0.0V.

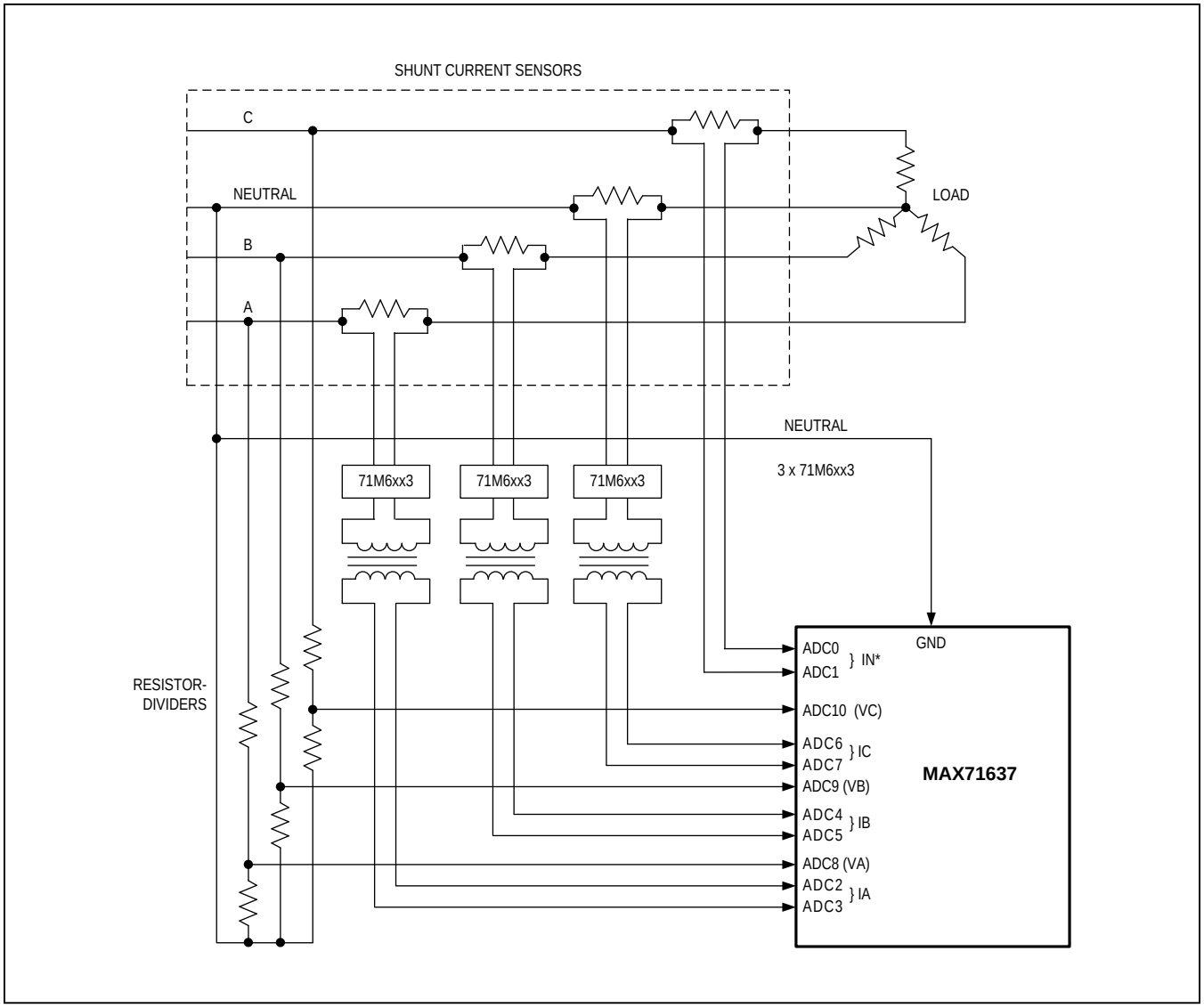
Note 8: Computed using a 64k point Fast Fourier Transform, Blackman-Harris window, 65Hz input frequency.

Note 9: V_{DD} must be greater than 1.8V to support flash write/erase operations.

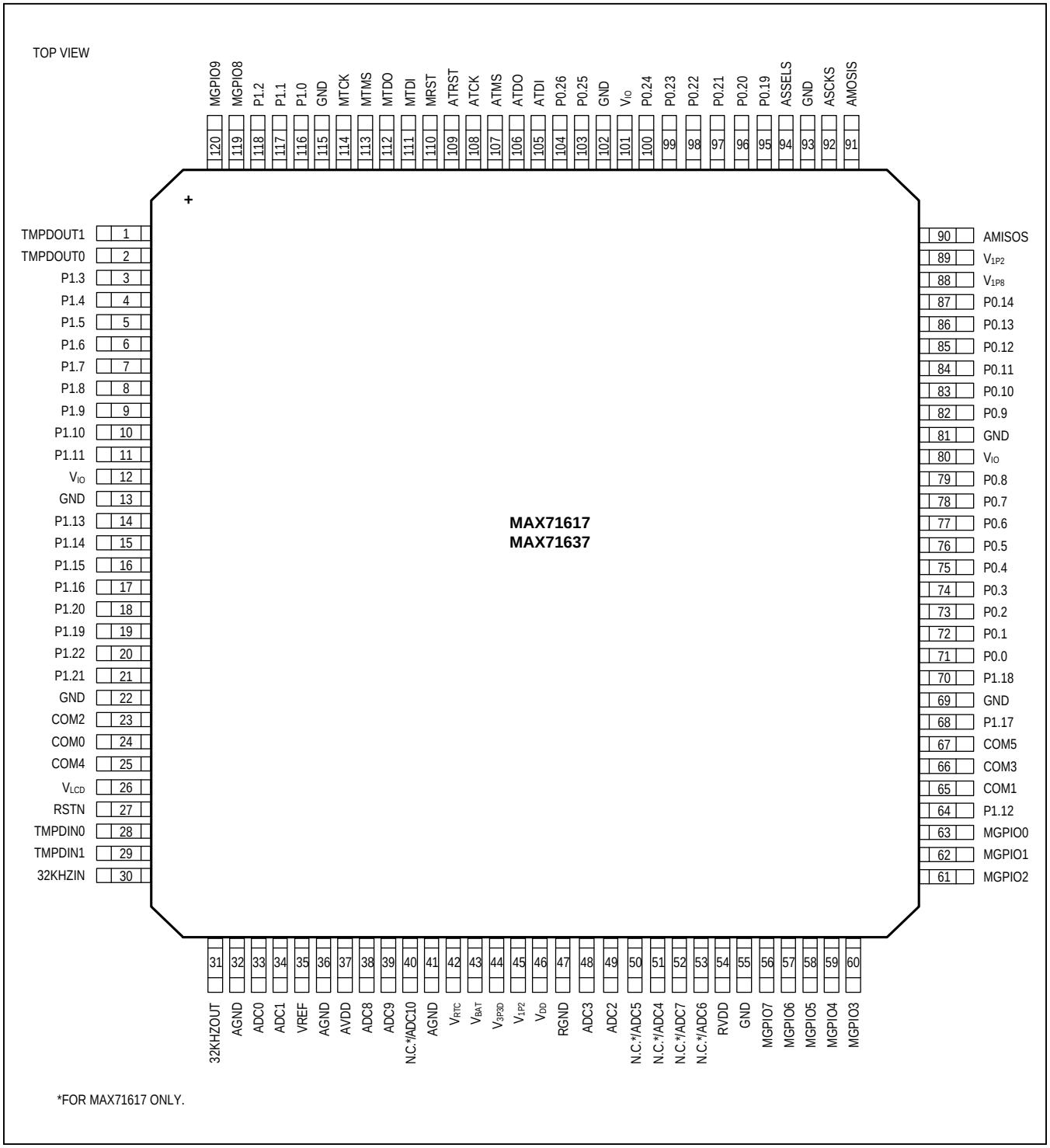
Typical Application Circuit (WYE Connected Load, Current Transformer Sensors)



Typical Application Circuit (WYE Connected Load, Shunt Sensors)



Pin Conf guration



Pin Description

PIN (MAX71617)	PIN (MAX71637)	PRIMARY FUNCTION	SECONDARY FUNCTION	DESCRIPTION
1	1	TMPDOUT1		Tamper Detect Output 1
2	2	TMPDOUT0		Tamper Detect Output 0
3	3	P1.3	SEG35/ISORST	GPIO 1.3/LCD Segment 35/ISO UART Reset
4	4	P1.4	SEG36/ISoCLK	GPIO 1.4/LCD Segment 36/ISO UART Clock
5	5	P1.5	SEG37/ISOIO	GPIO 1.5/LCD Segment 37/ISO UART I/O
6	6	P1.6	SEG38/MISO1	GPIO 1.6/LCD Segment 38 SPI Port 1 MISO
7	7	P1.7	SEG39/MOSI1	GPIO 1.7/LCD Segment 39/SPI Port 1 MOSI
8	8	P1.8	SEG40/SCLK1	GPIO 1.8/LCD Segment 40/SPI Port 1 SCLK
9	9	P1.9	SEG41/SSEL1	GPIO 1.9/LCD Segment 41/SPI Port 1 SSEL
10	10	P1.10	SEG42/TXD3	GPIO 1.10/LCD Segment 42/UART 3 Transmit Data
11	11	P1.11	SEG43/RXD3	GPIO 1.11/LCD Segment 43/UART 3 Receive Data
12, 80, 101	12, 80, 101	V_{IO}		I/O Power
13, 22, 55, 69, 81, 93, 102, 115	13, 22, 55, 69, 81, 93, 102, 115	GND		Digital Ground
14	14	P1.13	SEG45	GPIO 1.13/LCD Segment 45
15	15	P1.14	SEG46	GPIO 1.14/LCD Segment 46
16	16	P1.15	SEG47	GPIO 1.15/LCD Segment 47
17	17	P1.16	SEG48	GPIO 1.16/LCD Segment 48
18	18	P1.20	RXD2/TCLK1/MOSI0	GPIO 1.20/UART 2 Receive Data/Timer 1 I/O/SPI Port 0 MOSI
19	19	P1.19	TXD2/TCLK0/MISO0	GPIO 1.19/UART 2 Transmit Data/Timer 0 I/O/SPI Port 0 MISO
20	20	P1.22	RXD1/TCLK3/SSEL0	GPIO 1.22/UART 1 Receive Data/Timer 3 I/O/SPI Port 0 SSEL
21	21	P1.21	TXD1/TCLK2/SCLK0	GPIO 1.21/UART 1 Transmit Data/Timer 2 I/O/SPI Port 0 SCLK
23	23	COM2		LCD Common Pin 2
24	24	COM0		LCD Common Pin 0
25	25	COM4		LCD Common Pin 4
26	26	V_{LCD}		LCD Supply
27	27	RSTN		Device Reset
28	28	TMPDIN0		Tamper Detect Input 0
29	29	TMPDIN1		Tamper Detect Input 1
30	30	32KHZ IN		Crystal In
31	31	32KHZ OUT		Crystal Out
32, 36, 41	32, 36, 41	AGND		Analog Ground
33	33	ADC0		ADC Input 0, Positive Input to Converter 0, typically Phase A Positive Current Input

Pin Description (continued)

PIN (MAX71617)	PIN (MAX71637)	PRIMARY FUNCTION	SECONDARY FUNCTION	DESCRIPTION
34	34	ADC1		ADC Input 1, Negative Input to Converter 0, typically Phase A Negative Current Input
35	35	V_{REF}		Reference Voltage
37	37	AVDD		Analog Power
38	38	ADC8		ADC Input 8, Single-Ended Input to Converter 4, typically Phase A Voltage Input
39	39	ADC9		ADC Input 9, Single-Ended Input to Converter 5, typically Phase B Voltage Input
40, 50–53	—	N.C.		No Connection
—	40	ADC10		ADC Input 10, Single-Ended Input to Converter 6, typically Phase C Voltage Input
42	42	V_{RTC}		RTC Battery Power
43	43	V_{BAT}		Primary Battery Voltage Input
44	44	V_{3P3D}		Bypass Point for Internal 3.3V Rail
45, 89	45, 89	V_{1P2}		1.2V Core Voltage Bypass
46	46	V_{DD}		Digital Power
47	47	RGND		Remote Ground
48	48	ADC3	RMT0N	ADC Input 3, Negative Input to Converter 1, typically Phase B Negative Current Input; Remote Interface 0 Negative Input
49	49	ADC2	RMT0P	ADC Input 2, Positive Input to Converter 1, typically Phase B Positive Current Input; Remote Interface 0 Positive Input
—	50	ADC5	RMT1N	ADC Input 5, Negative Input to Converter 2, typically Phase C Negative Current Input; Remote Interface 1 Negative Input
—	51	ADC4	RMT1P	ADC Input 4, Positive Input to Converter 2, typically Phase C Positive Current Input; Remote Interface 1 Positive Input
—	52	ADC7	RMT2N	ADC Input 7, Negative Input to Converter 3, typically Neutral Negative Current Input; Remote Interface 2 Negative Input
—	53	ADC6	RMT2P	ADC Input 6, Positive Input to Converter 3, typically Neutral Positive Current Input; Remote Interface 2 Positive Input
54	54	RVDD		Remote Power
56	56	MGPIO7	PULSEV/MP3	MAXQ GPIO Bit 7/CE Pulse V/MAXQ Meter Pulse 3
57	57	MGPIO6	PULSEW/MP2	MAXQ GPIO Bit 6/CE Pulse W/MAXQ Meter Pulse 2
58	58	MGPIO5	PULSEX/MP1	MAXQ GPIO Bit 5/CE Pulse X/MAXQ Meter Pulse 1
59	59	MGPIO4	PULSEY/MP0	MAXQ GPIO Bit 4/CE Pulse Y/MAXQ Meter Pulse 0
60	60	MGPIO3	MSCL1	MAXQ GPIO Bit 3/MAXQ I^2C SCL1
61	61	MGPIO2	MSDA1	MAXQ GPIO Bit 2/MAXQ I^2C SDA1
62	62	MGPIO1	MSCL0	MAXQ GPIO Bit 1/MAXQ I^2C SCL0

Pin Description (continued)

PIN (MAX71617)	PIN (MAX71637)	PRIMARY FUNCTION	SECONDARY FUNCTION	DESCRIPTION
63	63	MGPIO0	MSDA0	MAXQ GPIO Bit 0/MAXQ I²C SDA0
64	64	P1.12	SEG44	GPIO 1.12/LCD Segment 44
65	65	COM1		LCD Common Pin 1
66	66	COM3		LCD Common Pin 3
67	67	COM5		LCD Common Pin 5
68	68	P1.17	SEG49/TXD0/ SDA ARM	GPIO P1.17/LCD Segment 49/UART 0 Transmit Data/ Cortex I²C SDA
70	70	P1.18	RXD0/ SCL ARM	GPIO P1.18/UART 0 Receive Data/Cortex I²C SCL
71	71	P0.0	SEG0	GPIO P0.0/LCD Segment 0
72	72	P0.1	SEG1	GPIO P0.1/LCD Segment 1
73	73	P0.2	SEG2	GPIO P0.2/LCD Segment 2
74	74	P0.3	SEG3	GPIO P0.3/LCD Segment 3
75	75	P0.4	SEG4	GPIO P0.4/LCD Segment 4
76	76	P0.5	SEG5	GPIO P0.5/LCD Segment 5
77	77	P0.6	SEG6	GPIO P0.6/LCD Segment 6
78	78	P0.7	SEG7	GPIO P0.7/LCD Segment 7
79	79	P0.8	SEG8	GPIO P0.8/LCD Segment 8
82	82	P0.9	SEG9	GPIO P0.9/LCD Segment 9
83	83	P0.10	SEG10	GPIO P0.10/LCD Segment 10
84	84	P0.11	SEG11	GPIO P0.11/LCD Segment 11
85	85	P0.12	SEG12	GPIO P0.12/LCD Segment 12
86	86	P0.13	SEG13	GPIO P0.13/LCD Segment 13
87	87	P0.14	SEG14	GPIO P0.14/LCD Segment 14
88	88	V_{1P8}		1.8V Core Voltage Bypass
90	90	AMISOS	P0.15/SEG15	ARM SPI Slave MISO/GPIO P0.15/LCD Segment 15
91	91	AMOSIS	P0.16/SEG16	ARM SPI Slave MOSI/GPIO P0.16/LCD Segment 16
92	92	ASCKS	P0.17/SEG17	ARM SPI Slave SCK/GPIO P0.17/LCD Segment 17
94	94	ASSELS	P0.18/SEG18	ARM SPI Slave/SSEL GPIO P0.18/LCD Segment 18
95	95	P0.19	SEG19/ MISO MAXQ	GPIO P0.19/LCD Segment 19/MAXQ SPI MISO
96	96	P0.20	SEG20/ MOSI MAXQ	GPIO P0.20/LCD Segment 20/MAXQ SPI MOSI
97	97	P0.21	SEG21/ SSCK MAXQ	GPIO P0.21/LCD Segment 21/MAXQ SPI Clock
98	98	P0.22	SEG22/ SSEL MAXQ	GPIO P0.22/LCD Segment 22/MAXQ SPI Select
99	99	P0.23	SEG23/TXD5/ TMUX0	GPIO P0.23/LCD Segment 23/UART 5 Transmit Data/Test Multiplexer Output 0

Pin Description (continued)

PIN (MAX71617)	PIN (MAX71637)	PRIMARY FUNCTION	SECONDARY FUNCTION	DESCRIPTION
100	100	P0.24	SEG24/RXD5/ TMUX1	GPIO P0.24/LCD Segment 24/UART 5 Receive Data/Test Multiplexer Output 1
103	103	P0.25	SEG25/TXD4/ TMUXA	GPIO P0.25/LCD Segment 25/UART 4 Transmit Data/ Analog Test Multiplexer
104	104	P0.26	SEG26/RXD4	GPIO P0.26/LCD Segment 26/UART 4 Receive Data
105	105	ATDI	P0.27/SEG27	GPIO P0.27/LCD Segment 27/ARM Cortex-M3 TDI
106	106	ATDO	P0.28/SEG28	GPIO P0.28/LCD Segment 28/ARM Cortex-M3 TDO
107	107	ATMS	P0.29/SEG29	GPIO P0.29/LCD Segment 29/ARM Cortex-M3 TMS
108	108	ATCK	P0.30/SEG30	GPIO P0.30/LCD Segment 30/ARM Cortex-M3 TCK
109	109	ATRST	P0.31/SEG31	GPIO P0.31/LCD Segment 31/ARM Cortex-M3 TRST
110	110	MRST	MGPIO10	MAXQ GPIO Bit 10/MAXQ Reset (enabled when MAXQ JTAG active)
111	111	MTDI	MGPIO11	MAXQ JTAG TDI/MAXQ GPIO Bit 11
112	112	MTDO	MGPIO12	MAXQ JTAG TDO/MAXQ GPIO Bit 12
113	113	MTMS	MGPIO13	MAXQ JTAG TMS/MAXQ GPIO Bit 13
114	114	MTCK	MGPIO14	MAXQ JTAG TCK/MAXQ GPIO Bit 14
116	116	P1.0	SEG32	GPIO 1.0/LCD Segment 32
117	117	P1.1	SEG33	GPIO 1.1/LCD Segment 33
118	118	P1.2	SEG34	GPIO 1.2/LCD Segment 34
119	119	MGPIO8	TBA	MAXQ GPIO Bit 8/Timer A Output
120	120	MGPIO9	TBB	MAXQ GPIO Bit 9/Timer B Output

Pin Description (According to Function)

FUNCTION	PIN	DESCRIPTION
POWER		
V_{DD}	46	Primary Digital Power for the SoC. This pin provides power for the LCD DAC control logic and the main clock PLL, and indirectly through voltage regulators for all logic, memory and f ash, other than nonvolatile segments.
AVDD	37	Primary Analog Power for the SoC. This pin provides power for the ADC channels, the bandgap voltage reference and voltage comparators.
RVDD	54	Power for the Remote Interface Drivers
V_{IO}	12, 80, 101	Power for Output Drivers for All Digital Pins
V_{3P3D}	44	Bypass Point for the Internally Selected 3.3V Source. A switch in the SoC selects either V_{BAT} or V_{DD} to provide power to internal logic and regulators. Attach an appropriate capacitor to ground to this point. This pin also typically connects to the V_{IO} pins to provide nonvolatile power for the digital I/O section.

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
V_{BAT}	43	Primary Backup Battery Power. An internal switch selects this input to provide power to the digital logic section and main voltage regulators when V_{DD} is unavailable.
V_{RTC}	42	Backup Power for Nonvolatile Section. This battery is selected to provide power to the RTC, LCD RAM and the tamper detection subsystem should both V_{DD} and V_{BAT} fail.
V_{1P2}	45, 89	Bypass Point for the Internal 1.2V Core Regulator. Connect a good quality 0.1µF capacitor to each of these pins. Do not connect any load to this point.
V_{1P8}	88	Bypass Point for the Internal 1.8V Regulator for the Flash Memory Array. Connect a good quality 0.1µF capacitor to this pin. Do not connect any load to this point.
V_{LCD}	26	Bypass Point for Internal LCD Voltage (if the Internal LCD DAC is Selected). If external power is selected, this pin is the input point for power to the LCD waveform generators. The voltage applied to this pin should be no greater than V_{3P3D}, and in any event, no greater than 3.6V.
GND	13, 22, 55, 69, 81, 93, 102, 115	Digital Ground. Return point for all digital I/O.
AGND	32, 36, 41	Analog Ground. Reference point for all analog inputs.
RGND	47	Remote Ground. Return point for remote drivers.
CLOCK		
32KHZ OUT	31	Oscillator Output. Connect a 32.768kHz tuning fork crystal between this pin and the 32KHZ IN pin.
32KHZ IN	30	Oscillator Input. Connect a 32.768kHz tuning fork crystal between this pin and the 32KHZ OUT pin.
ANALOG		
ADC0	33	ADC Input 0, Positive Input to Converter 0, typically Phase A Positive Current Input. When using remote sensors, typically Neutral Positive Current Input.
ADC1	34	ADC Input 1, Negative Input to Converter 0, typically Phase A Negative Current Input. When using remote sensors, typically Neutral Positive Current Input.
ADC2	49	ADC Input 2, Positive Input to Converter 1, typically Phase B Positive Current Input
ADC3	48	ADC Input 3, Negative Input to Converter 1, typically Phase B Negative Current Input
ADC4	51	ADC Input 4, Positive Input to Converter 2, typically Phase C Positive Current Input
ADC5	50	ADC Input 5, Negative Input to Converter 2, typically Phase C Negative Current Input
ADC6	53	ADC Input 6, Positive Input to Converter 3, typically Neutral Positive Current Input
ADC7	52	ADC Input 7, Negative Input to Converter 3, typically Neutral Negative Current Input
ADC8	38	ADC Input 8, Single-Ended Input to Converter 4, typically Phase A Voltage Input
ADC9	39	ADC Input 9, Single-Ended Input to Converter 5, typically Phase B Voltage Input
ADC10	40	ADC Input 10, Single-Ended Input to Converter 6, typically Phase C Voltage Input
RMT0P	49	Remote Interface 0 Positive Input. The RMT0P and RMT0N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase A of a polyphase system.
RMT0N	48	Remote Interface 0 Negative Input. The RMT0P and RMT0N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase A of a polyphase system.
RMT1P	51	Remote Interface 1 Positive Input. The RMT1P and RMT1N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase B of a polyphase system.

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
RMT1N	50	Remote Interface 1 Negative Input. The RMT1P and RMT1N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase B of a polyphase system.
RMT2P	53	Remote Interface 2 Positive Input. The RMT2P and RMT2N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase C of a polyphase system.
RMT2N	52	Remote Interface 2 Negative Input. The RMT2P and RMT2N pins connect to the primary side of a pulse transformer to couple power and data to a 71M6xxx-type remote interface device. These pins typically connect to a current sensor on phase C of a polyphase system.
V_{REF}	35	Bypass Point for Internal Voltage Regulator. This pin should be connected only to a good quality 0.1µF capacitor and to no other node. In particular, it is recommended that this pin not be used to supply reference voltage to other devices.
SYSTEM		
RSTN	27	Active-Low System Reset. Asserting a low level on this pin resets the entire SoC. Connect this pin to a reset controller if one is used in the system; otherwise, connect the pin to V_{3P3D}. Note that no external reset is required; the device has an internal reset controller.
ATRST	109	JTAG TAP Controller Reset for the ARM Cortex-M3 core.
ATCK	108	JTAG Test Clock for the ARM Cortex-M3 core.
ATMS	107	JTAG Test Mode Select for the ARM Cortex-M3 core.
ATDO	106	JTAG Test Data Out for the ARM Cortex-M3 core.
ATDI	105	JTAG Test Data In for the ARM Cortex-M3 core.
MTCK	114	JTAG Test Clock for the MAXQ30 core.
MTMS	113	JTAG Test Mode Select for the MAXQ30 core.
MTDO	112	JTAG Test Data Out for the MAXQ30 core.
MTDI	111	JTAG Test Data In for the MAXQ30 core.
MRST	110	MAXQ30 Core Reset. This input is active only if the JTAG interface is enabled (TAP bit in the SC register). When asserted, program execution is forced to restart at 0x80 0000 in the utility RAM space.
GPIO		
P0.0	71	ARM Cortex-M3 GPIO Port 0 Bit 0
P0.1	72	ARM Cortex-M3 GPIO Port 0 Bit 1
P0.2	73	ARM Cortex-M3 GPIO Port 0 Bit 2
P0.3	74	ARM Cortex-M3 GPIO Port 0 Bit 3
P0.4	75	ARM Cortex-M3 GPIO Port 0 Bit 4
P0.5	76	ARM Cortex-M3 GPIO Port 0 Bit 5
P0.6	77	ARM Cortex-M3 GPIO Port 0 Bit 6
P0.7	78	ARM Cortex-M3 GPIO Port 0 Bit 7
P0.8	79	ARM Cortex-M3 GPIO Port 0 Bit 8
P0.9	82	ARM Cortex-M3 GPIO Port 0 Bit 9
P0.10	83	ARM Cortex-M3 GPIO Port 0 Bit 10

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
P0.11	84	ARM Cortex-M3 GPIO Port 0 Bit 11
P0.12	85	ARM Cortex-M3 GPIO Port 0 Bit 12
P0.13	86	ARM Cortex-M3 GPIO Port 0 Bit 13
P0.14	87	ARM Cortex-M3 GPIO Port 0 Bit 14
P0.15	90	ARM Cortex-M3 GPIO Port 0 Bit 15
P0.16	91	ARM Cortex-M3 GPIO Port 0 Bit 16
P0.17	92	ARM Cortex-M3 GPIO Port 0 Bit 17
P0.18	94	ARM Cortex-M3 GPIO Port 0 Bit 18
P0.19	95	ARM Cortex-M3 GPIO Port 0 Bit 19
P0.20	96	ARM Cortex-M3 GPIO Port 0 Bit 20
P0.21	97	ARM Cortex-M3 GPIO Port 0 Bit 21
P0.22	98	ARM Cortex-M3 GPIO Port 0 Bit 22
P0.23	99	ARM Cortex-M3 GPIO Port 0 Bit 23
P0.24	100	ARM Cortex-M3 GPIO Port 0 Bit 24
P0.25	103	ARM Cortex-M3 GPIO Port 0 Bit 25
P0.26	104	ARM Cortex-M3 GPIO Port 0 Bit 26
P0.27	105	ARM Cortex-M3 GPIO Port 0 Bit 27
P0.28	106	ARM Cortex-M3 GPIO Port 0 Bit 28
P0.29	107	ARM Cortex-M3 GPIO Port 0 Bit 29
P0.30	108	ARM Cortex-M3 GPIO Port 0 Bit 30
P0.31	109	ARM Cortex-M3 GPIO Port 0 Bit 31
P1.0	116	ARM Cortex-M3 GPIO Port 1 Bit 0
P1.1	117	ARM Cortex-M3 GPIO Port 1 Bit 1
P1.2	118	ARM Cortex-M3 GPIO Port 1 Bit 2
P1.3	3	ARM Cortex-M3 GPIO Port 1 Bit 3
P1.4	4	ARM Cortex-M3 GPIO Port 1 Bit 4
P1.5	5	ARM Cortex-M3 GPIO Port 1 Bit 5
P1.6	6	ARM Cortex-M3 GPIO Port 1 Bit 6
P1.7	7	ARM Cortex-M3 GPIO Port 1 Bit 7
P1.8	8	ARM Cortex-M3 GPIO Port 1 Bit 8
P1.9	9	ARM Cortex-M3 GPIO Port 1 Bit 9
P1.10	10	ARM Cortex-M3 GPIO Port 1 Bit 10
P1.11	11	ARM Cortex-M3 GPIO Port 1 Bit 11
P1.12	64	ARM Cortex-M3 GPIO Port 1 Bit 12
P1.13	14	ARM Cortex-M3 GPIO Port 1 Bit 13
P1.14	15	ARM Cortex-M3 GPIO Port 1 Bit 14
P1.15	16	ARM Cortex-M3 GPIO Port 1 Bit 15
P1.16	17	ARM Cortex-M3 GPIO Port 1 Bit 16
P1.17	68	ARM Cortex-M3 GPIO Port 1 Bit 17

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
P1.18	70	ARM Cortex-M3 GPIO Port 1 Bit 18
P1.19	19	ARM Cortex-M3 GPIO Port 1 Bit 19
P1.20	18	ARM Cortex-M3 GPIO Port 1 Bit 20
P1.21	21	ARM Cortex-M3 GPIO Port 1 Bit 21
P1.22	20	ARM Cortex-M3 GPIO Port 1 Bit 22
MGPIO0	63	MAXQ30 GPIO Bit 0
MGPIO1	62	MAXQ30 GPIO Bit 1
MGPIO2	61	MAXQ30 GPIO Bit 2
MGPIO3	60	MAXQ30 GPIO Bit 3
MGPIO4	59	MAXQ30 GPIO Bit 4
MGPIO5	58	MAXQ30 GPIO Bit 5
MGPIO6	57	MAXQ30 GPIO Bit 6
MGPIO7	56	MAXQ30 GPIO Bit 7
MGPIO8	119	MAXQ30 GPIO Bit 8
MGPIO9	120	MAXQ30 GPIO Bit 9
MGPIO10	110	MAXQ30 GPIO Bit 10
MGPIO11	111	MAXQ30 GPIO Bit 11
MGPIO12	112	MAXQ30 GPIO Bit 12
MGPIO13	113	MAXQ30 GPIO Bit 13
MGPIO14	114	MAXQ30 GPIO Bit 14
ARM CORTEX-M3 PERIPHERALS		
UART		
TxD0	68	UART Channel 0 Transmit Data
RxD0	70	UART Channel 0 Receive Data
TxD1	21	UART Channel 1 Transmit Data
RxD1	20	UART Channel 1 Receive Data
TxD2	19	UART Channel 2 Transmit Data
RxD2	18	UART Channel 2 Receive Data
TxD3	10	UART Channel 3 Transmit Data
RxD3	11	UART Channel 3 Receive Data
TxD4	103	UART Channel 4 Transmit Data
RxD4	104	UART Channel 4 Receive Data
TxD5	99	UART Channel 5 Transmit Data
RxD5	100	UART Channel 5 Receive Data
SMART CARD INTERFACE		
SCIO	5	Smart Card I/O
SCCLK	4	Smart Card Data Clock
SCRST	3	Smart Card Reset

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
I²C PORT		
ASDA	68	ARM Cortex-M3 I²C Serial Data Circuit
ASCL	70	ARM Cortex-M3 I²C Serial Clock Circuit
SPI PORTS		
AMOSI0	18	ARM Cortex-M3 SPI port 0—Master Out Slave In
AMISO0	19	ARM Cortex-M3 SPI port 0—Master In Slave Out
ASSEL0	20	ARM Cortex-M3 SPI port 0—Slave Select
ASCLK0	21	ARM Cortex-M3 SPI port 0—Serial Clock
AMOSI1	7	ARM Cortex-M3 SPI port 1—Master Out Slave In
AMISO1	6	ARM Cortex-M3 SPI port 1—Master In Slave Out
ASSEL1	9	ARM Cortex-M3 SPI port 1—Slave Select
ASCLK1	8	ARM Cortex-M3 SPI port 1—Serial Clock
AMOSIS	91	ARM Cortex-M3 SPI port 2—Master Out Slave In
AMISOS	90	ARM Cortex-M3 SPI port 2—Master In Slave Out
ASSELS	94	ARM Cortex-M3 SPI port 2—Slave Select
ASCLKS	92	ARM Cortex-M3 SPI port 2—Serial Clock
TIMERS		
ATCLK0	19	ARM Cortex-M3 Timer 0 I/O Pin
ATCLK1	18	ARM Cortex-M3 Timer 1 I/O Pin
ATCLK2	21	ARM Cortex-M3 Timer 2 I/O Pin
ATCLK3	20	ARM Cortex-M3 Timer 3 I/O Pin
MAXQ30 PERIPHERALS		
LCD		
COM0	24	LCD Common Output 0. If the LCD is enabled in any mode, this pin forms one of the common element drivers.
COM1	65	LCD Common Output 1. If the LCD is enabled in /2 mode or greater, this pin forms one of the common element drivers.
COM2	23	LCD Common Output 2. If the LCD is enabled in /3 mode or greater, this pin forms one of the common element drivers.
COM3	66	LCD Common Output 3. If the LCD is enabled in /4 mode or greater, this pin forms one of the common element drivers.
COM4	25	LCD Common Output 4. If the LCD is enabled in /6 mode, this pin forms one of the common element drivers.
COM5	67	LCD Common Output 5. If the LCD is enabled in /6 mode, this pin forms one of the common element drivers.
SEG0	71	LCD Segment Driver 0
SEG1	72	LCD Segment Driver 1
SEG2	73	LCD Segment Driver 2
SEG3	74	LCD Segment Driver 3

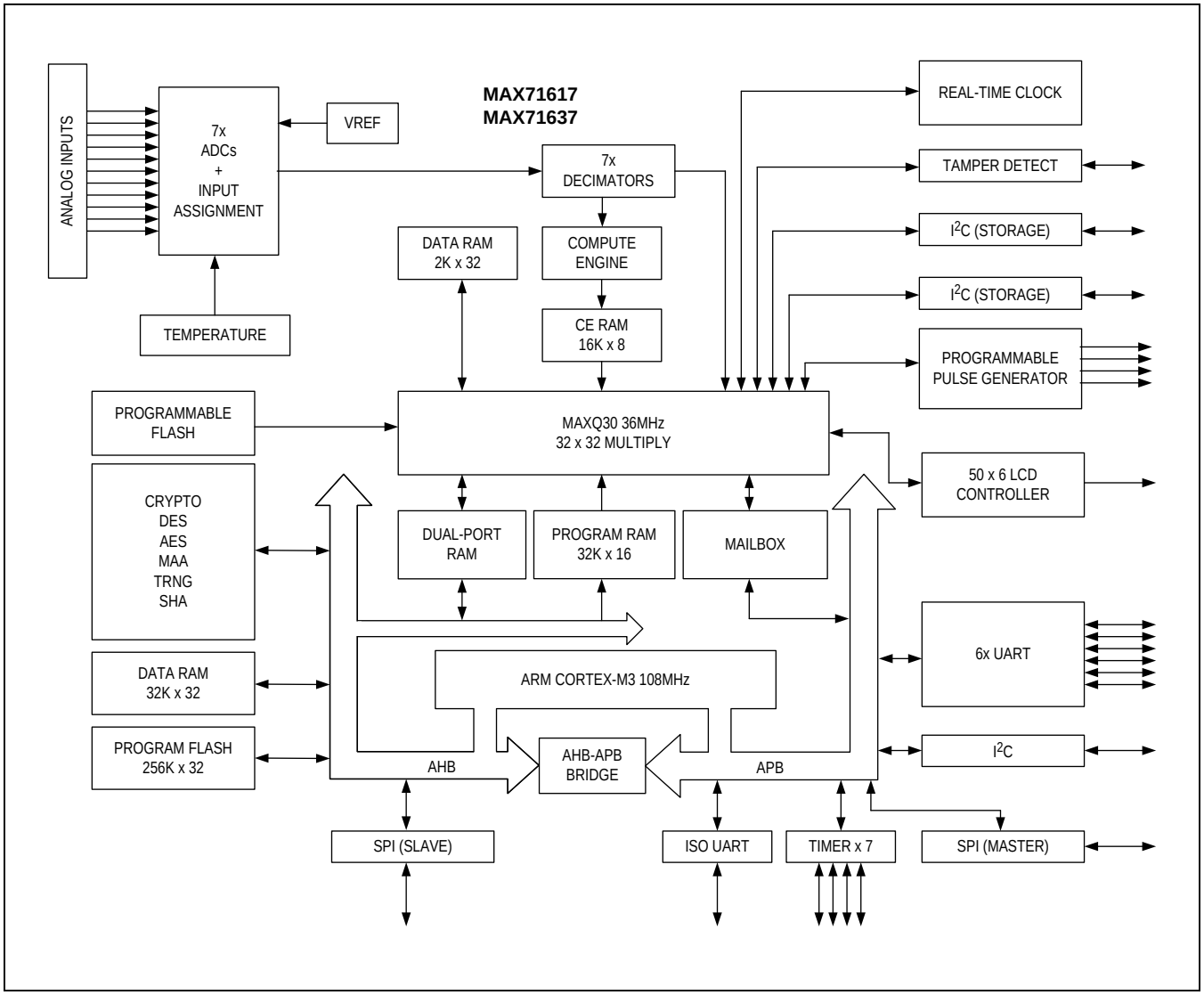
Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
SEG4	75	LCD Segment Driver 4
SEG5	76	LCD Segment Driver 5
SEG6	77	LCD Segment Driver 6
SEG7	78	LCD Segment Driver 7
SEG8	79	LCD Segment Driver 8
SEG9	82	LCD Segment Driver 9
SEG10	83	LCD Segment Driver 10
SEG11	84	LCD Segment Driver 11
SEG12	85	LCD Segment Driver 12
SEG13	86	LCD Segment Driver 13
SEG14	87	LCD Segment Driver 14
SEG15	90	LCD Segment Driver 15
SEG16	91	LCD Segment Driver 16
SEG17	92	LCD Segment Driver 17
SEG18	94	LCD Segment Driver 18
SEG19	95	LCD Segment Driver 19
SEG20	96	LCD Segment Driver 20
SEG21	97	LCD Segment Driver 21
SEG22	98	LCD Segment Driver 22
SEG23	99	LCD Segment Driver 23
SEG24	100	LCD Segment Driver 24
SEG25	103	LCD Segment Driver 25
SEG26	104	LCD Segment Driver 26
SEG27	105	LCD Segment Driver 27
SEG28	106	LCD Segment Driver 28
SEG29	107	LCD Segment Driver 29
SEG30	108	LCD Segment Driver 30
SEG31	109	LCD Segment Driver 31
SEG32	116	LCD Segment Driver 32
SEG33	117	LCD Segment Driver 33
SEG34	118	LCD Segment Driver 34
SEG35	3	LCD Segment Driver 35
SEG36	4	LCD Segment Driver 36
SEG37	5	LCD Segment Driver 37
SEG38	6	LCD Segment Driver 38
SEG39	7	LCD Segment Driver 39
SEG40	8	LCD Segment Driver 40
SEG41	9	LCD Segment Driver 41

Pin Description (According to Function) (continued)

FUNCTION	PIN	DESCRIPTION
SEG42	10	LCD Segment Driver 42
SEG43	11	LCD Segment Driver 43
SEG44	64	LCD Segment Driver 44
SEG45	14	LCD Segment Driver 45
SEG46	15	LCD Segment Driver 46
SEG47	16	LCD Segment Driver 47
SEG48	17	LCD Segment Driver 48
SEG49	68	LCD Segment Driver 49
I²C PORTS		
MSDA0	63	MAXQ30 I²C Channel 0 Serial Data Circuit
MSCL0	62	MAXQ30 I²C Channel 0 Serial Clock Circuit
MSDA1	61	MAXQ30 I²C Channel 1 Serial Data Circuit
MSCL1	60	MAXQ30 I²C Channel 1 Serial Clock Circuit
SPI PORT		
MMOSI	96	MAXQ30 SPI Master Out Slave In
MMISO	95	MAXQ30 SPI Master In Slave Out
MSSEL	98	MAXQ30 SPI Slave Select
MSCLK	97	MAXQ30 SPI Serial Clock
METER PULSE OUTPUTS		
WPULSE	57	Meter Pulse W Output. Typically used for real energy output (Watts). Can be directly generated from compute engine or by the MAXQ30 core.
VPULSE	56	Meter Pulse V Output. Typically used for reactive energy output (VARs). Can be directly generated from compute engine or by the MAXQ30 core.
XPULSE	58	Meter Pulse X Output. Typically used to indicate a zero-crossing event on a voltage input. Can be directly generated from compute engine or by the MAXQ30 core.
YPULSE	59	Meter Pulse Y Output. Typically used to indicate voltage sag on one of the voltage inputs. Can be directly generated from compute engine or by the MAXQ30 core.
TAMPER DETECTION		
TMPDOUT0	2	Tamper Detect Channel 0 Output
TMPDIN0	28	Tamper Detect Channel 0 Input
TMPDOUT1	1	Tamper Detect Channel 1 Output
TMPDIN1	29	Tamper Detect Channel 1 Input
TIMER		
TBA	119	MAXQ30 Timer I/O Pin A. When conf gured as an input, this pin provides a clock that can be used to increment the counter on each selected clock edge. When conf gured as an output, this pin can be used to generate a square wave that toggles on each timer match.
TBB	120	MAXQ30 Timer I/O Pin B. This pin is an input to the timer module used for multiple purposes, depending on the timer conf guration. It can be used to reload the counter, to reverse the direction of count or to trigger an interrupt. In PWM modes, this pin outputs the PWM signal.

Functional Diagram



Detailed Description

Description

The MAX71617/MAX71637 are systems-on-chip (SoCs) for next-generation electricity meters placed on the smart grid. The MAX71617/MAX71637 provide three high-performance computing cores: an industry-standard ARM Cortex-M3 core for handling communication and other supervisory functions, a 32-bit MAXQ30 core for general metering functions, and a programmable compute engine (CE) to handle signal processing tasks.

The use of multiple cores in this way makes it easy to separate metering and billing functions that can be regulated by local or national authorities from the administrative and communications functions that typically are unregulated. The MAXQ30 core receives data from the compute engine and manages the energy accumulation process, the LCD and the meter pulse outputs, while the ARM core handles bulk storage and communications over the various UART channels.

ARM Core Overview

The ARM Cortex-M3 core is a low-power 32-bit RISC core, widely used for embedded applications. In the MAX71617/MAX71637, the application core is coupled to 1MB of flash memory, 128KB of static RAM (two 64KB blocks), and a number of peripherals for communication and external device control.

The ARM Cortex-M3 core provides services such as communication management and usage reporting. The MAX71617/MAX71637 are designed to allow this core (the application core) to manage relatively risky operations such as communication over an insecure link, while permitting the more sensitive operations, such as energy measurement and accumulation, to proceed on a more secure microcontroller (the metering core).

The ARM Cortex-M3 core controls the following peripherals:

- Up to 55 GPIO pins
- Up to six full-duplex UARTs
- Seven configurable general-purpose timers, four with optional output pins
- One I^2C port, configurable as a master or slave
- Three SPI ports: two configurable as a master or slave, and one permanently configured as a slave
- One smart card interface
- A block of cryptographic peripherals

The ARM Cortex-M3 core communicates with the MAXQ30 metering core by means of a mailbox scheme by which it can leave messages for and retrieve data from the metering core. Additionally, the cores can exchange bulk data by means of a 4KB shared RAM block.

Note that there is no direct hardware control of the MAXQ30 metering core by the ARM Cortex-M3 application core. The application core can only request services from the metering core, and service requests are rejected unless they are properly formatted. This reduces the likelihood of rogue code running in the ARM Cortex-M3, corrupting the operation of critical metering functions being performed in the MAXQ30 core.

MAXQ30 Core

The 32-bit MAXQ30 core is a Harvard architecture microcontroller core well-suited for low-power signal processing. Because the instruction bus is separate from the data bus, most instructions execute in one cycle.

The MAXQ30 core is coupled to a single-cycle 32-bit multiply/accumulate unit. Because of the transfer-triggered nature of the MAXQ30 core, the DSP core is completely static and only the active modules of the core consume power when operating. When the core is idle, it can be unclocked and draws only leakage current.

The MAXQ30 core contains no ROM or flash memory. Instead, the program store is implemented as fast static RAM. This means that the MAXQ30 core cannot begin running code before the ARM core has loaded its program store. See the Security section for details on this mechanism.

The purpose of the MAXQ30 core is to isolate critical metering functions into a separate core that does not directly communicate over potentially unsecured communication channels. Since programs running on the MAXQ30 core can choose how to respond (or not respond) to messages arriving from the ARM Cortex-M3 application core, the likelihood of hacking by outside threats is reduced.

The MAXQ30 core manages the following peripherals:

- Up to 14 GPIO pins
- The LCD controller capable of controlling up to 300 segments (6 x 50).
- A time-of-day clock with alarm functions
- Two I^2C ports. These ports can be used for any purpose, but typically are configured so that one I^2C port manages external nonvolatile storage for measured energy while the other I^2C port might be configured for management of an external LCD controller, if needed.

- One SPI master/slave
- Four programmable meter pulse generators
- One programmable timer

In addition, the MAXQ30 core configures and manages the AFE. It also controls the compute engine, although this control is typically limited to setting up the AFE and the compute engine such that the compute engine runs whenever a new set of samples are available in the CE RAM.

Intercore Communications

The application core and the MAXQ30 metering core must communicate with one another to transfer configuration data as well as metrology results. This communication is handled by a small block of memory that appears as registers to the MAXQ30 processor and as standard RAM to the application core. A larger block of memory is reserved to transfer complete vectors of acquired samples from any input channel.

The application core typically starts a transfer by writing a code to the MREQ (Master REQuest) register. This action sets a flag toward the MAXQ30 core that can serve as an interrupt source. The MAXQ30 core performs the requested action and loads the results into the SRSP (Slave ReSPonse) register, setting a bit toward the application core. The application core can then retrieve the results.

For results that occupy more than the 32-bits available in the slave response register, the MAX71617/MAX71637 provide a 4KB buffer that can be assigned to either the application core or the metering core at any particular time. The MAXQ30 metering core controls the ownership of the RAM block. In typical use, the application core makes a request for bulk data, the metering core populates the buffer and transfer control to the application core before loading a status value in the slave response register. Once the application core has recovered the data, the buffer ownership can be transferred back to the metering core.

In addition to metrology results, intercore communications are also used to transfer cryptographic blocks from the MAXQ30 metering core and the ARM Cortex-M3 application core. The actual crypto hardware is physically in the domain of the application core. When the metering core requires cryptographic services, it can place a request in the mailbox to request encryption services of the application core.

ADC

The MAX71637 provides seven 24-bit ΔΣ ADC channels, and the MAX71617 provides four ADC channels.

In the MAX71637, the channels can be dynamically configured into multiple arrangements so that external pins can be flexibly routed to particular ADC channels. By default, the ADCs are arranged so that the three current inputs drive dedicated ADC channels, and the neutral current input drives its own dedicated ADC channel. The three voltage inputs are sensed by the remaining three ADC channels. Further arrangements are possible, including routing all signals to a single multiplexed ADC channel and turning off all other ADC channels.

In the MAX71617, two input are dedicated to current channels (for line and neutral current to support tamper detection) and two channels are dedicated to two phase voltages. This arrangement permits the single-phase version of the SoC to operate in standard single-phase (equation 0), split-phase (equation 1) and applications with two independent voltages (equation 2).

In the MAX71637, the connections between the eleven input pins and the actual inputs to the ADC channels are made through input multiplexers attached to each ADC channel. Additionally, the multiplex connections can be optionally configured on a time-slot basis if it is not desired to use dedicated ADCs. Input assignments are configurable and depend on code running on the compute engine to determine how inputs are assigned to ADC channels.

Remote Interfaces

The MAX71637 provides three analog input pin pairs (ADC0-1, ADC2-3, and ADC4-5), and the MAX71617 provides two analog input pin pairs (ADC0-1 and ADC2-3) that are configurable to support remote interfaces.

The MAX71617/MAX71637 metering SoC devices support 71M6000 series single-channel remote interfaces. The 71M6000 remote interface permits the connection of nonisolated current sensors (such as resistive shunts) to the SoC. In a typical usage scenario, the MAX71637 is referenced to the neutral point in a three-phase wye system, with voltage monitored by means of conventional resistive divider networks on each phase and current monitored by means of shunts connected through three 71M6000-series interfaces and their associated pulse transformers.

The 71M6000 interfaces receive power from the SoC by means of power pulses that are inserted into the data stream. These current pulses are coupled to the remote interfaces by means of a pulse transformer that also provides isolation to the circuit. Data from the 71M6000 is coupled back to the SoC by means of the same transformer. The MAX71617/MAX71637 SoCs contain a set of FIR decimation filters that convert the bit stream from the remote interfaces into usable current samples.

Refer to the 71M6103/71M6113/71M6201/71M6203/71M 71M6601/71M6603 data sheet for more information about the remote interfaces and how to use them.

Compute Engine

The MAX71617/MAX71637 provide a dedicated, 32-bit fixed-point compute engine to perform the initial processing of received samples and to convert them into increments of real and reactive energy. The compute engine runs every time the ADC deposits a set of samples into CE RAM. From time to time (typically once per second) the CE notifies the MAXQ30 core that it should retrieve data for long-term accumulation. The compute engine also calculates ancillary values such as per-phase RMS voltage and current, line frequencies, and phasor angles between phases.

The code for compute engine is stored in volatile RAM during operation. On power-up, the RAM must be loaded by the ARM Cortex-M3 application core prior to releasing the compute engine to run.

To ensure the integrity of the code running on the compute engine, the MAXQ30 metering core can periodically perform a verification of the compute engine code base. This involves no performance penalty since the compute engine, the MAXQ30 core and the AFE share access to the common memory block on a time-interleaved basis. Code running on the MAXQ30 can be checked by routines in the utility RAM.

Silergy provides CE code for most common configurations of load connections, pulse generation schemes, harmonic analysis and current and voltage sensors. Alternately, the compute engine can be completely disabled and the MAXQ30 core can provide per sample processing services.

Temperature Sensor

The MAX71617/MAX71637 provide a built-in temperature sensor that determines the temperature of the semiconductor die. This temperature sensor is periodically connected to one of the ADC channels to record the die temperature. The value determined by the ADC is then used to compensate the on-chip bandgap voltage reference for variations due to temperature.

LCD

The MAX71617/MAX71637 provide a 50-segment, 6-common LCD controller peripheral.

A display is essential to an electricity meter. Also under many regulatory structures, the display must be logically separate from the communications process to prevent malicious attacks that might cause the meter to display incorrect information.

The LCD controller is managed by the MAXQ30 metering processor. Since the MAXQ30 processor has no direct connection to the communications mechanisms, the LCD is guaranteed to be logically separated at all times from the network.

For applications that do not require strict separation between communications and display, a small piece of software can be loaded into the MAXQ30 core that allows the ARM core to directly write display contents to memory. The data thus written is then picked up by the MAXQ30 core and directly transferred to the display controller.

Real-Time Clock

Like the LCD, the real-time clock is considered a critical component that must be segregated from the communications media. The real-time clock is a peripheral of the MAXQ30 core and is managed by sending commands from the application core to software running on the MAXQ30 core. The software can validate the commands before making changes to the time-of-day clock.

The clock itself uses a standard tuning-fork crystal as its timebase. The crystal is always allowed to operate at its natural frequency. Corrections to the timebase are applied digitally by inserting or deleting half-cycles of the crystal's natural frequency to achieve a long-term average of a 32,768Hz nominal frequency.

UART

The MAX71617/MAX71637 provide six UART peripherals. Each UART is connected into the application core in order to maintain the segregation of functional elements between the application core and the metering core. Each UART has its own baud rate generator based around the principle of the phase accumulator. This type of baud rate generator assures the most accurate timing at high baud rates.

The primary UART channel includes hardware to assist with amplitude modulated infrared (IR) based readers. The UART contains an independent timer that generates a carrier signal in the range of 10kHz to 500kHz. The carrier signal can be transmitted during either mark or space times, with the alternate signal level being represented by either a 1 or a 0 level.

I2C

The application core of the MAX71617/MAX71637 provide one I2C peripheral, and the MAXQ30 metering core provides two I2C peripherals.

I2C is frequently used to control external memory devices and display drivers. All I2C peripherals in the MAX71617/MAX71637 support master and slave mode, and obey standard protocol practices such as clock stretching.

The two I2C ports on the MAXQ30 core can be used for any purpose, but are recommended as connections to external flash memory for storage of metrology values and for an external display controller. Two ports are provided so that a single failure cannot disable both peripherals.

SPI

The MAX71617/MAX71637 provide four SPI peripherals: three on the ARM Cortex-M3 application core, and one on the MAXQ30 metering core.

Two of the three application-core SPI channels serve as a master or slave. SPI masters generate the SPI clock and drive the slave select (SSEL) circuit. When configured as a slave, the SPI channels expect an external master to provide the clock and to drive the SSEL circuit. The third SPI channel is configured as slave only.

The SPI controller on the MAXQ30 metering core can be configured as master or slave, and can be configured for eight-bit or sixteen-bit operation.

Smart Card

The MAX71617/MAX71637 provide an ISO7816-compatible UART that supports an interface to a smart card. If a 3.3V-compatible card is used, the pins may be able to be used directly (with appropriate protection for ESD). The port can also be used with smart card interface ICs that provide level shifting and circuit protection.

Contact Silergy orappropriate smart card interface devices that can be used with the MAX71617/MAX71637.

Tamper Detection

The MAX71617/MAX71637 provide two active tamper detection channels.

Active tamper detection means that the device generates a pseudo-random bit sequence and drives that bit sequence through external circuitry. After passing through external switches or perhaps through a metal foil serpentine mesh, the signal returns to an input that compares the received signal to the transmitted signal. If the signals differ, a tamper event is declared and the MAXQ30 metrology processor is interrupted.

This scheme differs from simply assigning a GPIO port for tamper detection because it resists simply pulling the pin high or low to force the processor to ignore a tamper event. Two separate circuits provide the possibility to issue a warning when the first seal is breached, and a higher alert level when a further breach has occurred.

On either tamper detection event, the MAXQ30 metering core can be interrupted. The metering core can then send a signal to the application core so that the tamper event can be logged and reported. The tamper detect circuitry operates on the nonvolatile power domain, so that tamper events can be configured to wake the metering core even when the device is in sleep mode.

Timers

The ARM Cortex-M3 application core provides seven programmable timers. These timers are uncommitted and can be used for any purpose, including the support of multitasking operating systems. Four of the timers have outputs that can be routed to external pins.

In addition to the timers attached to the application core, one programmable timer is attached to the MAXQ30 core for general use, including PWM applications.

Meter Pulse Generation

Meter pulse generation is a critical function during calibration and, in some cases, to support the metering function itself. The MAX71617/MAX71637 provide four programmable precision pulse generators to provide pulse generation services independent of either the application core or the metering core.

While there are four pulse outputs, there are actually eight pulse generators. Four of these programmable pulse generators are built into the compute engine and are active when the CE is used to perform the basic metrology tasks. When operating in this mode, the metering core only manages pulse configuration and meter constants.

When the CE is disabled and the MAXQ30 core is handling DSP tasks, the set of programmable pulse generators assigned to the MAXQ30 are used. In any event, the pulse outputs are always mapped to the same set of external pins.

Security

Security in the MAX71617/MAX71637 SoC means several things:

- **Communications security:** messages transmitted by the SoC cannot be intercepted by others. Messages to the SoC cannot be forged by an impostor.
- **Data security:** Data stored in external media (e.g., I^2C or SPI connected EEPROM) is stored in such a way that even if the device is removed from the meter, the data stored on the device cannot be used. Conversely, billing data stored in an external EEPROM is encrypted and authenticated to prevent attackers from installing devices preloaded with fraudulent data.
- Software security: Software loaded onto the ARM Cortex-M3 core is executed only if it is appropriately signed by a party with a secret key corresponding to a public key stored in the SoC. The secret key can be loaded by the customer using provided software, or can be loaded by Silergy at final test. And since the ARM core loads the MAXQ30 core on each reset event, the software for the MAXQ30 core and the compute engine is implicitly protected.
- **Metrology security:** Accumulated energy usage and other metrology results can be embedded in a security envelope. This envelope can be passed through the communication protocol layers so that the end recipient can be sure the results are authentic.
- **Physical security:** A dynamic tamper detection system ensures that if the meter is tampered with, the SoC records the event and takes appropriate countermeasures. These can include everything from alerting an operator to destroying cryptographic keys to render the meter inert.

To support these security features, the MAX71617/MAX71637 provide the following cryptographic and security-related resources:

- **Encryption engines:** MAX71617/MAX71637 provide DES, 3DES, and AES encryption engines. These facilities provide fast encryption and decryption services for either communication security or protection of data stored in external memory devices.
    - **AES:** AES is a modern block cipher that uses a 128-bit or 256-bit key and operates on a 128-bit cipher block. AES combines four logical operations that involve mixing and substitution over 14-18 rounds to convert a plain-text block to a cipher block under control of the key. At the time of this writing, AES is considered secure.
    - **DES:** DES is a block cipher, published in 1977, that although still in wide use is now largely deprecated. It has a 56-bit key and a 64 bit cipher block size. DES is provided in the MAX71617/MAX71637 to support legacy applications; its 56-bit key is considered too short for modern cryptographic security and the US government has withdrawn the single-key version of DES as a standard as of 2005. Triple-DES (3DES), which encrypts data with three rounds of the DES algorithm using two or three 56-bit keys is still considered secure, but not as secure as AES. Both two-key and three-key 3DES are fully supported in the MAX71617/MAX71637.
- **Secure hash:** The MAX71617/MAX71637 provide a secure hash generator that is compatible with SHA-1 to SHA-512 standards. The secure hash engine provides a 160- to 512-bit message digest of a data set in such a way that it is infeasible to create a second data set that produces an identical hash.
- **Modular arithmetic accelerator:** The MAX71617/MAX71637 provide a modular arithmetic accelerator (MAA). The MAA provides hardware acceleration for popular cryptosystems such as elliptic-curve cryptography (ECC) and asymmetric-key cryptosystems such as RSA. Many modern encryption algorithms work by operating over a finite integer field. Performing computations in a large finite field is difficult and time-consuming for general purpose microcontrollers.. The MAA computes the result of common arithmetic functions (sum, additive inverse, product, multiplicative inverse, exponentiation) in an integer field of size up to 2,048 bits.
- **True random number generator:** The MAX71617/MAX71637 provide a true random number generator which is used to generate one-time keys that secure communications sessions. The entropy source of the true random number generator is derived from the outputs of three unsynchronized counters that are non-linearly mixed to produce an output that is verifiably random.
- **Tamper detection:** The MAX71617/MAX71637 provide four tamper detect pins (two input/output pairs) protect the physical security of the meter. The output pin of each pin pair presents a pseudo-random bit sequence that is hard for an observer to predict. The input pin of each pin pair presents the detected signal to internal logic. This internal logic compares the received signal to the signal presented on the output pin, and provides an alert if the signals significantly

differ from each other. Each tamper detection pair can be configured to provide a response to a confirmed tamper event that may range from latching an output to illuminate a tamper indicator, to sending a message to the network, to making a log entry all the way to destroying the keys and becoming inert.

- **Resource Protection Unit (RPU):** Resources on the peripheral bus of the ARM Cortex-M3 are protected by hardware. The RPU implements a protection matrix that defines which peripheral or resource can be used by a particular process.

ARM Cortex-M3 Details

The ARM Cortex-M3 application core is a 32-bit RISC microcontroller that supports the widely-used ARM instruction set. In the MAX71617/MAX71637, the ARM Cortex-M3 operates at a nominal frequency of 108MHz. The processor clock to the ARM Cortex-M3 can be divided by 1, 2, 4, and 8 to provide effective clock frequencies of 108MHz, 54MHz, 27MHz, and 13.5MHz.

The application core has access to 1MB of flash memory and 128KB of RAM for its own use, with other memory blocks shared with the other processor cores.

The 1MB flash memory block appears to the processor as 256K x 32. Internally, the flash memory is organized as 64K x 128, but it supports programming one longword (32 bits) at a time. The flash controller can be accessed by user code to perform in-system updates to the flash program, if desired. Like all peripherals, the flash controller can be protected by the RPU so that only authorized software can perform flash upgrades.

The 128KB of RAM is provided as two blocks: one 64K block of code RAM and a second 64K block of system RAM. The system RAM block has a bit-band alias to support RAM bit operations.

In addition to the code RAM and system RAM, the application core has conditional access to four additional memory blocks: the MAXQ30 program RAM, the MAXQ30 page RAM, the CE RAM, and a shared RAM block. The MAXQ30 program RAM and page RAM are used to contain software for the MAXQ30 metering core. The 64KB program RAM block is loaded once by the application core, then assigned for exclusive access to the MAXQ30 core; the 16KB page RAM can be loaded and reloaded by the application core as requirements change. The CE RAM is also loaded by the application core and is assigned to shared access by the MAXQ30 metering core and the compute engine. Finally, the shared RAM block is used to communicate data blocks between the metering core and the application core as an adjunct to the mailbox system.

See Table 1 for all addresses and lengths, which are expressed in bytes.

Table 1. ARM Cortex-M3 Memory Map

LOCATION	LENGTH	NAME	DESCRIPTION
MEMORY SEGMENT			
0x0000 0000	1M	Code Flash	Primary code memory for the ARM Cortex-M3
0x0040 0000	64K	Code SRAM	
0x2000 0000	64K	System SRAM	
0x2200 0000	32M	Bit Band Alias for System SRAM	
PERIPHERAL SEGMENT			
0x4000 0000	4K	GPIO 0	
0x4000 1000	4K	GPIO 1	
0x4001 0000	4K	Timer 0	General-purpose 32-bit timer
0x4001 1000	4K	Timer 1	General-purpose 32-bit timer
0x4001 2000	4K	Timer 2	General-purpose 32-bit timer
0x4001 3000	4K	Timer 3	General-purpose 32-bit timer
0x4001 4000	4K	Timer 4	General-purpose 32-bit timer
0x4001 5000	4K	Timer 5	General-purpose 32-bit timer
0x4001 6000	4K	Timer 6	General-purpose 32-bit timer

Table 1. ARM Cortex-M3 Memory Map (continued)

LOCATION	LENGTH	NAME	DESCRIPTION
0x4002 0000	4K	UART 0	UART with IR modulator
0x4002 1000	4K	UART 1	General purpose UART
0x4002 2000	4K	UART 2	General purpose UART
0x4002 3000	4K	UART 3	General purpose UART
0x4002 4000	4K	UART 4	General purpose UART
0x4002 5000	4K	UART 5	General purpose UART with debug capability
0x4002 8000	4K	SPI 0	SPI Master
0x4002 9000	4K	SPI 1	SPI Master
0x4003 0000	4K	I^2C 0	I^2C Master
0x4003 8000	4K	Smart Card	
0x4004 0000	4K	Watchdog Timer	
0x4006 0000	4K	DMA Controller	
0x4006 1000	4K	Flash Controller	
0x4006 2000	4K	Cache Controller	
0x4006 4000	4K	Mailbox	ARM-MAXQ30 communications
0x4007 0000	4K	Crypto Engine	
0x4007 1000	4K	True Random Number Generator	
0x4007 2000	4K	Modular Arithmetic Accelerator	
0x400A 0000	4K	Global control	
0x400A 1000	4K	Resource Protection Unit	
0x400A 2000	4K	System Initialization	
0x400A 3000	4K	CRC/Checksum	
0x4010 0000	4K	MAXQ30 Shared RAM	Shared RAM segment for MAXQ30-ARM Cortex M3 coordination.
0x4011 0000	16K	MAXQ30 Page RAM	Swappable code segment to allow MAXQ30 core to page in new code.
0x4012 0000	64K	MAXQ30 Program RAM	Primary MAXQ30 code space. Read/write by ARM Cortex M3 when MAXQ30 core is held at reset.
0x4013 0000	16K	CE RAM	Primary compute engine memory segment. Writable by ARM Cortex M3 only when MAXQ30 core is held at reset.
0x4200 0000	32M	Bit Band Alias for Peripheral Segment	

MAXQ30 Core Details

The MAXQ30 core in the MAX71617/MAX71637 manages sensitive peripherals, executes signal-processing related tasks, and performs general metering-related housekeeping functions.

The MAXQ30 core is a 32-bit RISC core running at 36MHz. In addition to its rich peripheral complement, the MAXQ30 core also manages a number of RAM blocks.

MAXQ30 Core Peripherals

Unlike the ARM architecture, peripheral devices in the MAXQ30 do not reside in the general memory map. Instead, peripheral devices are first-class data objects and reside in register modules along with CPU registers, accumulators, and other core components of the microcontroller.

Table 2 provides information about the peripheral complement available to the MAXQ30 core. For details about these peripherals, how to set them up, and how to use them, refer to the MAX71617/MAX71637 User's Guide.

Table 2. RAM Block Management

RAM BLOCK	SIZE	DESCRIPTION
Data Memory	8KB	This is the general-purpose working RAM block for the MAXQ30 core. It appears at 0x00 0000 in the data space map and is automatically mapped into code space at 0xA0 0000.
Page Memory	16KB	The page memory is an auxiliary program segment for the MAXQ30 core. The ARM Cortex-M3 can load specialized, transient subroutines in this memory segment and then remove them as required. If assigned to the MAXQ30 core, it appears in the program space at location 0x00 8000.
Shared Memory	4KB	The shared memory is a region that can be arbitrarily handed between the ARM Cortex-M3 application core and the MAXQ30 metering core. The MAXQ30 core controls the ownership of the memory. Note that this is not true dual-port memory, since only one core at a time has read-write privilege to the memory segment. If mapped to the MAXQ30 core, it appears in data space at byte address 0x00 2000.
Program Memory	64KB	This is the primary code memory for the MAXQ30 core. It is loaded by the ARM Cortex-M3 core at startup, and then is locked to the MAXQ30 core so that code can run from the memory segment. It appears in code space at address 0x00 0000.
CE Memory	16KB	The CE memory block is initially loaded by the ARM Cortex-M3 core at startup. It contains the CE program (generally provided by Silergy) and is accessible o a time-interleaved basis to the compute engine, the MAXQ30 core and the ADC block. The CE acts as a coprocessor and converts raw ADC samples to energy units for the MAXQ30 core to further accumulate and process.
Utility Memory	8KB	The utility memory block contains utility functions that support the pseudo-Von Neumann architecture of the MAXQ30 core, debug functions and other ancillary functions. Once loaded, the utility memory behaves as ROM, blocking all write attempts to the memory segment. It appears in code space at address 0x80 0000.

Table 3. Peripherals Available to the MAXQ30 Core

MODULE 0		
I²C 0 (STORAGE)		
REG	**REG NAME**	**DESCRIPTION**
0	I2C0CN	I²C Control
1	I2C0INT	I²C Interrupt Conf guration
2	I2C0ST	I²C Status
3	I2C0DATA	I²C Data
4	I2C0MCN	I²C Master Conf guration
8	I2C0RX	I²C Receive
9	I2C0RXCFG	I²C Receive Conf guration
10	I2C0TX	I²C Transmit
11	I2C0TXCFG	I²C Transmit Conf guration
12	I2C0SLA	I²C Slave Address
13	I2C0CKH	I²C Clock Divide High
14	I2C0CKL	I²C Clock Divide Low
15	I2C0HSCK	I²C High-Speed Clock Conf guration
16	I2C0TO	I²C Timeout Counter
17	I2C0FIFO	I²C FIFO Control
SPI		
REG	**REG NAME**	**DESCRIPTION**
5	SPICN	SPI Control
6	SPIST	SPI Status
7	SPIB	SPI Data Buffer
18	SPICF	SPI Conf guration
19	SPICK	SPI Clock
TEST		
REG	**REG NAME**	**DESCRIPTION**
31	TM	Reserved (system register)
JTAG		
REG	**REG NAME**	**DESCRIPTION**
24	ICDT0	In-Circuit Debug Temporary 0
25	ICDT1	In-Circuit Debug Temporary 1
26	ICDC	In-Circuit Debug Control
27	ICDF	In-Circuit Debug Flag
28	ICDB	In-Circuit Debug Buffer
29	ICDA	In-Circuit Debug Address
30	ICDD	In-Circuit Debug Data

MODULE 1		
I²C 1 (DISPLAY)		
REG	**REG NAME**	**DESCRIPTION**
0	I2C1CN	I²C Control
1	I2C1INT	I²C Interrupt Conf guration
2	I2C1ST	I²C Status
3	I2C1DATA	I²C Data
4	I2C1MCN	I²C Master Conf guration
8	I2C1RX	I²C Receive Data
9	I2C1RXCFG	I²C Receive Conf guration
10	I2C1TX	I²C Transmit Data
11	I2C1TXCFG	I²C Transmit Conf guration
12	I2C1SLA	I²C Slave Address
13	I2C1CKH	I²C Clock Divide High
14	I2C1CKL	I²C Clock Divide Low
15	I2C1HSCK	I²C High-Speed Clock Conf guration
16	I2C1TO	I²C Timeout Counter
17	I2C1FIFO	I²C FIFO Control
TIMER B		
REG	**REG NAME**	**DESCRIPTION**
5	TB0CN	Timer B Conf guration
6	TB0V	Timer B Value
7	TB0R	Timer B Reload
MODULE 2		
MULTIPLY-ACCUMULATE UNIT		
REG	**REG NAME**	**DESCRIPTION**
0	MCNT	Multiplier Control
1	MA	Multiplier Operand A
2	MB	Multiplier Operand B
8	MC0	Accumulator bits 31–0
9	MC1	Accumulator bits 63–32
11	MC0R	Result bits 31–0 (read only)
12	MC1R	Result bits 63–32 (read only)
PULSE		
REG	**REG NAME**	**DESCRIPTION**
3	CFCN	Meter Pulse Conf guration
4	CFINC0	Meter Pulse Increment 0

Table 3. Peripherals Available to the MAXQ30 Core (continued)

PULSE		
REG	**REG NAME**	**DESCRIPTION**
5	CFINC1	Meter Pulse Increment 1
6	CFINC2	Meter Pulse Increment 2
7	CFINC3	Meter Pulse Increment 3
14	CFACT0	Meter Pulse Active Period 0
15	CFACT1	Meter Pulse Active Period 1
16	CFACT2	Meter Pulse Active Period 2
17	CFACT3	Meter Pulse Active Period 3
MODULE 3		
COMPUTE ENGINE		
REG	**REG NAME**	**DESCRIPTION**
5	CEI	Compute Engine Interrupt
7	CEPCN	Compute Engine Pulse Control
8	CECN	Compute Engine Control
REMOTE		
REG	**REG NAME**	**DESCRIPTION**
1	RMTCN	Isolated Remote Conf guration
2	RMTCMD	Command sent to Isolated Remote
6	RMTERR	Isolated Remote Error Status
9	RMTDATA	Isolated Remote Data
ADC		
REG	**REG NAME**	**DESCRIPTION**
3	ADCN	ADC Control
4	ADCFG	ADC Conf guration
10	ADCLK	ADC Clock
11	ADMUX0	ADC Multiplexer Select 0
12	ADMUX1	ADC Multiplexer Select 1
13	ADMUX2	ADC Multiplexer Select 2
14	ADMUX3	ADC Multiplexer Select 3
15	ADMUX4	ADC Multiplexer Select 4
16	ADMUX5	ADC Multiplexer Select 5
17	ADMUX6	ADC Multiplexer Select 6
18	FIRLEN	ADC FIR Filter Length
19	SLEN	ADC Length of S State
20	SDLY	ADC Delay from S State
21	VDLY	ADC Delay from V State
22	VZERO	ADC Number of Zero Volt Samples
23	MUXCN	ADC Multiplexer Conf guration

REAL-TIME MONITOR		
REG	**REG NAME**	**DESCRIPTION**
24	RTM0	Real-Time Monitor Channel 0
25	RTM1	Real-Time Monitor Channel 1
26	RTM2	Real-Time Monitor Channel 2
27	RTM3	Real-Time Monitor Channel 3
MODULE 4		
LCD		
REG	**REG NAME**	**DESCRIPTION**
0	LCDCFG	LCD Conf guration
1	LCDBLINK	LCD Segment Blink Mask
2	LCDADDR	LCD Address
3	LCDSEG	LCD Segment Data
8	LCDCN	LCD Control Register
9	LCDMAP0	LCD Segment Map 0
10	LCDMAP1	LCD Segment Map 1
11	LCDMAP2	LCD Segment Map 2
MAILBOX		
REG	**REG NAME**	**DESCRIPTION**
4	SRSP0	Mailbox Slave Response 0
5	SRSP1	Mailbox Slave Response 1
18	MREQ0	Mailbox Master Request 0
19	MREQ1	Mailbox Master Request 1
20	MREQ2	Mailbox Master Request 2
GPIO		
REG	**REG NAME**	**DESCRIPTION**
6	PO2	GPIO Port 2 Output
7	EIF2	GPIO Port 2 Interrupt Flag
14	PI2	GPIO Port 2 Input
15	PD2	GPIO Port 2 Direction
16	EIE2	GPIO Port 2 Interrupt Enable
17	EIES2	GPIO Port 2 Interrupt Edge Select
MODULE 5		
REAL-TIME CLOCK		
REG	**REG NAME**	**DESCRIPTION**
2	RTCI	RTC Interrupt
10	RTCSTAT	RTC Status
11	RTCCN	RTC Control
12	RTCSBSC	RTC Subsecond Counter

Table 3. Peripherals Available to the MAXQ30 Core (continued)

REAL-TIME CLOCK		
REG	**REG NAME**	**DESCRIPTION**
13	RTCTIME	RTC Time
14	RTCDATE	RTC Date
15	RTCALRM	RTC Alarm
16	RTCCAL	RTC Calibration
17	RTCTCA	RTC Temperature Coeff cient A
18	RTCTCB	RTC Temperature Coeff cient B
19	RTCMISC	
20	RTCBTM	

SECURITY MONITOR		
REG	**REG NAME**	**DESCRIPTION**
0	EXTSST	External Sensor Status
6	EXTSINT	External Sensor Interrupt
8	EXTSCN	External Sensor Control
9	EXTSCFG	External Sensor Conf guration
23	EXTSINTCN	External Sensor Interrupt Control
MEMORY CONTROL		
REG	**REG NAME**	**DESCRIPTION**
7	MEMCTL	Memory Control

Using the MAX71617/MAX71637

Power

The MAX71617/MAX71637 require a single 3.3V supply to operate. However, in an electricity metering environment continuity of measured values and nominal operation in the absence of line power is a critical requirement.

There are ten power connections that, together with associated grounds, assure the integrity and continuity of the power supply to the MAX71617/MAX71637.

AVDD: This input provides power to the ADC converter array, the bandgap voltage reference and voltage comparators. It is generally connected to a 3.3V supply driven from line power. While this input can be battery-backed by means of an external connection, it is most often unnecessary to do this: in the absence of line power, the ADC converters have nothing to measure. Currents into AVDD return through AGND.

RVDD: This power input supplies the remote interface driver. It is provided as a separate input (and ground return) to isolate the fast rise time, high-current pulses that provide power to the remote ADC interfaces. As with AVDD, it is typically not battery backed, since in the absence of line power there is nothing to measure.

V_{LCD}: This connection can serve as an input or output. If V_{LCD} is internally generated, the pin is a bypass point for LCD voltage. If external V_{LCD} is selected, this pin serves as the supply pin for the LCD. Note that this pin supplies the waveform generator and the contrast DAC, but does not supply the LCD data registers. The data registers are maintained on a nonvolatile supply.

V_{DD}: This is the main digital power input to the device. In normal operation, the application circuit supplies 3.3V to this pin. If power is removed, internal logic automatically switches power to the V_{BAT} input. This pin supplies the primary core regulator that drives all logic in the device. It also nominally supplies power to the control logic for the LCD contrast DAC.

V_{BAT}: This is the primary backup power connection. In most cases, a relatively high-capacity primary battery is connected to this pin (often, a 1.1Ah lithium thionyl cell). When V_{DD} falls below the power fail threshold, a switch automatically selects V_{BAT} instead of V_{DD} as the primary power supply. When this occurs, it is the responsibility of software to switch to a low-power mode to minimize the drain on the backup battery.

V_{3P3D}: This pin is an output, driven by the selected primary power input: either V_{BAT} or V_{DD}. Frequently, it is directly connected to the I/O power input (V_{IO}) to provide power for I/O pins in the event of a brownout event.

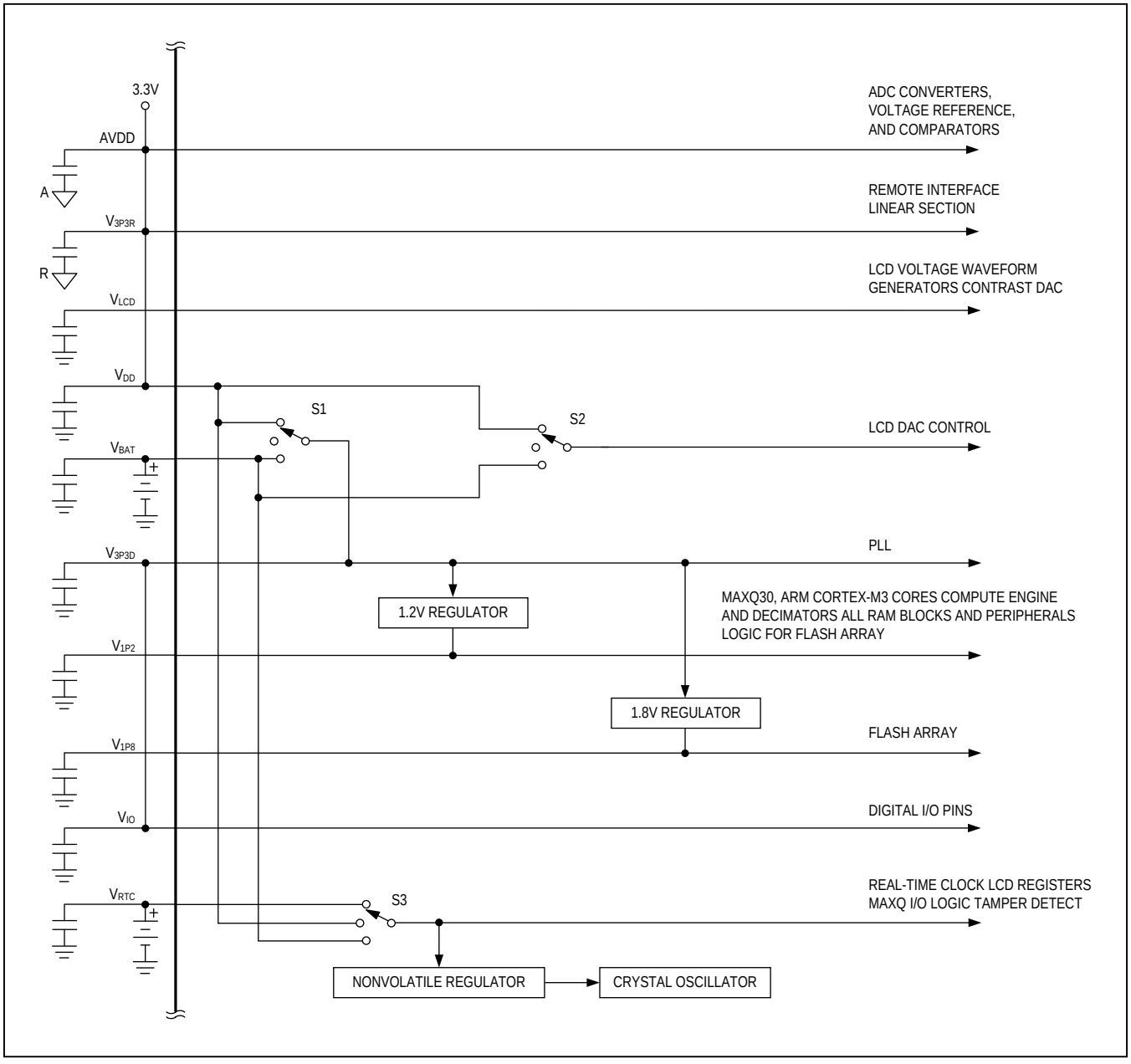
V_{1P2}: This pin is a bypass point for the core power supply. An internal regulator reduces the 3.3V supply to the 1.2V required by internal logic. Connect an appropriate bypass capacitor to this pin.

V_{1P8}: This pin is a bypass point for the flash memory power supply. An internal regulator reduces the 3.3V supply to the 1.8V required by the flash memory array. An appropriate bypass capacitor should be connected to this pin.

V_{IO}: This is the power input for the I/O pad ring. When configured as outputs, I/O pins use this supply to source high logic-level output voltage and current. It can be connected to any available source of 3.3V power, but is most frequently connected to the V_{3P3D} output pin.

V_{RTC}: This is the power connection for the real-time clock and other nonvolatile circuits. In most cases, a low-capacity primary battery (often a coin cell) is attached to this pin. Unlike V_{BAT}, the supply attached to this pin cannot drive the primary logic voltage regulator. Instead, if V_{DD} and V_{BAT} both fail, V_{RTC} maintains the integrity of the clock and other critical functions, such as LCD registers, tamper detect circuitry and I/O cells attached to the MAXQ30 metering core.

Power Diagram



There are three internal switches that select power for the devices:

- S1 selects whether V_{DD} or V_{BAT} provides power to the logic and flash memory voltage regulators. Additionally, software can force S1 into SLEEP mode to disconnect the regulators completely from any source of power. This mode is the lowest power mode, but requires an external event to wake the processor and switch S1 back to either V_{DD} or V_{BAT}.
- S2 selects whether V_{DD} or V_{BAT} provides power for the LCD DAC control logic. This is a block of low-power, 3.3V logic that manages the operation of the LCD DAC.

- S3 selects the source for nonvolatile power. It operates automatically and does not require software intervention. If V_{DD} is available, nonvolatile power is derived from that source; otherwise, nonvolatile power is derived from V_{BAT}. If neither V_{BAT} nor V_{DD} are available, V_{RTC} is the power source.

These automatic mechanisms, combined with software controlled switches, provide several operating modes:

Mission mode: When V_{DD} and AVDD are available, the device is considered to be in mission mode. In this mode, the 1.2V core regulator and the 1.8V flash regulator are turned on, the core is capable of running at full speed, and the AFE is processing samples and accumulating data. This is also the highest power mode.

Brownout mode: When AVDD and V_{DD} are no longer available, the device switches automatically to derive core power from V_{BAT}. This mode is considered brownout mode. In this mode, the core can still run at full speed, but because AVDD is not available the AFE is not active. In brownout mode, the full power for the core is provided by the V_{BAT} battery, so it is important for system software to quickly reduce power consumption.

Sleep mode: The lowest-power mode. In sleep mode, S1 is in the off position, and the voltage regulators are effectively turned off. That means that power is removed from all CPU cores and memory blocks and that the PLL clock multiplier is turned off. Only the nonvolatile bus is powered.

Sleep mode can actually be enabled at any time, whether V_{DD} is available or not. If V_{DD} is not available, V_{BAT} supplies the nonvolatile power bus; if neither V_{DD} nor V_{BAT} are available, V_{RTC} supplies the nonvolatile power bus.

Waking from sleep mode involves a cold restart of the application core, and reloading the program RAM for the MAXQ30 metering core as well as the compute engine RAM block.

LCD Only mode: This is a special version of sleep mode in which the regulators are disabled, but the LCD is still active and driving a display glass. In LCD Only mode, S2 selects either V_{DD} or V_{BAT} to provide power to the LCD DAC control registers. The actual input for the LCD DAC (and thus the primary power to the waveform generators) is provided on the V_{LCD} pin. The LCD data registers are maintained in the nonvolatile power domain and so do not lose their contents even in sleep mode.

LCD Only mode provides most of the power benefits of sleep mode while continuing to drive the LCD.

Other Power Considerations

To conserve power and still maintain full operational capability, both cores support a stop mode. When either the application core or the metering core is in stop mode, the core is halted and there is no dynamic power consumption in the core itself. There is still static power consumption, and peripherals can still operate. In most systems, it is wise to maintain the cores in stop mode for as much of the time as possible to minimize power consumption.

The ARM Cortex-M3 application core contains a clock divider that can provide 108MHz, 54MHz, 27MHz, or 13.5MHz as the main CPU clock. The MAXQ30 metering core always runs at 36MHz.

Software Development

The MAX71617/MAX71637 typically require at least three software modules. The first is the CE module, provided by Silergy. This module provides the low-level DSP functions, and periodically reports the usage over a brief period of time (by default one second) to software running on the MAXQ30 metering core. Contact Silergy for information about obtaining loadable files for use with the MAX71617/MAX71637.

Software on the MAXQ30 core is tasked with managing long-term accumulation of results from the CE module and managing the external storage and the display subsystems, among other tasks. Silergy provides several versions of the MAXQ30 code to serve as samples; alternately, MAXQ30 code can be developed directly by the meter designer. Contact Silergy to determine what MXQ30 modules are available.

If the designer elects to develop the MAXQ30 operating code, a development environment is needed. If development is occurring in assembly language, use the free MAX-IDE software development kit. MAX-IDE is a complete toolkit that includes assembler, editor and debugger. For C development, Silergy recommends the Rowley CrossWorks compiler and IDE. Contact Silergy for details about how to obtain a license for this tool.

Finally, a software module for the ARM Cortex-M3 must be provided. This module typically takes results from the MAXQ30 core, format them as required and transmit them through communication facilities attached to the ARM Cortex-M3. Additionally, software running on the application core frequently formats messages for the metering core to control the peripherals under its control, such as the LCD and the metrology subsystem.

There are many development toolkits available for the ARM architecture, in both freely available and paid versions. A reference meter is available from Silergy that includes source code for the ARM core and that demonstrates the interaction between the various cores. Contact Silergy for availability information.

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY ARM CORTEX-M3 FLASH (MB)	DATA MEMORY ARM CORTEX-M3 (KB)	METROLOGY CHANNELS	PIN-PACKAGE
MAX71617ECD+	-40°C to +85°C	+2.7 to +3.6	1	128	4	120 LQFP
MAX71617ECD+T	-40°C to +85°C	+2.7 to +3.6	1	128	4	120 LQFP
MAX71637ECD+	-40°C to +85°C	+2.7 to +3.6	1	128	7	120 LQFP
MAX71637ECD+T	-40°C to +85°C	+2.7 to +3.6	1	128	7	120 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

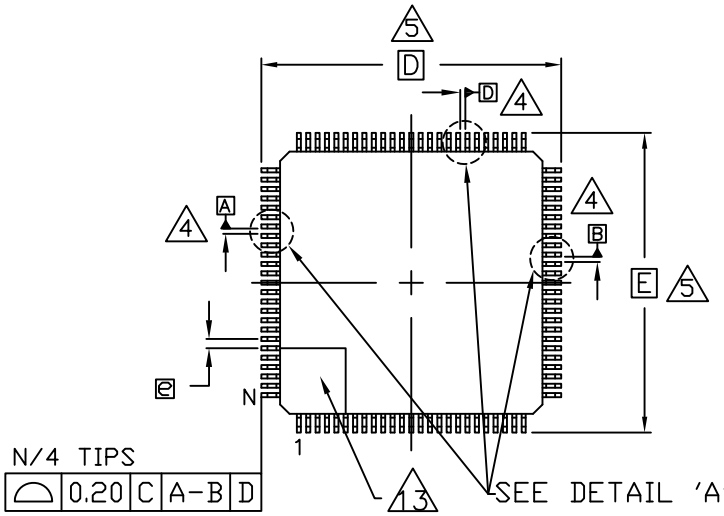
PROCESS: BiCMOS

Package Information

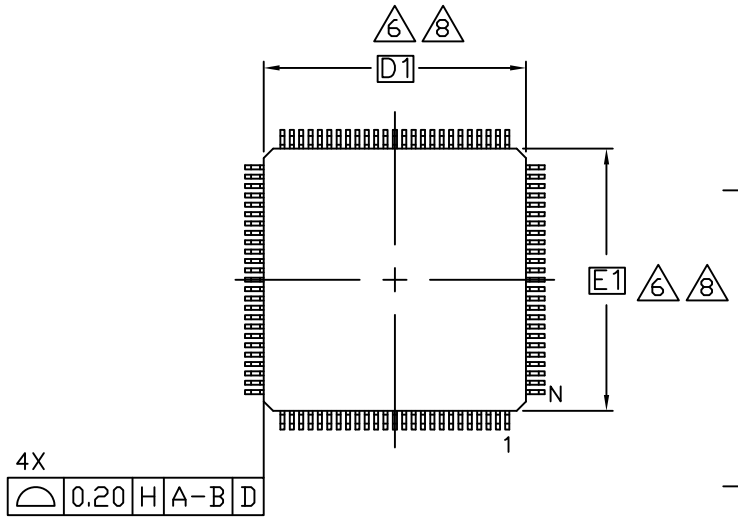
Package outline information and land patterns (footprints) are appended to this document.

Revision History

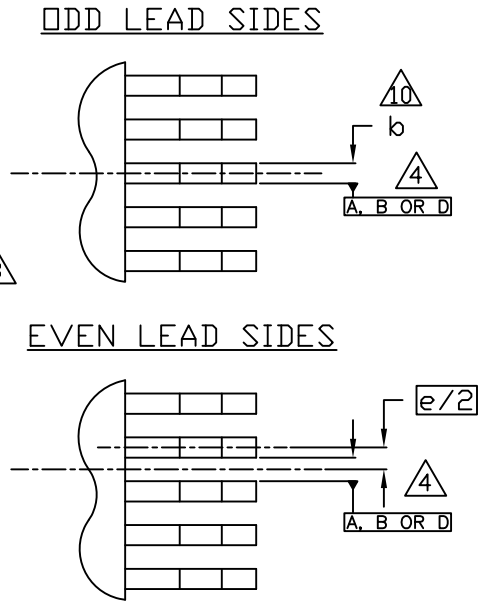
REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	3/15	Updated *Benef ts and Features* section and removed future product references	1, 33
2	4/16	Rebranding only	



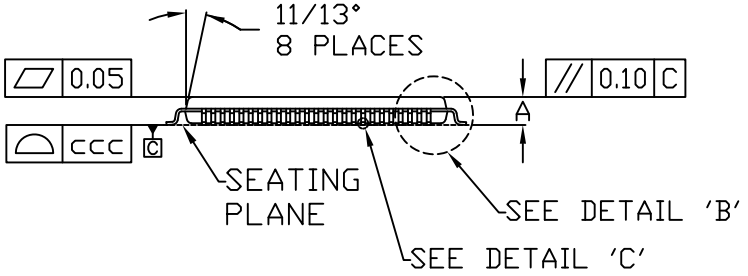
TOP VIEW



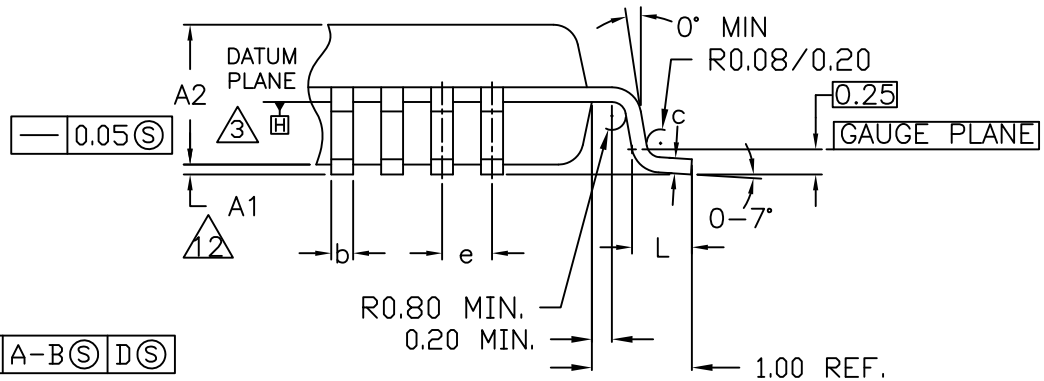
BOTTOM VIEW



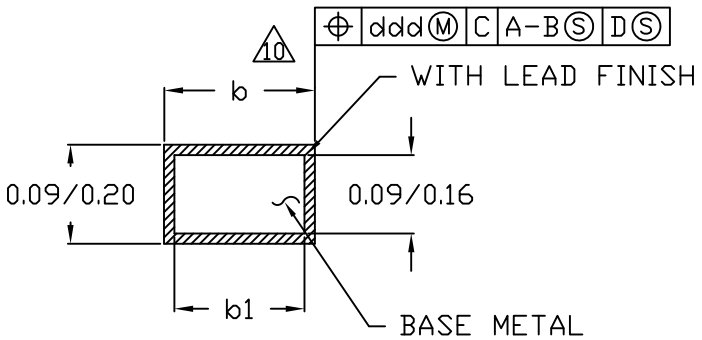
DETAIL 'A'



SIDE VIEW



DETAIL 'B'



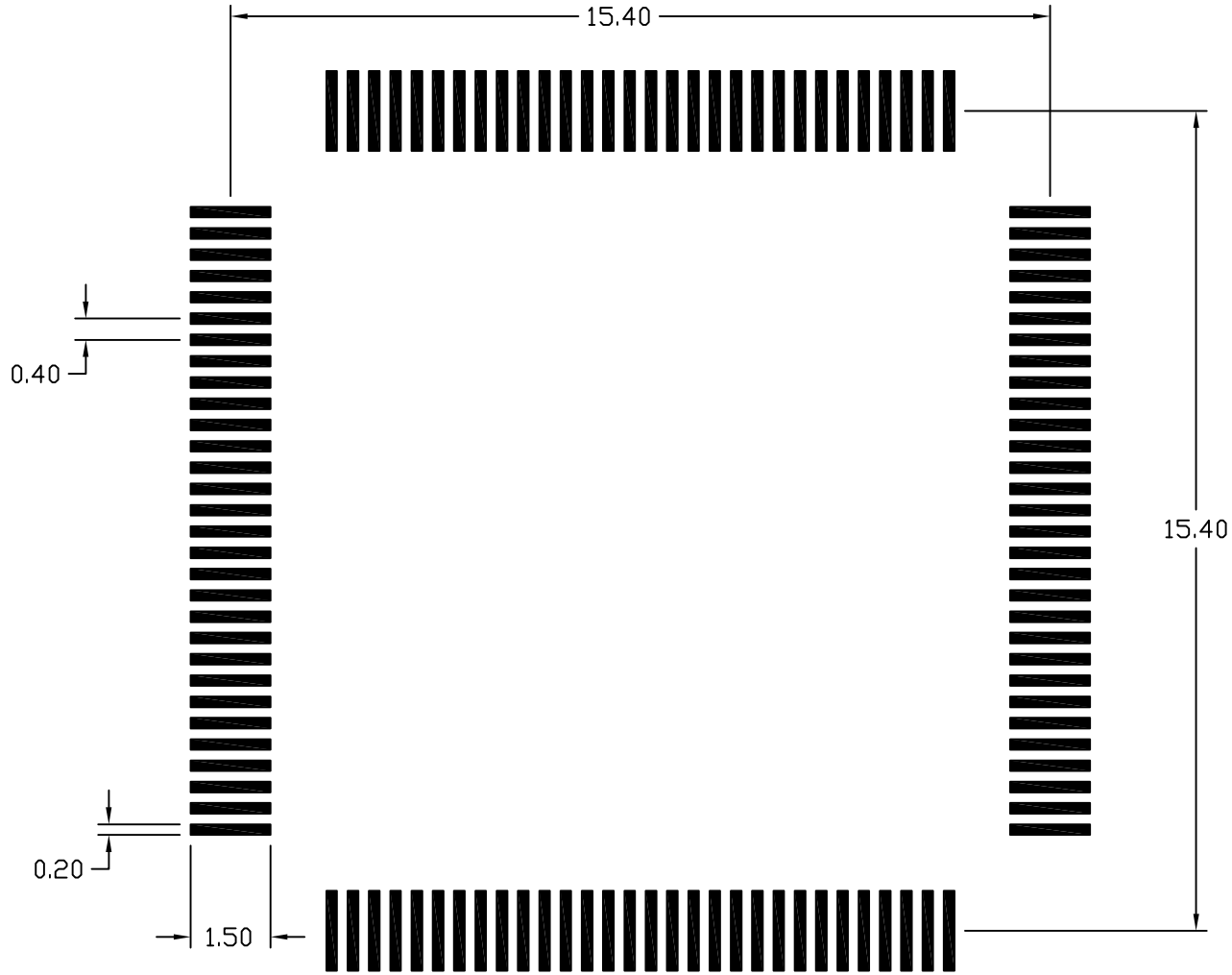
DETAIL 'C'

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-2009.
3. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUMS [A-B] AND [D] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE [H] .
5. TO BE DETERMINED AT SEATING PLANE [C]
6. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE.
7. "N" IS THE TOTAL NUMBER OF TERMINALS.
8. TO BE DETERMINED AT DATUM PLANE [H]
9. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
10. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026,
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

SYMBOL	VARIATION B		
	MIN.	NOM.	MAX.
N	120		
e	0.40 BSC		
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
ccc	–	–	0.08
ddd	–	–	0.07
PKG CODE	C120L-1		

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	16.00 BSC.		
D_1	14.00 BSC.		
E	16.00 BSC.		
E_1	14.00 BSC.		
L	0.45	0.60	0.75



NOTES:
1. ALL DIMENSIONS IN MM.
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.