MAX77816

High-Efficiency Buck-Boost Regulator with 5A Switches

General Description

The MAX77816 is a high-current, high-efficiency buck-boost regulator targeting single-cell Li-ion battery-powered applications. It supports a wide output voltage range from 2.60V to 5.14V. The IC allows 5A (typ) maximum switch current. In buck mode, the output current can go as high as 4A, and in boost mode, the maximum output current can be 3A. A unique control algorithm allows high efficiency, outstanding line/load transient response, and seamless transition between buck and boost modes.

The IC features an I²C-compatible serial interface. The I²C interface allows the output voltage to be dynamically adjusted, thus enabling finer control of system power consumption. The I²C interface also provides features such as enable control and device status monitoring.

The multifunction GPIO pin is register settable to 5 different options, such as FPWM mode enable and inductor peak current level selection. These options provide design flexibility that allows the IC to cover a wide range of applications and use cases.

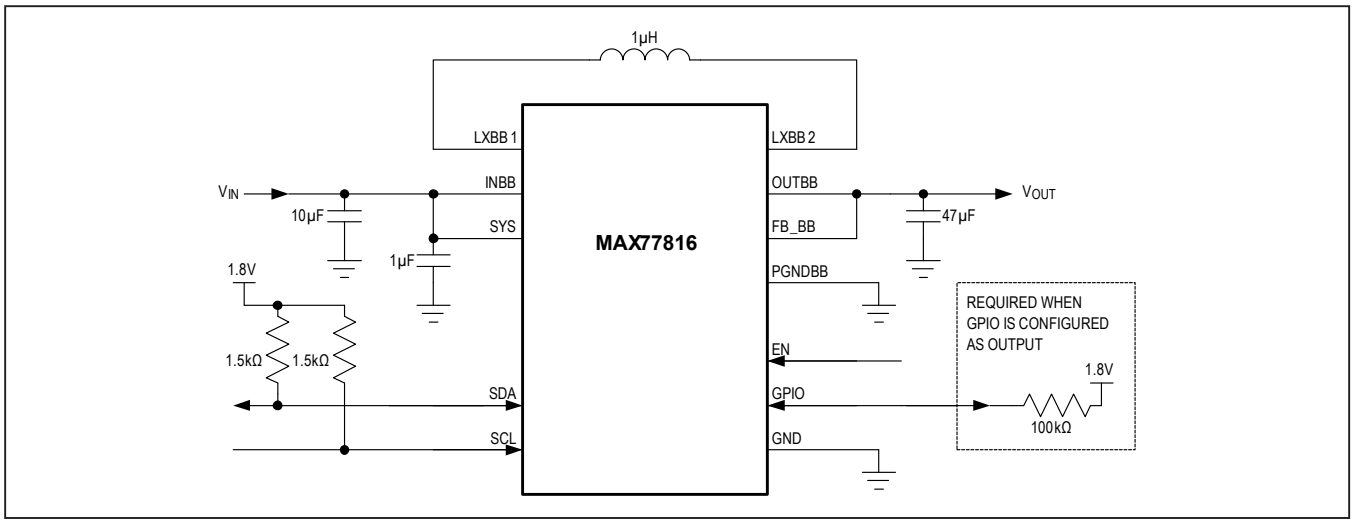
Applications

- Smartphones and Tablets
- Wearable Devices
- Wireless Communication Devices
- RF Power Amplifiers
- Battery-Powered Applications

Benefits and Features

- Buck and Boost Operation Including Seamless Transition between Buck and Boost Modes
  - 2.3V to 5.5V V_{IN} Range
  - 2.60V to 5.14V V_{OUT} with 20mV Step
  - 3A Minimum Continuous Output Current (V_{INBB} ≥ 3.0V, V_{OUTBB} = 3.3V)
  - Burst Current: 3.6A Minimum Output Current for 800µs (V_{INBB} ≥ 3.0V, V_{OUTBB} = 3.3V)
- I²C Serial Interface Allows Dynamic V_{OUT} Adjustment and Provides Design Flexibility
- 97.5% Peak Efficiency
- 40µA Quiescent Current
- Safety Features Enhance Device and System Reliability
  - Soft-Start
  - True Shutdown™
  - Thermal Shutdown and Short-Circuit Protection
- Multifunction GPIO Pin
  - **MAX77816A/F:** FPWM Mode Enable
  - **MAX77816B:** Inductor Peak Current-Limit selection
  - **MAX77816C:** Output Voltage Selection
  - **MAX77816D:** Power-OK indicator
  - **MAX77816E:** Interrupt Indicator
- Small Size: 1.827mm x 2.127mm, 20-Bump WLP, 0.4mm Pitch

Typical Application Circuit



Ordering Information ***appears at end of data sheet.***

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Absolute Maximum Ratings

SYS to GND .....-0.3V to +6.0V
INBB, OUTBB to PGNDBB .....-0.3V to +6.0V
PGNDBB to GND .....-0.3V to +0.3V
SCL, SDA to GND ..... -0.3V to (V_{SYS} + 0.3V)
EN, GPIO to GND ..... -0.3V to (V_{SYS} + 0.3V)
FB_BB to GND .....-0.3V to (V_{OUTBB} + 0.3V)
LXBB1 to PGNDBB ..... -0.3V to (V_{INBB} + 0.3V)
LXBB2 to PGNDBB .....-0.3V to (V_{OUTBB} + 0.3V)
LXBB to PGND (Pulsed < 5ns Voltage) .....-2.4V to 8.0V
LXBB1/LXBB2 Continuous RMS Current (Note 1) 4.8A
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C
Continuous Power Dissipation at T_A = +70°C
(Derate 23.8mW/°C above +70°C) 1905mW

Note 1: LXBB1/LXBB2 node has internal clamp diodes to PGNDBB and INBB. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed the power dissipation limit of IC package.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....55.49°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{INBB}		2.3		5.5	V
Shutdown Supply Current	I_{SHDN_25C}	EN = low, T_A = +25°C			1	µA
	I_{SHDN_85C}	EN = low, T_A = +85°C (Note 5)		1		
Input Supply Current	I_{Q_SKIP}	SKIP mode, no switching		40	60	µA
	I_{Q_PWM}	FPWM mode, no load		6		mA
Active Discharge Resistance	R_{DISCHG}			100		Ω
Thermal Shutdown	T_{SHDN}	Rising, 20°C hysteresis		+165		°C
H-BRIDGE						
Output Voltage Range	V_{OUT}	I²C programmable (20mV step)	2.60		5.14	V
Default Output Voltage		MAX77816A only, VOUT [6:0] = 0x28		3.4		V
		MAX77816B/C/D/E/F, VOUT [6:0] = 0x23		3.3		
Output Voltage Accuracy	V_{OUT_ACC1}	PWM mode, no load	-1.0		+1.0	%
	V_{OUT_ACC2}	SKIP mode, no load, T_A = +25°C	-1.0		+4.5	
Line Regulation		V_{INBB} = 2.3V to 5.5V		0.200		%/V
Load Regulation		(Note 4)		0.125		%/A
Line Transient Response	V_{OS1} V_{US1}	I_{OUT} = 1.5A, V_{INB} changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, C_{OUT_NOM} = 47µF (Note 4)		50		mV

Electrical Characteristics (continued)

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Transient Response	V_{OS2} V_{US2}	I_{OUT} changes from 10mA to 1.5A in 15µs, L = 1µH, C_{OUT_NOM} = 47µF (Note 4)		50		mV
Output Voltage Ramp-Up Slew Rate		BB_RU_SR = 0 (Note 6)		20		mV/µs
		BB_RU_SR = 1 (Note 6)		40		
Output Voltage Ramp-down Slew Rate		BB_RD_SR = 0 (Note 6)		5		mV/µs
		BB_RD_SR = 1 (Note 6)		10		
Typical Load Efficiency	η_{IOUT_TYP}	I_{OUT} = 100mA (Note 4)		95		%
Peak Efficiency	η_{PK}	(Note 4)		97.5		%
LXBB1/2 Current Limit	I_{LIM_LXBB}	ILIM[1:0] = 11b or GPIO_CFG[2:0] = 010b, GPIO = high	4	5	5.8	A
		ILIM[1:0] = 10b		3.1		
		ILIM[1:0] = 01b or GPIO_CFG[2:0] = 010b, GPIO = low		1.80		
		ILIM[1:0] = 00b		1.15		
High-Side PMOS ON Resistance	$R_{DSON(PMOS)}$	I_{LXBB} = 100mA per switch		34		mΩ
Low-Side NMOS ON Resistance	$R_{DSON(NMOS)}$	I_{LXBB} = 100mA per switch		45		mΩ
Switching Frequency	f_{SW}	PWM mode, T_A = +25°C	2.25	2.50	2.75	MHz
Turn-On Delay Time	t_{ON_DLY}	From EN asserting to LXBB switching (Note 6)		100		µs
Soft-Start Time	t_{SS}	I_{OUT} = 10mA, ILIM[1:0] = 11b or 10, or GPIO_CFG[2:0] = 010b, GPIO = high (Note 4)		120		µs
		IOUT = 10mA, ILIM[1:0] = 01b or 00, or GPIO_CFG[2:0] = 010b, GPIO = low (Note 4)		800		
Minimum Effective Output Capacitance	$C_{EFF(MIN)}$	0A < I_{OUT} < 3000mA		16		µF
LXBB1, LXBB2 Leakage Current	I_{LK_25}	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V, T_A = +25°C		0.1	1	µA
	I_{LK_85}	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V, T_A = +85°C (Note 5)		0.2		
SYS Undervoltage Lockout Threshold	V_{UVLO_R}	V_{SYS} rising	2.375	2.50	2.625	V
	V_{UVLO_F}	V_{SYS} falling		2.05		

Electrical Characteristics (continued)

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUT (EN)						
EN Logic-Low Threshold	V_{EN_L}	V_{SYS} ≤ 5.5V, T_A = +25°C			0.4	V
EN Logic-High Threshold	V_{EN_H}	V_{SYS} ≤ 5.5V, T_A = +25°C	1.2			V
EN Internal Pulldown Resistance	R_{EN}	Pulldown resistor to GND	400	800	1600	kΩ
GENERAL PURPOSE INPUT/OUTPUT (GPIO)						
Input Logic-Low Threshold	V_{GPI_L}	GPIO[2:0] = 001b or 010b or 011b, V_{SYS} ≤ 4.5V, T_A = +25°C			0.4	V
Input Logic-High Threshold	V_{GPI_H}	GPIO[2:0] = 001b or 010b or 011b, V_{SYS} ≤ 4.5V, T_A = +25°C	1.2			V
Input Internal Pulldown Resistance	R_{EN}	GPIO[2:0] = 001b or 010b or 011b, Pulldown resistor to GND	400	800	1600	V
Output Low Voltage	V_{GPO_L}	GPIO[2:0] = 100b or 101b, I_{SINK} = 1mA			0.4	V
Output Leakage Current	I_{GPO_25C}	GPIO[2:0]=100b or 101b, T_A = +25°C	-1		+1	µA
	I_{GPO_85C}	GPIO[2:0] = 100b or 101b, T_A = +85°C (Note 5)		0.1		
POK Threshould	VPOK_R	GPIO[2:0] = 100b, V_{OUTBB} rising, expressed as a percentage of V_{OUTBB}		92.5		%
	VPOK_F	GPIO[2:0] = 100b, V_{OUTBB} falling, expressed as a percentage of V_{OUTBB}		90		
I²C-COMPATIBLE INTERFACE—I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}		1.4			V
SCL, SDA Input Low Voltage	V_{IL}				0.4	V
SCL, SDA Input Hysteresis	V_{HYS}	(Note 5)		0.1		V
SCL, SDA Input Current	I_I		-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
SCL, SDA Input Capacitance	C_I				10	pF
Maximum Pulse Width of Spikes that must be suppressed by the input filter	t_{SP}	(Note 5)		50		ns

Electrical Characteristics (continued)

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

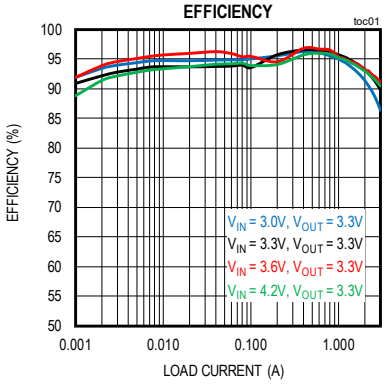
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE—TIMING (Note 5)						
Clock Frequency	f_{SCL}				1	MHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
DATA Hold Time	t_{HD_DAT}		0			µs
DATA Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 4: Guaranteed by design. Not production tested.
Note 5: Guaranteed by ATE characterization. Not directly tested in production.
Note 6: Guaranteed by design. Production tested through scan.

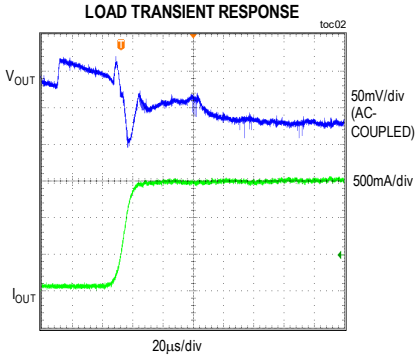
Typical Operating Characteristics

(V_{SYS} = V_{INBB} = +3.8V , V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = +25°C.)

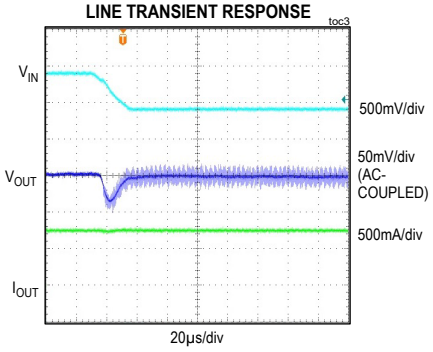
EFFICIENCY



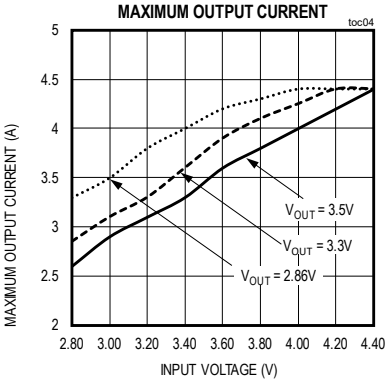
LOAD TRANSIENT RESPONSE



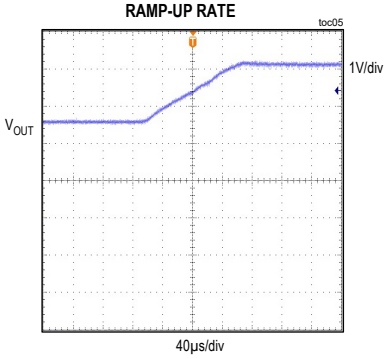
LINE TRANSIENT RESPONSE



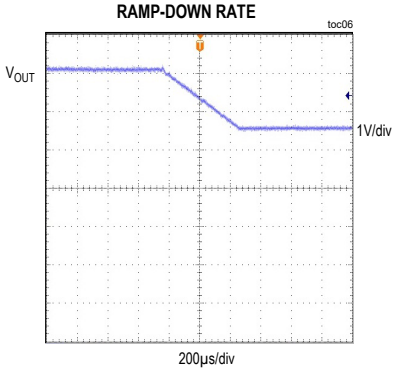
MAXIMUM OUTPUT CURRENT



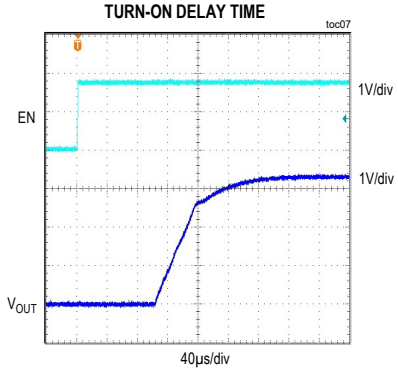
OUTPUT VOLTAGE RAMP-UP RATE



OUTPUT VOLTAGE RAMP-DOWN RATE

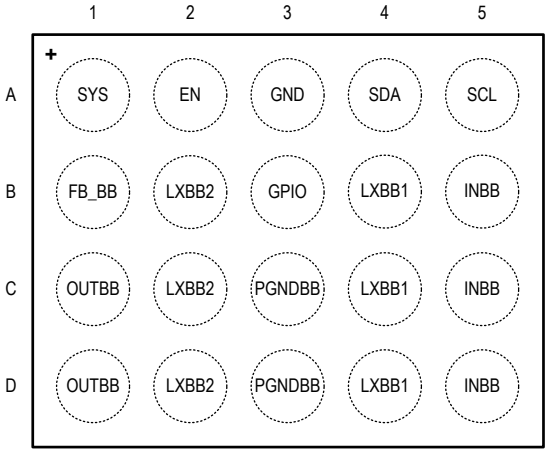


TURN-ON DELAY TIME



Bump Configuration

TOP VIEW
(BUMP SIDE DOWN)



20-BUMP WLP
(2.13mm x 1.83mm, 0.4mm PITCH)

Bump Description

BUMP	NAME	FUNCTION
A1	SYS	System (Battery) Voltage Input. Bypass to GND with a 1µF capacitor.
A2	EN	Active-High, Buck-Boost External Enable Input. An 800kΩ internal pulldown resistance to the GND.
A3	GND	Quite Ground. Star-ground connection to system GND.
A4	SDA	I^2C Data I/O (Hi-Z in OFF State). This pin requires a pullup resistor to I^2C power supply. Connect to GND if not used.
A5	SCL	I^2C Clock Input (Hi-Z in OFF State). This pin requires a pullup resistor to I^2C power supply. Connect to GND if not used.
B1	FB_BB	Buck-Boost Output Voltage Feedback
B2, C2, D2	LXBB2	Buck-Boost Switching Node 2
B3	GPIO	Multifunction GPIO: MAX77816A/B/C/F: General Purpose Input. An 800kΩ internal pulldown resistance to the GND. MAX77816D/E: Open-Drain Output. An external pullup resistor is required.
B4, C4, D4	LXBB1	Buck-Boost Switching Node 1
B5, C5, D5	INBB	Buck-Boost Input. Bypass to PGNDBB with a 10µF capacitor.
C1, D1	OUTBB	Buck-Boost Output
C3, D3	PGNDBB	Buck-Boost Power Ground. Star-ground connection to system GND.

Detailed Description

Enable Control

When EN pin is set to high, the IC turns on the internal bias circuitry, which takes typically 100µs (t_{ON_DLY}) to be settled. As soon as the bias is ready, all user registers are accessible through I²C. Write BB_EN bit to 1 to enable (register default) buck-boost output voltage regulation. The V_{OUTBB} takes 800µs (t_{SS}) to the nominal regulated voltage after BB_EN's setting.

When EN pin is pulled low, the IC goes into shut-down mode. This event also resets all type-O registers to their POR default values.

Immediate Turn-Off Events

The following events initiate immediate turn-off.

- Thermal protection (T_J > +165°C)
- V_{SYS} < SYS UVLO falling threshold (V_{UVLO_F})
- Overcurrent protection
  (I_{LIM} is consistently hit for 3ms)

The events in this category disable buck-boost until the hazardous conditions come back to normal conditions.

Inductor Peak Current Limit (I_{LIM})

The buck-boost regulator's high-side MOSFETs peak current limit (I_{LIM_LXBB}) is register programmable. Applications can use I_{LIM_LXBB} programmability to ensure that the regulator never exceeds the saturation current rating of the inductor on the PCB. In MAX77816B, I_{LIM_LXBB} is GPIO pin programmable. See the *Multifunction GPIO Pin* section.

Multifunction GPIO Pin

The IC has a general-purpose input and output (GPIO) pin which can be configured as 5 different functions through GPIO_CFG[2:0]. The default function of the GPIO pin is listed below:

- **MAX77816A/MAX77816F:** FPWM Mode Enable
  When the GPIO pin is connected to GND, the buck-boost regulator automatically transitions from SKIP mode to fixed-frequency operation (PWM) as load current increases. SKIP mode helps maximize the buck-boost regulator's efficiency at light load. When the GPIO is connected to a voltage above V_{GPI_H}, forced PWM (FPWM) switching behavior is enabled. The FPWM mode benefits applications where lowest output ripple is required. The BB_FPWM bitfield is ignored when GPIO_CFG[2:0] = 001b.

  The MAX77816A has a 3.4V default output voltage, and the MAX77816F has a 3.3V default output voltage.
- **MAX77816B:** Inductor Peak Current-Limit (ILIM) Selection
  The buck-boost regulator's high-side MOSFETs peak current limit (I_{LIM_LXBB}) is GPIO pin programmable. The ILIM[1:0] bitfield is ignored when GPIO_CFG[2:0] = 010b. Connect GPIO to GND to set ILIM to 1.8A (typ). Connect GPIO to a voltage above V_{GPI_H} to program ILIM to 5A (typ).
- **MAX77816C:** Output Voltage Selection
  The GPIO pin sets the output voltage dynamically between VOUT[6:0] (GPIO = LOW) and VOUT_H[6:0] (GPIO = HIGH). When EN pin is asserted, the status of the GPIO pin is latched until completing soft-start so that changes on the GPIO pin are ignored. After soft-start is done, internal logic sets V_{OUTBB} based on the GPIO input.
- **MAX77816D:** Power-OK (POK) Indicator
  The device features an open-drain GPIO output to monitor the output voltage. The GPIO pin requires an external pullup resistor. GPIO goes high (high impedance) after the output increases above 92.5% (V_{POK_R}) of the nominal regulated voltage (V_{OUT_REG}). GPIO goes low when the regulator output drops below 90% (V_{POK_F}) of V_{OUT_REG}.
- **MAX77816E:** Interrupts Indicator
  The GPIO indicates the application processor that the status of the device has changed.

  INT[3:0], INT_MASK[3:0], and the GPIO pin work together to present the buck-boost regulator's abnormal status, including overvoltage, overcurrent, power OK, and thermal shutdown. GPIO goes low when one or more bits of INT[3:0] becomes 1, and the related interrupts are not masked in INT_MASK[3:0]. GPIO becomes high (cleared) as soon as the read action of INT[3:0] starts.

Table 1. Enable Control Logic Truth Table

EN PIN	BB_EN BIT	OPERATING MODE
low	x	Device off
high	0	Disable output
high	1 (default)	Enable output

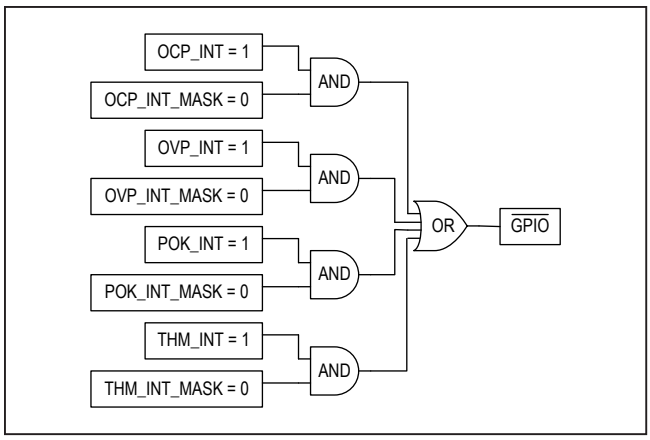


Figure 1. Interrupt Network

Buck-Boost Regulator

The MAX77816 buck-boost regulator utilizes a four-switch H-bridge configuration to realize buck, buck-boost, and boost operating modes. In this way, this topology maintains output voltage regulation when the input voltage is greater than, equal to, or less than the output voltage. The MAX77816 buck-boost is ideal in Li-ion battery-powered applications providing 2.60V to 5.14V of output voltage range and up to 3A of output current. High switching frequency and a unique control algorithm allow the smallest solution size, low output noise, and highest efficiency across a wide input voltage and output current range.

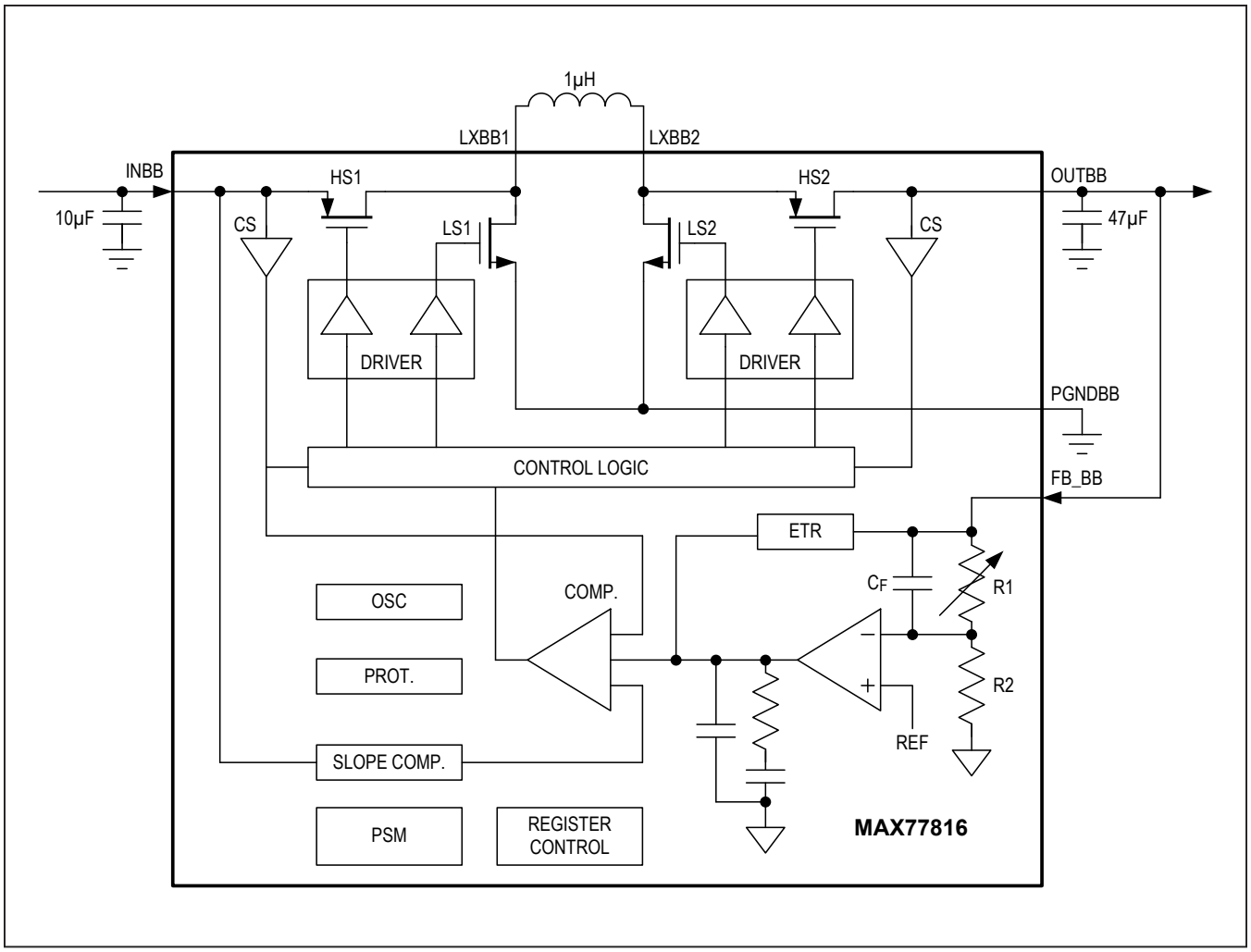


Figure 2. Buck-Boost Block Diagram

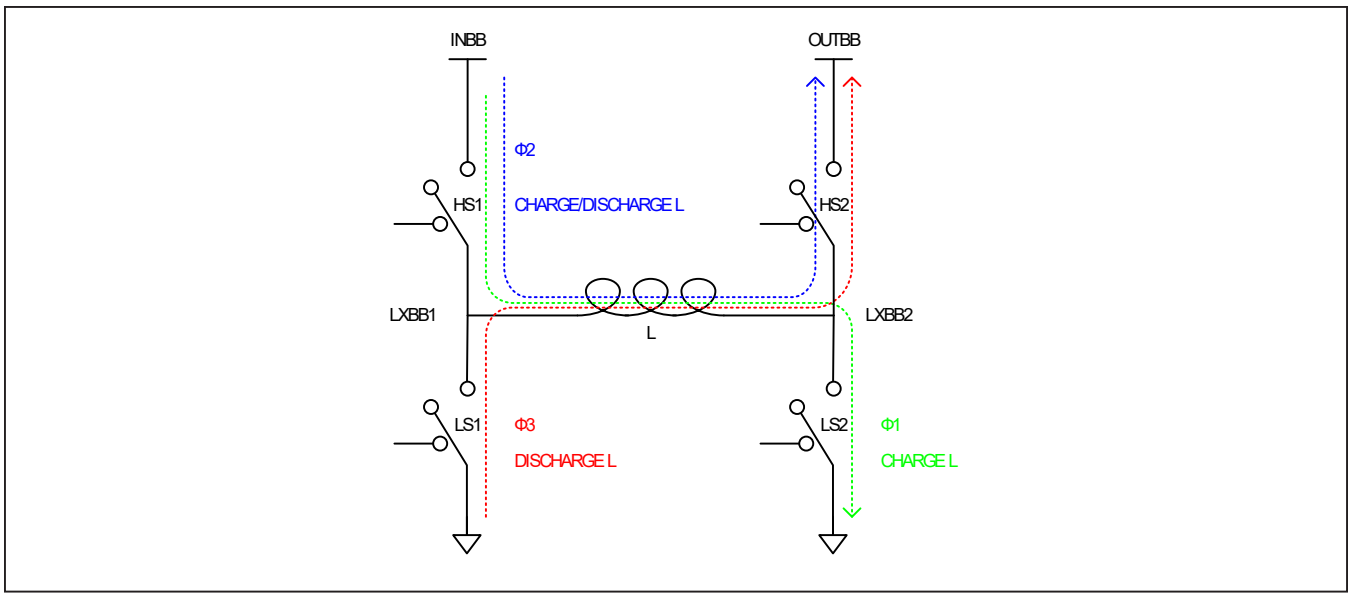


Figure 3. Buck-Boost Switching Intervals

H-Bridge Controller

H-bridge architecture operates at a 2.5MHz fixed frequency with a pulse-width-modulated (PWM), current-mode control scheme. This topology is in a cascade of a boost regulator and a buck regulator using a single inductor and output capacitor. Buck, buck-boost, and boost stages are 100% synchronous for highest efficiency in portable applications.

There are three phases implemented with the H-bridge switch topology, as shown in Figure 3:

- Φ1 Switch period (Phase-1: HS1 = ON, LS2 = ON) stores energy in the inductor, ramping up the inductor current at a rate proportional to the input voltage divided by inductance; V_{INBB}/L.
- Φ2 Switch period (Phase-2: HS1 = ON, HS2 = ON) ramps the inductor current up or down, depending on the differential voltage across the inductor, divided by inductance; $\pm(V_{INBB} - V_{OUTBB})/L$.
- Φ3 Switch period (Phase-3: LS1 = ON, HS2 = ON) ramps down the inductor current at a rate proportional to the output voltage divided by inductance; $-V_{OUTBB}/L$.

2-Phase buck topology is utilized when $V_{INBB} > V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ2 is followed by switch period Φ3, resulting in an inductor current waveform similar to Figure 4.

2-Phase boost topology is utilized when $V_{INBB} < V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ1 is followed by switch period Φ2, resulting in an inductor current waveform similar to Figure 5.

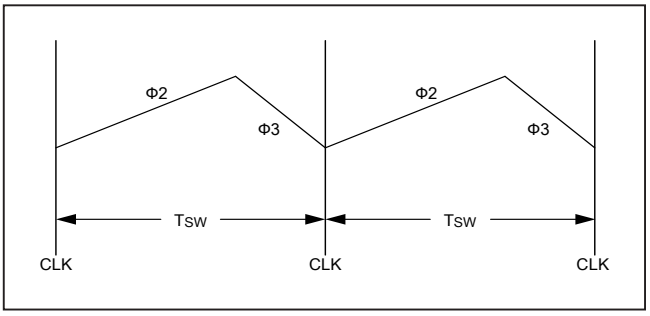


Figure 4. 2-Phase Buck Mode Switching Current Waveforms

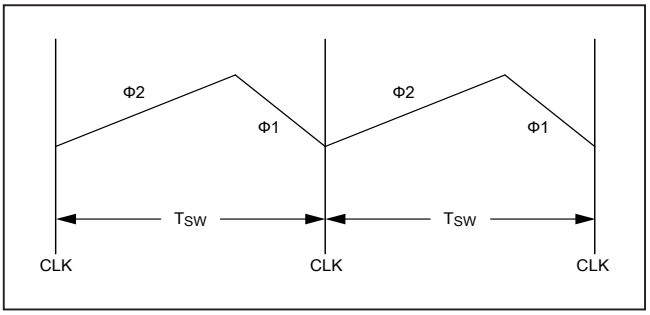


Figure 5. 2-Phase Boost Mode Switching Current Waveforms

Output Voltage Slew-Rate Control

The buck-boost regulator supports programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew-rate can be set to 20mV/µs or 40mV/µs through the BB_RU_SR bit, while the ramp-down slew-rate is programmable to 5mV/µs or 10mV/µs through the BB_RD_SR bit.

Output Active Discharge

Buck-boost provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (BB_AD = 1), the internal resistor discharges the energy stored in the output capacitor to PGNDBB whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (BB_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

Inductor Selection

Buck-boost is optimized for a 1µH inductor. The lower the inductor DCR, the higher buck-boost efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for buck-boost.

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 16µF of minimum effective output capacitance. Considering the DC bias characteristic of ceramic capacitors, a 47µF 6.3V capacitor is recommended for most of applications.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 6 shows an example HDI PCB layout for the MAX77816 WLP package.

When designing the PCB, follow these guidelines:

1) Place the input capacitors C_{IN} and output capacitors C_{OUT} immediately next to the IN pin and OUT pin, respectively, of the IC. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high-voltage spikes and may damage the internal switching MOSFETs.
2) Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3) Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and inductor. Cutting this ground plane risks interrupting the switching current loops.

Table 2. Suggested Inductors for Buck-Boost

MANUFACTURER	SERIES	NOMINAL INDUCTANCE (µH)	DC RESISTANCE (typ) (mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = -40°C RISE	DIMENSIONS L x W x H (mm)
TDK	TFM201610GHM-1R0MTAA	1.0	50	3.8	3.0	2.0 x 1.6 x 1.0
TOKO	DFE322512C	1.0	34	4.6	3.7	3.2 x 2.5 x 1.2
Coilcraft	XAL4020-102MEB	1.0	13	8.7	9.6	4.0 x 4.0 x 2.1

4) AGND must carefully connect to PGND on the PCB's low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
5) The IC requires a quiet supply input (SYS) which is often the same net as IN. Carefully bypass SYS to AGND with a dedicated capacitor (C_{SYS}) as close as possible to the IC. Route a dedicated trace between C_{SYS} and the SYS bump. Avoid connecting SYS directly to the nearest IN bumps without dedicated bypassing.
6) Connect the OUTS bump to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.
7) Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
8) Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to Tutorial 5527 for more information.

Serial Interface

The I²C-compatible, 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the *Register Map* section for details.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (of 500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 8 shows an example of a typical I²C system. A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77816 I²C

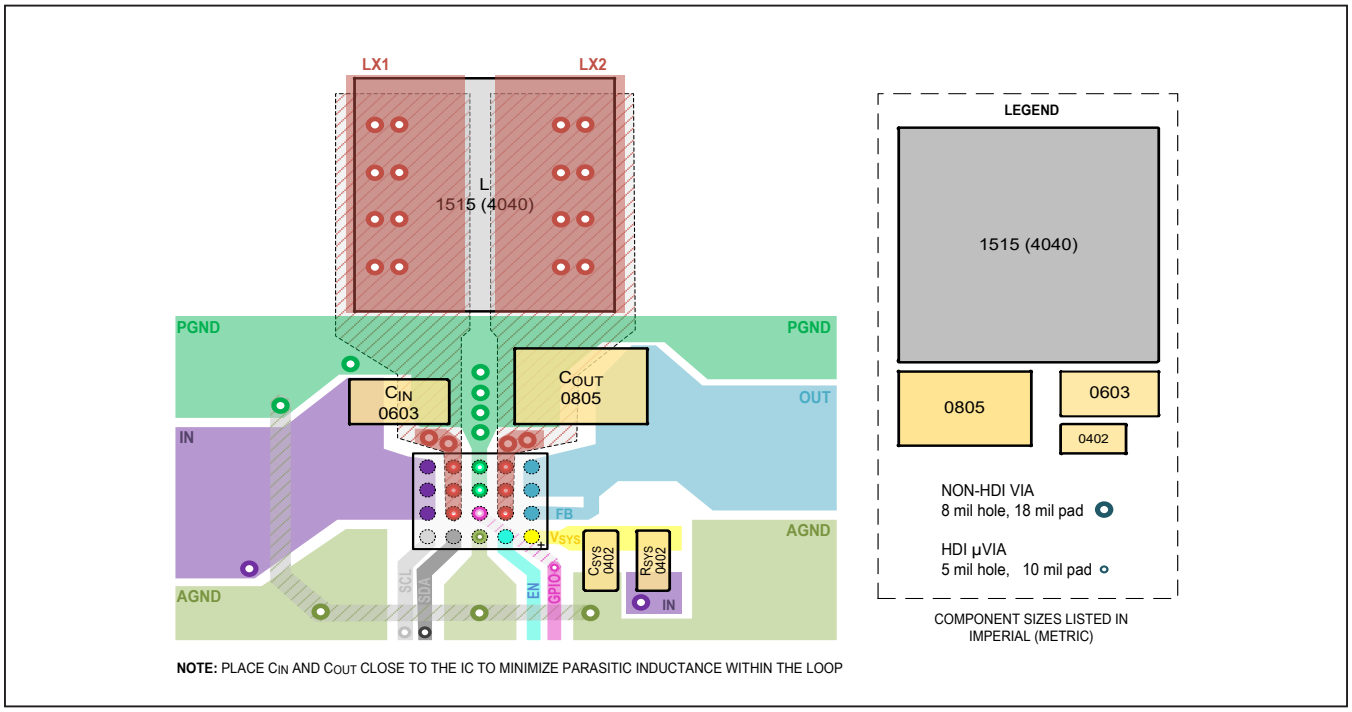


Figure 6. PCB Layout Example (WLP)

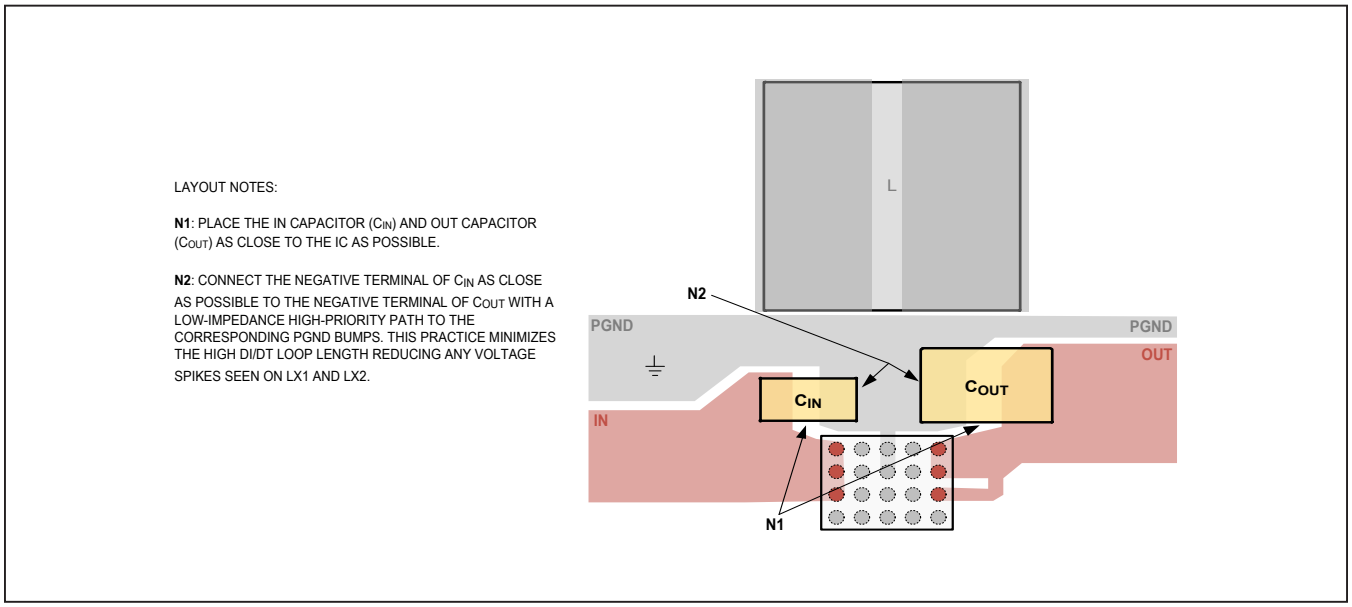


Figure 7. Recommended Capacitor Placement

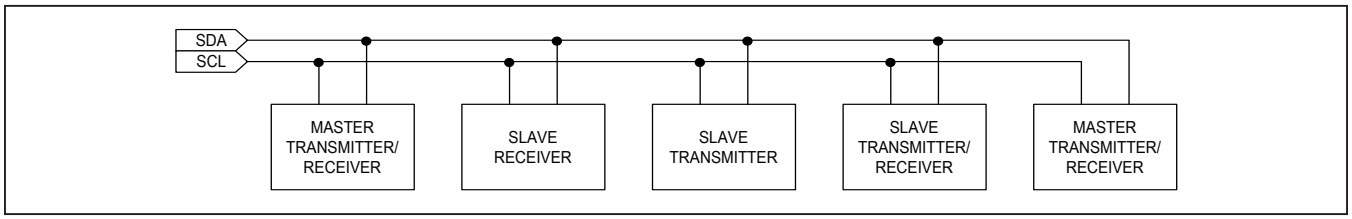


Figure 8. Functional Logic Diagram for Communications Controller

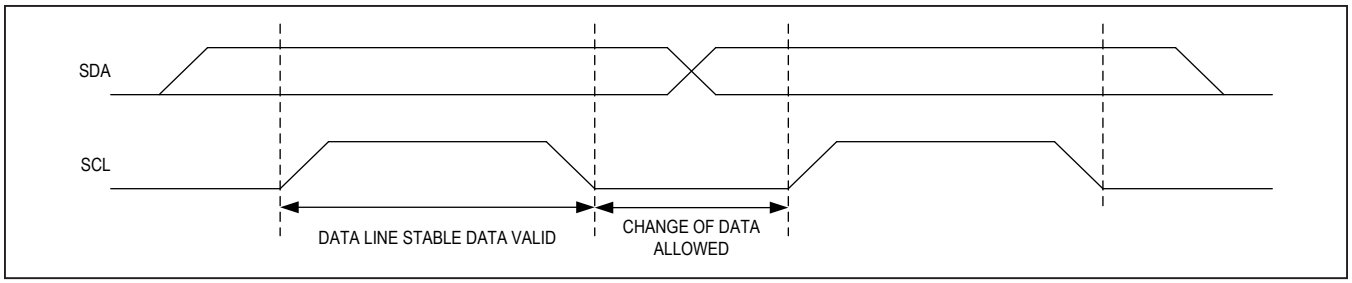


Figure 9. I²C Bit Transfer

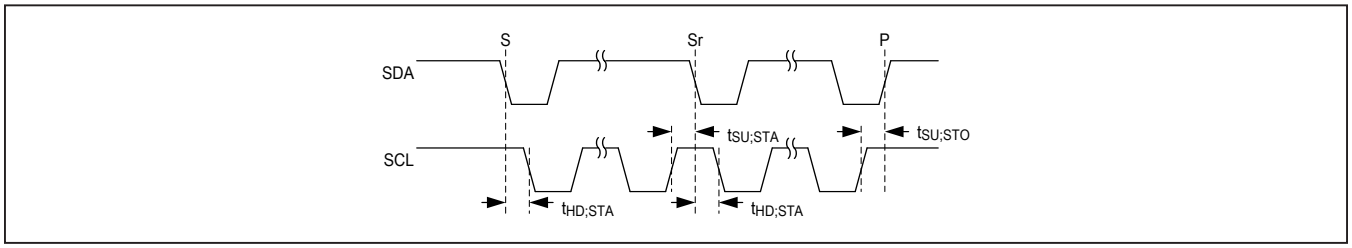


Figure 10. START and STOP Conditions

compatible interface is operating, it is a slave on I2C bus and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the MAX77816. The master terminates transmission by issuing a NOT-ACKNOWLEDGE followed by a STOP condition.

The STOP condition frees the bus. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from I2C serial interface until the next START condition, minimizing digital noise and feedthrough.

Acknowledged

Both the I2C bus master and MAX77816 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The I2C slave address of the IC is shown in Table 3.

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The IC does not implement the I2C specification called a general call address. If the IC sees a general call address (00000000b), it will not issue an ACKNOWLEDGE (A).

Table 3. I2C Slave Address

SLAVE ADDRESS (7 bit)	SLAVE ADDRESS (Write)	SLAVE ADDRESS (Read)
001 1000 (7'h18)	0x30 (0011 0000)	0x31 (0011 0001)

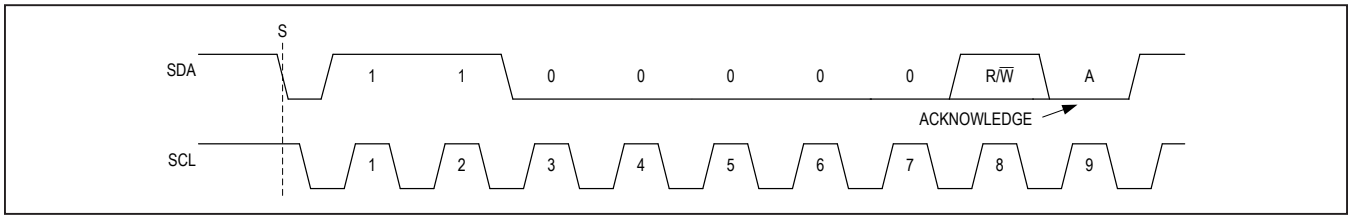


Figure 11. Slave Address Byte Example

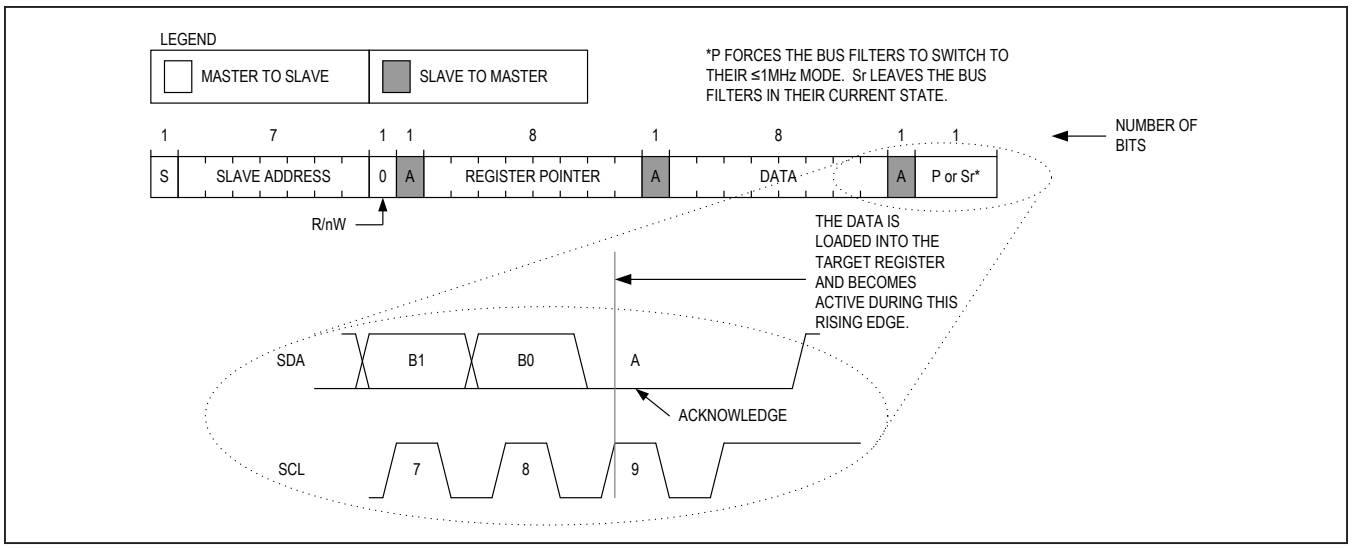


Figure 12. Writing to a Single Register with Write Byte Protocol

Communication Speed

The IC provides I2C 3.0-compatible (3.4MHz) serial interface.

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz).

Communication Protocols

The IC supports both writing and reading from its registers. The following sections show the I2C communication protocols for each functional block. The power block uses the same communications protocols.

Writing to a Single Register

Figure 12 shows the protocol for the I2C master device to write one byte of data to the IC. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

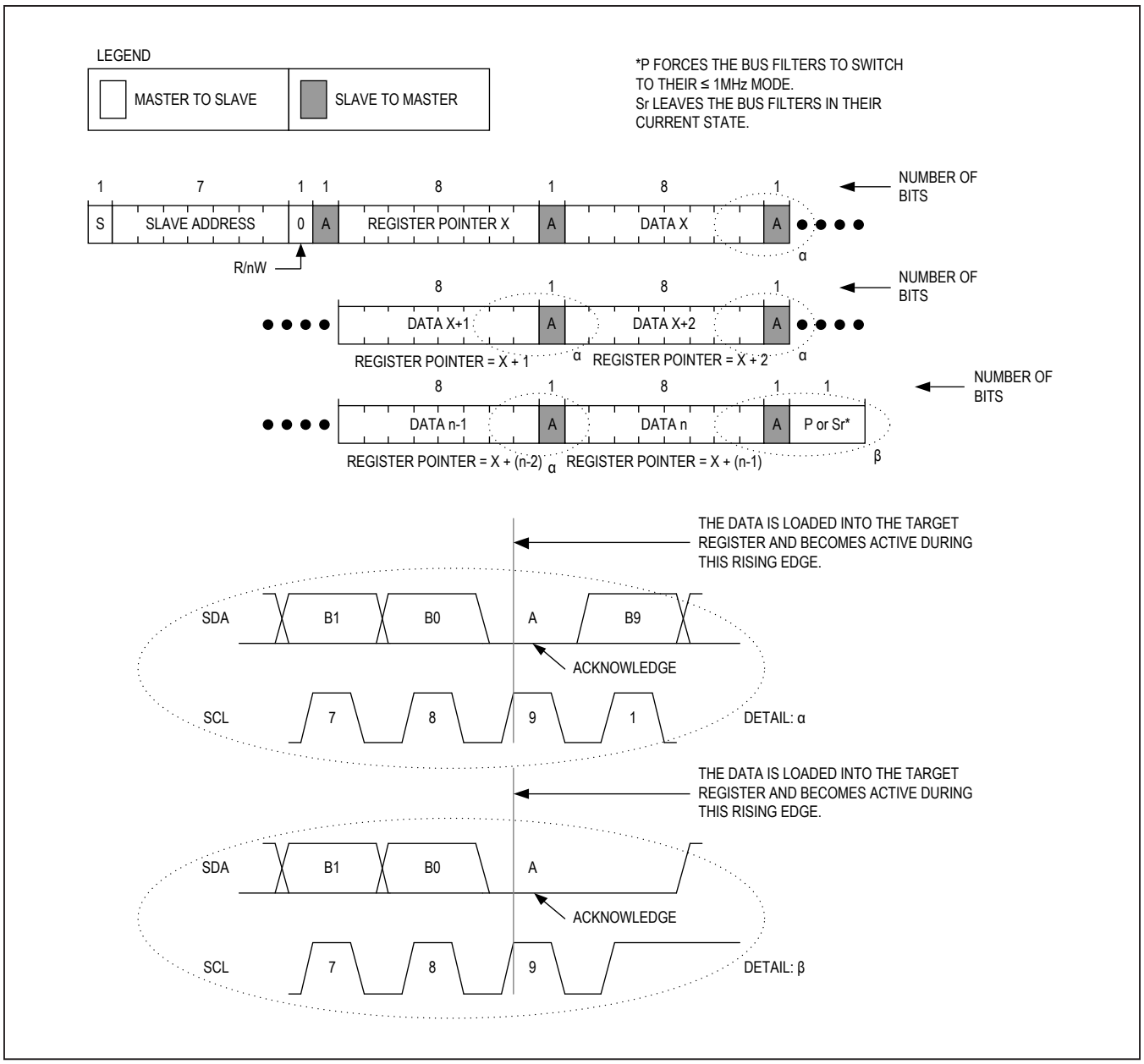


Figure 13. Writing to Sequential Registers X to N

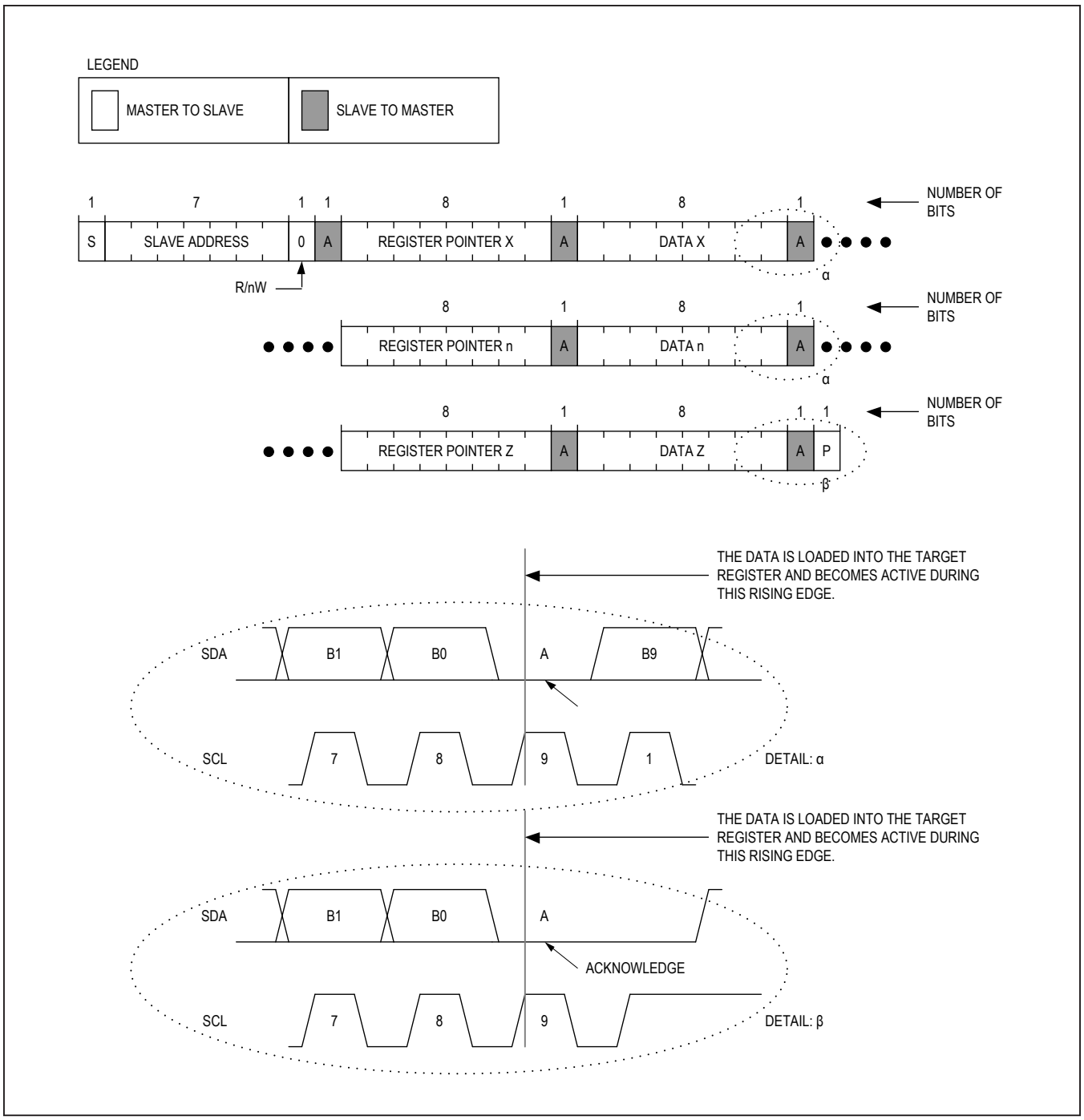


Figure 14. Writing to Multiple Registers with Multiple Byte Register-Data Pairs Protocol

Writing to a Sequential Register

Figure 13 shows the protocol for writing to a sequential register. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The writing to sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Writing Multiple Bytes using Register-Data Pairs

Figure 14 shows the protocol for the I2C master device to write multiple bytes to the IC using register-data pairs. This protocol allows I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP condition.

The multiple byte register-data pair protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) Steps 4 to 7 are repeated as many times as the master requires.
9) The master sends a STOP condition.

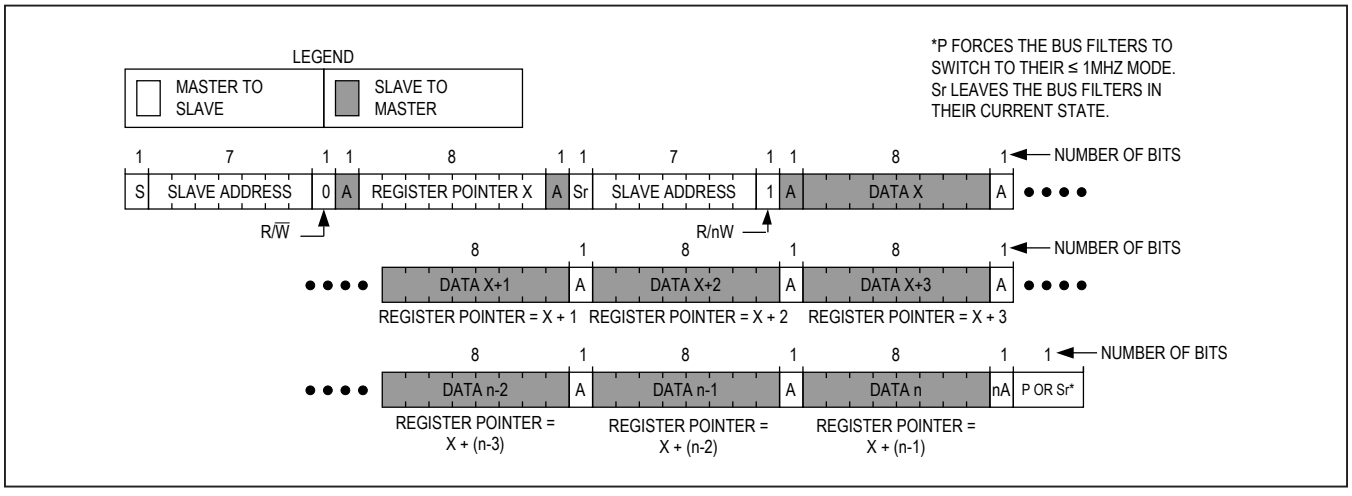


Figure 15. Reading Continuously from Sequential Registers X to N

Reading from a Single Register

The I2C master device reads one byte of data to the IC. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a NOT-ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Reading from a Sequential Register

Figure 15 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data. When the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Registers

Register Map

I2C Slave Address (W/R): 0x30 / 0x31

ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
0x00	DEVICE_ID	RSVD	VERSION[3:0]				CHIP_REV[2:0]			—
0x01	STATUS	RSVD	RSVD	RSVD	RSVD	TSHDN	BB_POKn	BB_OVP	BB_OCP	—
0x02	CONFIG1	ILIM[1:0]		BB_RU_SR	BB_RD_SR	BB_OVP_TH[1:0]		BB_AD	BB_FPWM	0xCE
0x03	CONFIG2	RSVD	BB_EN	EN_PD	POK_POL	RSVD	GPIO_CFG[2:0]			0x71
0x04	VOUT	RSVD	VOUT[6:0]							0x28/ 0x23
0x05	VOUT_H	RSVD	VOUT_H[6:0]							0x78
0x06	INT_MASK	RSVD	RSVD	RSVD	RSVD	THM_INT_MASK	POK_INT_MASK	OVP_INT_MASK	OCP_INT_MASK	0x00
0x07	INT	RSVD	RSVD	RSVD	RSVD	THM_INT	POK_INT	OVP_INT	OCP_INT	—

Register Reset Conditions

Type-O: Registers are reset when $V_{SYS} < V_{UVLO\_F}$ OR EN = LOW

DEVICE_ID

Device ID Register

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: N/A
0x00	Read Only			
BIT	NAME	POR	DESCRIPTION	
7	RESERVED	—		
6:3	VERSION[3:0]	—	Version 0000b: Default	
2:0	CHIP_REV[2:0]	—	Chip Revision History 001b: PASS1	

STATUS

Status Register

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: N/A
0x01	Read Only			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:4	RESERVED	—		
3	TSHDN	—	Thermal Shutdown Status 0: Junction temperature (T_{JCT}) ≤ 165°C 1: Junction temperature (T_{JCT}) > 165°C	
2	BB_POKn	—	Power-OK Status 0: V_{OUTBB} is below the POK threshold 1: V_{OUTBB} is above the POK threshold	
1	BB_OVP	—	Overvoltage Status 0: V_{OUTBB} is below the OVP threshold 1: V_{OUTBB} is above the OVP threshold The OVP threshold is set by BB_OVP_TH[1:0]	
0	BB_OCP	—	Overcurrent Status 0: Inductor peak current is below the ILIM threshold 1: Inductor peak current is above the ILIM threshold The ILIM threshold is set by ILIM[1:0]	

CONFIG1

Configuration Register1

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: 0xCE
0x02	Read, Write			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	ILIM[1:0]	11	Inductor Peak Current Limit 00b: 1.15A 01b: 1.80A 10b: 3.1A 11b: 5A When GPIO_CFG[2:0] = 010b, ILIM[1:0] does not set inductor peak current level. Inductor peak current level is set by GPIO	
5	BB_RU_SR	0	Rising Ramp-Rate Control 0: 20mV/µs 1: 40mV/µs	
4	BB_RD_SR	0	Ramp-Down Slew Rate Control 0: 5mV/µs 1: 10mV/µs	
3:2	BB_OVP_TH[1:0]	11	Output OVP Threshold 00b: No OVP 01b: 110% of V_{OUT} 10b: 115% of V_{OUT} 11b: 120% of V_{OUT}	
1	BB_AD	1	Output Active Discharge 0: Disable active discharge 1: Enable active discharge	
0	BB_FPWM	0	Forced PWM Enable 0: SKIP mode 1: Forced PWM When GPIO_CFG[2:0] = 001b, BB_FPWM does not set inductor peak current level. Inductor peak current level is set by GPIO	

CONFIG2

Configuration Register2

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: 0x71
0x03	Read, Write			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7	RESERVED	0		
6	BB_EN	1	0: Disable buck-boost output 1: Enable buck-boost output	
5	EN_PD	1	EN Input Pulldown Resistor Enable Setting 0: Disable 1: Enable	
4	POK_POL	1	0: Active low 1: Active high	
3	RESERVED	0		
2:0	GPIO_CFG[2:0]	001 (A version)	GPIO Pin Function Configuration 001b: FPWM mode enable, MAX77816A/MAX77816F default 010b: Inductor peak current-limit selection, MAX77816B default 011b: Output voltage selection, MAX77816C default 100b: Power-OK status indication, MAX77816D default 101b: Interrupt indication, MAX77816E default	

VOUT

Output Voltage Setting Register

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: 0x23 (MAX77816B/C/D/E/F) 0x28 (MAX77816A)		
0x04	Read, Write					
BIT	NAME	POR	DESCRIPTION			
7	RESERVED	0				
6:0	VOUT[6:0]	011 1000	Buck-Boost Output Voltage GPIO_CFG[2:0] = 011b: V_{OUT} sets the output voltage when GPIO = low			
			0x00 = 2.60V	0x20 = 3.24V	0x40 = 3.88V	0x60 = 4.52V
			0x01 = 2.62V	0x21 = 3.26V	0x41 = 3.90V	0x61 = 4.54V
			0x02 = 2.64V	0x22 = 3.28V	0x42 = 3.92V	0x62 = 4.56V
			0x03 = 2.66V	0x23 = 3.30V	0x43 = 3.94V	0x63 = 4.58V
			0x04 = 2.68V	0x24 = 3.32V	0x44 = 3.96V	0x64 = 4.60V
			0x05 = 2.70V	0x25 = 3.34V	0x45 = 3.98V	0x65 = 4.62V
			0x06 = 2.72V	0x26 = 3.36V	0x46 = 4.00V	0x66 = 4.64V
			0x07 = 2.74V	0x27 = 3.38V	0x47 = 4.02V	0x67 = 4.66V
			0x08 = 2.76V	0x28 = 3.40V	0x48 = 4.04V	0x68 = 4.68V
			0x09 = 2.78V	0x29 = 3.42V	0x49 = 4.06V	0x69= 4.70V
			0x0A = 2.80V	0x2A = 3.44V	0x4A = 4.08V	0x6A = 4.72V
			0x0B = 2.82V	0x2B = 3.46V	0x4B = 4.10V	0x6B = 4.74V
			0x0C = 2.84V	0x2C = 3.48V	0x4C = 4.12V	0x6C = 4.76V
			0x0D = 2.86V	0x2D = 3.50V	0x4D = 4.14V	0x6D = 4.78V
			0x0E = 2.88V	0x2E = 3.52V	0x4E = 4.16V	0x6E = 4.80V
			0x0F = 2.90V	0x2F = 3.54V	0x4F = 4.18V	0x6F = 4.82V
			0x10 = 2.92V	0x30 = 3.56V	0x50 = 4.20V	0x70 = 4.84V
			0x11 = 2.94V	0x31 = 3.58V	0x51 = 4.22V	0x71 = 4.86V
			0x12 = 2.96V	0x32 = 3.60V	0x52 = 4.24V	0x72 = 4.88V
			0x13 = 2.98V	0x33 = 3.62V	0x53 = 4.26V	0x73 = 4.90V
			0x14 = 3.00V	0x34 = 3.64V	0x54 = 4.28V	0x74 = 4.92V
			0x15 = 3.02V	0x35 = 3.66V	0x55 = 4.30V	0x75 = 4.94V
			0x16 = 3.04V	0x36 = 3.68V	0x56 = 4.32V	0x76 = 4.96V
			0x17 = 3.06V	0x37 = 3.70V	0x57 = 4.34V	0x77 = 4.98V
			0x18 = 3.08V	0x38 = 3.72V	0x58 = 4.36V	0x78 = 5.00V
			0x19 = 3.10V	0x39 = 3.74V	0x59 = 4.38V	0x79 = 5.02V
			0x1A = 3.12V	0x3A = 3.76V	0x5A = 4.40V	0x7A = 5.04V
			0x1B = 3.14V	0x3B = 3.78V	0x5B = 4.42V	0x7B = 5.06V
			0x1C = 3.16V	0x3C = 3.80V	0x5C = 4.44V	0x7C = 5.08V
			0x1D = 3.18V	0x3D = 3.82V	0x5D = 4.46V	0x7D = 5.10V
			0x1E = 3.20V	0x3E = 3.84V	0x5E = 4.48V	0x7E = 5.12V
			0x1F = 3.22V	0x3F = 3.86V	0x5F = 4.50V	0x7F = 5.14V

VOUT_H

Output Voltage Setting Register for MAX77816C, GPIO = HIGH

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: 0x78		
0x05	Read, Write					
BIT	NAME	POR	DESCRIPTION			
7	RESERVED	0				
6:0	VOUT_H[6:0]	011 1000	Buck-Boost Output Voltage GPIO_CFG[2:0]=011b: VOUT_H sets the output voltage when GPIO = high GPIO_CFG[2:0]≠011b: VOUT_H does not control the output voltage			
			0x00 = 2.60V	0x20 = 3.24V	0x40 = 3.88V	0x60 = 4.52V
			0x01 = 2.62V	0x21 = 3.26V	0x41 = 3.90V	0x61 = 4.54V
			0x02 = 2.64V	0x22 = 3.28V	0x42 = 3.92V	0x62 = 4.56V
			0x03 = 2.66V	0x23 = 3.30V	0x43 = 3.94V	0x63 = 4.58V
			0x04 = 2.68V	0x24 = 3.32V	0x44 = 3.96V	0x64 = 4.60V
			0x05 = 2.70V	0x25 = 3.34V	0x45 = 3.98V	0x65 = 4.62V
			0x06 = 2.72V	0x26 = 3.36V	0x46 = 4.00V	0x66 = 4.64V
			0x07 = 2.74V	0x27 = 3.38V	0x47 = 4.02V	0x67 = 4.66V
			0x08 = 2.76V	0x28 = 3.40V	0x48 = 4.04V	0x68 = 4.68V
			0x09 = 2.78V	0x29 = 3.42V	0x49 = 4.06V	0x69 = 4.70V
			0x0A = 2.80V	0x2A = 3.44V	0x4A = 4.08V	0x6A = 4.72V
			0x0B = 2.82V	0x2B = 3.46V	0x4B = 4.10V	0x6B = 4.74V
			0x0C = 2.84V	0x2C = 3.48V	0x4C = 4.12V	0x6C = 4.76V
			0x0D = 2.86V	0x2D = 3.50V	0x4D = 4.14V	0x6D = 4.78V
			0x0E = 2.88V	0x2E = 3.52V	0x4E = 4.16V	0x6E = 4.80V
			0x0F = 2.90V	0x2F = 3.54V	0x4F = 4.18V	0x6F = 4.82V
			0x10 = 2.92V	0x30 = 3.56V	0x50 = 4.20V	0x70 = 4.84V
			0x11 = 2.94V	0x31 = 3.58V	0x51 = 4.22V	0x71 = 4.86V
			0x12 = 2.96V	0x32 = 3.60V	0x52 = 4.24V	0x72 = 4.88V
			0x13 = 2.98V	0x33 = 3.62V	0x53 = 4.26V	0x73 = 4.90V
			0x14 = 3.00V	0x34 = 3.64V	0x54 = 4.28V	0x74 = 4.92V
			0x15 = 3.02V	0x35 = 3.66V	0x55 = 4.30V	0x75 = 4.94V
			0x16 = 3.04V	0x36 = 3.68V	0x56 = 4.32V	0x76 = 4.96V
			0x17 = 3.06V	0x37 = 3.70V	0x57 = 4.34V	0x77 = 4.98V
			0x18 = 3.08V	0x38 = 3.72V	0x58 = 4.36V	0x78 = 5.00V
			0x19 = 3.10V	0x39 = 3.74V	0x59 = 4.38V	0x79 = 5.02V
			0x1A = 3.12V	0x3A= 3.76V	0x5A = 4.40V	0x7A = 5.04V
			0x1B = 3.14V	0x3B = 3.78V	0x5B = 4.42V	0x7B = 5.06V
			0x1C = 3.16V	0x3C = 3.80V	0x5C = 4.44V	0x7C = 5.08V
			0x1D = 3.18V	0x3D = 3.82V	0x5D = 4.46V	0x7D = 5.10V
			0x1E = 3.20V	0x3E = 3.84V	0x5E = 4.48V	0x7E = 5.12V
			0x1F = 3.22V	0x3F = 3.86V	0x5F = 4.50V	0x7F = 5.14V

INT_MASK

Interrupt Mask Register

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: 0x00
0x06	Read, Write			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:4	RESERVED	0000		
3	THM_INT_MASK	0	Thermal Shutdown Interrupt Mask Bit 0: Unmask 1: Mask	
2	POK_INT_MASK	0	Power-OK Interrupt Mask Bit 0: Unmask 1: Mask	
1	OVP_INT_MASK	0	OVP Interrupt Mask Bit 0: Unmask 1: Mask	
0	OCP_INT_MASK	0	OCP interrupt mask bit 0: Unmask 1: Mask	

INT

Interrupt Status Register

ADDRESS	ACCESS TYPE		TYPE: O	RESET VALUE: N/A
0x07	Read and Clear			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:4	RESERVED	0000		
3	THM_INT	0	Thermal Shutdown Interrupt Bit 0: No status change or status change from 1 to 0 for TSHDN 1: Status change from 0 to 1 happened for TSHDN	
2	POK_INT	0	Power-OK Interrupt Bit 0: No status change or status change from 1 to 0 for BB_POKn 1: Status change from 1 to 0 happened for BB_POKn	
1	OVP_INT	0	OVP Interrupt Bit 0: No status change or status change from 1 to 0 for BB_OVP 1: Status change from 0 to 1 happened for BB_OVP	
0	OCP_INT	0	OCP Interrupt Bit 0: No status change or status change from 1 to 0 for BB_OCP 1: Status change from 0 to 1 happened for BB_OCP	

Ordering Information

PART	DEFAULT V_{OUT}	GPIO DEFAULT TYPE	GPIO DEFAULT FUNCTION
MAX77816AEWP+T	3.4V	Input	FPWM Mode Enable
MAX77816BEWP+T	3.3V	Input	Inductor Peak Current Limit Selection
MAX77816CEWP+T	3.3V/5V	Input	Output Voltage Selection
MAX77816DEWP+T	3.3V	Output	Power-OK Status Indication
MAX77816EEWP+T*	3.3V	Output	Interrupt Indication
MAX77816FEWP+T*	3.3V	Input	FPWM Mode Enable

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—Contact Maxim for availability.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W201F2+1	**21-0771**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	3/18	Released MAX77816B and MAX77816C, added MAX77816F information	1, 2, 7, 8, 18, 21–23, 25, 26
2	6/19	Updated package measurements, added *PCB Layout Guidelines* section, updated *Ordering Information* table	7, 11, 27
3	10/19	Updated LXBB in the *Absolute Maximum Ratings* section, updated Shutdown Supply Current and LXBB1/2 Current Limit in the *Electrical Characteristics* table	2, 3