MAX77887

Nano Power Buck-Boost with Input Voltage Monitor

General Description

The MAX77887 is a high-efficiency nano power buck-boost converter with an input voltage monitoring feature, ensuring that the battery voltage does not drop below the pre-set threshold levels to protect the battery.

The converter operates on an input supply between 1.8V and 5.5V. Output voltage between 1.8V and 5.2V is configured through a resistor connected to the hardware control pin, R_{SEL1}. It can operate in CCM, Skip, and Low Power Mode to ensure maximum efficiency over a wide range of load currents.

MAX77887 offers two unique hardware control pins R_{SEL1} and R_{SEL2}. The resistor connected at SEL1 (R_{SEL1}) selects the predefined output voltage from 1.8V to 5.2V as OUT. The resistor connected at SEL2 (R_{SEL2}) allows the configuration of two different Switching Current Limit (I_{LIM}) levels and 16 Input Voltage Monitoring Threshold levels.

The MAX77887 is available in 1.36mm x 1.36mm, 9-bump, 0.4mm pitch, wafer-level package (WLP).

Applications

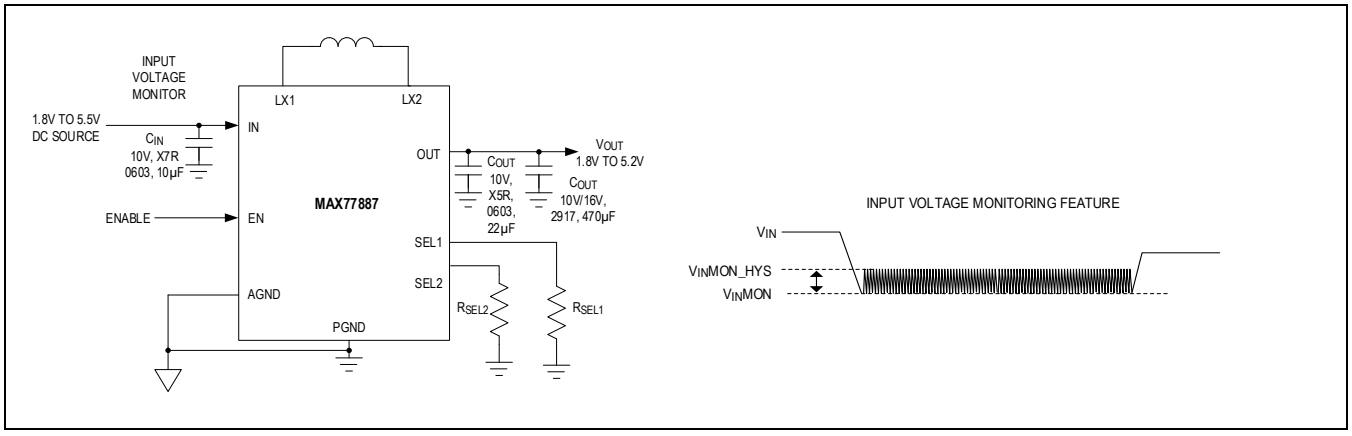
- LPWAN SoC Companion Power Solution
- IoT and Wearable Applications
- Asset Trackers
- Smart Meters

Benefits and Features

- 1.8V to 5.5V Input Voltage
- Output Voltage from 1.8V to 5.2V
- Peak Efficiency of 92.5% ($5.5V_{IN}$, $3.8V_{OUT}$)
- 430nA Typical Quiescent Current
- 10nA Shutdown Current
- R_{SEL} Configurations
  - Output Voltage
  - 400mA/200mA Switching Current Limit
  - 16 Input Voltage Monitoring Threshold Levels
- Protection Features
  - Input Undervoltage Lockout (UVLO)
  - Switching Current Limit
  - Thermal Shutdown (THS)
- 1.36mm x 1.36mm, 9-Bump, 0.4mm Pitch, WLP

***Ordering Information* appears at end of data sheet.**

1-Cell Buck-Boost Converter with Input Voltage Protection Application Circuit



19-101837; Rev 0; 3/24

Absolute Maximum Ratings

IN, OUT, LX1, LX2 to GND ..... -0.3V to +6.0V

EN, SEL1, SEL2 to GND ..... -0.3V to V_{IN} + 0.3V

Continuous Power Dissipation for WLP Package at T_A = +70°C (derate 11.91mW/°C above +70°C) (Note 1)..... 952.56mW

Maximum Junction Temperature .....+150°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (reflow).....+260°C

Note 1: Package thermal measurement is based on the JESD-51 series.

Note 2: Thermal parameters are based on FR-4, 4-layer board.

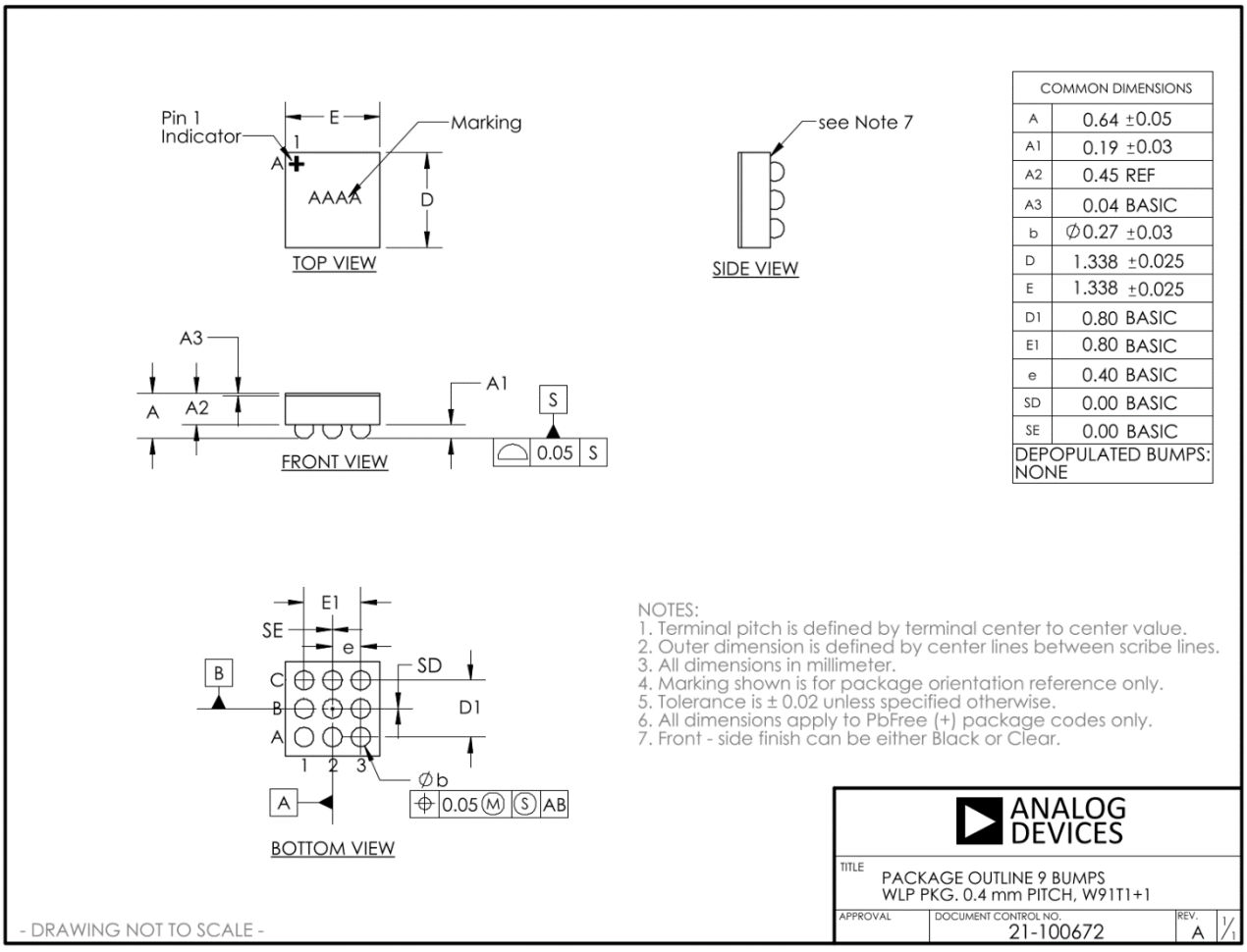
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W91T1+1
Outline Number	*21-100672*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	83.98°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	1.338 ±0.025
E	1.338 ±0.025
D1	0.80 BASIC
E1	0.80 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE
PACKAGE OUTLINE 9 BUMPS
WLP PKG. 0.4 mm PITCH, W91T1+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100672	A	1/1

- DRAWING NOT TO SCALE -

Electrical Characteristics

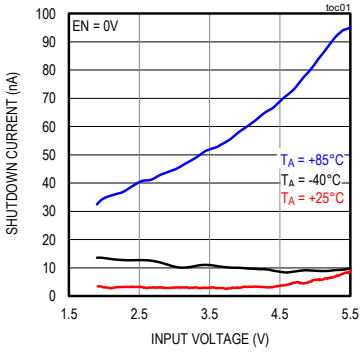
(Typical values are at $T_J \approx T_A$ = +25°C, V_{IN} = +3.6V, V_{OUT} = +3.3V, unless otherwise specified. Limits are 100% tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant supply voltage range are guaranteed by design and characterization unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Operating Voltage Range	V_{IN}			1.8		5.5	V
Input Undervoltage Lockout	V_{UVLO_rising}			1.7	1.75	1.8	V
UVLO Hysteresis	V_{UVLO_Hys}	$V_{UVLO\_rising} - V_{UVLO\_falling}$			60		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = +25°C			10	100	nA
Input Quiescent Current	I_Q	EN = HIGH, no switching, T_J = +25°C			430	930	nA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}			1.8		5.2	V
Output Voltage Accuracy	V_{OUT_ACC}	In CCM mode, T_J = -40°C to +125°C		-2		+2	%
		LPM and Skip mode at T_J = 25°C		-1.0		+4.0	
EN LOGIC LEVEL							
Input LOW Level	V_{IL}					0.4	V
Input HIGH Level	V_{IH}			1.2			V
THERMAL PROTECTION							
Thermal Shutdown Threshold	T_{SHDN}	T_J rising			165		°C
Thermal shutdown Hysteresis	T_{HYS}	$T_{SHDN\_R} - T_{SHDN\_F}$			20		°C
BUCK-BOOST REGULATOR							
High-Side Switching Current Limit	I_{LIM}	V_{IN} = 1.8V to 5.5V, L = 4.7µH	66.5kΩ ≤ R_{SEL2}	340	400	460	mA
			R_{SEL2} ≤ 56.2kΩ	160	200	240	
Low-Side Switch On Resistance	R_{DSON_LOW}	I_{LX} = +180mA			250		mΩ
High-Side Switch On Resistance	R_{DSON_HIGH}	I_{LX} = -180mA			250		mΩ
Turn-On Delay Time	t_{DLY_EN}	Delay from rising edge of EN signal to start of output voltage ramp			1.6	2.7	ms
Line Regulation	$\Delta V/\Delta V_{INx}$	V_{IN} = 1.8V to 5.5V, I_{OUT} = 0A, 50mA		-1.1		+1.1	%
Load Regulation	ΔV	I_{OUT} = 10mA to 200mA (CCM mode), I_{LIM} = 400mA, V_{IN} = 3.6V, V_{OUT} = 3.3V			0.7		%
		I_{OUT} = 10mA to 75mA (CCM mode), I_{LIM} = 200mA, V_{IN} = 3.6V, V_{OUT} = 3.3V			0.8		
Minimum Effective Output Capacitance	$C_{EFF(Min)}$				100		µF

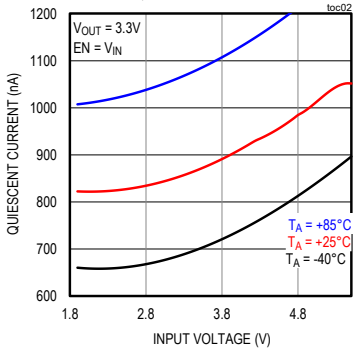
Typical Operating Characteristics

(V_{IN} = 3.6V, V_{OUT} = 3.3V, L = 4.7µH (Murata DFE201610E-4R7M = P2), C_{OUT} = 22µF Ceramic + 100µF Electrolytic, I_{LIM} = 400mA, $V_{IN}MON$ = 1.8V, T_A = +25°C, unless otherwise noted.)

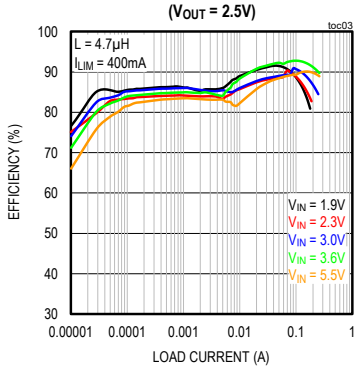
SHUTDOWN CURRENT



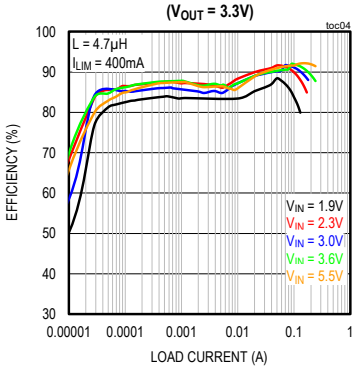
QUIESCENT CURRENT



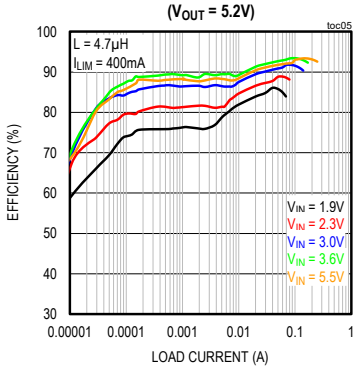
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V)



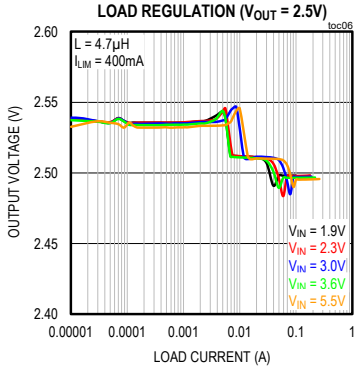
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



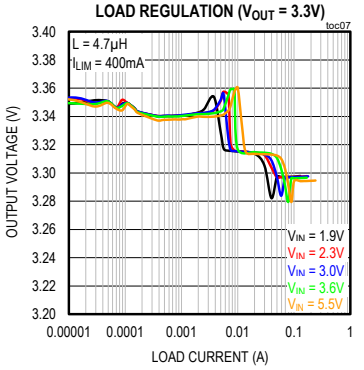
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5.2V)



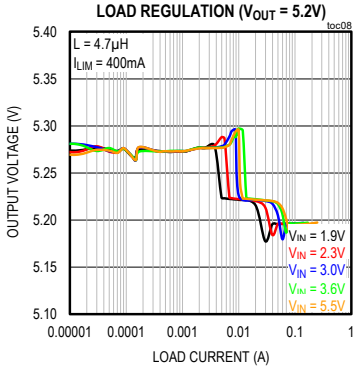
LOAD REGULATION (V_{OUT} = 2.5V)



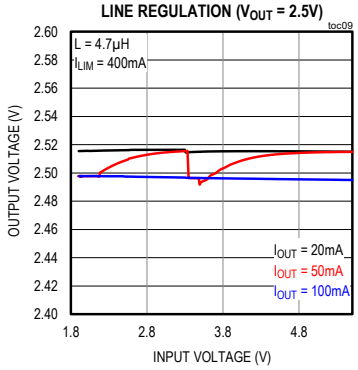
LOAD REGULATION (V_{OUT} = 3.3V)



LOAD REGULATION (V_{OUT} = 5.2V)

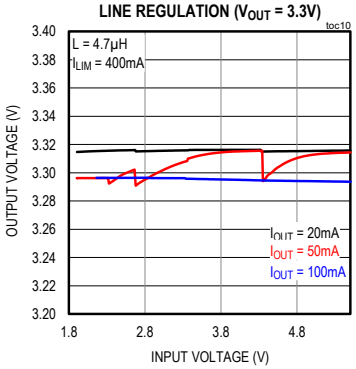


LINE REGULATION (V_{OUT} = 2.5V)

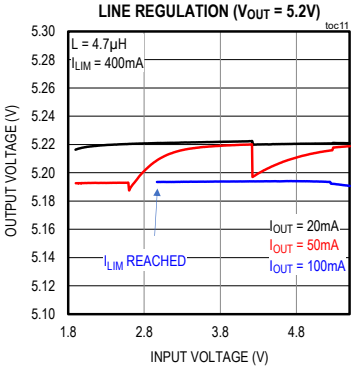


(V_{IN} = 3.6V, V_{OUT} = 3.3V, L = 4.7µH (Murata DFE201610E-4R7M = P2), C_{OUT} = 22µF Ceramic + 100µF Electrolytic, I_{LIM} = 400mA, V_{IN}MON = 1.8V, T_A = +25°C, unless otherwise noted.)

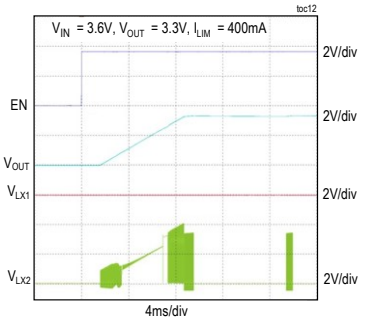
LINE REGULATION (V_{OUT} = 3.3V)



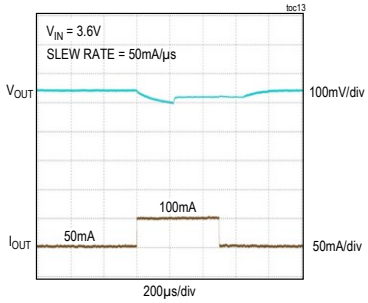
LINE REGULATION (V_{OUT} = 5.2V)



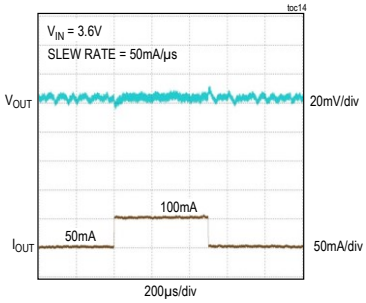
ENABLE STARTUP WAVEFORM



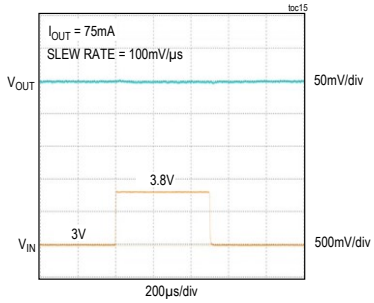
LOAD TRANSIENT
V_{OUT} = 3.3V



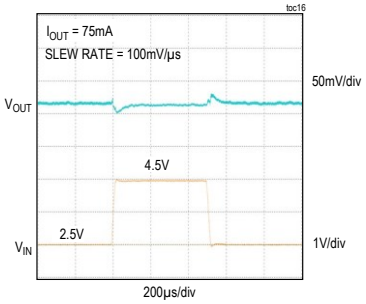
LOAD TRANSIENT
V_{OUT} = 5.2V



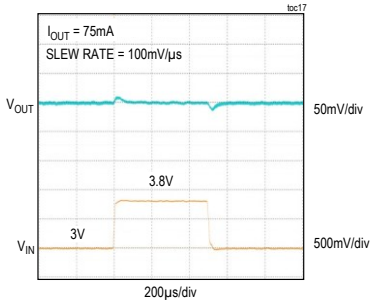
LINE TRANSIENT
V_{OUT} = 2.0V



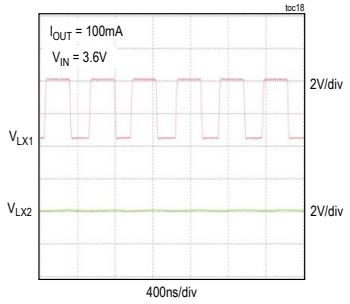
LINE TRANSIENT
V_{OUT} = 3.3V



LINE TRANSIENT
V_{OUT} = 5.2V



SWITCHING WAVEFORM
V_{OUT} = 2.0V



(V_{IN} = 3.6V, V_{OUT} = 3.3V, L = 4.7µH (Murata DFE201610E-4R7M = P2), C_{OUT} = 22µF Ceramic + 100µF Electrolytic, I_{LIM} = 400mA, $V_{IN}MON$ = 1.8V, T_A = +25°C, unless otherwise noted.)

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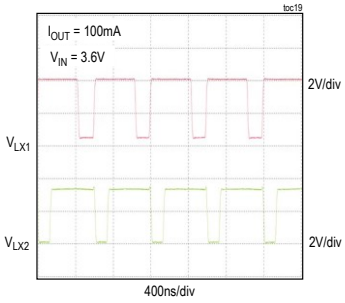
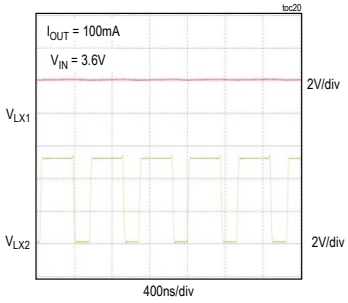
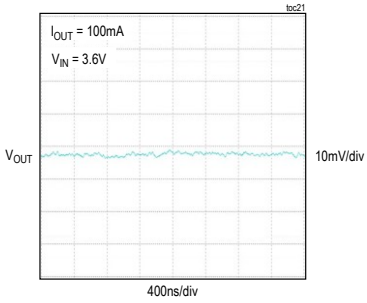


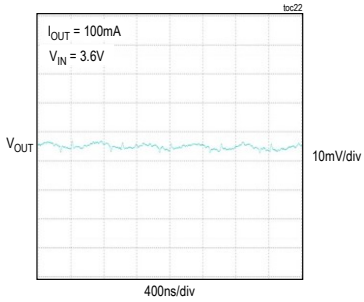
SWITCHING WAVEFORM
V_{OUT} = 5.2V



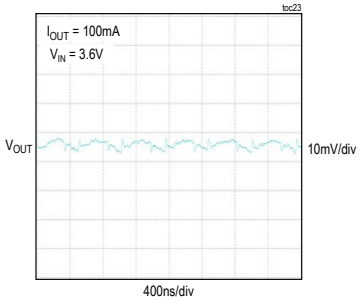
OUTPUT VOLTAGE RIPPLE
V_{OUT} = 2.0V



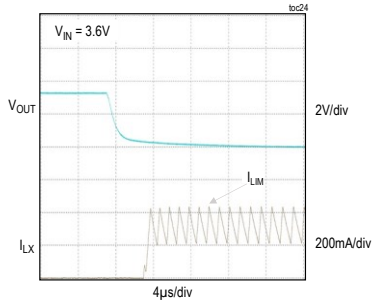
OUTPUT VOLTAGE RIPPLE
V_{OUT} = 3.3V



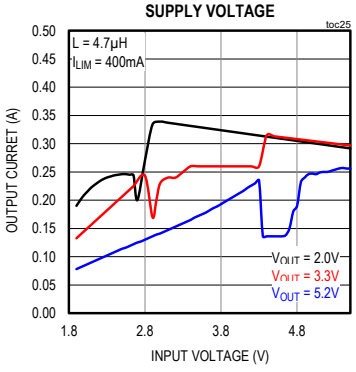
OUTPUT VOLTAGE RIPPLE
V_{OUT} = 5.2V



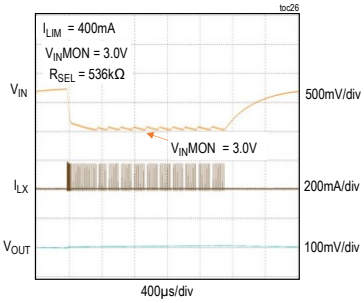
SHORT-CIRCUIT RESPONSE
3.3V OUTPUT (I_{LIM} = 400 mA)



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE

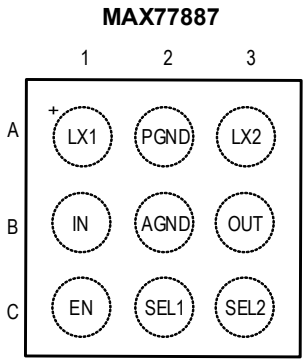


V_{IN} MONITOR FUNCTIONALITY
V_{OUT} = 3.3V, SOURCE IMPEDANCE = 100Ω



Pin Configuration

TOP VIEW
(BUMP SIDE DOWN)

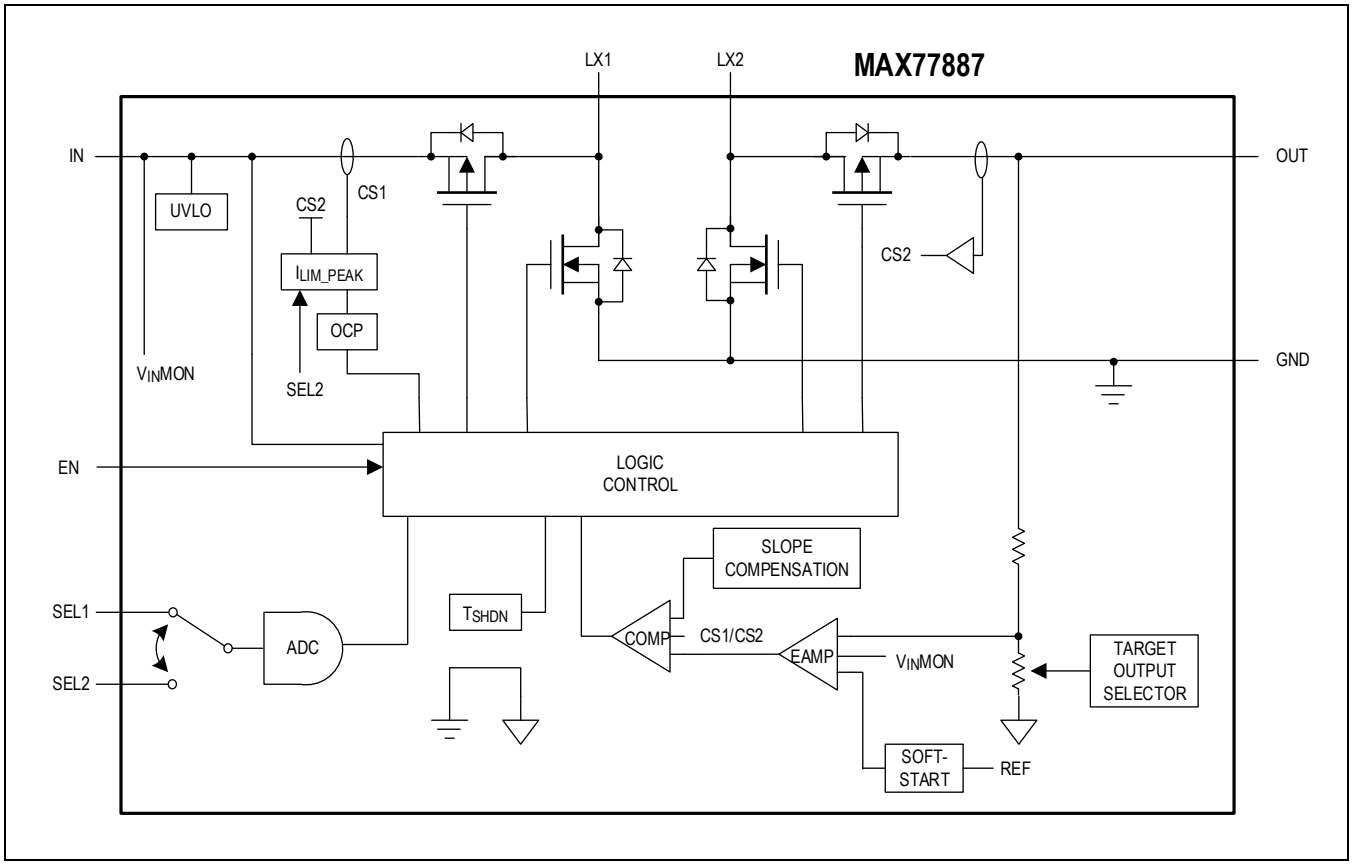


9-BUMP WLP
(1.36mm x 1.36mm x 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION	Type
A1	LX1	Switching Node 1 of Buck-Boost Converter	Power
A2	PGND	Buck-Boost Converter Power Ground	Power Ground
A3	LX2	Switching Node 2 of Buck-Boost Converter	Power
B1	IN	Buck-Boost Converter Input. Bypass with a 10V 10µF ceramic capacitor to GND pin.	Power Input
B2	AGND	Buck-Boost Converter Analog Ground	Analog Ground
B3	OUT	Buck-Boost Converter Output. Bypass with a 10V 22µF ceramic capacitor to GND pin.	Power Output
C1	EN	Buck-Boost Enable Input	Digital Input
C2	SEL1	Configuration Selection. Connect a resistor between SEL1 and PGND. See *Table 1* for resistor values and configurations.	Analog Input
C3	SEL2	Configuration Selection. Connect a resistor between SEL2 and PGND. See *Table 2* for resistor values and configurations.	Analog Input

Block Diagram



Detailed Description

The MAX77887 is a nano power buck-boost with ultra-low quiescent current (430nA, typ) and high efficiency with an input range of 1.8V to 5.5V. The IC offers the Input Voltage Monitor feature which can protect the battery voltage from dropping below the preset threshold level in pulse load conditions. The IC is ideal for either primary battery-powered applications or double alkaline battery-powered applications that require long standby/idling time with short working time, such as asset tracking devices, or wearables. The IC operates in Low Power Mode (LPM), Skip Mode, or CCM Mode depending on operating conditions to achieve optimized efficiency performance.

The resistor between the SEL1 pin and GND (R_{SEL1}) can be used to select the output voltage level within a range of 1.8V to 5.2V. The resistor between the SEL2 pin and GND (R_{SEL2}) is used to set the following:

- Switching Current Limit (I_{LIM})
- Input Voltage Monitor Threshold levels (V_{MINMON})

See the *SEL Pin Configuration* section for more details.

Start-Up

The start-up behavior is depicted in *Figure 1*. When EN goes logic HIGH and $V_{IN} > V_{UVLO\_R}$, the IC starts up by turning on the bias circuits, after which the resistance value at the two SEL pins is read sequentially. The IC typically takes 1.6ms (T_{DLY_EN}, start-up delay time) after the rising edge of the EN signal to start the soft-start process.

During soft-start, the slew rate is maintained at 0.5V/ms. The soft-start procedure is completed when the output reaches the target regulation voltage.

If the output is pre-biased to the target voltage level, the device skips the soft-start procedure and directly enters normal regulation.

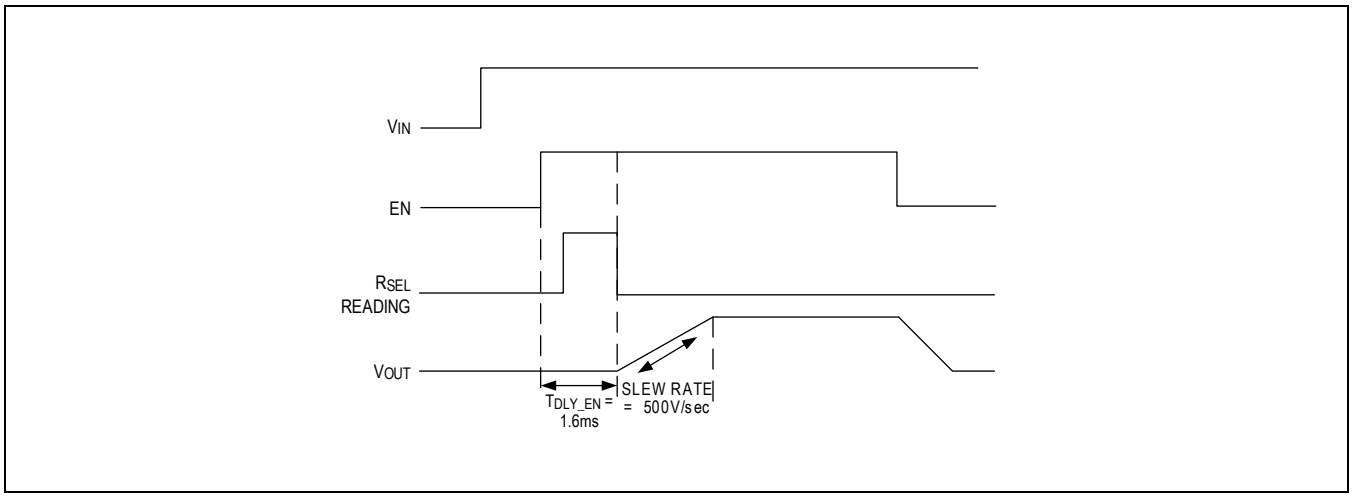


Figure 1. Start-Up Behavior

Buck-Boost Control Scheme

The buck-boost converter operates using adaptive on-time current-mode control. The buck-boost utilizes an H-bridge topology to regulate the output voltage using a single inductor and output capacitor.

The H-bridge topology has three switching phases. See *Figure 2* for details.

- $\Phi 1$ switch period (Phase 1: HS1 = ON, LS2 = ON) stores energy in the inductor. Inductor current ramps up at a rate proportional to the input voltage divided by inductance: V_{IN}/L.
- $\Phi 2$ switch period (Phase 2: HS1 = ON, HS2 = ON) ramps inductor current up or down depending on the differential voltage across the inductor: $(V_{IN} - V_{OUT})/L$.
- $\Phi 3$ switch period (Phase 3: LS1 = ON, HS2 = ON) ramps inductor current down at a rate proportional to the output voltage divided by inductance: $(-V_{OUT}/L)$.

Boost operation ($V_{IN} < V_{OUT}$) utilizes $\Phi 2$ and $\Phi 1$ within one cycle during the preconfigured off time. See the representation of the inductor current waveform for boost mode operation in *Figure 2*.

Buck operation ($V_{IN} > V_{OUT}$) utilizes $\Phi 2$ and $\Phi 3$ within one cycle during the preconfigured on time. See the representation of the inductor current waveform for buck mode operation in *Figure 2*.

Three-phase operation (V_{IN} close to V_{OUT}) utilizes $\Phi 1$ for a pre-configured buck-boost on time, $\Phi 2$ is triggered for preconfigured on time, and then $\Phi 3$ is triggered till the current reaches zero. See the representation of the inductor current waveform for the three-phase mode operation in *Figure 2*.

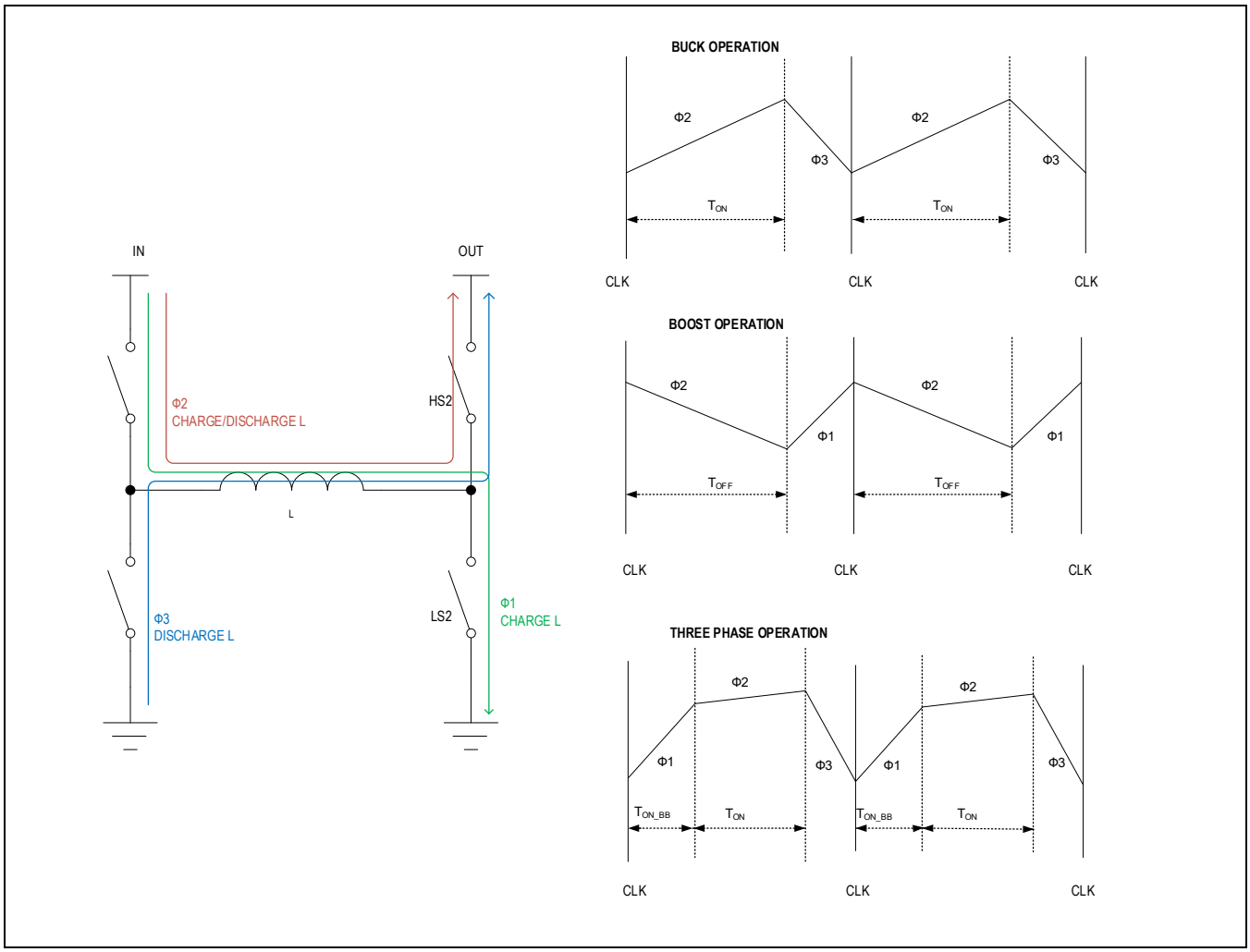


Figure 2. Buck-Boost H-Bridge Topology

Low Power Mode

The IC automatically enters Low Power Mode (LPM) when the load current is very low to achieve high efficiency at light loads. In this mode, the error amplifier and other internal blocks are deactivated to lower I_Q consumption. A low-power voltage comparator is used to monitor the output voltage in LPM.

When the load current reduces and the switching frequency falls to F_{MIN} (133kHz, typ), the part switches at F_{MIN} till the output voltage reaches above 2% of the target output voltage. After the output voltage crosses this level, the part is in Low Power Mode. In Low Power Mode, the IC generates an on-time of predetermined length when the output voltage reaches 2% above the target output voltage. When the load is increased, the IC must switch at a higher frequency to service the load and when the switching frequency reaches F_{MIN}, the part switches at F_{MIN} till the output falls to the target voltage. When the output hits the target voltage, the part enters Skip Mode.

SKIP Mode and CCM Mode

When the load is high enough and the switching frequency is higher than the F_{MIN} (133kHz, typ), the part exits Low Power Mode and enters Skip Mode. In the Skip Mode of operation, an on-time of predetermined length is triggered when the output voltage reaches the target value. During the Skip Mode of operation, the negative inductor current is prevented by turning off the FETs after the inductor current crosses 0A.

At higher output load currents when the inductor current does not have zero crossing, the part enters CCM (Continuous Conduction Mode) where the part operates using adaptive on-time control. The IC regulates to target voltage during the CCM mode of operation.

Thermal Shutdown

When the junction temperature exceeds T_{SHDN_R} (165°C, typ), thermal protection of the MAX77887 is triggered causing the buck-boost converter output to be disabled until the junction temperature drops below thermal protection falling threshold level T_{SHDN_F} (145°C, typ). The part automatically starts up again when the junction temperature drops below the thermal protection falling threshold.

Undervoltage Lockout

When V_{IN} falls below V_{UVLO_F} (1.69V, typ), the buck-boost regulator is disabled, and all registers are reset. The IC is re-enabled only when V_{IN} rises above V_{UVLO_R} (1.75V, typ).

Switching Current Limit

The MAX77887 provides cycle by cycle-by-cycle switching current limit to protect the IC and the system. The IC senses the peak switching current of the high side switches during on time. When the peak current reaches the Switching Current Limit (I_{LIM}), the switches for the charging phase are turned off and the switches used to discharge the inductor current are turned on until the peak current reaches the valley current limit. This procedure continues until the peak switching current no longer hits the I_{LIM} threshold. The IC supports two different Switching Current Limits 400mA (higher limit) and 200mA (lower limit) which can be configured using R_{SEL2}. For more information see the *SEL Pin Configuration* section.

Input Voltage Monitor

The MAX77887 provides an input voltage monitor feature which ensures battery voltage does not drop below the preset threshold – Input Voltage Monitor Threshold level (V_{IN}MON) to protect the battery. When the MAX77887 detects the input recovers to the V_{IN}MON_HYS level, the IC starts switching again. This procedure continues until the IC does not detect V_{IN} dropping to the V_{IN}MON level. If V_{IN} does not drop to the V_{IN}MON level any further, the IC resumes its normal switching pattern.

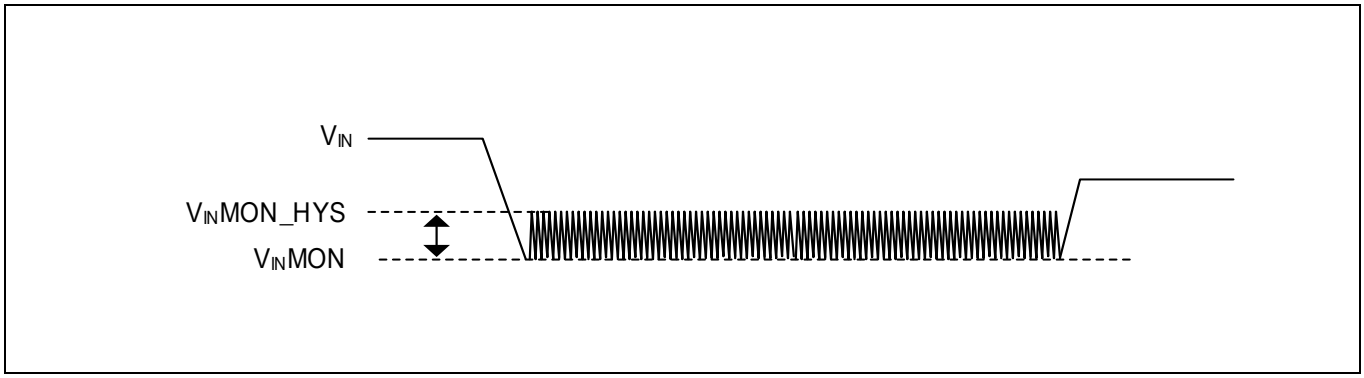


Figure 3. V_{IN}MON Feature

SEL Pin Configurations

MAX77887 has two hardware configuration pins (SEL1 and SEL2) to configure the features of the part. A resistor tied between SEL1 and ground (R_{SEL1}) is used to select the output voltage level (OUT). A resistor tied between SEL2 and ground (R_{SEL2}) is used to select the Switching Current Limit and Input Voltage Monitor Threshold levels.

Table 1. R_{SEL1} Selection Table

R_{SEL1} (kΩ)	OUT (V)	R_{SEL1} (kΩ)	OUT (V)
Short	3.3	66.5	3.4
4.99	1.8	80.6	3.6
5.90	1.9	95.3	3.7
7.15	2.0	113	3.8
8.45	2.1	133	3.9
10.0	2.2	162	4.0
11.8	2.3	191	4.1
14.0	2.4	226	4.2
16.9	2.5	267	4.3
20.0	2.6	324	4.4
23.7	2.7	383	4.5
28.0	2.8	453	4.6
34.0	2.9	536	4.7
40.2	3.0	634	5.0
47.5	3.1	768	5.1
56.2	3.2	909/OPEN	5.2

Table 2. R_{SEL2} Selection Table

R_{SEL2} (kΩ)	$V_{IN}MON$ (V)	I_{LIM} (mA)	R_{SEL2} (kΩ)	$V_{IN}MON$ (V)	I_{LIM} (mA)
Short	1.8	200	66.5	1.8	400
4.99	1.9	200	80.6	1.9	400
5.90	2.0	200	95.3	2.0	400
7.15	2.1	200	113	2.1	400
8.45	2.2	200	133	2.2	400
10.0	2.3	200	162	2.3	400
11.8	2.4	200	191	2.4	400
14.0	2.5	200	226	2.5	400
16.9	2.6	200	267	2.6	400
20.0	2.7	200	324	2.7	400
23.7	2.8	200	383	2.8	400
28.0	2.9	200	453	2.9	400
34.0	3.0	200	536	3.0	400
40.2	3.1	200	634	3.1	400
47.5	3.2	200	768	3.2	400
56.2	3.4	200	909/OPEN	3.4	400

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. *Figure 4* shows an example PCB layout.

When designing the PCB, use the following guidelines:

1) The input capacitor should be placed immediately next to the IN pin of the device. Since the device operates at a high switching frequency, this placement is critical for the effective decoupling of high-frequency noise from the IN pin.
2) Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and the inductor. Cutting this ground plane risks interrupting the switching current loops.
3) AGND must carefully connect to PGND. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
4) Keep the power traces and load connections short and wide. This practice is essential for high efficiency.

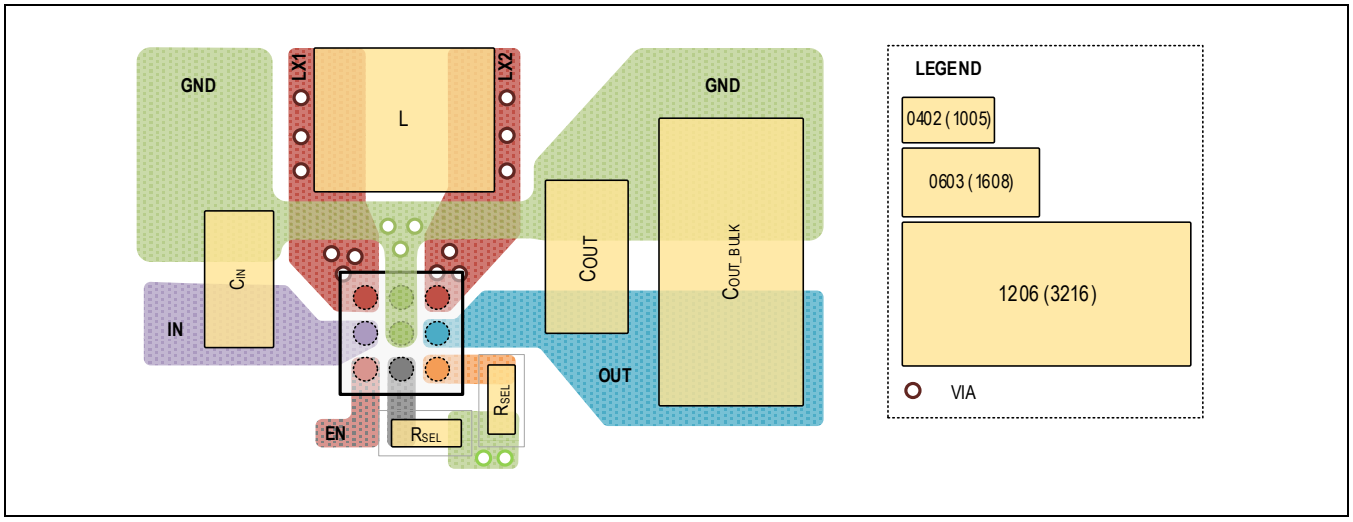
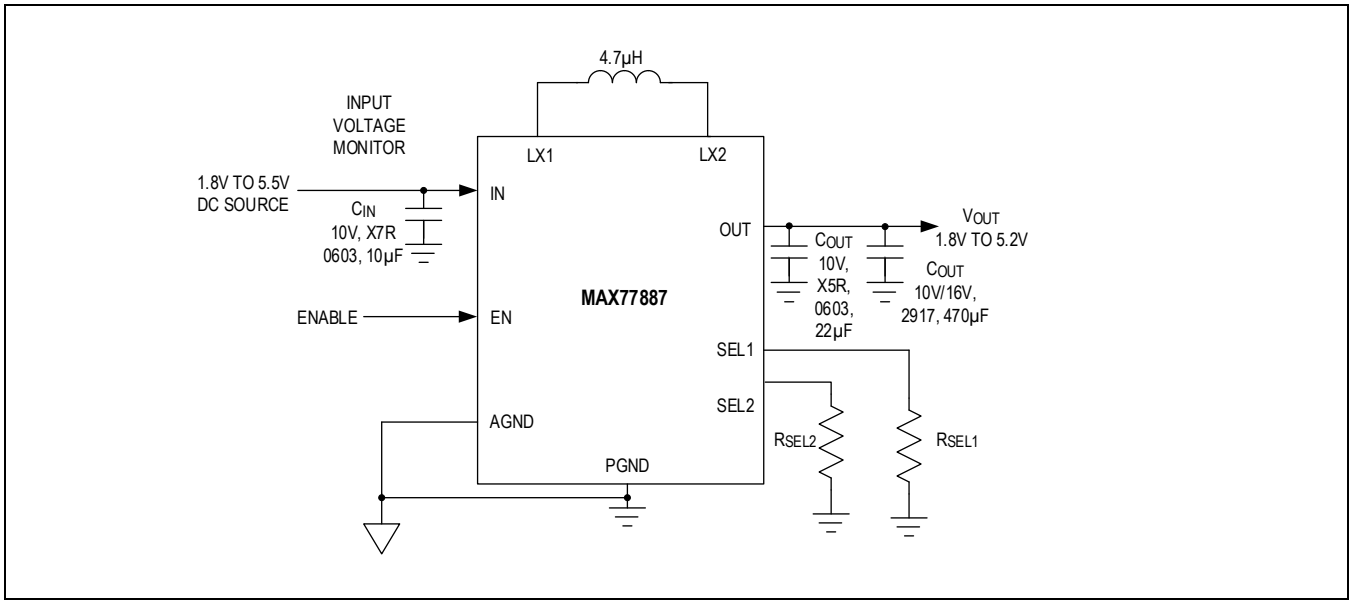


Figure 4. Example Layout

Typical Application Circuit



Ordering Information

PART NUMBER	PIN-PACKAGE
MAX77887AEWL+T	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/24	Release for Market Intro	—