19-3349; Rev 2; 4/05

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

General Description

The MAX8594/MAX8594A complete power-management chips for low-cost personal digital assistants (PDAs) operates from a 1-cell lithium-ion (Li+) or 3-cell NiMH battery. They include all regulators, outputs, and voltage monitors necessary for small portable devices while requiring a bare minimum of external components. Featured are three linear regulators, a boost DC-DC converter for LCD bias, an efficient 4MHz buck DC-DC converter for core power, a microprocessor (µP) reset output, and low-battery shutdown in a 0.8mm high thin QFN package.

The COR1 buck DC-DC converter supplies a pin-selectable output at 400mA. All linear regulators feature PMOS pass elements for efficient low-dropout operation. A MAIN LDO supplies 3.3V at 500mA. A secure-digital (SD) card slot output supplies 3.3V at 500mA, and a COR2 LDO supplies 1.8V at 50mA. Each output has its own logic-controlled enable. For other output voltage combinations, contact Maxim.

An LCD bias boost DC-DC converter features an on-board MOSFET and True Shutdown™ when off. This means that during shutdown, input power is disconnected from the inductor so the boost output falls to 0V rather than remaining one diode drop below the input voltage.

A µP reset output clears 20ms (typ) after the COR1 output achieves regulation to ensure an orderly start. In addition, the COR1 regulator is not started until the 3.3V main output is in regulation. Also included are a 1% accurate reference and low-battery monitor. Thermal shutdown protects the die from overheating.

The MAX8594/MAX8594A operate from a 3.1V to a 5.5V supply voltage and consume 46µA no-load supply current. They are packaged in a tiny, 4mm x 4mm, 24-pin thin QFN capable of dissipating 1.67W. The devices are specified for operation from -40°C to +85°C.

Applications

PDAs
Organizers
Cellular and Cordless Phones
MP3 Players
Handheld Devices

Ordering Information

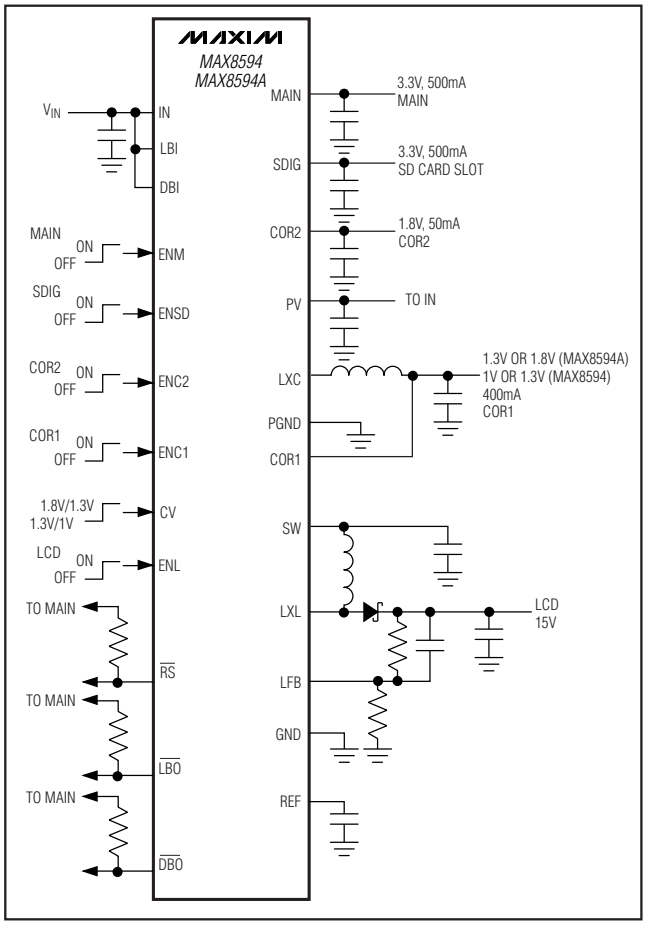
PART	TEMP RANGE	PIN-PACKAGE
MAX8594ETG	-40°C to +85°C	24 Thin QFN-EP* 4mm x 4mm (T2444-4)
MAX8594AETG	-40°C to +85°C	24 Thin QFN-EP* 4mm x 4mm (T2444-4)

*EP = Exposed pad.

Features

- ♦ Minimum External Components
- ♦ Efficient Step-Down DC-DC Powers CPU Core
- ♦ 1V/1.3V Selectable Core Voltage, 400mA (MAX8594)
- ♦ 1.3V/1.8V Selectable Core Voltage, 400mA (MAX8594A)
- ♦ Main LDO 3.3V, 500mA
- ♦ SD Card Output 3.3V, 500mA
- ♦ Second Core LDO 1.8V, 50mA
- ♦ High-Efficiency LCD Boost
- ♦ LCD 0V True Shutdown when Off
- ♦ 46µA Quiescent Current

Typical Operating Circuit



Pin Configuration appears at end of the data sheet.

True Shutdown is a trademark of Maxim Integrated Products, Inc.

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

ABSOLUTE MAXIMUM RATINGS

IN, PV, ENSD, ENC1, ENC2, ENL, $\overline{RS}$, SDIG, LBI, DBI to GND .....-0.3V to +6V
LXL to GND .....-0.3V to +30V
MAIN, COR1, COR2, REF, LFB, CV, ENM, $\overline{LBO}$, $\overline{DBO}$, LXC, SW to GND.....-0.3V to (V_{IN} + 0.3V)
PV to IN.....-0.3V to +0.3V
PGND to GND .....-0.3V to +0.3V
Current into LXL.....300mA_{RMS}
Current out of SW .....300mA_{RMS}
Current into LXC .....400mA_{RMS}
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin Thin QFN Package
(derate 20.8mW/°C above +70°C).....1.67W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = V_{CV} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, PV Voltage Range		3.1		5.5	V
V_{IN} Complete Shutdown Threshold	V_{DBI} = V_{IN}, V_{IN} falling	2.950	3.0	3.050	V
	V_{DBI} = V_{IN}, V_{IN} rising	3.135	3.3	3.525	
V_{DBI} Complete Shutdown Threshold	V_{DBI} falling	1.234	1.25	1.263	V
	V_{DBI} rising	1.306	1.375	1.478	
V_{LBI} $\overline{LBO}$ Threshold	V_{LBI} rising	1.234	1.25	1.263	V
	V_{LBI} falling	1.103	1.125	1.140	
V_{IN} $\overline{LBO}$ Threshold	V_{LBI} = V_{IN}, V_{IN} falling	3.262	3.33	3.366	V
	V_{LBI} = V_{IN}, V_{IN} rising	3.625	3.7	3.744	
DBI Input Dual Mode™ Threshold	Preset mode, V_{IN} = 2.9V	V_{IN} - 0.3			V
	ADJ mode, V_{IN} = 2.9V			V_{IN} - 1.2	
LBI Input Dual-Mode Threshold with Respect to IN	Preset mode, V_{IN} = 3.2V	V_{IN} - 0.3			V
	ADJ mode, V_{IN} = 3.2V			V_{IN} - 1.2	
DBI Complete Shutdown Input Program Range	V_{IN} falling	3.0		5.5	V
DBI Input Bias Current	V_{DBI} = 1.25V	-50		+50	nA
LBI Input Bias Current	V_{LBI} = 1.25V	-50		+50	nA
IN, PV Operating Current	Shutdown (DBI remains on, REF off), V_{IN} = V_{PV} = V_{DBI} = V_{LBI} = 2.7V		2	10	µA
	All off (REF on)		30	55	
	All on; LXL, LXC not switching		130	180	
IN Operating Current	Main on, no load		46	75	µA
	Main on, no load, COR1 on, LXC not switching		80	110	
	All on except LCD, V_{ENL} = 0V, LXL and LXC not switching		115	160	

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = V_{CV} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LDOs					
MAIN, SDIG Soft-Start Time		300	600	1200	µs
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.218	3.3	3.383	V
MAIN Current Limit		550	800	1200	mA
MAIN Dropout Voltage	I_{LOAD} = 1mA		1		mV
	I_{LOAD} = 300mA		210	330	
	I_{LOAD} = 500mA		350	595	
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.218	3.3	3.383	V
SDIG Current Limit		525	718	900	mA
SDIG Dropout Voltage	I_{LOAD} = 1mA		0.75		mV
	I_{LOAD} = 200mA		170	300	
	I_{LOAD} = 500mA		525	1010	
SDIG Reverse Leakage Current	V_{SDIG} = 5.5V, V_{ENSD} = V_{IN} = 0V		7	15	µA
COR2 Output Voltage	I_{LOAD} = 100µA to 50mA, V_{IN} = 3.6V to 5.5V	1.755	1.8	1.845	V
COR2 Current Limit		65	98	150	mA
COR1 PWM BUCK					
COR1 Output Voltage Accuracy	CV = high (MAX8594A)	1.743	1.8	1.855	V
	CV = high (MAX8594) or CV = low (MAX8594A)	1.259	1.3	1.340	
	CV = low (MAX8594)	0.972	1	1.023	
p-Channel On-Resistance	I_{LXC} = -180mA		0.70	1.34	Ω
	I_{LXC} = -180mA, V_{PV} = 3.1V		0.8	1.58	
n-Channel On-Resistance	I_{LXC} = 180mA		0.25	0.46	Ω
	I_{LXC} = 180mA, V_{PV} = 3.1V		0.30	0.53	
p-Channel Current-Limit Threshold		-0.500	-0.75	-0.925	A
n-Channel Current-Limit Threshold		-0.50	-0.72	-0.92	A
Minimum On- and Off-Times	$t_{ON(MIN)}$		0.1		µs
	$t_{OFF(MIN)}$		0.1		
LXC Leakage Current	V_{LXC} = 0V, V_{ENC1} = 0V	-10	+0.1	+10	µA
REF AND RESET OUTPUT					
REF Voltage Accuracy	I_{REF} = 0.1µA	1.236	1.25	1.264	V
REF Line Regulation	3.1V < V_{IN} < 5.5V, I_{REF} = 0.1µA		0.1	3	mV
REF Load Regulation	0.1µA < I_{REF} < 10µA		1	3	mV
$\overline{RS}$ Deassert Threshold for COR1 Rising (Note 1)	CV = low (MAX8594A), CV = low or CV = high (MAX8594)	88.00	90	93.25	%
	CV = high (MAX8594A)	67.0	69	72.7	

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = V_{CV} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RS}$ Assert Threshold	CV = low or CV = high (MAX8594), CV = low (MAX8594A)		80		%
	CV = high (MAX8594A)		62.5		
$\overline{RS}$ Deassert Delay		10	20	30	ms
$\overline{RS}$ Assert Delay	50mV overdrive		5		µs
LCD					
LXL Voltage Range				28	V
LXL Current Limit	L1 = 10µH	195	235	275	mA
LXL On-Resistance			1.7		Ω
LXL Leakage Current	V_{LXL} = 28V		0.2	2	µA
Maximum LXL On-Time		2	3	4	µs
Minimum LXL Off-Time	V_{LFB} > 1.1V	0.8	1	1.2	µs
	V_{LFB} < 0.8V (soft-start)	3.9	5	6.0	
LFB Feedback Threshold		1.229	1.25	1.270	V
LFB Input Bias Current	V_{LFB} = 1.3V		5	50	nA
SW Off-Leakage Current	V_{SW} = 0V, V_{PV} = 5.5V, V_{ENL} = 0V		0.01	1	µA
SW PMOS On-Resistance			1	1.5	Ω
SW PMOS Peak Current Limit			700		mA
SW PMOS Average Current Limit			300		mA
Soft-Start Time	C_{SW} = 1µF		0.13		ms
LOGIC					
EN_, CV Input Low Level	V_{IN} = 3.1V to 5.5V			0.35	V
EN_, CV Input High Level	V_{IN} = 3.1V to 5.5V	1.4			V
EN_, CV Input Leakage Current			0.01	1	µA
$\overline{RS}$, $\overline{LBO}$, $\overline{DBO}$ Output Low Level	Sinking 1mA, V_{IN} = 2.5V		0.02	0.1	V
$\overline{DBO}$ Output Low Level	Sinking 100µA, V_{IN} = 1.0V		0.02	0.1	V
$\overline{RS}$, $\overline{LBO}$, $\overline{DBO}$ Output High Leakage	V_{OUT} = 5.5V, V_{IN} = 5.5V			1	µA
THERMAL PROTECTION					
Thermal-Shutdown Temperature	Rising temperature		+160		°C
Thermal-Shutdown Hysteresis			15		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, PV Voltage Range		3.1		5.5	V
V_{IN} Complete Shutdown Threshold	V_{DBI} = V_{IN}, V_{IN} falling	2.93		3.06	V
	V_{DBI} = V_{IN}, V_{IN} rising	3.135		3.525	
V_{DBI} Complete Shutdown Threshold	V_{DBI} falling	1.228		1.264	V
	V_{DBI} rising	1.306		1.478	
V_{LBI} $\overline{LBO}$ Threshold	V_{LBI} rising	1.228		1.264	V
	V_{LBI} falling	1.103		1.140	
V_{IN} $\overline{LBO}$ Threshold	V_{LBI} = V_{IN}, V_{IN} falling	3.248		3.366	V
	V_{LBI} = V_{IN}, V_{IN} rising	3.609		3.744	
DBI Input Dual-Mode Threshold	Preset mode, V_{IN} = 2.9V	V_{IN} - 0.3			V
	ADJ mode, V_{IN} = 2.9V			V_{IN} - 1.25	
LBI Input Dual-Mode Threshold with Respect to IN	Preset mode, V_{IN} = 3.2V	V_{IN} - 0.3			V
	ADJ mode, V_{IN} = 3.2V			V_{IN} - 1.25	
DBI Complete Shutdown Input Program Range	V_{IN} falling	3.0		5.5	V
DBI Input Bias Current	V_{DBI} = 1.25V	-50		+50	nA
LBI Input Bias Current	V_{LBI} = 1.25V	-50		+50	nA
IN, PV Operating Current	Shutdown (DBI remains on, REF off), V_{IN} = V_{PV} = V_{DBI} = V_{LBI} = 2.7V			10	µA
	All off (REF on)			55	
	All on, LXL, LXC not switching			180	
IN Operating Current	Main on, no load			75	µA
	Main on, no load, COR1 on, LXC not switching			110	
	All on except LCD, V_{ENL} = 0V, LXL and LXC not switching			160	
LDOs					
MAIN, SDIG Soft-Start Time	Ramp ILIM from 0% to 100%	300		1200	µs
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.209		3.383	V
MAIN Current Limit		550		1230	mA
MAIN Dropout Voltage	I_{LOAD} = 300mA			330	mV
	I_{LOAD} = 500mA			595	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.218		3.383	V
SDIG Current Limit		485		900	mA
SDIG Dropout Voltage	I_{LOAD} = 200mA			300	mV
	I_{LOAD} = 500mA			1250	
SDIG Reverse Leakage Current	V_{SDIG} = 5.5V, V_{ENSD} = V_{IN} = 0V			15	µA
COR2 Output Voltage	I_{LOAD} = 100µA to 50mA, V_{IN} = 3.6V to 5.5V	1.750		1.845	V
COR2 Current Limit		60		150	mA
COR1 PWM BUCK					
COR1 Output Voltage Accuracy	CV = high (MAX8594A)	1.743		1.855	V
	CV = high (MAX8594) or CV = low (MAX8594A)	1.255		1.340	
	CV = low (MAX8594)	0.969		1.023	
p-Channel On-Resistance	I_{LXC} = -180mA			1.34	Ω
	I_{LXC} = -180mA, V_{PV} = 3.1V			1.58	
n-Channel On-Resistance	I_{LXC} = 180mA			0.46	Ω
	I_{LXC} = 180mA, V_{PV} = 3.1V			0.53	
p-Channel Current-Limit Threshold		-0.460		-0.925	A
n-Channel Current-Limit Threshold		-0.46		-0.92	A
LXC Leakage Current	V_{PV} = 5.5V, V_{LXC} = 0V or V_{PV}, V_{ENC1} = 0V	-10		+10	µA
REF AND RESET OUTPUT					
REF Voltage Accuracy	I_{REF} = 0.1µA	1.229		1.264	V
REF Line Regulation	3.1V < V < 5.5V, I_{REF} = 0.1µA			3	mV
REF Load Regulation	0.1µA < I_{REF} < 10µA			3	mV
$\overline{RS}$ Deassert Threshold for COR1 Rising (Note 1)	CV = low or CV = high (MAX8594), CV = low (MAX8594A)	88.00		93.25	%
	CV = high (MAX8594A)	67.0		72.7	
$\overline{RS}$ Deassert Delay		10		30	ms
LCD					
LXL Voltage Range				28	V
LXL Current Limit	L1 = 10µH	180		280	mA
LXL Leakage Current	V_{LXL} = 28V			2	µA
Maximum LXL On-Time		2		4	µs
Minimum LXL Off-Time	V_{LFB} > 1.1V	0.8		1.2	µs
	V_{LFB} < 0.8V (soft-start)	3.9		6.0	
LFB Feedback Threshold		1.223		1.270	V
LFB Input Bias Current	V_{LFB} = 1.3V			50	nA
SW Off-Leakage Current	V_{SW} = 0V, V_{PV} = 5.5V, V_{ENL} = 0V			1	µA
SW PMOS On-Resistance				1.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PV} = V_{ENSD} = V_{ENC2} = V_{ENL} = V_{ENM} = V_{ENC1} = V_{DBI} = V_{LBI} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC					
EN_, CV Input Low Level	V_{IN} = 3.1V to 5.5V			0.35	V
EN_, CV Input High Level	V_{IN} = 3.1V to 5.5V	1.4			V
EN_, CV Input Leakage Current				1	µA
$\overline{RS}$, $\overline{LBO}$, $\overline{DBO}$ Output Low Level	Sinking 1mA, V_{IN} = 2.5V			0.1	V
$\overline{DBO}$ Output Low Level	Sinking 100µA, V_{IN} = 1.0V			0.1	V
$\overline{RS}$, $\overline{LBO}$, $\overline{DBO}$ Output High Leakage	V_{OUT} = 5.5V, V_{IN} = 5.5V			1	µA

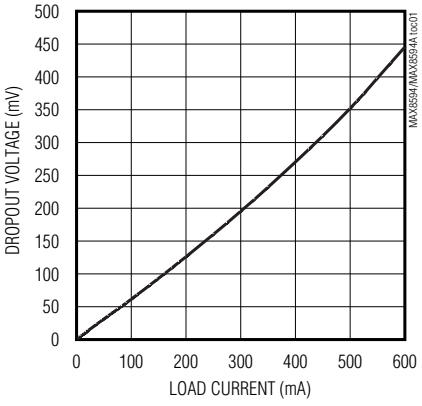
Note 1: The reset trip point tracks the COR1 voltage. For example, a minimum reset spec does not occur with a maximum COR1 spec, and a minimum COR1 spec does not occur with a maximum reset spec.

Note 2: Specifications to -40°C are guaranteed by design, not production tested.

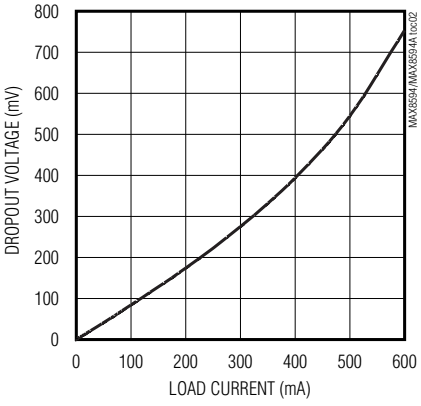
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 4V, T_A = +25°C, unless otherwise noted.)

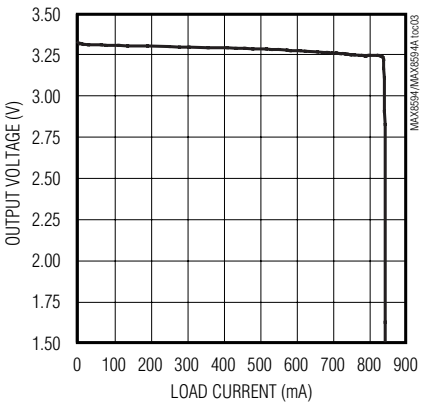
MAIN DROPOUT VOLTAGE vs. LOAD CURRENT



SDIG DROPOUT VOLTAGE vs. LOAD CURRENT



MAIN OUTPUT VOLTAGE vs. LOAD CURRENT

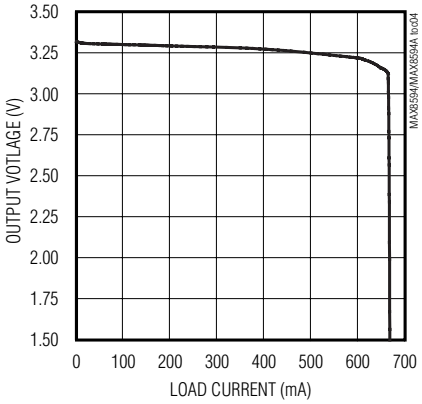


5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

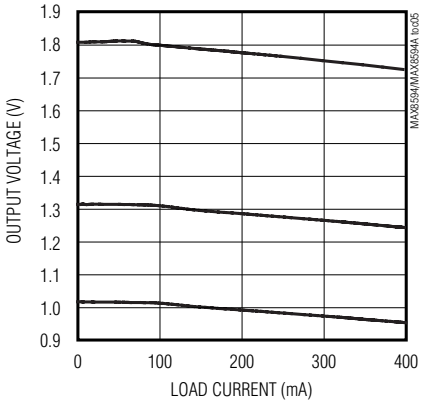
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 4V, T_A = +25°C, unless otherwise noted.)

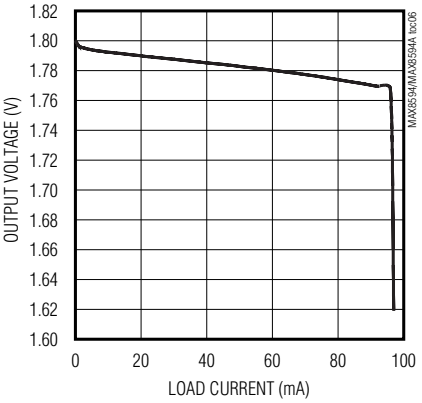
SDIG OUTPUT VOLTAGE vs. LOAD CURRENT



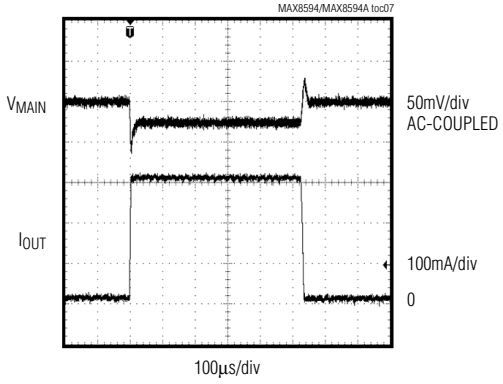
COR1 OUTPUT VOLTAGE vs. LOAD CURRENT



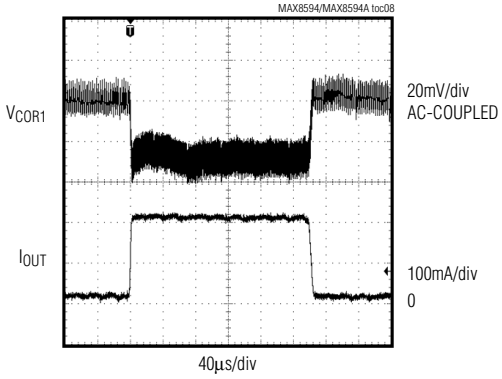
COR2 OUTPUT VOLTAGE vs. LOAD CURRENT



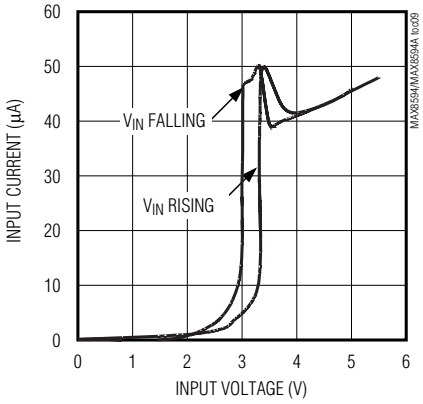
LOAD-TRANSIENT MAIN



LOAD-TRANSIENT COR1



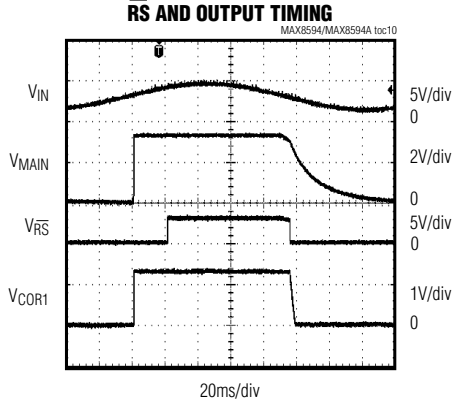
INPUT CURRENT vs. INPUT VOLTAGE



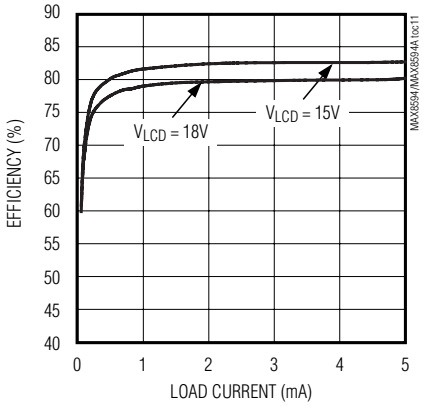
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 4V, T_A = +25°C, unless otherwise noted.)

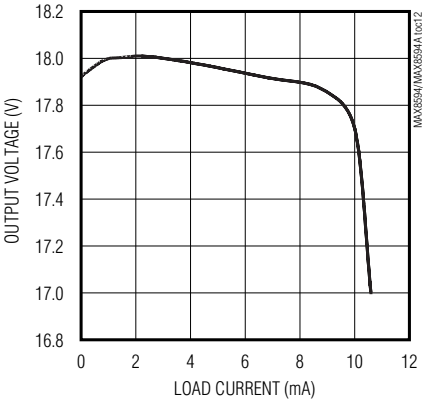
$\overline{RS}$ AND OUTPUT TIMING



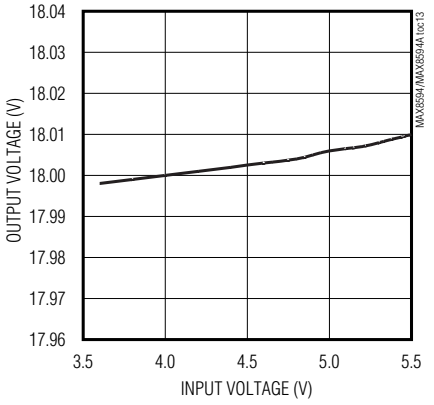
LCD EFFICIENCY vs. LOAD CURRENT



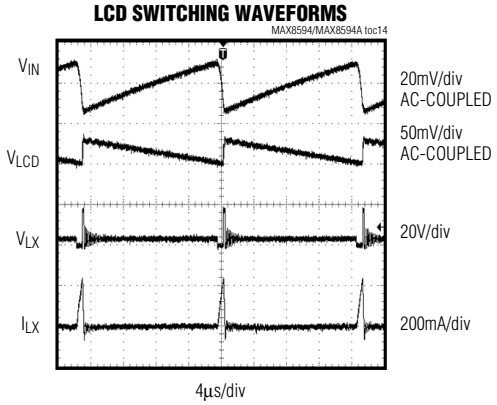
LCD OUTPUT VOLTAGE vs. LOAD CURRENT



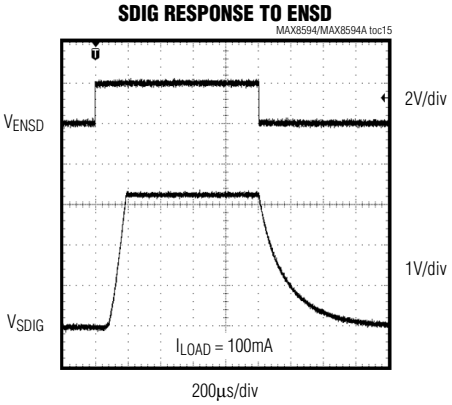
LCD OUTPUT VOLTAGE vs. INPUT VOLTAGE



LCD SWITCHING WAVEFORMS



SDIG RESPONSE TO ENSD

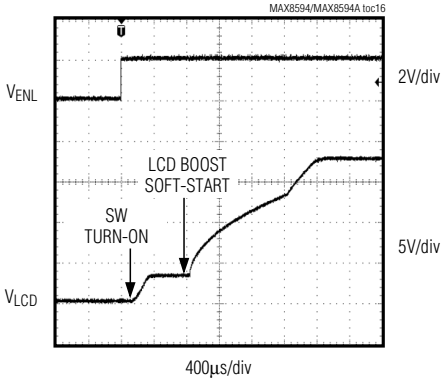


5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

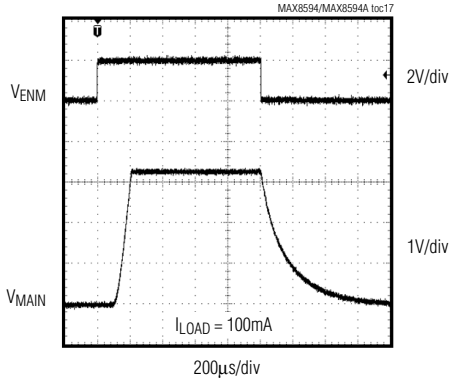
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 4V, T_A = +25°C, unless otherwise noted.)

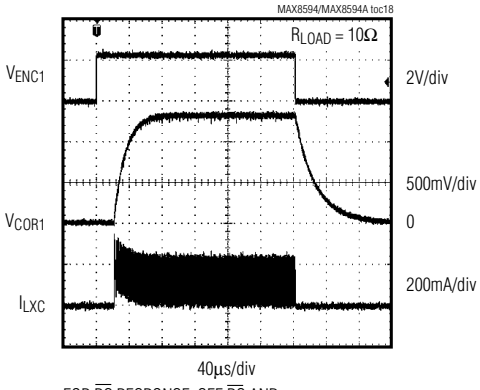
LCD RESPONSE TO ENL



MAIN RESPONSE TO ENM

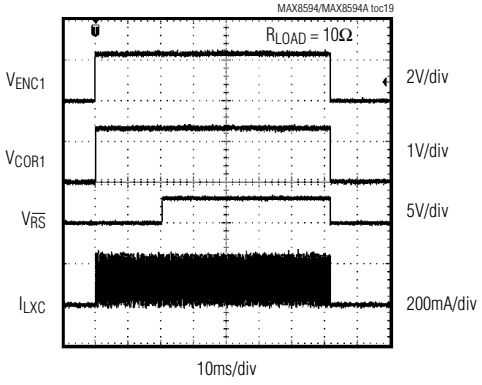


COR1 RESPONSE TO ENC1

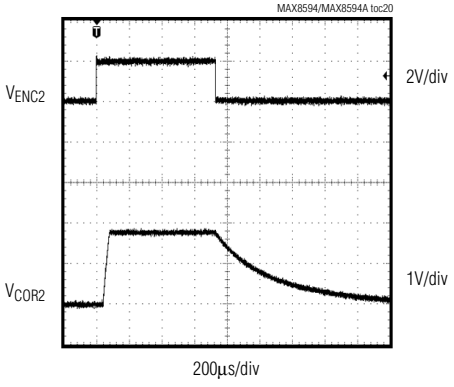


FOR $\overline{RS}$ RESPONSE, SEE $\overline{RS}$ AND COR1 RESPONSE TO ENC1

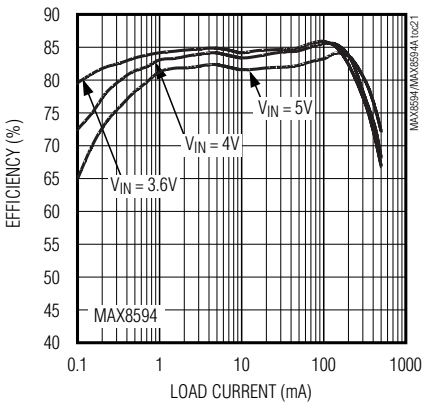
$\overline{RS}$ AND COR1 RESPONSE TO ENC1



COR2 RESPONSE TO ENC2



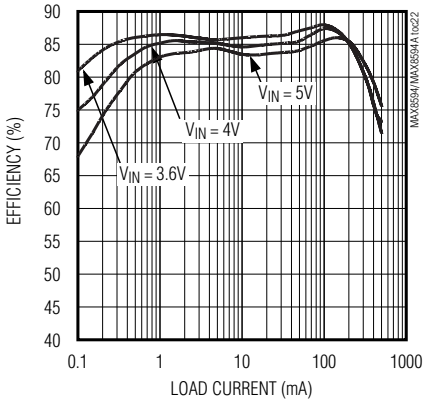
COR1 EFFICIENCY vs. LOAD CURRENT WITH 1V OUTPUT



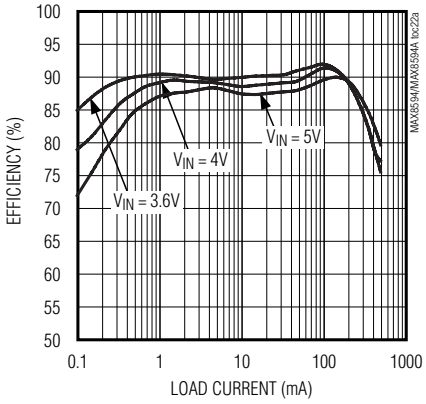
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 4V, T_A = +25°C, unless otherwise noted.)

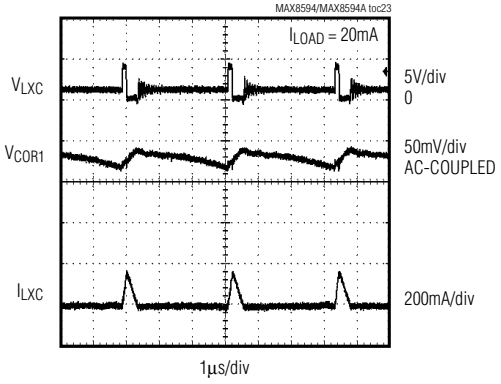
COR1 EFFICIENCY vs. LOAD CURRENT WITH 1.3V OUTPUT



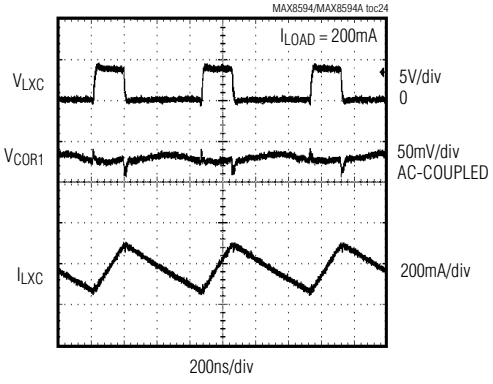
COR1 EFFICIENCY vs. LOAD CURRENT WITH 1.8V OUTPUT



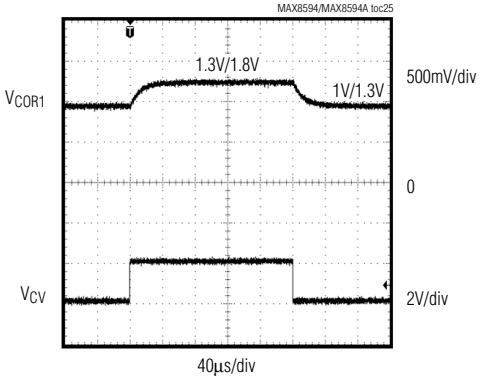
LIGHT-LOAD SWITCHING COR1



HEAVY-LOAD SWITCHING COR1



COR1 RESPONSE TO CV



5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

Pin Description

PIN	NAME	FUNCTION
1	SDIG	3.3V, 500mA LDO Output for Secure-Digital Card Slot. SDIG has reverse current protection so SDIG can be biased when no power is present at IN. SDIG output turns off when V_{IN} is below the DBI threshold, ENSD goes low, or MAIN is out of regulation. When SDIG turns off, the output is discharged at a rate depending on the load and the internal feedback resistors (typically 1.3MΩ).
2	IN	Input Voltage to the MAX8594/MAX8594A. Bypass IN to GND with a 1µF ceramic capacitor.
3	$\overline{RS}$	Reset Output. $\overline{RS}$ is an active-low, open-drain output that goes high impedance 20ms (typ) after COR1 is in regulation. COR1 does not turn on until MAIN is in regulation. If MAIN falls out of regulation, COR1 turns off and $\overline{RS}$ goes low. If MAIN is still in regulation, then $\overline{RS}$ goes low when V_{IN} is below the DBI threshold. $\overline{RS}$ goes low when ENC1 is low.
4	$\overline{LBO}$	Low-Battery Detector Open-Drain Output. $\overline{LBO}$ is an active-low, open-drain output that goes high impedance when V_{IN} is greater than both the DBI and LBI thresholds. $\overline{LBO}$ goes low when V_{IN} falls below the LBI threshold.
5	$\overline{DBO}$	Dead-Battery Detector Open-Drain Output. When V_{IN} is below the DBI threshold, both $\overline{DBO}$ and $\overline{LBO}$ go low, all outputs shut down, and the MAX8594/MAX8594A enter the lowest possible quiescent-current state. Once this occurs, MAIN does not turn back on until both V_{IN} exceeds the DBI threshold and ENM = high. $\overline{DBO}$ is an active-low, open-drain output that goes high impedance when V_{IN} exceeds the DBI threshold.
6	DBI	Dead-Battery Detector. DBI remains active at all times. If DBI = IN, the DBI threshold is 3.0V when IN is falling and 3.3V when rising. The DBI threshold can also be adjusted to other values by connecting DBI to a resistor voltage-divider. Also see the $\overline{DBO}$ description.
7	LBI	Low-Battery Detector. If LBI = IN, the LBI threshold is 3.33V when IN is falling and 3.7V when rising. The LBI threshold can also be adjusted to other values by connecting LBI to a resistor voltage-divider. Also see the $\overline{LBO}$ description.
8	CV	Selects 1V or 1.3V COR1 Output Voltage for MAX8594, and 1.3V or 1.8V COR1 for MAX8594A. Drive CV high or connect to IN for a 1.3V COR1 output (1.8V COR1 for MAX8594A). Drive CV low or connect to GND for a 1V COR1 output (1.3V COR1 for MAX8594A).
9	ENM	Enable Input for MAIN. No other outputs turn on until MAIN is in regulation. If MAIN is pulled out of regulation, all other outputs turn off and $\overline{RS}$ goes low. MAIN cannot be activated when V_{IN} is below the DBI threshold.
10	GND	Ground
11	REF	1.25V 1% Reference. Bypass REF with a 0.1µF capacitor to GND. REF is enabled when V_{IN} is greater than the DBI threshold. REF is off when V_{IN} is below the DBI threshold.
12	LFB	LCD Feedback Input. Connect LFB to a resistor-divider network between the LCD output and GND. The feedback threshold is 1.25V. LCD turns off when V_{IN} is below the DBI threshold, when ENL goes low, or when MAIN is out of regulation. When off, the LCD output is discharged at a rate depending on the load and the external feedback resistors (typically 2.4MΩ).
13	ENL	Enable Input for LCD (Boost Regulator). Drive ENL high to activate the LCD boost. Drive ENL low to shut down the LCD output. The LCD converter cannot be activated when V_{IN} is below the DBI threshold or before MAIN is in regulation.
14	LXL	LCD Boost Switch. Connect LXL to a boost inductor and Schottky diode. See Figure 1.

Pin Description (continued)

PIN	NAME	FUNCTION
15	SW	LCD True-Shutdown Switch Output. SW is the power source for the LCD boost inductor. SW turns on when ENL is high. For best efficiency, bypass SW with a 4.7µF capacitor to GND. SW is disconnected from PV when LCD is shut down.
16	PV	Power Input for COR1 Buck Converter and LCD True-Shutdown Switch. Connect IN to PV.
17	PGND	Power Ground
18	LXC	COR1 Switching Node. Connect LXC to the COR1 inductor. See Figure 1.
19	ENC1	Enable Input for Primary Core Buck Converter (COR1). Drive ENC1 high to turn on COR1 and low to turn off. COR1 cannot be activated if V_{IN} is below the DBI threshold or before MAIN is in regulation.
20	ENSD	Enable Input for Secure Digital Card (SDIG). Drive ENSD low to turn off SDIG and high to turn on. SDIG cannot be activated when V_{IN} is below the DBI threshold or before MAIN is in regulation.
21	COR1	Feedback Sense Input for COR1 Output. COR1 turns off when V_{IN} is below the DBI threshold, when ENC1 goes low, or when MAIN is out of regulation. When off, the output is discharged by LXC through an internal 1MΩ (typ) resistor.
22	ENC2	Enable Input for Secondary Core LDO (COR2). Drive ENC2 high to turn on COR2 and low to turn off. COR2 cannot be activated when V_{IN} is below the DBI threshold or before MAIN is in regulation. COR2 can be activated when V_{IN} is greater than the DBI threshold and MAIN is in regulation.
23	COR2	1.8V, 50mA LDO Output for Secondary Core. COR2 turns off when V_{IN} is below the DBI threshold, when ENC2 goes low, or when MAIN is out of regulation. The COR2 output is discharged at a rate depending on the load and the internal feedback resistors (typically 700kΩ).
24	MAIN	3.3V, 500mA LDO Output for Main Supply. MAIN output turns off when V_{IN} is below the DBI threshold or when ENM goes low. When off, the output is discharged at a rate depending on the load and the internal feedback resistors (1.3MΩ typ).
—	EP	Exposed Pad. Connect to ground for enhanced power dissipation.

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

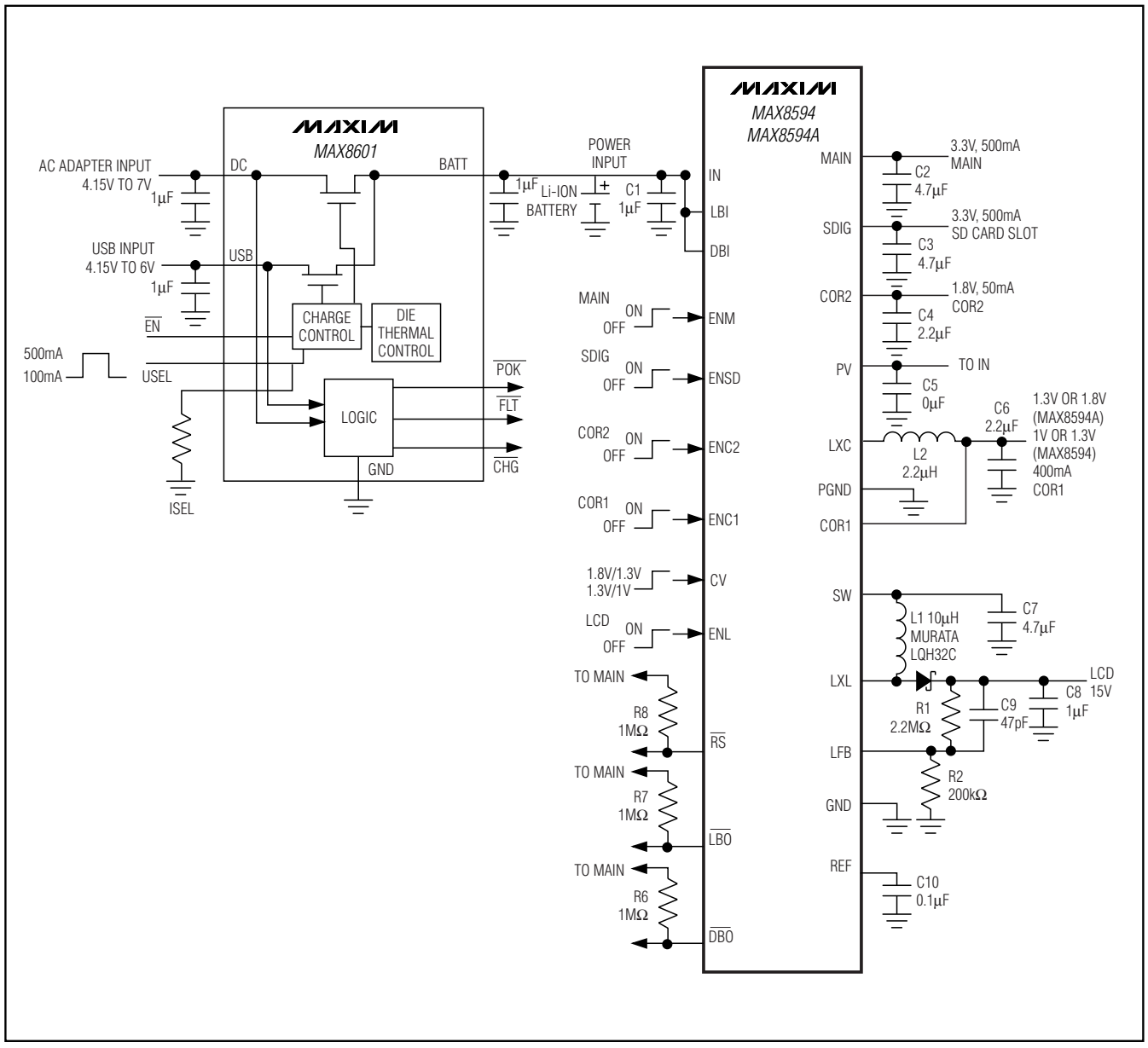


Figure 1. Typical Application Circuit with Charger

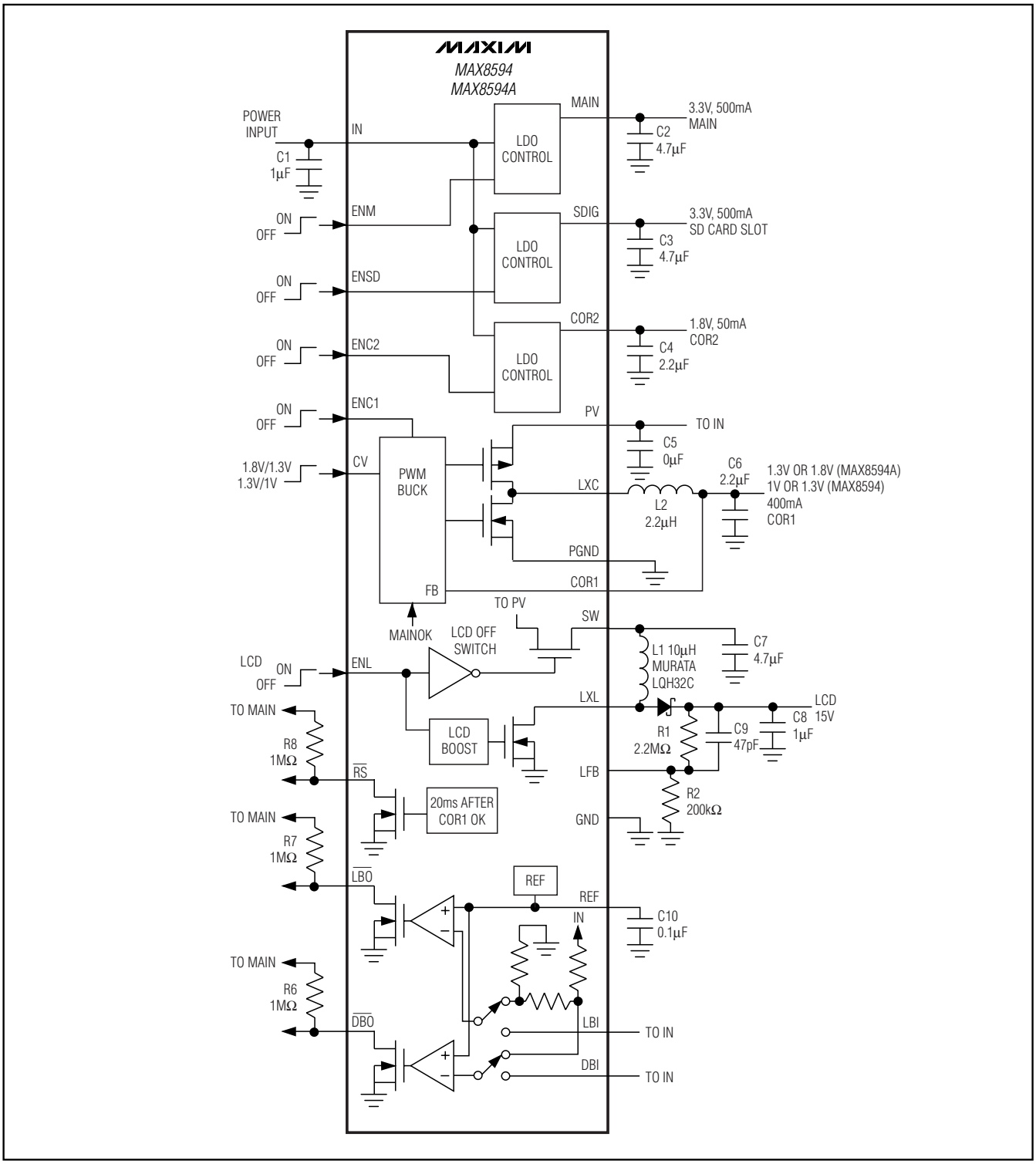


Figure 2. Block Diagram

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

Detailed Description

COR1 Step-Down DC-DC Converter

The COR1 regulator is a proprietary hysteretic PWM control step-down converter that supplies up to 400mA. The output voltage is set to either 1V or 1.3V by CV for the MAX8594 and 1.3V or 1.8V for the MAX8594A.

Under moderate to heavy loading, COR1 operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. With light loads (<30mA), COR1 operates in an efficiency-enhanced Idle Mode™ during which the converter switches only as needed to service the load.

Linear Regulators

Power for main logic, a SD card slot, and CODEC are provided by three LDOs:

- MAIN—Provides 3.3V at a guaranteed 500mA with a typical current limit of 800mA.
- SDIG—Provides 3.3V at a guaranteed 500mA for SD cards with a typical current limit of 718mA.
- COR2—Provides 1.8V at a guaranteed 50mA for a CODEC core with a typical current limit of 98mA.

Note that it may not be possible to draw the full rated current of MAIN and SDIG at all operating input voltages due to the dropout limitations of those regulators. The typical dropout resistance of the MAIN regulator is 0.7Ω (350mV drop at 500mA), and the typical dropout resistance of the SDIG regulator is 0.85Ω (525mV drop at 500mA).

All voltage outputs have separate enable inputs (ENM, ENL, ENSD, ENC1, and ENC2); however, no other output turns on until MAIN is in regulation. MAIN cannot be activated until V_{IN} exceeds the DBI threshold. When SDIG is turned off, reverse current is blocked so the SDIG output can be biased with an external source when no power is present at IN. Leakage current is typically 3µA with 3.3V at SDIG.

LCD DC-DC Boost

The MAX8594/MAX8594A include a low-current, high-voltage boost DC-DC converter for LCD bias. This circuit can output up to 28V and is adjustable with either an analog or PWM control signal using external components.

SW provides an input-power disconnect for the LCD when ENL is low (off). The input-power disconnect function is ideal for applications that require the output voltage to fall to 0V in shutdown (True Shutdown). If True Shutdown is not required, the SW switch can be bypassed by connecting the boost inductor directly to PV and removing the bypass cap on SW (C7 in Figure 1).

System Sleep

All regulated outputs turn off when V_{DBI} < 1.25V (or V_{IN} = 3.0V if DBI = IN, Figure 1). The MAX8594/MAX8594A resume normal operation when V_{DBI} >1.375V (or V_{IN} = 3.3V if DBI = IN, Figure 1).

Reset Output ($\overline{RS}$)

Reset $\overline{RS}$ asserts when COR1 falls 20% below its set level (38% for 1.8V setting in the MAX8594A). $\overline{RS}$ is an open-drain, active-low output. Connect a pullup resistor from $\overline{RS}$ to the logic supply of the gate receiving the reset signal. $\overline{RS}$ deasserts a minimum of 10ms after the COR1 output is in regulation. Upon application of valid input power, the MAIN output activates first (if ENM = high) followed by other outputs (if EN_ = high). Power and output sequencing are shown in Figure 3.

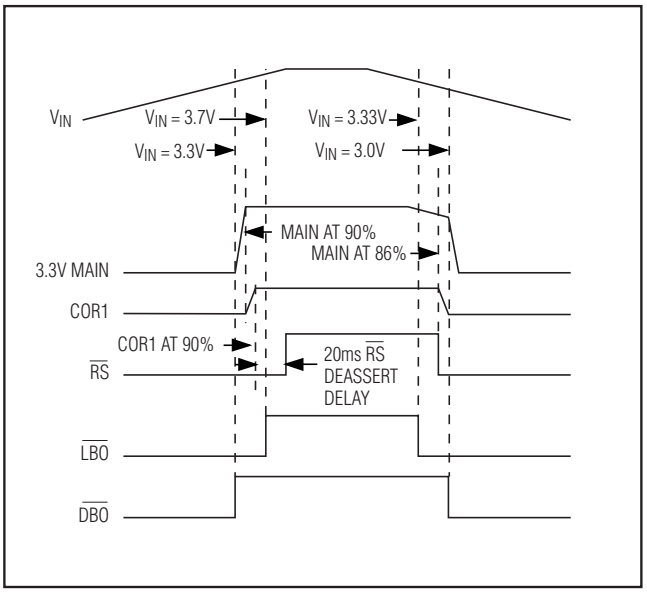


Figure 3. Power Sequence for Rising and Falling Input Voltage. Note that V_{IN} thresholds are for LBI and DBI connected to V_{IN}. Other thresholds can be set with resistors.

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Power Sequencing

As V_{IN} increases from 0V, sequencing is as follows:

1) The DBI comparator is always on. $\overline{DBO}$, $\overline{LBO}$, and $\overline{RS}$ are pulled low at approximately V_{IN} = 0.7V. MAIN, SDIG, COR1, COR2, and LCD are off.
2) When V_{IN} rises above the DBI threshold (3.3V if DBI = IN), $\overline{DBO}$ goes high impedance immediately and the part turns on. The MAIN LDO turns on if ENM = HIGH.
3) When the MAIN output reaches 90% of its nominal voltage, or 2.97V, all other regulators turn on if they are enabled.
4) $\overline{RS}$ goes high impedance 20ms after COR1 reaches 90% of its nominal voltage (69% when 1.8V setting in the MAX8594A is used).
5) When V_{IN} rises above the LBI threshold (3.7V if LBI = IN), $\overline{LBO}$ goes high impedance.

As IN decreases, sequencing is as follows:

1) When V_{IN} falls to the LBO threshold (3.33V if LBI = IN), $\overline{LBO}$ is pulled to GND.
2) If V_{IN} falls to the DBI threshold (3.0V if LBI = IN) before the MAIN output falls to 2.838V, $\overline{DBO}$ and $\overline{RS}$ go low, all regulators turn off, and the part is shut down.
3) If the MAIN output falls below 86% of its nominal voltage (2.838V) before IN reaches the DBI threshold (3.0V if DBI = IN), $\overline{RS}$ is pulled to GND and all other outputs turn off, but MAIN remains on (in dropout) and $\overline{DBO}$ remains high until IN falls to the DBI threshold.

Applications Information

COR1 Buck Output

COR1 Inductor

A 2.2µH inductor with a saturation current of at least 500mA is recommended. For lower load currents, the inductor current rating may be reduced. For maximum efficiency, the inductor's DC resistance should be as low as possible. Note that core materials differ among manufacturers and inductor types, resulting in variations in efficiency.

COR1 Capacitors

Ceramic input and output capacitors are recommended. For best stability over a wide temperature range, use capacitors with an X5R or X7R dielectric due to their low ESR and low temperature coefficient.

The COR1 output capacitor C6 (Figure 1) is required to keep the output voltage ripple small; 2.2µF is recommended for most applications.

Due to the pulsating nature of input current in a buck converter, a low-ESR input capacitor is required for input voltage filtering and to minimize interference with other circuits. The impedance of the input capacitor, C5 (Figure 1), should be kept very low at the switching frequency. A minimum value of 4.7µF is recommended at PV for most applications. The input capacitor can be increased to further improve input filtering.

LDO Output Capacitors (MAIN, SDIG, COR2)

Capacitors are required at each LDO output of the MAX8594/MAX8594A for stable operation over the full load and temperature range. See Figure 1 for recommended capacitor values for each output. To reduce noise and improve load-transient response, larger output capacitors up to 10µF can be used. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. X7R and X5R dielectrics are recommended. Note that some ceramic dielectrics, such as Z5U and Y5V, exhibit large capacitance and ESR variation with temperature and require larger than the recommended values to maintain stability overtemperature.

Setting LBI and DBI

The DBI and LBI inputs monitor input voltage (usually a battery) and trigger the $\overline{DBO}$ and $\overline{LBO}$ outputs. With LBI and DBI connected to IN, the LBI and DBI thresholds are internally set. For a rising input voltage, $\overline{DBO}$ goes high when V_{IN} exceeds 3.3V and $\overline{LBO}$ goes high when V_{IN} exceeds 3.7V. For a falling input voltage, $\overline{LBO}$ goes low when V_{IN} falls below 3.3V and $\overline{DBO}$ goes low when V_{IN} falls below 3.0V (see also the *Electrical Characteristics* table and Figure 3). Alternatively, the LBI and DBI thresholds can be set with external resistors as shown in Figures 4 and 5.

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

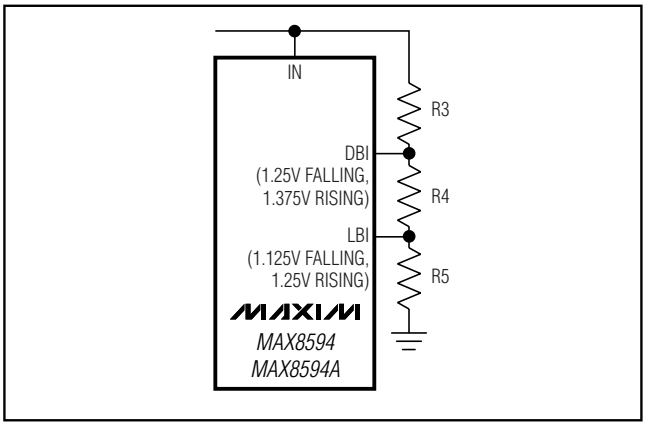


Figure 4. Setting the DBI and LBI Threshold with Three External Resistors

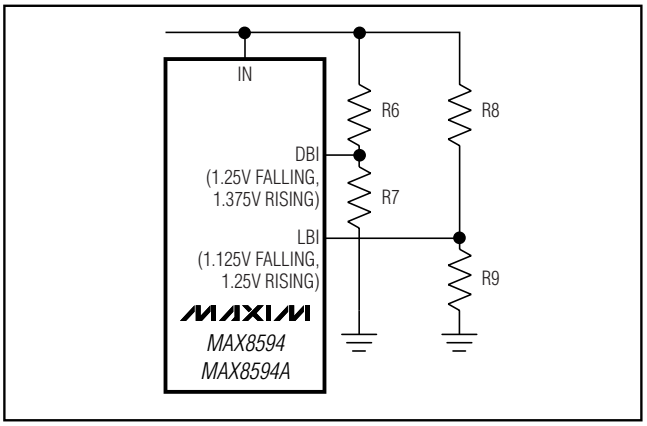


Figure 5. Setting the DBI and LBI Thresholds with Four Resistors

In Figure 4, one three-resistor-divider can set both DBI and LBI according to the following equations (shown for setting falling thresholds). Choose the lower resistor of the divider chain (R5 in Figure 4) to be between 100kΩ and 250kΩ. The equations for the two upper resistor-dividers as a function of each (falling) threshold are:

$$R3 = R5 \times \frac{V_{LBFALL}}{1.125} \times \left(1 - \frac{1.25}{V_{DBFALL}}\right)$$

$$R4 = R5 \times \frac{1.25 \times V_{LBFALL}}{1.125 \times V_{DBFALL}} - 1$$

where V_{DBFALL} and V_{LBFALL} are the desired falling thresholds to trigger the $\overline{DBO}$ and $\overline{LBO}$ outputs, respectively. Once those thresholds are selected, the rising DBI and LBI thresholds are:

$$V_{DBRISE} = 1.375 \times \frac{R3 + R4 + R5}{R4 + R5}$$

$$V_{LBRISE} = 1.25 \times \frac{R3 + R4 + R5}{R5}$$

Alternately, LBI and DBI can be set with separate resistor-dividers. The resistor calculation is simpler and the two settings do not interact, but one more resistor is needed and battery drain is slightly higher due to the extra resistor load. Choose the lower resistor of each divider chain (R7 and R9 in Figure 5) to be between 100kΩ and 250kΩ. The equations for upper resistor-dividers as a function of each (falling) threshold are:

$$R6 = R7 \times \left(\frac{V_{DBFALL}}{1.25} - 1\right)$$

$$R8 = R9 \times \left(\frac{V_{LBFALL}}{1.125} - 1\right)$$

where V_{DBFALL} and V_{LBFALL} are the desired falling thresholds to trigger the $\overline{DBO}$ and $\overline{LBO}$ outputs, respectively. Once those thresholds are selected, the rising DBI and LBI thresholds are:

$$V_{DBRISE} = 1.375 \times \frac{R6 + R7}{R7}$$

$$V_{LBRISE} = 1.25 \times \frac{R8 + R9}{R9}$$

Note that the low-battery threshold should not be set below the dead-battery threshold because both $\overline{DBO}$

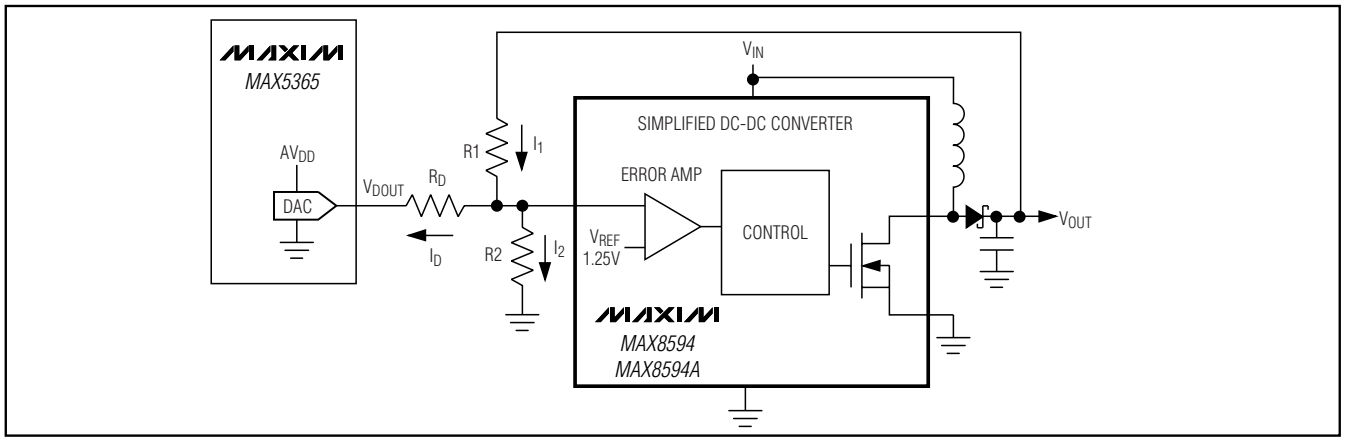


Figure 6. Adjusting the Output Voltage with a DAC

and $\overline{LBO}$ are automatically driven low and the part is shut down when the DBI threshold is crossed (going low).

LCD Boost Output

LCD Inductor

The LCD boost is designed to operate with a wide range of inductor values (4.7µH to 150µH). Smaller inductance values typically offer smaller size for a given series resistance or saturation current. Smaller values cause LX to switch more frequently for a given load and can reduce efficiency at low load currents. Larger values reduce switching losses due to less frequent switching for a given load, but higher DC resistance can reduce efficiency. Note that for inductors larger than 43µH, the peak inductor current does not reach 250mA before the LXL maximum on-time (3µs) expires. This reduces output current but may be beneficial for light-load efficiency. A 10µH inductor provides a good balance and works well for most applications. The inductor's saturation current rating should be greater than the peak switching current (250mA).

LCD Diode

Schottky diodes rated at 250mA or more, such as the MBR0530 or Nihon EP05Q03L, are recommended. The diode reverse-breakdown voltage rating must be greater than the LCD output voltage.

LCD Capacitors

For most applications, use a ceramic 1µF output capacitor. This typically provides a peak-to-peak output ripple of 30mV. In addition, bypass IN with 1µF and SW with 4.7µF ceramic capacitors. An LCD feed-forward capacitor, connected from the output to LFB, improves stability over a wide range of battery voltages. A 47pF capacitor is sufficient for most applications; however, the optimum value is affected by PC board layout.

Setting LCD Voltage

Adjust the output voltage by connecting a voltage-divider from the LCD output to LFB (see Figure 1). Select R2 between 10kΩ and 200kΩ. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{LFB}} - 1 \right)$$

where V_{LFB} = 1.25V and V_{OUT} can range from V_{IN} to 28V. The input bias current of LFB is typically only 5nA, allowing large-value resistors to be used. For less than 1% error, the current through R2 should be greater than 100 times the feedback input bias current (I_{LFB}).

LCD Adjustment

The LCD boost output can be digitally adjusted by either a DAC or PWM signal.

DAC Adjustment

Adding a DAC and a resistor, R_D, to the divider circuit (Figure 6) provides DAC adjustment of V_{OUT}. Ensure that $V_{OUT(MAX)}$ does not exceed the LCD panel rating. The output voltage (V_{OUT}) as a function of the DAC voltage (V_{DOUT}) is calculated using the following formula:

$$V_{OUT} = 1.25 \times \left(1 + \left(\frac{R1}{R2} \right) \right) + \frac{(1.25 - V_{DOUT}) \times R1}{R_D}$$

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

Using PWM Signals

Many µPs have the ability to create PWM outputs. These are digital outputs, based on either 16-bit or 8-bit counters, with a programmable duty cycle. In many applications, they are suitable for adjusting the output of the MAX8594/MAX8594A as seen in Figure 7.

The circuit consists of the PWM source, capacitor C11, and resistors R_D and R_W. To analyze the transfer function of the PWM circuit, it is easiest to first simplify it to its Thevenin equivalent. The Thevenin voltage is calculated using the following formula:

$$V_{THEV} = (D \times V_{OH}) + (1 - D) \times V_{OL}$$

where D is the duty cycle of the PWM signal, V_{OH} is the PWM output high level (often 3.3V), and V_{OL} is the PWM output low level (usually 0V). For CMOS logic, this equation simplifies to:

$$V_{THEV} = D \times V_{DD}$$

where V_{DD} is the logic-high output voltage of the PWM output. The Thevenin impedance is the sum of resistors R_W and R_D:

$$R_{THEV} = R_D + R_W$$

The output voltage (V_{OUT}) as a function of the PWM average voltage (V_{THEV}) is:

$$V_{OUT} = 1.25 \times \left(1 + \left(\frac{R1}{R2}\right)\right) + \frac{(1.25 - V_{THEV}) \times R1}{R_{THEV}}$$

When using the PWM adjustment method, R_D isolates the capacitor from the feedback loop of the MAX8594/MAX8594A. The cutoff frequency of the low-pass filter is defined as:

$$f_C = \frac{1}{2 \times \pi \times R_{THEV} \times C_{11}}$$

The cutoff frequency should be at least two decades below the PWM frequency to minimize the induced AC ripple at the output.

An important consideration is the turn-on transient created by the initial charge on filter capacitor C11. This capacitor forms a time constant with R_{THEV}, causing the output to initialize at a higher than intended voltage. This overshoot is minimized by scaling R_D as high as possible compared to R1 and R2. Alternatively, the µP can briefly keep the LCD disabled until the PWM voltage has had time to stabilize.

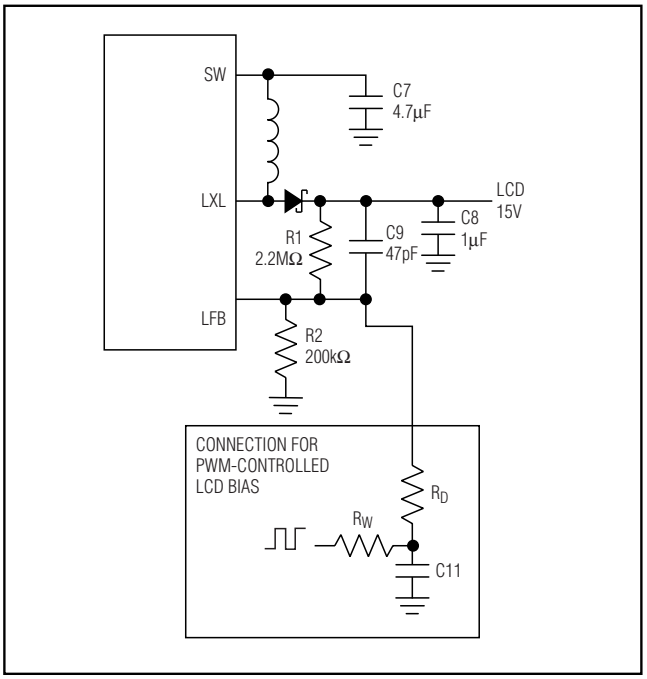


Figure 7. PWM-Controlled LCD Bias

PC Board Layout and Grounding

Careful PC board layout is important for minimizing ground bounce and noise. Keep the MAX8594/MAX8594A's ground pin and the ground leads of the input and output capacitors less than 0.2in (5mm) apart. In addition, keep all connections to LFB, COR1, LXC, and LXL as short as possible. In particular, external feedback resistors should be as close to LFB as possible. To minimize output voltage ripple and to maximize output power and efficiency, use a ground plane and solder PGND and exposed pad directly to the ground plane. Refer to the MAX8594 evaluation kit for a layout example.

Thermal Considerations

In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad of the thin QFN package to a large ground plane, preferably on a surface of the board that receives good airflow. Typical applications use multiple ground planes to minimize thermal resistance. Avoid large AC currents through the ground plane.

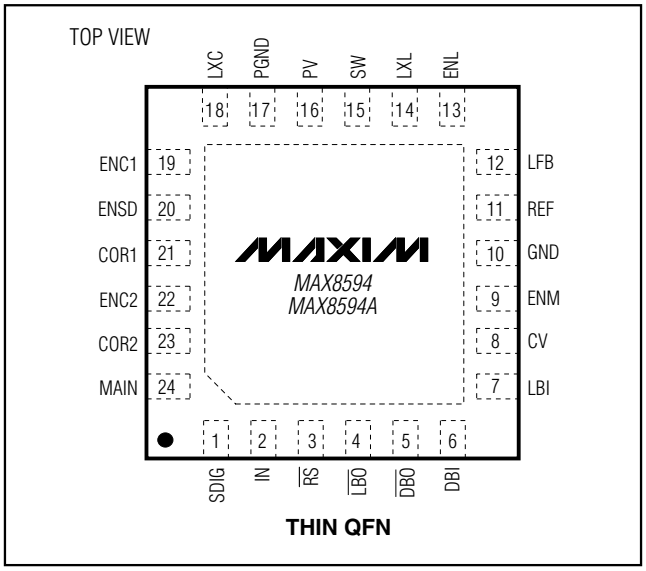
5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

Chip Information

TRANSISTOR COUNT: 3436

PROCESS: BiCMOS

Pin Configuration

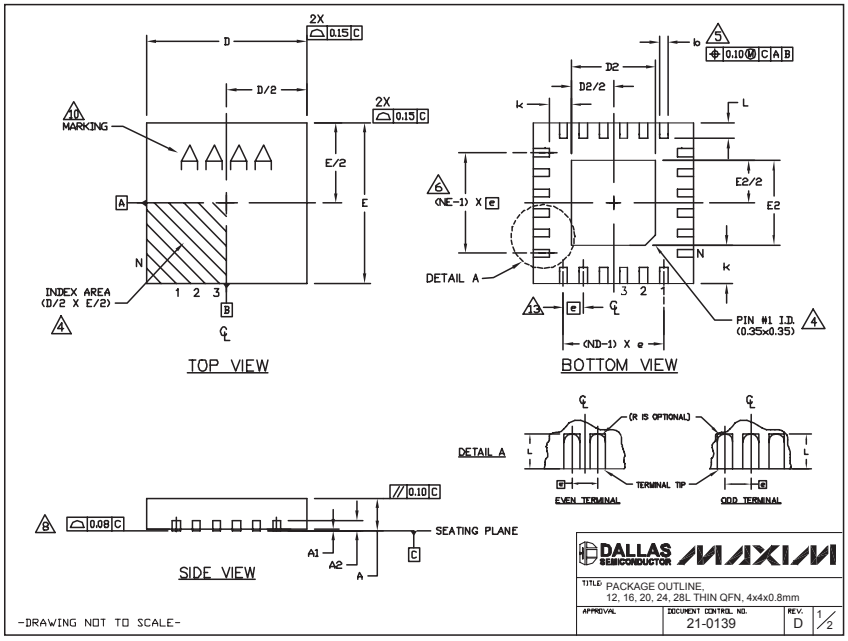


THIN QFN

5-Output PMICs with DC-DC Core Supply for Low-Cost PDAs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. D
2/2

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