19-1771; Rev 0; 9/00

MAXIM

Single/Dual LVDS Line Drivers with Ultra-Low Pulse Skew in SOT23

General Description

The MAX9110/MAX9112 single/dual low-voltage differential signaling (LVDS) transmitters are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single +3.3V supply, and feature ultra-low 250ps (max) pulse skew required for high-resolution imaging applications, such as laser printers and digital copiers.

The MAX9110 is a single LVDS transmitter, and the MAX9112 is a dual LVDS transmitter.

Both devices conform to the EIA/TIA-644 LVDS standard. They accept LVTTL/CMOS inputs and translate them to low-voltage (350mV) differential outputs, minimizing electromagnetic interference (EMI) and power dissipation. These devices use a current-steering output stage, minimizing power consumption, even at high data rates. The MAX9110/MAX9112 are available in space-saving 8-pin SOT23 and SO packages. Refer to the MAX9111/MAX9113 data sheet for single/dual LVDS line receivers.

Applications

- Laser Printers
- Digital Copiers
- Cellular Phone Base Stations
- Telecom Switching Equipment
- Network Switches/Routers
- LCD Displays
- Backplane Interconnect
- Clock Distribution

Features

- ♦ **Low 250ps (max) Pulse Skew for High-Resolution Imaging and High-Speed Interconnect**
- ♦ **Space-Saving 8-Pin SOT23 and SO Packages**
- ♦ **Pin-Compatible Upgrades to DS90LV017/017A and DS90LV027/027A (SO Packages)**
- ♦ **Guaranteed 500Mbps Data Rate**
- ♦ **Low 22mW Power Dissipation at 3.3V (31mW for MAX9112)**
- ♦ **Conform to EIA/TIA-644 Standard**
- ♦ **Single +3.3V Supply**
- ♦ **Flow-Through Pinout Simplifies PC Board Layout**
- ♦ **Driver Outputs High Impedance when Powered Off**

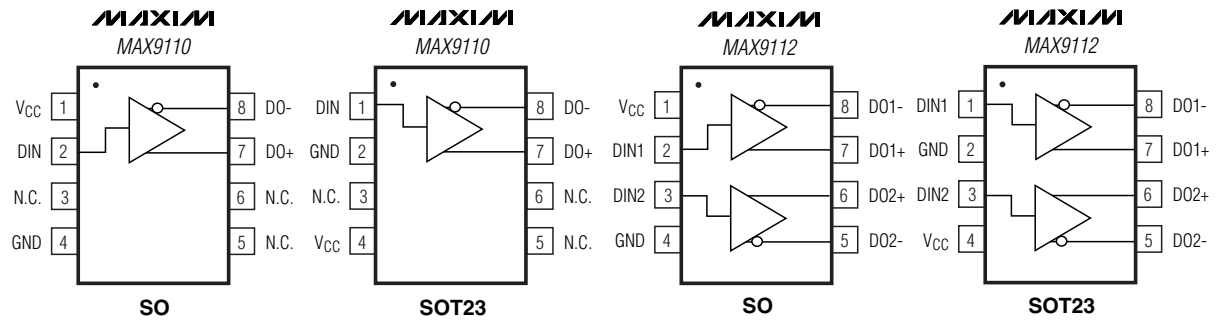
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9110EKA-T	-40°C to +85°C	8 SOT23-8	AADN
MAX9110ESA	-40°C to +85°C	8 SO	—
MAX9112EKA-T	-40°C to +85°C	8 SOT23-8	AADO
MAX9112ESA	-40°C to +85°C	8 SO	—

Typical Operating Circuit appears at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Table

TOP VIEW



DIN_	DO_+	DO_-
L	L	H
H	H	L
0.8V < $V_{DIN\_}$ < 2.0V	X	X

H = LOGIC LEVEL HIGH
L = LOGIC LEVEL LOW
X = UNDETERMINED

Single/Dual LVDS Line Drivers with Ultra-Low Pulse Skew in SOT23

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to GND) .....-0.3V to +4V
Input Voltage ($V_{DIN\_}$ to GND).....-0.3V to (V_{CC} + 0.3V)
Output Voltage (V_{DO_+}, V_{DO_-} to GND or V_{CC}) ...-0.3V to +3.9V
Output Short-Circuit Duration
(DO_+, DO_- to V_{CC} or GND) .....Continuous
ESD Protection (Human Body Model, DO_+, DO_-).....±11kV

Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 7.52mW/°C above +70°C).....602mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering,10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{OD}	Figure 1		250	350	450	mV
Change in Magnitude of Output Voltage for Complementary Output States	ΔV_{OD}	Figure 1		0	2	35	mV
Offset Voltage	V_{OS}	Figure 1		1.125	1.25	1.375	V
Change in Magnitude of Offset Voltage for Complementary Output States	ΔV_{OS}	Figure 1		0	2	25	mV
Power-Off Leakage Current	$I_{O(OFF)}$	$V_{DO\_\_}$ = 0 or V_{CC}, V_{CC} = 0 or open		-10		+10	µA
Short-Circuit Output Current	$I_{O(SHORT)}$	DIN_ = V_{CC}, V_{DO_+} = 0 or DIN_ = GND, V_{DO_-} = 0				-20	mA
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			GND		0.8	V
Input Current High	I_{IH}	DIN_ = V_{CC} or 2V		0	10	20	µA
Input Current Low	I_{IL}	DIN_ = GND or 0.8V		-20	-3	0	µA
No-Load Supply Current	I_{CC}	No load, DIN_ = V_{CC} or 0			4.5	6	mA
Supply Current	I_{CC}	DIN_ = V_{CC} or 0	MAX9110		6.7	8	mA
			MAX9112		9.4	13	

AC CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 3, 4, 5; Figures 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential High-to-Low Propagation Delay	t_{PHLD}		1	1.54	2.5	ns
Differential Low-to-High Propagation Delay	t_{PLHD}		1	1.58	2.5	ns
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (Note 6)	t_{SKD1}			40	250	ps
Channel-to-Channel Skew (Note 7)	t_{SKD2}			70	400	ps

AC CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 3, 4, 5; Figures 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Part-to-Part Skew	t_{SKD3}	(Note 8)			1	ns
	t_{SKD4}	(Note 9)			1.5	
High-to-Low Transition Time	t_{THL}		0.25	0.6	1	ns
Low-to-High Transition Time	t_{TLH}		0.25	0.6	1	ns
Maximum Operating Frequency	f_{MAX}	(Note 10)	250			MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design. Devices are production tested at T_A = +25°C.

Note 2: By definition, current into the device is positive and current out of the device is negative. Voltages are referred to device ground except V_{OD}.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes probe and fixture capacitance.

Note 5: Signal generator conditions for dynamic tests: V_{OL} = 0, V_{OH} = 3V, f = 20MHz, 50% duty cycle, R_O = 50Ω, $t_R \le$ 1ns, and $t_F \le$ 1ns (0 to 100%).

Note 6: t_{SKD1} is the magnitude difference of differential propagation delays in a channel; $t_{SKD1} = | t_{PHLD} - t_{PLHD} |$.

Note 7: t_{SKD2} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of the other channel on the same device (MAX9112).

Note 8: t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.

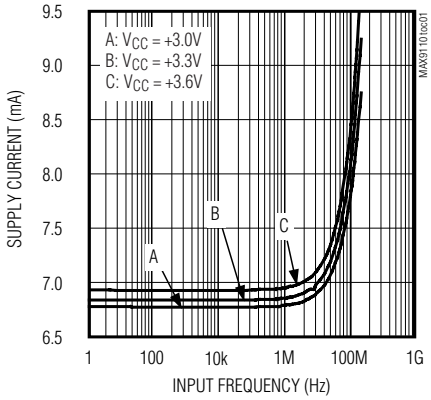
Note 9: t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Note 10: f_{MAX} signal generator conditions: V_{OL} = 0, V_{OH} = +3V, frequency = 250MHz, $t_R \le$ 1ns, $t_F \le$ 1ns (0 to 100%) 50% duty cycle. Transmitter output criteria: duty cycle = 45% to 55%, $V_{OD} \ge$ 250mV.

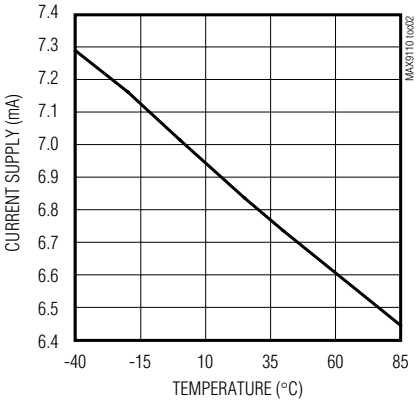
Typical Operating Characteristics

(V_{CC} = +3.3V, R_L = 100Ω, C_L = 5pF, V_{IH} = +3V, V_{IL} = GND, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.) (Figures 2, 3)

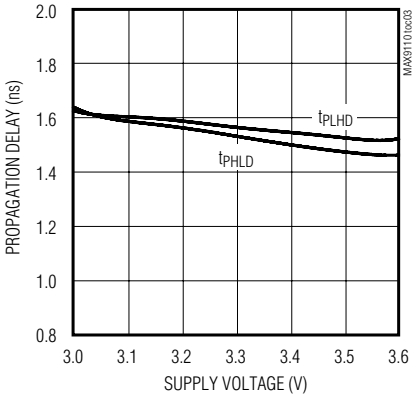
MAX9110 SUPPLY CURRENT vs. INPUT FREQUENCY



SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE

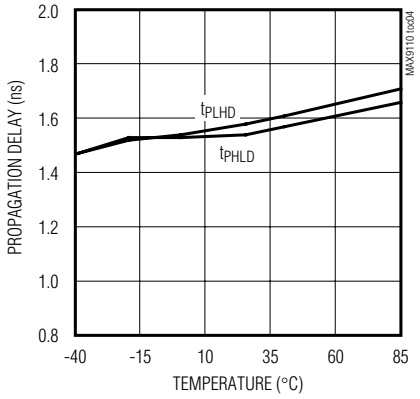


Single/Dual LVDS Line Drivers with Ultra-Low Pulse Skew in SOT23

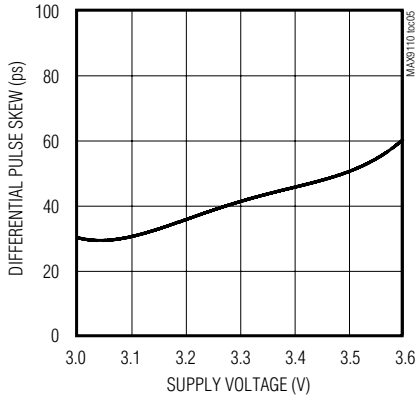
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω, C_L = 5pF, V_{IH} = +3V, V_{IL} = GND, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.) (Figures 2, 3)

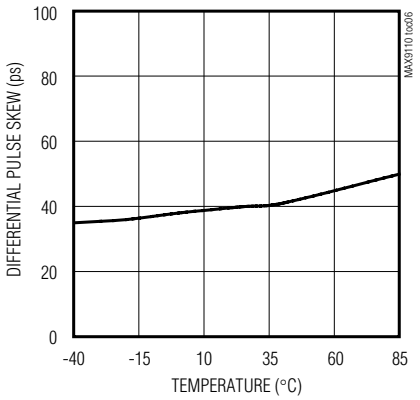
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



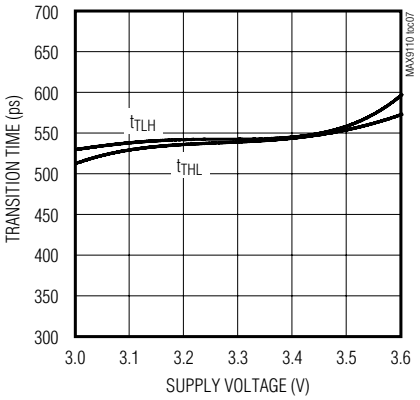
DIFFERENTIAL PULSE SKEW vs. SUPPLY VOLTAGE



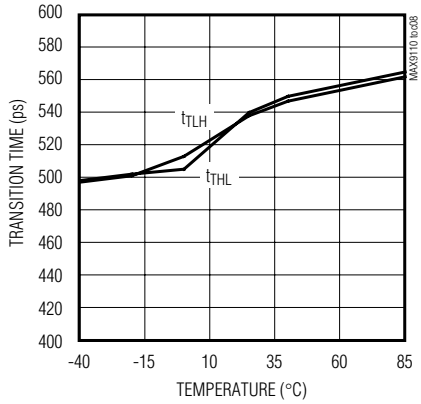
DIFFERENTIAL PULSE SKEW vs. TEMPERATURE



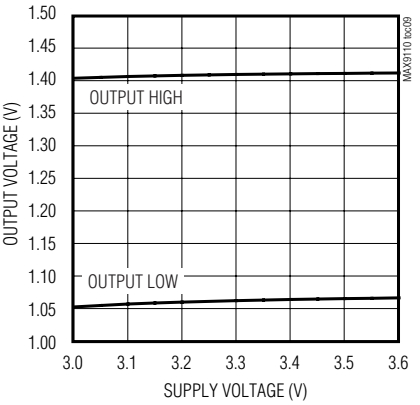
TRANSITION TIME vs. SUPPLY VOLTAGE



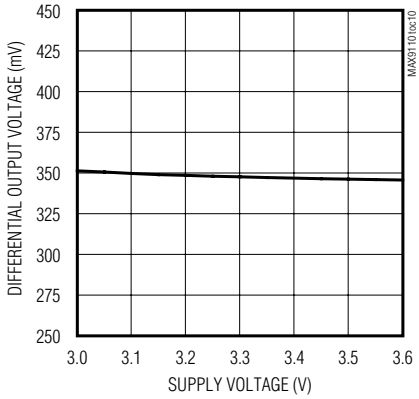
TRANSITION TIME vs. TEMPERATURE



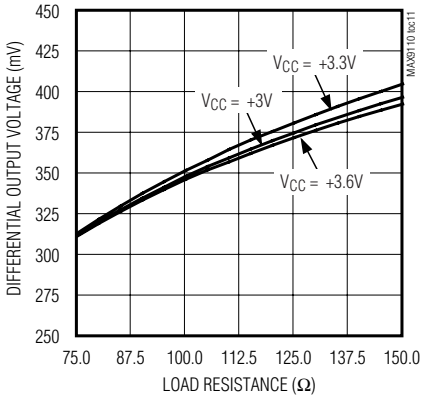
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



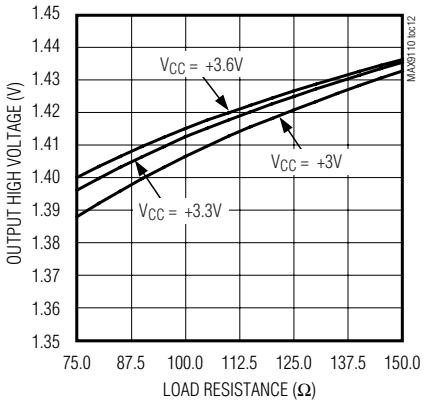
DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE



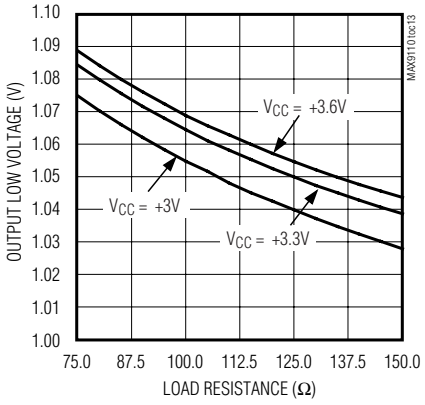
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω, C_L = 5pF, V_{IH} = +3V, V_{IL} = GND, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.) (Figures 2, 3)

OUTPUT HIGH VOLTAGE vs. LOAD RESISTANCE



OUTPUT LOW VOLTAGE vs. LOAD RESISTANCE



Pin Description

PIN				NAME	FUNCTION
MAX9110		MAX9112			
SOT23	SO	SOT23	SO		
4	1	4	1	V_{CC}	Positive Supply
1	2	—	—	DIN	Transmitter Input
—	—	1, 3	2, 3	DIN1, DIN2	
3, 5, 6	3, 5, 6	—	—	N.C.	No Connection. Not internally connected.
2	4	2	4	GND	Ground
7	7	—	—	DO+	Noninverting Transmitter Output
—	—	6, 7	6, 7	DO2+, DO1+	
8	8	—	—	DO-	Inverting Transmitter Output
—	—	5, 8	5, 8	DO2-, DO1-	

Detailed Description

The MAX9110/MAX9112 single/dual LVDS transmitters are intended for high-speed, point-to-point, low-power applications. These devices accept CMOS/LVTTL inputs with data rates exceeding 500Mbps. The MAX9110/MAX9112 reduce power consumption and EMI by translating these signals to a differential voltage in the 250mV to 450mV range across a 100Ω load while drawing only 9.4mA of supply current for the dual-channel MAX9112.

A current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The output

Single/Dual LVDS Line Drivers with Ultra-Low Pulse Skew in SOT23

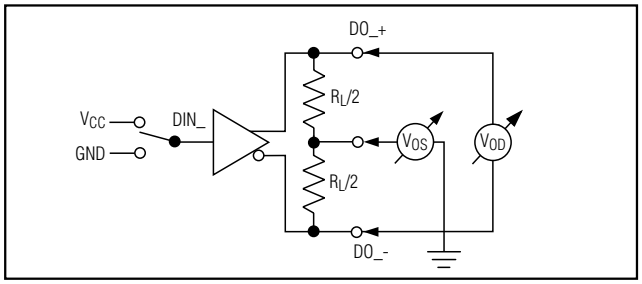


Figure 1. LVDS Transmitter V_{OD} and V_{OS} Test Circuit

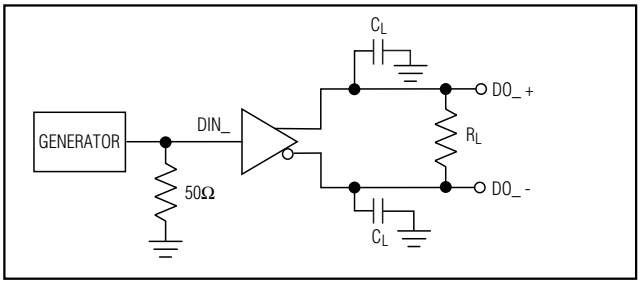


Figure 2. Transmitter Propagation Delay and Transition Time Test Circuit

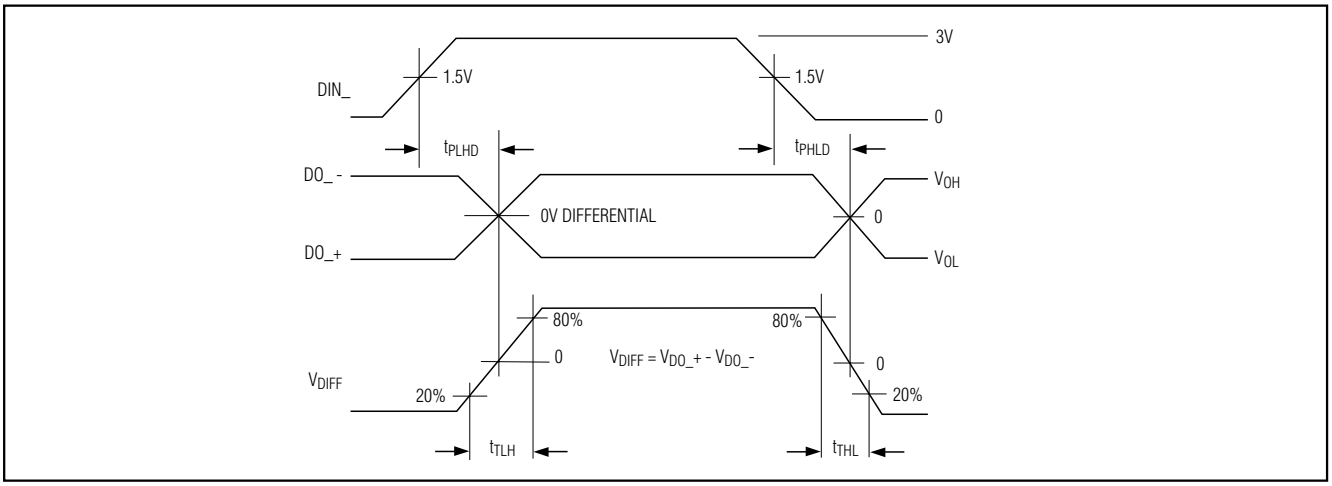


Figure 3. Transmitter Propagation Delay and Transition Time Waveforms

stage presents a symmetrical, high-impedance output, reducing differential reflection and timing distortion. The driver outputs are short circuit current limited and enter a high-impedance state when the device is not powered.

LVDS Operation

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance medium as defined by the EIA/TIA-644 LVDS standard. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

LVDS transmitters such as the MAX9110/MAX9112 convert CMOS/LVTTL signals to low-voltage differential signals at rates in excess of 500Mbps. The MAX9110/MAX9112 current-steering architecture requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches the direction of current flow and not voltage levels, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver. Logic states are determined by the direction of current flow through the termination resistor. With a typical 3.5mA output current, the MAX9110/MAX9112 produce an output voltage of 350mV when driving a 100Ω load. The steady-state-voltage peak-to-peak swing is twice the differential voltage, or 700mV (typ).

Applications Information

Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel, as close to the device as possible, with the smaller valued capacitor the closest. For additional supply bypassing, place a 10µF tantalum or ceramic capacitor at the point where power enters the circuit board.

Differential Traces

Output trace characteristics affect the performance of the MAX9110/MAX9112. Use controlled impedance traces to match trace impedance to both transmission medium impedance and termination resistor. Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a differential characteristic impedance of about 100Ω. Use cables and connectors that have matched impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon or simple coaxial cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

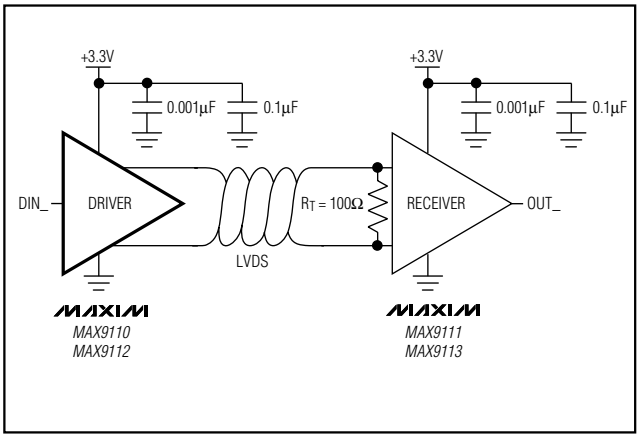
Termination resistors should match the differential characteristic impedance of the transmission line. Because the MAX9110/MAX9112 are current-steering devices, an output voltage will not be generated without a termination resistor. Output voltage levels are dependent upon the termination resistor value. Resistance values may range between 75Ω and 150Ω.

Minimize the distance between the termination resistor and receiver inputs. Use a single 1% to 2% surface-mount resistor across the receiver inputs.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the input and LVDS signals from each other to prevent coupling. Separate the input and LVDS signal planes with the power and ground planes for best results.

Typical Operating Circuit



Chip Information

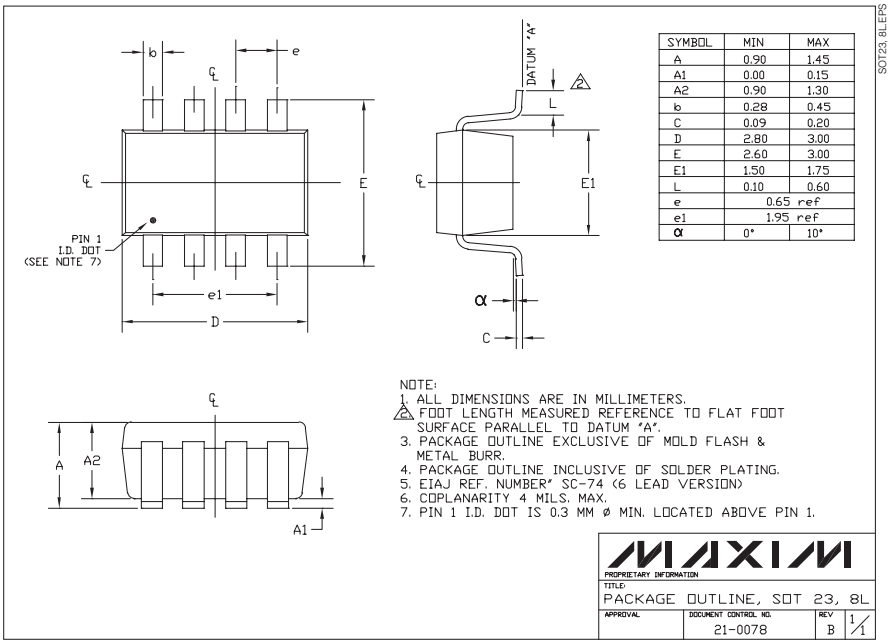
MAX9110 TRANSISTOR COUNT: 765

MAX9112 TRANSISTOR COUNT: 765

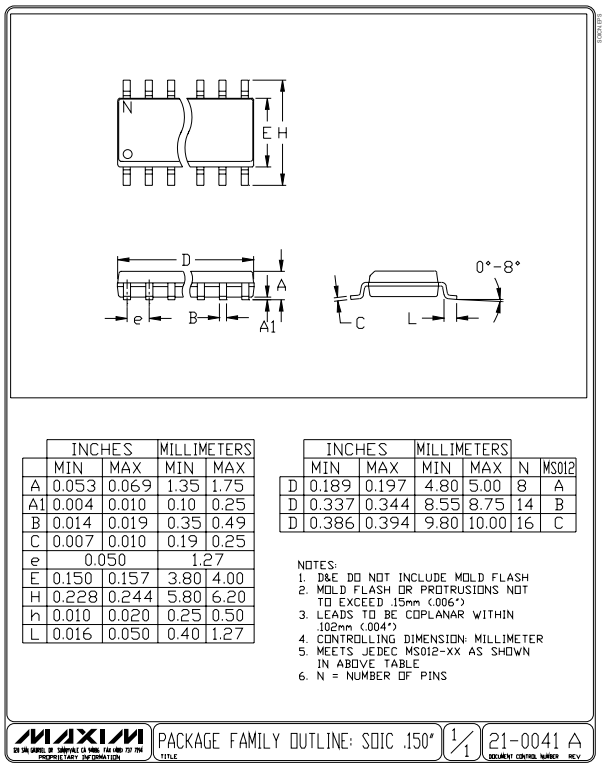
PROCESS: CMOS

Single/Dual LVDS Line Drivers with Ultra-Low Pulse Skew in SOT23

Package Information



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

PROPRIETARY INFORMATION
TITLE
PACKAGE FAMILY OUTLINE: SOIC .150"
1/1
DOCUMENT CONTROL NUMBER
21-0041 A
REV