19-0849; Rev 0; 7/07

10-Bit LVDS Serializer

General Description

The MAX9235 serializer transforms 10-bit-wide parallel LVCMOS/LVTTL data into a serial high-speed, low-voltage differential signaling (LVDS) data stream. The serializer typically pairs with deserializers like the MAX9206, which receives the serial output and transforms it back to 10-bit-wide parallel data.

The MAX9235 transmits serial data at speeds up to 400Mbps over PCB traces or twisted-pair cables. Since the clock is recovered from the serial data stream, clock-to-data and data-to-data skew that would be present with a parallel bus are eliminated.

The MAX9235 serializer requires no external components and no control signals and can lock to a 16MHz to 40MHz system clock. The serializer output is held in high impedance until the device is fully locked to the local system clock.

The MAX9235 operates from a single +3.3V supply, is specified for operation from -40°C to +105°C, and is available in a 16-pin TQFN (3mm x 3mm) package.

Applications

Lane Departures
Security Cameras
Rear View Cameras
Production Line Monitoring

Features

- **Stand-Alone Serializer (vs. SERDES) Ideal for Unidirectional Links**
- **Framing Bits for Deserializer Resync Allow Hot Insertion Without System Interruption**
- **LVDS Serial Output Rated for Point-to-Point Applications**
- **Wide Reference Clock Input Range 16MHz to 40MHz**
- **Low 31mA Supply Current**
- **10-Bit Parallel LVCMOS/LVTTL Interface**
- **Up to 400Mbps Payload Data Rate**
- **Small 16-Pin TQFN (3mm x 3mm) Package**

Ordering Information

PART	PIN-PACKAGE	REF CLOCK RANGE (MHz)	PKG CODE
MAX9235ETE+	16 TQFN-EP*	16 to 40	TI633-5

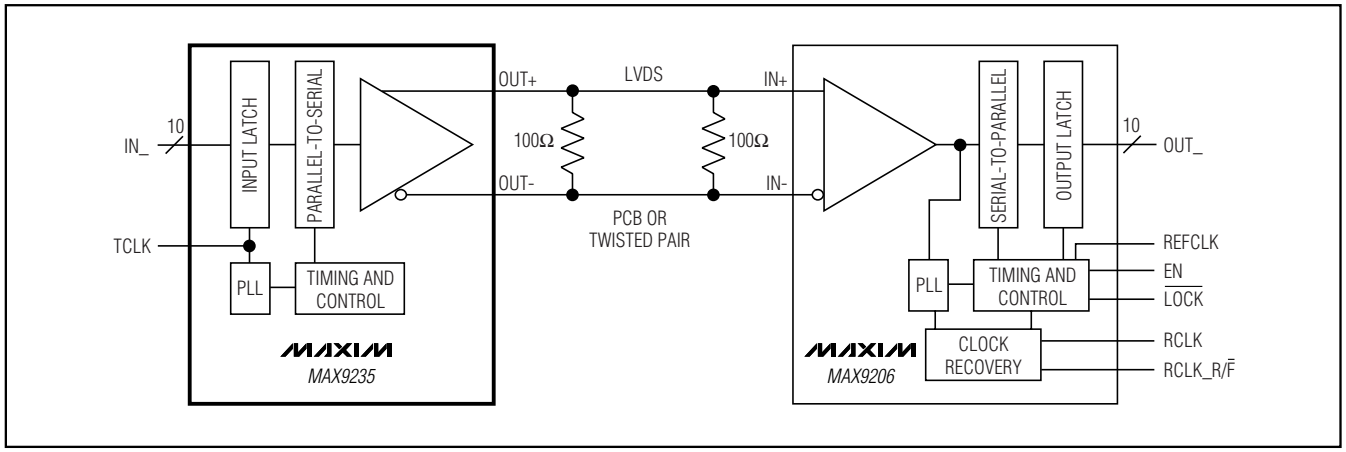
+Denotes a lead-free package.

***Note:** The device is specified over the -40°C to +105°C temperature range.*

**EP = Exposed pad.*

Pin Configuration and Functional Diagram appear at end of data sheet.

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN_, TCLK to GND .....-0.3V to (V_{CC} + 0.3V)
OUT+, OUT- to GND .....-0.3V to +4.0V
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 14.7mW/°C above +70°C) 1177mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +105°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection (Human Body Model, OUT+, OUT-) .....±8kV
ESD Protection (Human Body Model, IN_, TCLK) .....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 10pF, T_A = -40°C to +105°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVCMOS/LVTLL LOGIC INPUTS (IN0 TO IN9, EN, TCLK)							
High-Level Input Voltage	V_{IH}			2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}			GND		0.8	V
Input Current	I_{IN}	$V_{IN\_}$ = 0 or V_{CC}		-20		+20	µA
LVDS OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Figure 1	R_L = 100Ω	600	735	950	mV
			R_L = 50Ω	250	370	470	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1			1	35	mV
Output Offset Voltage	V_{OS}	Figure 1	R_L = 100Ω	1.025	1.265	1.375	V
			R_L = 50Ω	1.125	1.265	1.375	
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1			3	35	mV
Output Short-Circuit Current	I_{OS}	OUT+ or OUT- = 0, IN0 to IN9 = EN = high			-13	-15	mA
Power-Off Output Current	I_{OX}	V_{CC} = 0, OUT+ or OUT- = 0 or 3.6V		-10		+10	µA
POWER SUPPLY							
Supply Current	I_{CC}	R_L = 100Ω or 50Ω worst-case pattern (Figures 2, 4)	16MHz		22	35	mA
			40MHz		31	45	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 5pF, T_A = -40°C to +105°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT CLOCK (TCLK) TIMING REQUIREMENTS							
TCLK Center Frequency	f_{TCCF}			16		40	MHz
TCLK Frequency Variation	TCFV			-200		+200	ppm
TCLK Period	t_{TCP}			25		62.5	ns
TCLK Duty Cycle	TCDC			40		60	%
TCLK Input Transition Time	t_{CLKT}	Figure 3			3	6	ns
TCLK Input Jitter	t_{JIT}					150	ps (RMS)
SWITCHING CHARACTERISTICS							
Low-to-High Transition Time	t_{LHT}	Figure 4	R_L = 100Ω		370	500	ps
			R_L = 50Ω		350	500	
High-to-Low Transition Time	t_{HLT}	Figure 4	R_L = 100Ω		370	500	ps
			R_L = 50Ω		350	500	
IN_ Setup to TCLK	t_S	Figure 5		1			ns
IN_ Hold from TCLK	t_H	Figure 5		3			ns
PLL Lock Time	t_{PL}	Figure 6		2048 x t_{TCP}		2049 x t_{TCP}	ns
Bus LVDS Bit Width	t_{BIT}			t_{TCP} / 12			ns
Serializer Delay	t_{SD}	Figure 7		t_{TCP} / 6		(t_{TCP} / 6) + 5	ns

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{OD}, ΔV_{OD}, and V_{OS}.

Note 2: C_L includes scope probe and test jig capacitance.

Note 3: Parameters 100% tested at T_A = +25°C. Limits over operating temperature range guaranteed by design and characterization.

Note 4: AC parameters are guaranteed by design and characterization.

10-Bit LVDS Serializer

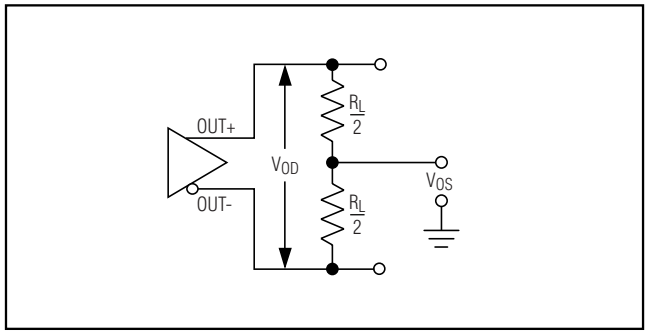


Figure 1. Output Voltage Definitions

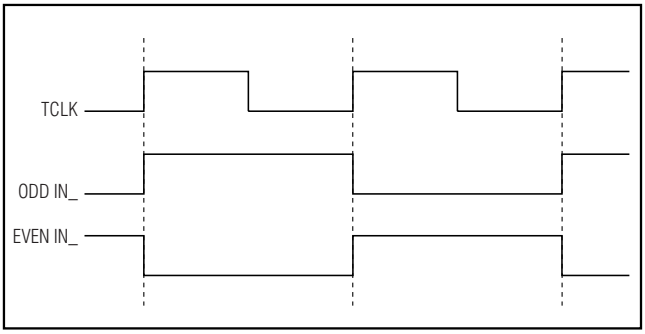


Figure 2. Worst-Case I_{CC} Test Pattern

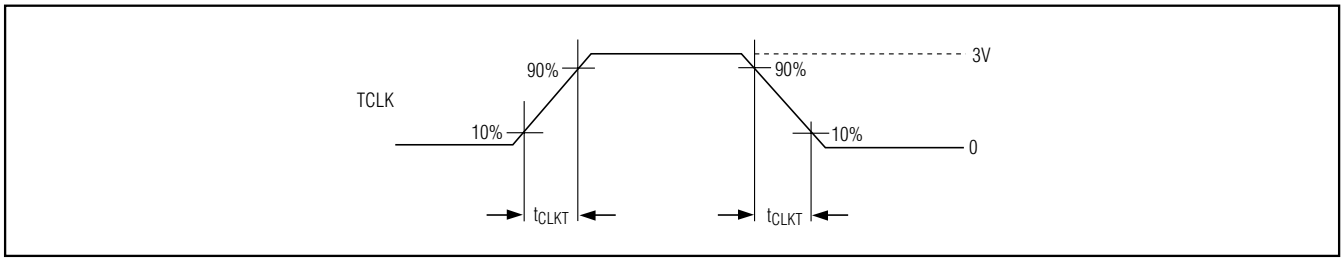


Figure 3. Input Clock Transition Time Requirement

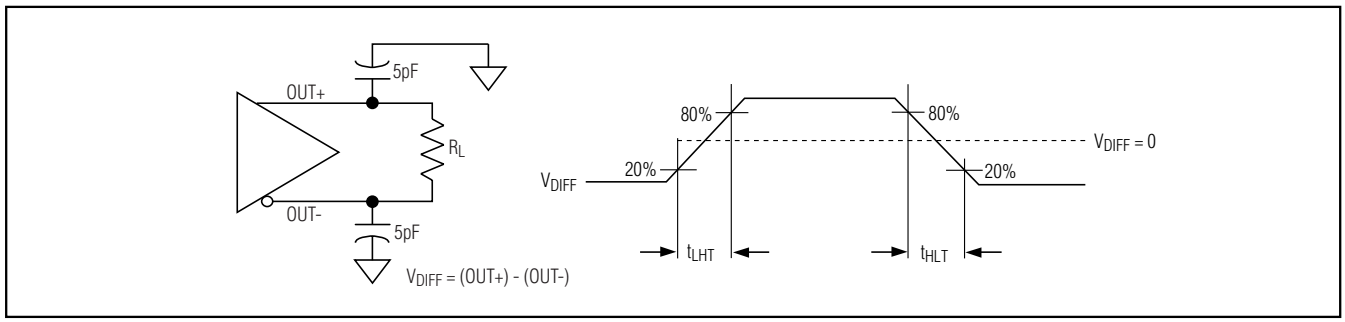


Figure 4. Output Load and Transition Times

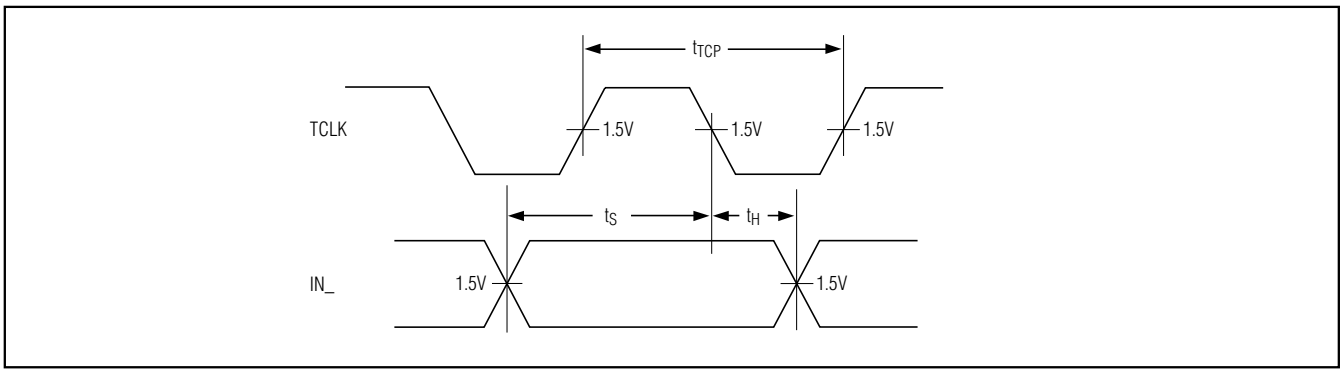


Figure 5. Data Input Setup and Hold Times

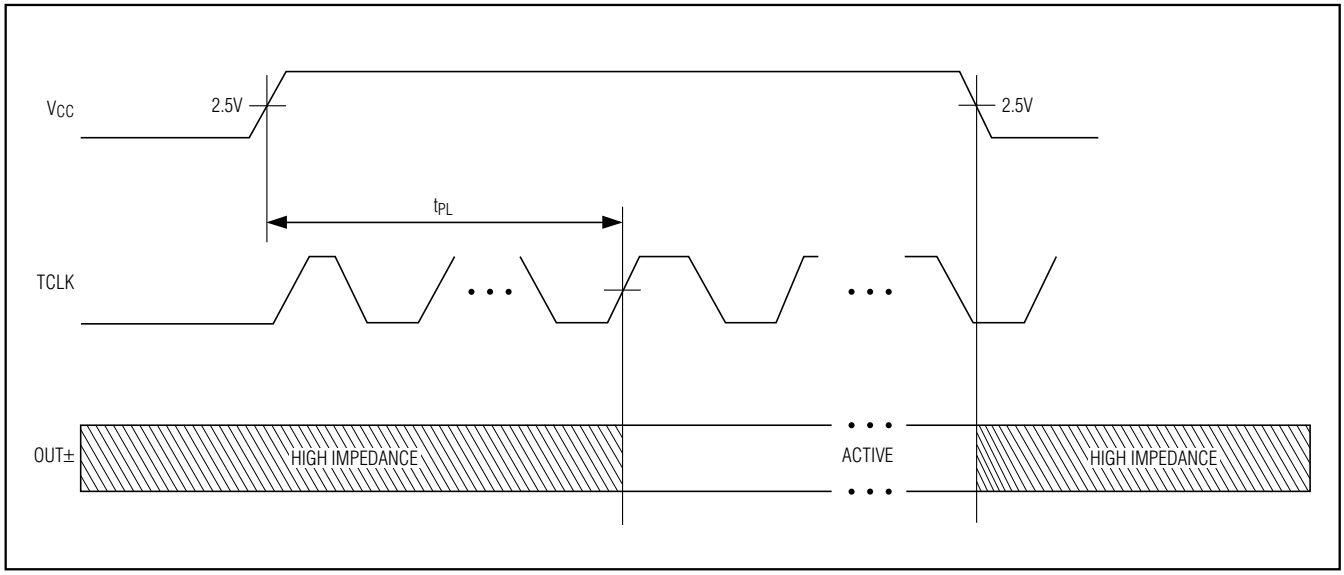


Figure 6. PLL Lock Time

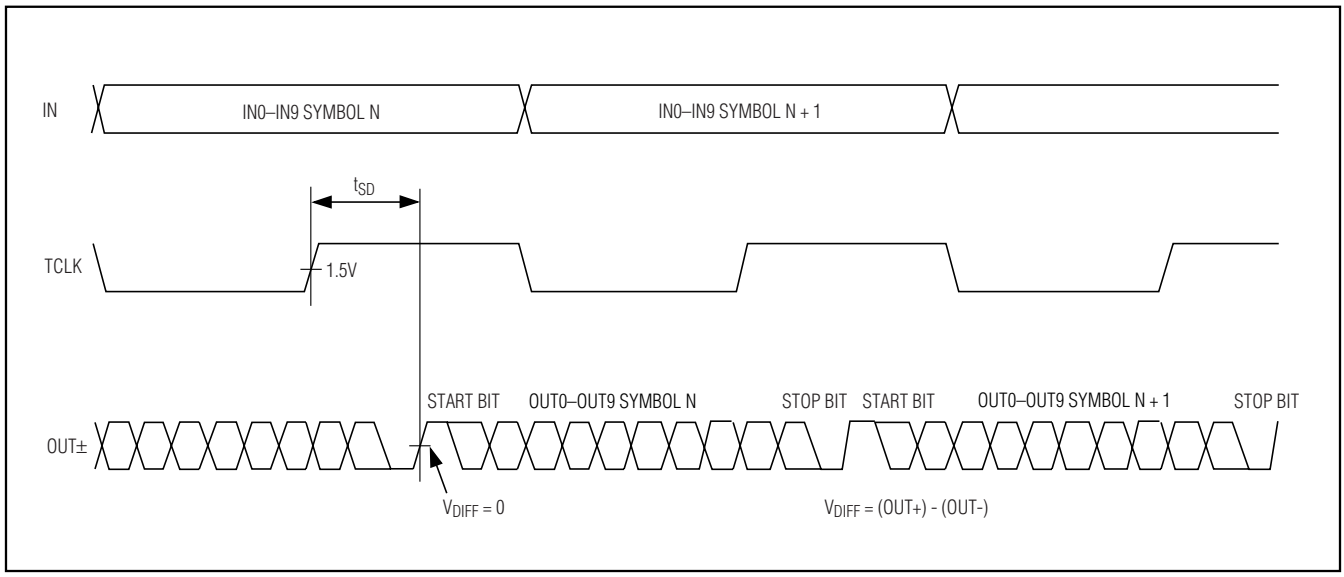


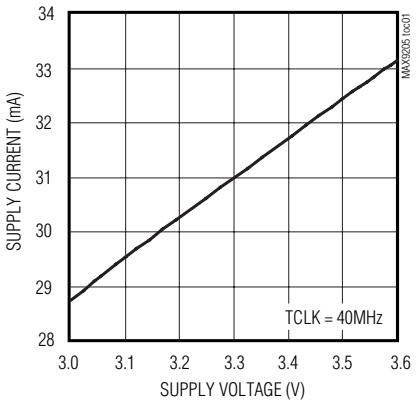
Figure 7. Serializer Delay

10-Bit LVDS Serializer

Typical Operating Characteristics

(V_{CC} = +3.3V, R_L = 50Ω, C_L = 5pF, T_A = +25°C, unless otherwise noted.)

WORST-CASE PATTERN SUPPLY CURRENT vs. SUPPLY VOLTAGE



PIN	NAME	FUNCTION
1–7, 14, 15, 16	IN3–IN9, IN0, IN1, IN2	LVCMOS/LVTTL Data Inputs. Data is loaded into a 10-bit latch by the rising TCLK edge. Each input is internally pulled to ground.
8	TCLK	LVCMOS/LVTTL Reference Clock Input. Accepts a 16MHz to 40MHz clock. TCLK provides a frequency reference to the PLL and strobes parallel data into the input latch on the rising edge.
9, 12	GND	Ground
10	OUT-	Inverting Bus LVDS Differential Output
11	OUT+	Noninverting Bus LVDS Differential Output
13	V_{CC}	Power-Supply Input. Bypass to ground with a 0.1µF capacitor and a 0.001µF capacitor. Place the 0.001µF capacitor closest to V_{CC}.
—	EP	Exposed Pad. Solder EP to ground for improved heat dissipation.

Detailed Description

The MAX9235 10-bit serializer transmits data over balanced media that may be a standard twisted-pair cable or PCB traces at 100Mbps to 400Mbps. The interface may be single- or double-terminated point-to-point. A double-terminated point-to-point interface uses a 100Ω-termination resistor at each end of the interface, resulting in a 50Ω load. The serializer requires a deserializer such as the MAX9206 for a complete data transmission application.

A high-state start bit and a low-state stop bit, added internally, frame the 10-bit parallel input data and ensure a transition in the serial data stream. Therefore, 12 serial bits are transmitted for each 10-bit parallel input. The MAX9235 accepts a 16MHz to 40MHz reference clock, producing a serial data rate of 192Mbps (12 bits x 16MHz) to 480Mbps (12 bits x 40MHz). Since only 10 bits are from input data, the actual throughput is 10 times the TCLK frequency.

To transmit data, the serializer sequences through two modes: initialization mode and data transmission mode.

Initialization Mode

When V_{CC} is applied, the outputs are held in high impedance and internal circuitry is disabled by on-chip power-on-reset circuitry. When V_{CC} reaches 2.35V, the PLL starts to lock to a local reference clock. The reference clock, TCLK, is provided by the system. The serializer locks within 2049 cycles of TCLK. Once locked, the serializer is ready to send data.

Data Transmission Mode

After initialization, input data at IN0–IN9 are clocked into the serializer by the TCLK input. Data strobes on the rising edge of TCLK.

A start bit high and a stop bit low frame the 10-bit data and function as the embedded clock edge in the serial data stream. The serial rate is the TCLK frequency times the data and appended bits. For example, if TCLK is 40MHz, the serial rate is 40 x 12 (10 + 2 bits) = 480Mbps. Since only 10 bits are from input data, the payload rate is 40 x 10 = 400Mbps.

High-Impedance State

The serializer output pins (OUT+ and OUT-) are held in high impedance when V_{CC} is first applied and while the PLL is locking to the local reference clock. If the serializer goes into high impedance, the deserializer loses PLL lock and needs to reestablish phase lock before data transfer can resume. This is done by transmitting all zeroes for at least one frame.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces and Termination

Use controlled-impedance media and terminate at both ends of the transmission line in the media's characteristic impedance. Termination with a single resistor at the end of a point-to-point link typically provides acceptable performance. The MAX9235 output levels are specified for double-terminated point-to-point applications. With a single 100Ω termination, the output swing is larger.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by a differential receiver.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

The differential output signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

10-Bit LVDS Serializer

Topologies

The MAX9235 can operate in point-to-point or broadcast topologies.

A point-to-point connection terminated at each end in the characteristic impedance of the cable or PCB traces is shown in Figure 8. The total load seen by the serializer is 50Ω. The double termination typically reduces reflections compared to a single 100Ω termination. A single 100Ω termination at the deserializer input is feasible and will make the differential signal swing larger.

A point-to-point broadcast configuration is shown in Figure 9. The low-jitter MAX9150 10-port repeater is used to reproduce and transmit the serializer output over 10 double-terminated point-to-point links.

The repeater eliminates nine serializers compared to 10 individual point-to-point serializer-to-deserializer connections. Since repeater jitter subtracts from the serializer-deserializer timing margin, a low-jitter repeater is essential in most high data rate applications.

Board Layout

For LVDS applications, a four-layer PCB that provides separate power, ground, and input/output signals is recommended. Separate LVTTL/LVCMOS and LVDS signals from each other to prevent coupling into the LVDS lines.

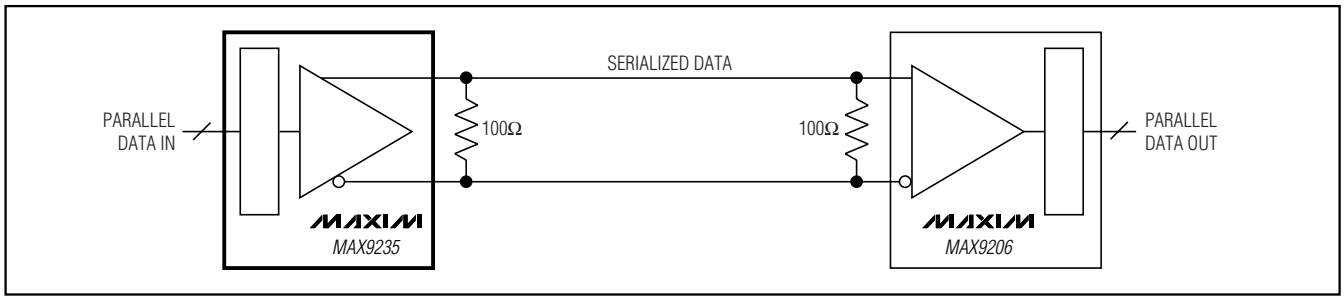


Figure 8. Double-Terminated Point-to-Point

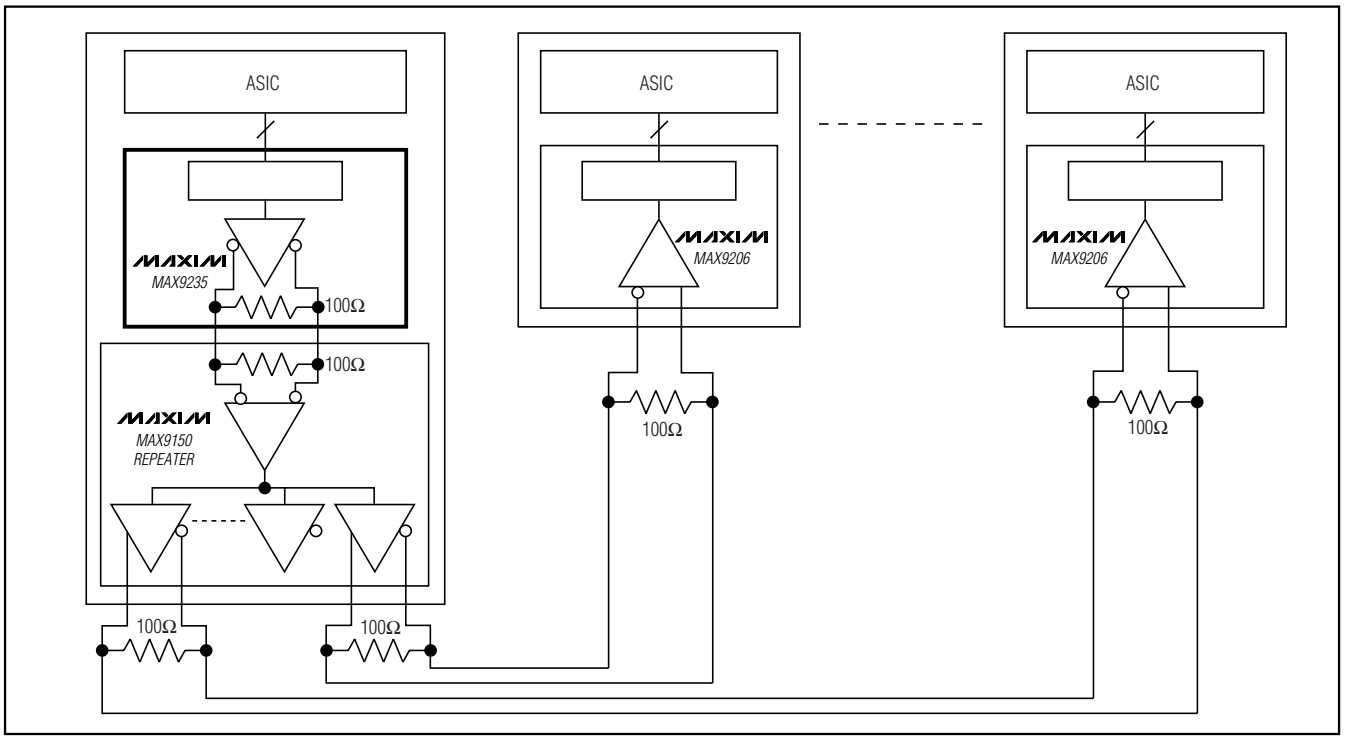
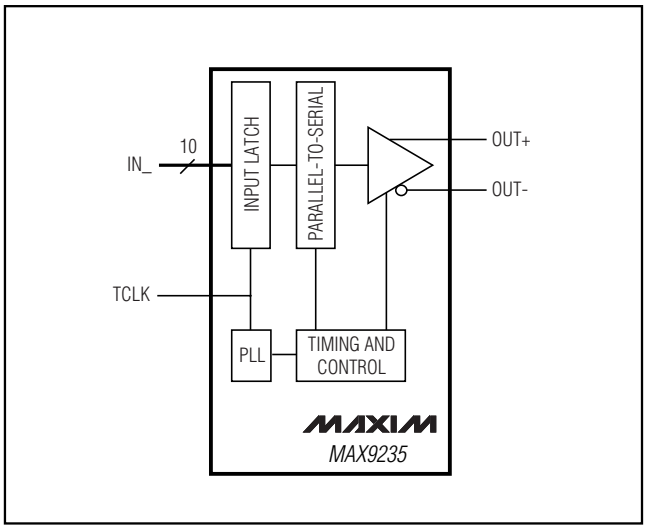
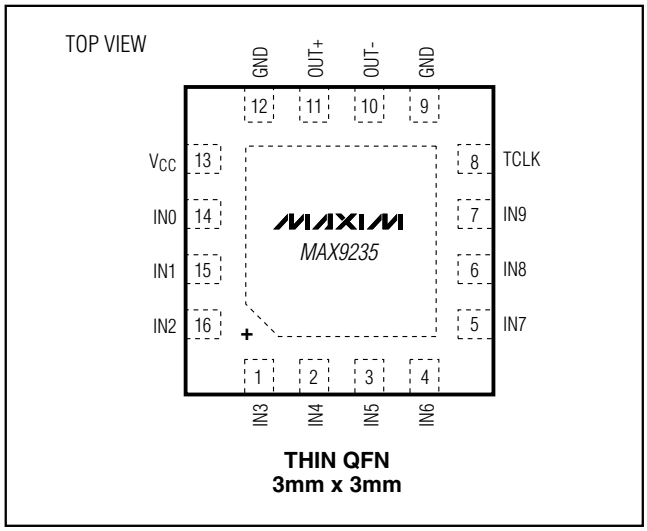


Figure 9. Point-to-Point Broadcast Using MAX9150 Repeater

Functional Diagram



Pin Configuration



THIN QFN
3mm x 3mm

Chip Information

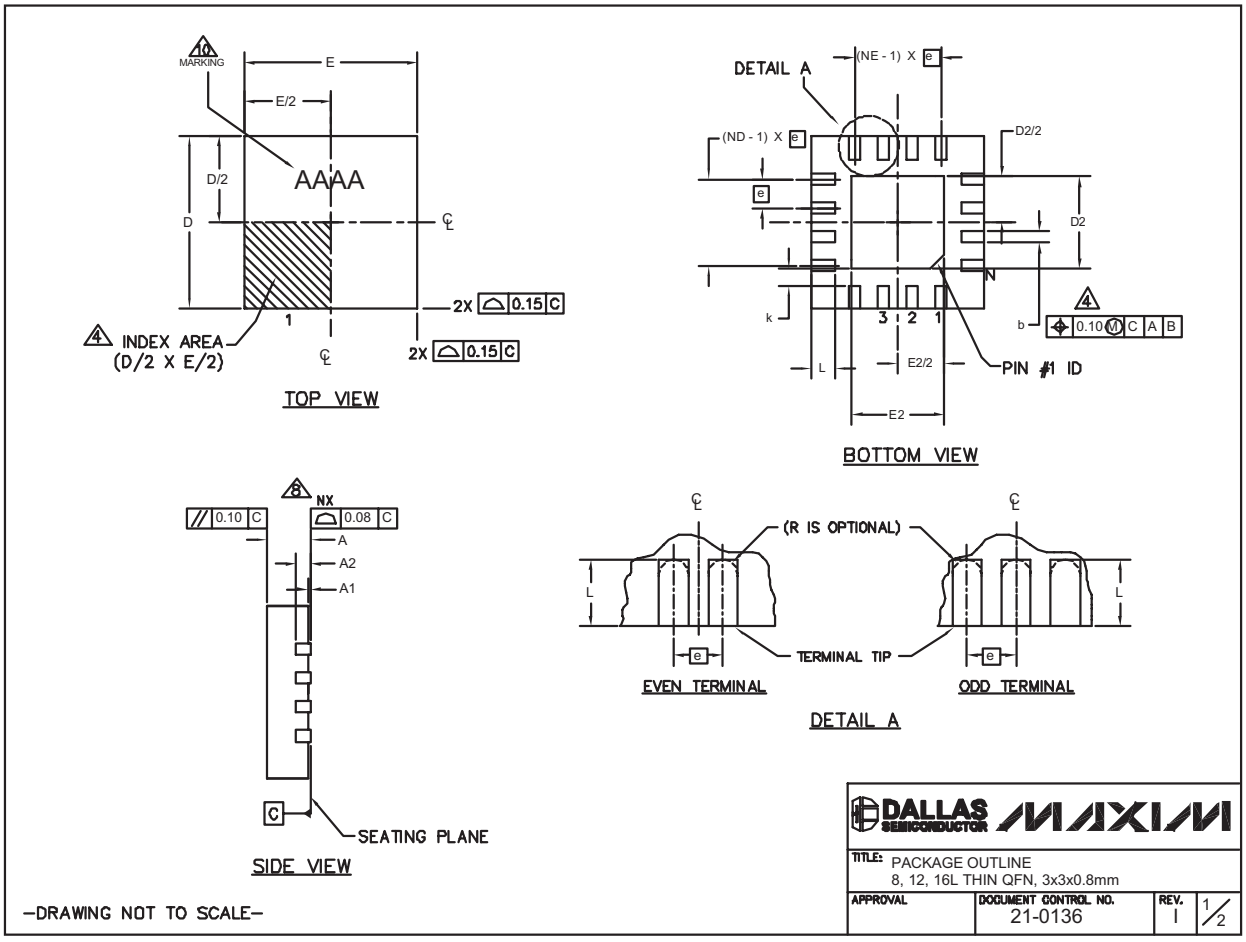
PROCESS: CMOS

10-Bit LVDS Serializer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	I	2/2