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MAX96714/MAX96714F/ MAX96714R

Single GMSL2/GMSL1 to CSI-2 Deserializer

General Description

The MAX96714/F/R deserializers convert a GMSL™2/1 input to MIPI CSI-2 output. The devices allow a simultaneously transmit bidirectional control channel while forward video transmissions are in progress. The MAX96714/F/R operate at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in the reverse direction.

Data can be transmitted over low-cost 50Ω Coax or 100Ω STP cables that meet the GMSL2 channel specifications.

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, 105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at 105°C (m)**		
3Gbps/187.5Mbps	20	10	11
6Gbps/187.5Mbps	13	7	6.3

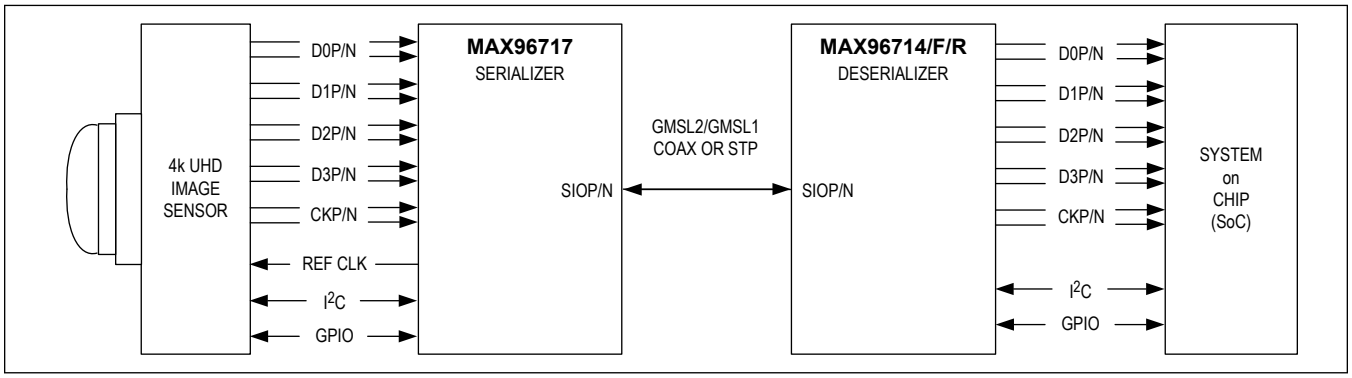
Applications

- Advanced Driver Assistance Systems (ADAS)
- Forward Vision Camera Systems (FVC)
- Rear View Camera (RVC)
- Driver-Monitor Systems (DMS)

Benefits and Features

- Automotive Grade High-Speed Link
  - -18dB at 3GHz (6Gbps) Max Insertion Loss
  - -19.5dB at 1.5GHz (3Gbps) Max Insertion Loss
  - Auto Adapt for Changes in Channel Conditions
  - Operates -40°C to +105°C Ambient
- Single GMSL Input Can Support up to 8MP Imagers
  - 6/3Gbps in GMSL2 Forward Link-Rates
  - 3.12Gbps in GMSL1 Forward Link-Rates
  - 187.5Mbps/1Mbps (GMSL2/1) Reverse Link-Rates
- High-Speed 1x4-lane MIPI Output Port, CSI-2 v1.3
  - MIPI D-PHY v1.2 Rated at 2.5Gbps/Lane
  - Polarity Flip and Data-Lane Reassignment
  - Supports 16 Virtual Channels
- Bidirectional Reverse Channel Supports
  - Nine Configurable GPIOs
  - 1 x I^2C/UART Ports, up to 1MHz
  - 2 x Pass-Through I^2C/UART
- Reduces BOM and Space Savings
  - Tiny 5mm x 5mm TQFN Standard and Side-Wettable
  - Industry's Smallest Power over Coax (PoC)
- RoR for Crystal-Free Operation on Serializers
- ASIL-B Compliant in GMSL2 Mode (MAX96714/F)
- Supports ASIL-B(D) Decomposition (MAX96714/F)
- MAX96714: 6Gbps, GMSL2, ASIL-B
- MAX96714F: 3Gbps, GMSL2, ASIL-B
- MAX96714R: 3Gbps, GMSL2, QM, I^2C Only

Simplified Application Circuit and Block Diagram



Ordering Information appears at end of data sheet.

19-101134; Rev 2; 6/23

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Absolute Maximum Ratings

(All voltages with respect to ground) .....

V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
V_{TERM} ..... -0.3V to +1.32V
CAP_VDD ..... -0.3V to +1.2V
SIO_(Active State) (Note 1)..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ (Inactive State) (Note 1)..... -0.3V to +1.1V
D-PHY Pins (Note 2)..... -0.3V to (V_{TERM} + 0.1V)
XRES, X2..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (Note 3)..... -0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation (Note 4).....1896mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (Reflow).....+260°C

Note 1: Active State means the device is powered up and not in power-down modes. Inactive means the device is not powered up or powered up in power-down mode.

Note 2: Specified maximum voltage or 1.36V, whichever is lower.

Note 3: Specified maximum voltage or 3.9V, whichever is lower.

Note 4: Derate 34.5mW/°C above T_A = +70°C. Maximum dissipation is determined using specified θ_{JA} and assuming maximum acceptable die temperature of 125°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN-SW (Side-Wettable)

Package Code	T3255Y+8
Outline Number	21-100156
Land Pattern Number	90-100067
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

32-Pin TQFN

Package Code	T3255+8
Outline Number	21-0140
Land Pattern Number	90-0013
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL SERIAL OUTPUTS (SEE Figure 1)							
Output Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%		190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage		380	500	620	mV
Change in V_{OD} between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state		V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$				25	mV
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CHANNEL SERIAL OUTPUTS							
Differential High Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODH}	Forward channel disabled. See Figure 2.	HIM disabled.	30		75	mV
			HIM enabled.	50		120	
Differential Low Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODL}	Forward channel disabled. See Figure 2.	HIM disabled.	-75		-30	mV
			HIM enabled.	-120		-50	
Single-Ended High-Output Peak Voltage	V_{ROSH}	Forward channel disabled.	HIM disabled.	30		75	mV
			HIM enabled.	50		120	
Single-Ended Low-Output Peak Voltage	V_{ROSL}	Forward channel disabled.	HIM disabled.	-75		-30	mV
			HIM enabled.	-120		-50	
Differential Output Offset Voltage ($V_{(SIO\_P)}$ + $V_{(SIO\_N)}$)/2	V_{DOS}			V_{DD18} - 0.3		V_{DD18}	V
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / D-PHY LP TRANSMITTER							
High-Level Output Voltage	V_{OH}			0.95	1.2	1.3	V
Low-Level Output Voltage	V_{OL}			-50		50	mV
Output Impedance	Z_{OLP}			110			Ω
DC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER							
HS Transmit Static Common-Mode Voltage	V_{CMTX}	See Figure 3.		150	200	250	mV
V_{CMTX} Mismatch When Output is Differential-1 or Differential-0	$\lvert \Delta V_{CMTX(1,0)} \rvert$	$\Delta V_{CMTX(1,0)}$ = ($V_{CMTX(1)}$ - $V_{CMTX(0)}$)/2 See Figure 4.				5	mV

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HS Transmit Differential Voltage	$\|V_{OD}\|$	See Figure 3.	140	200	270	mV
V_{OD} Mismatch When Output is Differential-1 or Differential-0	$\|\Delta V_{OD}\|$	See Figure 4.			14	mV
HS Output High Voltage	V_{OHHS}				360	mV
Single-Ended Output Impedance	Z_{OS}		40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				15	%
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistor	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Pulldown Resistance	R_{PD}				1		MΩ
Input Capacitance	C_{IN}				3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS							
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA		V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE FAULT DETECTION INPUT (SEE Figure 35 for STP and Coax configurations)							
Open Pin Voltage	V_{O0}	LMN0			1.25		V
	V_{O1}	LMN1			0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)							
X1 Input Capacitance	C_{IN_X1}				3		pF
X2 Input Capacitance	C_{IN_X2}				1		pF
Internal X2 Limit Resistor	R_{LIM}				1.2		kΩ
Internal Feedback Resistor	R_{FB}				10		kΩ
Transconductance	g_m				28		mA/V
DC ELECTRICAL CHARACTERISTICS / DO NOT USE WITH RoR - REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)							
High-Level Input Voltage	V_{IH}			0.9			V
Low-Level Input Voltage	V_{IL}					0.4	V
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				3		pF
DC ELECTRICAL CHARACTERISTICS / GMSL2 POWER SUPPLY CURRENT							
Supply Current	I_{DD}	6Gbps link, 5.2Gbps video payload, PRBS24, four data lanes, 1.3Gbps per lane.(MAX96714)	V_{DD} = 1.0V		120	260	mA
			V_{DD} = 1.2V		124	250	
			V_{DD18} = 1.8V		115	158	
			V_{TERM} = 1.2V		14	25	
		3Gbps link, 2.4Gbps video payload, PRBS24, four data lanes, 600Mbps per lane.(MAX96714F/R)	V_{DD} = 1.0V		78	220	
			V_{DD} = 1.2V		80	210	
			V_{DD18} = 1.8V		114	155	
			V_{TERM} = 1.2V		14	22	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL1 POWER SUPPLY CURRENT							
Supply Current	I_{DD}	3.12Gbps link, 2.5Gbps video payload, RGB888 color bar pattern, four data lanes, 600Mbps per lane, High-Bandwidth Mode.	V_{DD} = 1.0V		50	190	mA
			V_{DD} = 1.2V		55	180	
			V_{DD18} = 1.8V		60	82	
			V_{TERM} = 1.2V		14	22	
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DDIO} at 3.6V	T_A = 25ºC		6		µA
			T_A = 105ºC		6		
		V_{TERM} at 1.26V	T_A = +25°C		1		
			T_A = +105°C		1		
		V_{DD18} at 1.9V	T_A = 25ºC		1		
			T_A = 105ºC		10		
		V_{DD} at 1.26V	T_A = 25ºC		1		
			T_A = 105ºC		1		
AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL SWITCHING CHARACTERISTICS							
Lock Time	t_{LOCK2}	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. (*Note 9*, *Note 9*)			31		ms
	t_{LOCK}	MAX96714R: From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. (*Note 9*, *Note 10*)			20		
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packets at SIO_ to valid packets at the CSI-2 output (assumes link locked and registers configured and frame filter is disabled).			0.1ms + (6600 x T_{PCLK})		ms
Maximum Video Latency	t_{VL}	Time from the first pixel in a GMSL2 packet at SIO_ to the first pixel in the CSI-2 output packet. See Figure 5.			1 video line + (128 x T_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.			1		ms
AC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL SERIAL OUTPUTS (SIOP, SION)							
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω			2300		ps
Total Serial Output p-p Jitter	t_{TSOJ}	PRBS7, single-ended or differential output.			0.15		UI
Deterministic Serial Output p-p Jitter	t_{DSOJ}	PRBS7, single-ended or differential output.			0.1		UI

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPI-GPO Delay Reverse Path	t_{GPDR}	Delay-compensated mode See Figure 16.		15		µs
		Non-delay-compensated mode See Figure 16.		6		
GPI-GPO Skew Reverse Path	t_{SKEW}	Delay-compensated mode, between GPI-GPO within a single link or link-to-link See Figure 16.		7		ns
AC ELECTRICAL CHARACTERISTICS / GMSL1 SWITCHING CHARACTERISTICS						
Maximum Lock Time	t_{LOCK1}	See Figure 6.		4		ms
Maximum Power-up Delay	t_{PU}	See Figure 7.		19.5		ms
		See Figure 7.		8.5		
Maximum Video Latency	t_{VL}	Time from the first pixel in a video line at SIO_ to the first pixel in the CSI-2 output packet. See Figure 8.		1 video line + (128 x T_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.		1		µs
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included). See Figure 9. (*Note 7*)			350	µs
AC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz, See Figure 4. (*Note 6*)			15	mV_{RMS}
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50MHz to 450MHz, See Figure 4. (*Note 6*)			25	mV_{PEAK}
20% to 80% Rise Time and Fall Time	t_R and t_F	(*Note 6*)			0.4	UI
		(*Note 6*)	50			ps
TX Differential Return Loss	Sdd_{TX}	f_{MAX} = 1.25GHz		-10		dB
		f_{MAX} = 1.875GHz		-8		
TX Common-Mode Return Loss	Scc_{TX}	f_{MAX} = 1.875GHz		-7		dB
Data Lane Bit Rate	DL_{BR}		80		2500	Mbps
Clock Lane Frequency	CL_{FREQ}		40		1250	MHz
CSI-2 Output Inter-Packet Spacing	t_{SPACE}			300ns + 370UI		ns
AC ELECTRICAL CHARACTERISTICS / D-PHY LP TRANSMITTER (*Note 7*)						
15% to 85% Rise Time and Fall Time	T_{RLP}/T_{FLP}	(*Note 8*)			25	ns
30% to 85% Rise Time	T_{REOT}	See Figure 12 and Figure 14. (*Note 8*)			35	ns
Load Capacitance	C_{LOAD}	(*Note 7*)	0		70	pF
AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING (*Note 6*)						
UI Instantaneous	UI_{INST}		0.4		12.5	ns

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UI Variation	ΔUI	UI ≥ 1ns within a single burst	-10%		10%	UI
		0.667ns ≤ UI ≤ 1ns within a single burst	-5%		5%	
Data to Clock Skew	T_{SKEW}	0.08Gbps to 1.0Gbps, See Figure 11.	-0.15		0.15	UI_{INST}
		> 1.0Gbps to 1.5Gbps, See Figure 11.	-0.2		0.2	
Static Data to Clock Skew (TX)	T_{SKEW} Static	> 1.5Gbps, See Figure 11.	-0.2		0.2	UI_{INST}
Dynamic Data to Clock Skew (TX)	T_{SKEW} Dynamic	> 1.5Gbps, See Figure 11.	-0.15		0.15	UI_{INST}
AC ELECTRICAL CHARACTERISTICS / D-PHY GLOBAL OPERATION TIMING (*Note 6*)						
Time the HS Clock must be Driven by the Transmitter Prior to Any Associated Data Lane Beginning the Transition from LP to HS Mode	$T_{CLK-PRE}$	See Figure 13.	8			UI
Time the Transmitter Drives the Clock Lane LP-00 Line State Immediately before the HS-0 Line State Starting the HS Transmission	$T_{CLK\_PREPARE}$	See Figure 13.	38		95	ns
$T_{CLK-PREPARE}$ + Time the Transmitter Drives the HS-0 State Prior to Starting the Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	See Figure 13.	300			ns
Transmitted Time Interval from the Start of $T_{HS-TRAIL}$ to the Start of the LP-11 State Following an HS Burst	T_{EOT}	See Figure 12, Figure 13, and Figure 14.			105 + 12xUI	ns
Time the Transmitter Drives LP-11 Following an HS Burst	$T_{HS-EXIT}$	See Figure 12, Figure 13, and Figure 14.	100			ns
Time the Transmitter Drives the Data Lane LP-00 Line State Immediately before the HS-0 Line State Starting the HS Transmission	$T_{HS-PREPARE}$	See Figure 12, Figure 13, and Figure 14.	40 + 4xUI		85 + 6xUI	ns
$T_{HS-PREPARE}$ + Time the Transmitter Drives the HS-0 State Prior to Transmitting the Sync Sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	See Figure 12 and Figure 14.	145 + 10xUI			ns

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time the Transmitter Drives the Flipped Differential State after Last Payload Data Bit of a HS Transmission Burst	$T_{HS-TRAIL}$	See Figure 12 and Figure 14.	60 + 4xUI			ns
Initialization Time	T_{INIT}		100			µs
Transmitted Length of Any Low-Power State Period	T_{LPX}	See Figure 12, Figure 13, and Figure 14.	50			ns
Time the Transmitter Drives the Skew-Calibration Sync Pattern, 0xFFFF	$T_{SKEWCAL\_SYNC}$	See Figure 14.		16		UI
Time the Transmitter Drives the Skew-Calibration Pattern in the Initial Skew-Calibration Mode	$T_{SKEWCAL}$	See Figure 14.			100	µs
		See Figure 14.	2^{15}			UI
Time the Transmitter Drives the Skew-Calibration Pattern in the Periodic Skew-Calibration Mode	$T_{SKEWCAL}$	See Figure 14.			10	µs
		See Figure 14.	2^{10}			UI
AC ELECTRICAL CHARACTERISTICS / I²C/UART PORT TIMING (MAX96714/MAX96714F)						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO}	20 x V_{DDIO}/5.5V		150	ns
I²C/UART Wake Time	t_{WAKEUP}	From power-up, or rising edge of PWDNB to local register access. For remote register access, I²C/UART Wake Time is the same as lock time ($t_{LOCK\_}$).		12.25		ms
AC ELECTRICAL CHARACTERISTICS / I²C PORT TIMING (MAX96714R)						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO}	20 x V_{DDIO}/5.5V		150	ns
I²C Wake Time	t_{WAKEUP}	From power-up, or rising edge of PWDNB to local register access. For remote register access, I²C Wake Time is the same as lock time (t_{LOCK}).		2.25		ms
AC ELECTRICAL CHARACTERISTICS / I²C TIMING (SEE Figure 15)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range	9.6		100	kHz
		Mid f_{SCL} range	100		400	
		High f_{SCL} range	400		1000	

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load on Each Bus Line	C_B				100	pF
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2) (*Note 6*)						
Frequency	f_{XTAL}			25		MHz

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) *Note 5Note 5Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED) (*Note 6*) **External Oscillator cannot be used while operating in RoR Mode**						
Frequency	F_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}		-200		+200	ppm
Duty Cycle	DC		40	50	60	%
Input Jitter	t_{JIN}	Forward data rate = 6/3Gbps Reverse data rate = 187.5Mbps Sinusoidal jitter < 1MHz (rising edge)			150	ps (p-p)
Input Rise Time	t_R	10% to 90%		5		ns
Input Fall Time	t_F	90% to 10%		5		ns

Note 5: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 6: Not production tested. Guaranteed by design and characterization.

Note 7: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

Note 8: Additional 60pF at Rx termination center tap.

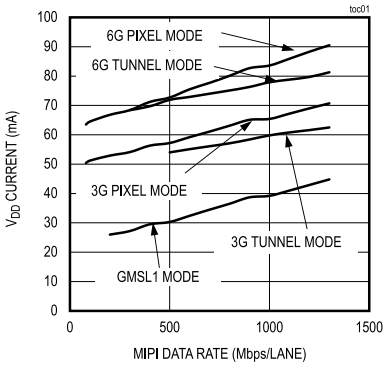
Note 9: Production tested using ECS ECS-250-18-33Q-DS crystal.

Note 10: From power-up, release of RESET_LINK, or rising edge of the PWDNB pin, to rising edge of the LOCK pin. t_{RD} must be < 90ms if serializer powers up or is released from link reset before deserializer. For more information, see the *GMSL2 Link Lock* section.

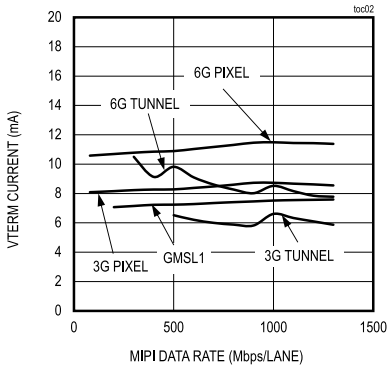
Typical Operating Characteristics

(V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C unless otherwise noted.)

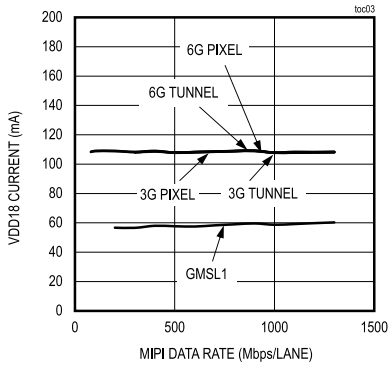
V_{DD} CURRENT vs MIPI DATA RATE



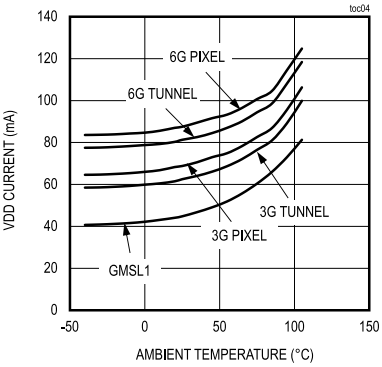
V_{TERM} CURRENT vs MIPI DATA RATE



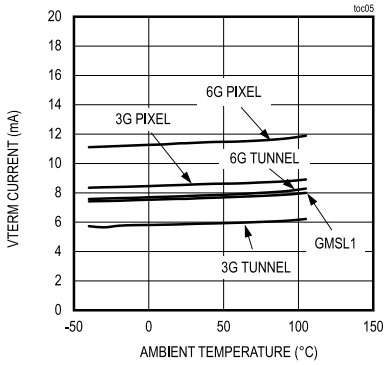
V_{DD18} CURRENT vs MIPI DATA RATE



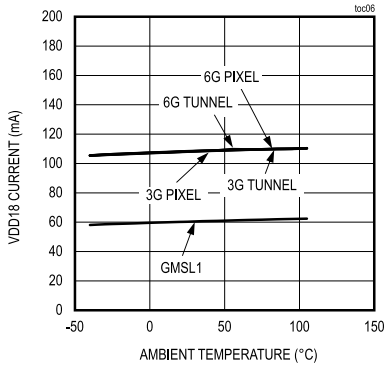
V_{DD} CURRENT vs TEMPERATURE



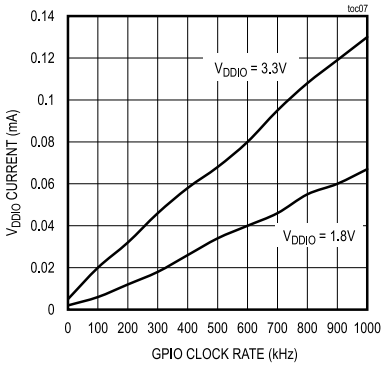
V_{TERM} CURRENT vs TEMPERATURE



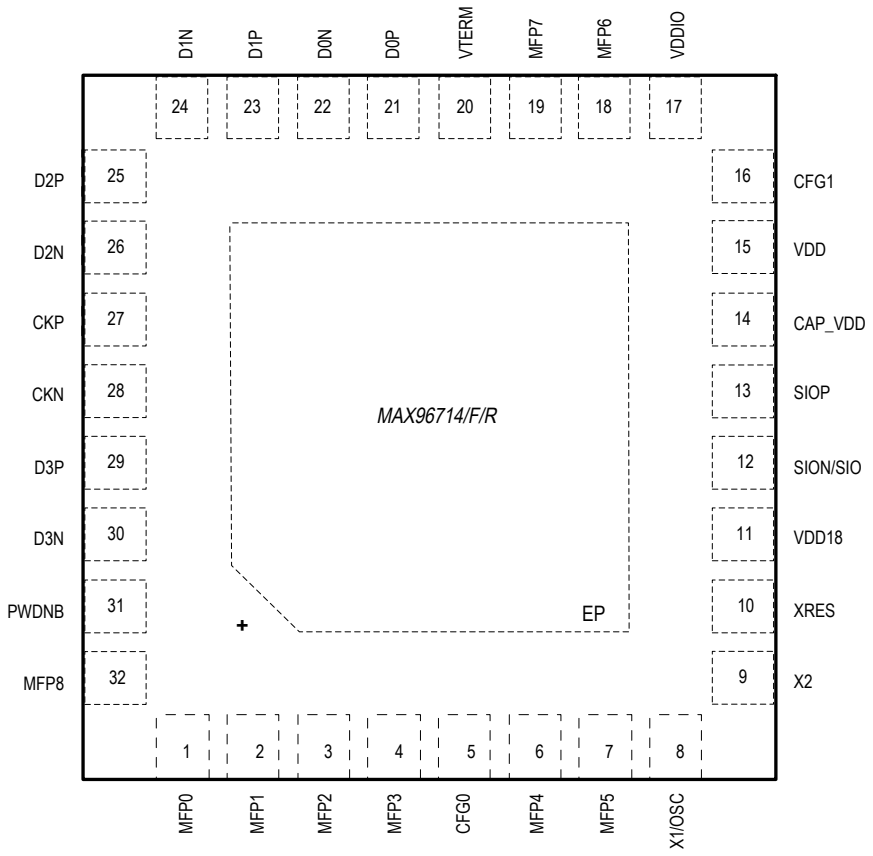
V_{DD18} CURRENT vs TEMPERATURE



V_{DDIO} CURRENT vs GPIO CLOCK SPEED (ONE PUSH-PULL GPIO, 27pF LOAD)



Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION MODE			FUNCTION
		MAX96714/F	MAX96714R	GMSL1	
SERIAL I/O					
12	SION/SIO	SION SIO	SION SIO	SION SIO	SION: Inverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration. SIO: Coax Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
13	SIOP	SIOP	SIOP	SIOP	SIOP: Noninverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
CSI-2 PORT					
21	D0P	D0P	D0P	D0P	Data Lane 0 Noninverted Output
22	D0N	D0N	D0N	D0N	Data Lane 0 Inverted Output

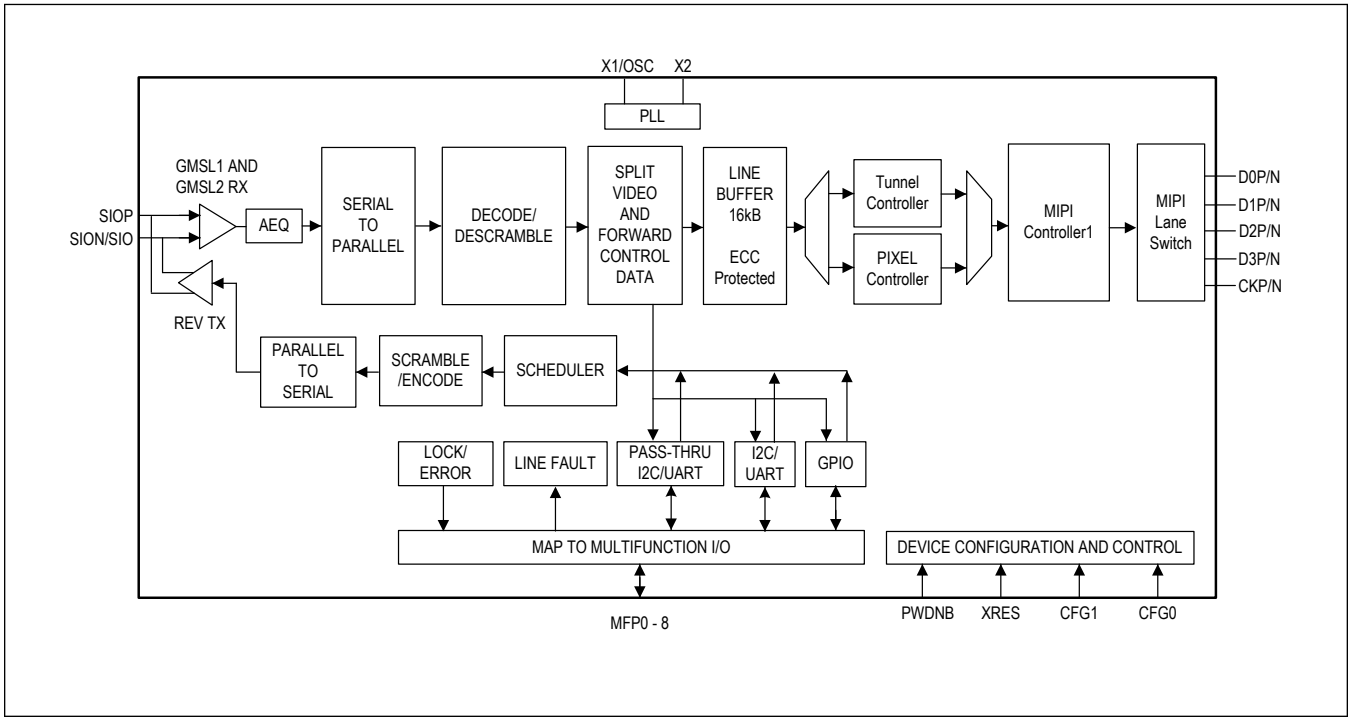
PIN	NAME	FUNCTION MODE			FUNCTION
		MAX96714/F	MAX96714R	GMSL1	
23	D1P	D1P	D1P	D1P	Data Lane 1 Noninverted Output
24	D1N	D1N	D1N	D1N	Data Lane 1 Inverted Output
25	D2P	D2P	D2P	D2P	Data Lane 2 Noninverted Output
26	D2N	D2N	D2N	D2N	Data Lane 2 Inverted Output
27	CKP	CKP	CKP	CKP	Clock Lane Noninverted Output
28	CKN	CKN	CKN	CKN	Clock Lane Inverted Output
29	D3P	D3P	D3P	D3P	Data Lane 3 Noninverted Output
30	D3N	D3N	D3N	D3N	Data Lane 3 Inverted Output
MULTIFUNCTION PINS see Table 5 for more info.					
1	MFP0	MS VS FSYNC_OUT DE/DV GPIO0*	MS VS FSYNC_OUT DE/DV GPIO0*	MS VS FSYNC_IN/ OUT DE/DV CNTL1 GPIO0**	MS: UART Mode Select with 1MΩ Pulldown to Ground. Set MS low to select base mode. Set MS high to select bypass mode. MS state can also be temporarily overwritten by a register write. VS: Video Stream Vertical Sync Monitor Push-Pull Output. FSYNC_OUT: Frame Sync Push-Pull Output. DE/DV: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. GPIO0: Configurable General-Purpose Input or Output. Power-up default is GPI0 (general-purpose input) with a 1MΩ pulldown to ground. FSYNC_IN/OUT: Frame Sync Input with 1MΩ Pulldown to Ground or Frame Sync Push-Pull Output. CNTL1: Control 1 Push-Pull Output.
2	MFP1	SDA1 RX1* SDA2 RX2 GPIO1	GPIO1	CNTL3 GPI** GPIO1	SDA1: Pass-Through I^2C Data Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO}. RX1: Pass-Through UART Input with 40kΩ Pullup to V_{DDIO} (Default 1Mbps Rate). SDA2: Pass-Through I^2C Data Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO}. RX2: Pass-Through UART Input with 40kΩ Pullup to V_{DDIO}. GPIO1: Configurable General-Purpose Input or Output. CNTL3: Control 3 Push-Pull Output. GPI: General-Purpose Input with 40kΩ Pulldown to V_{DDIO}.

PIN	NAME	FUNCTION MODE			FUNCTION
		MAX96714/F	MAX96714R	GMSL1	
3	MFP2	SCL1 TX1* SCL2 TX2 MS FSYNC_OUT GPIO2	FSYNC_OUT GPIO2	MS FSYNC_IN/ OUT CNTL4 GPIO2**	SCL1: Pass-Through I^2C Clock Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO}. TX1: Pass-Through UART Open-Drain Output with 40kΩ Pullup to V_{DDIO} (Default 1Mbps Rate). SCL2: Pass-Through I^2C Clock Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO}. TX2: Pass-Through UART Open-Drain Output with 40kΩ Pullup to V_{DDIO}. MS: UART Mode Select with 1MΩ Pulldown to Ground. Set MS low to select base mode. Set MS high to select bypass mode. MS state can also be temporarily overwritten by a register write. FSYNC_OUT: Frame Sync Push-Pull Output. GPIO2: General-purpose input or output. FSYNC_IN/OUT: Frame Sync Input with 1MΩ Pulldown to Ground or Frame Sync Push-Pull Output. CNTL4: Control 4 Push-Pull Output.
4	MFP3	SDA RX	SDA	SDA RX	SDA: I^2C Data Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO} RX: UART Input with 40kΩ Pullup to V_{DDIO}
6	MFP4	SCL TX	SCL	SCL TX	SCL: I^2C Clock Input/Open-Drain Output with 40kΩ Pullup to V_{DDIO} TX: UART Open-Drain Output with 40kΩ Pullup to V_{DDIO}
7	MFP5	LOCK VS DE/DV GPIO5	LOCK VS DE/DV GPIO5	LOCK VS DE/DV GPIO5	LOCK: Open-Drain Lock Indication Output with 40kΩ Pull-up to V_{DDIO}. VS: Video Stream Vertical Sync Monitor Push-Pull Output. DE/DV: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. GPIO5: Configurable General-Purpose Input or Output.
18	MFP6	LMN0 GPIO6	LMN0 GPIO6	LMN0 CNTL2 GPIO6	LMN0: Line Fault Monitor Input. GPIO6: Configurable General-Purpose I/O. Power-up default is GPI6 with 1MΩ pulldown to ground CNTL2: Control 2 Push-Pull Output.
19	MFP7	LMN1 GPIO7	LMN1 GPIO7	LMN1 CNTL0 GPIO7	LMN1: Line Fault Monitor Input. GPIO7: Configurable General-Purpose I/O. Power-up default is GPI7 with 1MΩ pulldown to ground CNTL0: Control 0 Push-Pull Output.
32	MFP8	ERRB GPIO8	ERRB GPIO8	ERRB GPIO8	ERRB: Open-Drain Error Indication Output with 40kΩ Pullup to V_{DDIO}. ERRB low indicates an error has been detected GPIO8: Configurable General-Purpose I/O
MISCELLANEOUS - See Table 2					
5	CFG0	CFG0	CFG0	CFG0	Configuration Pin. Voltage is latched at power-up. See Table 8.

PIN	NAME	FUNCTION MODE			FUNCTION
		MAX96714/F	MAX96714R	GMSL1	
8	X1/OSC	X1/OSC	X1/OSC	—	Crystal/Oscillator Input. Connect 25MHz crystal. If an oscillator is used, connect to X1
9	X2	X2	X2	—	Crystal Input: Connect other terminal of 25MHz crystal. If an oscillator is used, leave X2 floating.
10	XRES	XRES	XRES	XRES	Connect a 402Ω ±1% resistor between XRES and ground.
14	CAP_VDD	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1.0V Core Supply.
16	CFG1	CFG1	CFG1	CFG1	Configuration Pin. Voltage is latched at power-up. See Table 9.
31	PWDNB	PWDNB	PWDNB	PWDNB	PWDNB: Active-low, Input with a 1MΩ pulldown to ground. Set low to enter power-down mode.
POWER SUPPLIES - SEE Table 2					
11	VDD18	VDD18	VDD18	VDD18	1.8V Analog Supply.
15	VDD	VDD	VDD	VDD	1.0V Core Supply. This pin includes an optional on-chip LDO. Connect a 0.95V to 1.05V supply to bypass LDO. Connect a 1.14V to 1.26V supply to use the internal 1.0V regulator. In order to use the internal 1V regulator, first write REG_ENABLE=1, and then write LDO_TEST=1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
17	VDDIO	VDDIO	VDDIO	—	1.8V to 3.3V I/O Supply.
20	VTERM	VTERM	VTERM	—	1.2V D-PHY Supply.
EP	EP	EP	EP	EP	Exposed pad: Connect to ground

Functional Diagrams

MAX96714/F/R



Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews, and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- **Errata sheets** contain deviations from published device specifications, and are specific to part number and revision ID.

Contact the factory to receive these documents, and for additional guidance on MAX96714/F/R features.

Table 1. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{TERM}		1.14	1.2	1.26	V
	V_{DD18}		1.7	1.8	1.9	
	V_{DD}	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	V_{DDIO}		1.7		3.6	
Operating Junction Temperature (T_J)			-40		125	°C

Table 2. External Component Requirements

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}	Connect R_{XRES} resistor between XRES pin and ground.		402 ±1%, use a single resistor	Ω
Line Fault Pulldown Resistor	R_{PD}	Connect R_{PD} to ground at far end of COAX/STP cable from active line fault detector; only required at side of link opposite active line fault detector.		49.9 ±1%	kΩ
Line Fault Series Resistor	R_{EXT}	Connect R_{EXT} between active LMN input(s) and GMSL interconnect; only required on side of link where line fault detectors are located.	LMN0 (STP)	42.2 ±1%	kΩ
			LMN0 (Coax)	48.7 ±1%	
			LMN1 (STP/ Coax)	48.7 ±1%	
Link Isolation Capacitors	C_{LINK}	Place close to the SIO_ pins (12, 13) used in the application.	GMSL2	0.1	µF
			GMSL1 HIM Enabled	0.1	
			GMSL1 HIM Disabled	0.22	
Termination Resistor for Unused Input in Coax Mode	R_{TERM}	Place close to the Link Isolation Capacitor for the unused input (SIOP) in Coax Mode. See Figure 35.		49.9 ±1%	Ω

Table 2. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
Crystal		Place as close as possible to pins 8 and 9.	25MHz ±200ppm	
Crystal Load Capacitors		Use loading capacitors guidance from the crystal manufacturer.		
V_{DDIO} Decoupling Capacitor*		Place a 10nF capacitor as close as possible to pin 17. Include a minimum of 10µF bulk decoupling on the PCB.		
V_{DD18} Decoupling Capacitor*		Place a 10nF capacitor as close as possible to pin 11. Include a minimum of 10µF bulk decoupling on the PCB.		
V_{TERM} Decoupling Capacitor*		Place a 10nF capacitor as close as possible to pin 20. Include a minimum of 10µF bulk decoupling on the PCB.		
V_{DD} Decoupling Capacitor*		Place a 10nF capacitor as close as possible to pin 15. Include a minimum of 10µF bulk decoupling on the PCB.		
CAP_VDD Decoupling Capacitor		Place a 10nF capacitor as close as possible to pin 14. Include a minimum of 10µF bulk decoupling near the pin.		
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction pin configurations.		
Resistors for Configuration Pin Resistor Divider	R1, R2	Place resistor divider close to pin 5 (CFG0).	Use ±1% See Table 8.	Ω
	R1, R2	Place resistor divider close to pin 16 (CFG1).	Use ±1% See Table 9.	Ω

* With the exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Table 3. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, CS = 100pF		±8		kV
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, CS = 150pF, Air Discharge		±6		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Figures

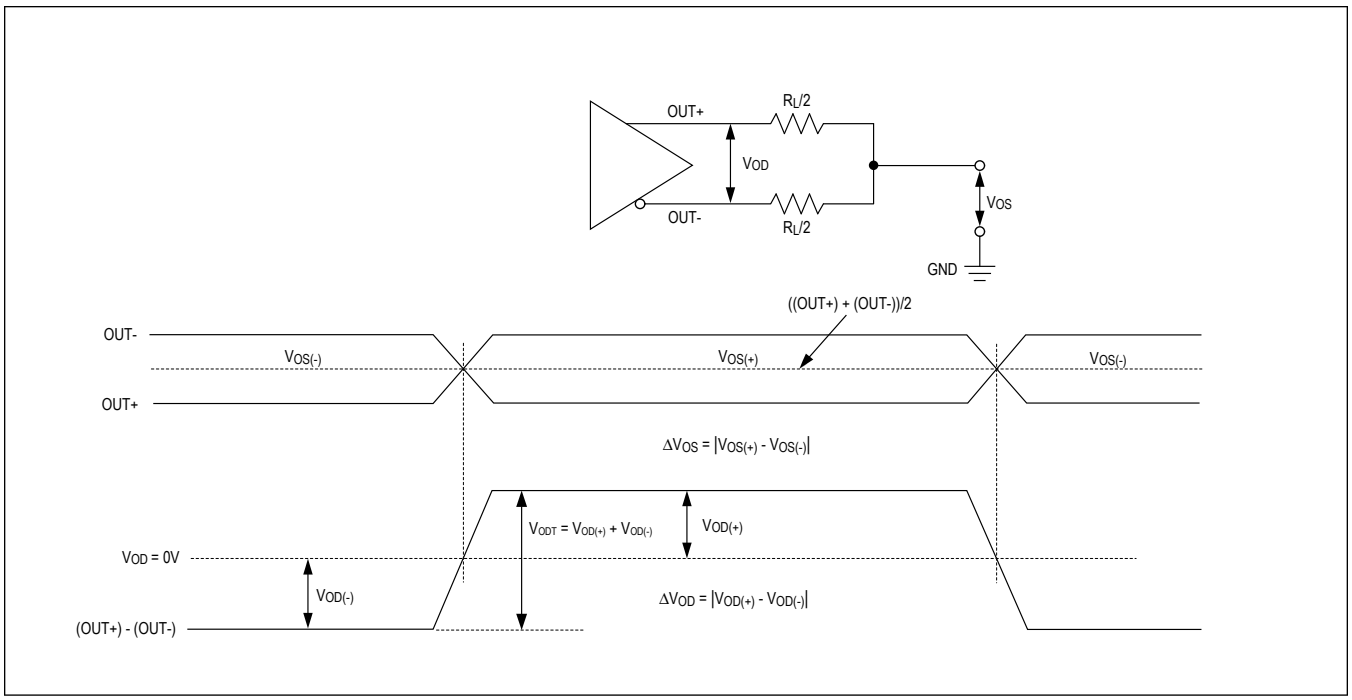


Figure 1. GMSL2 Reverse Channel Serial Outputs

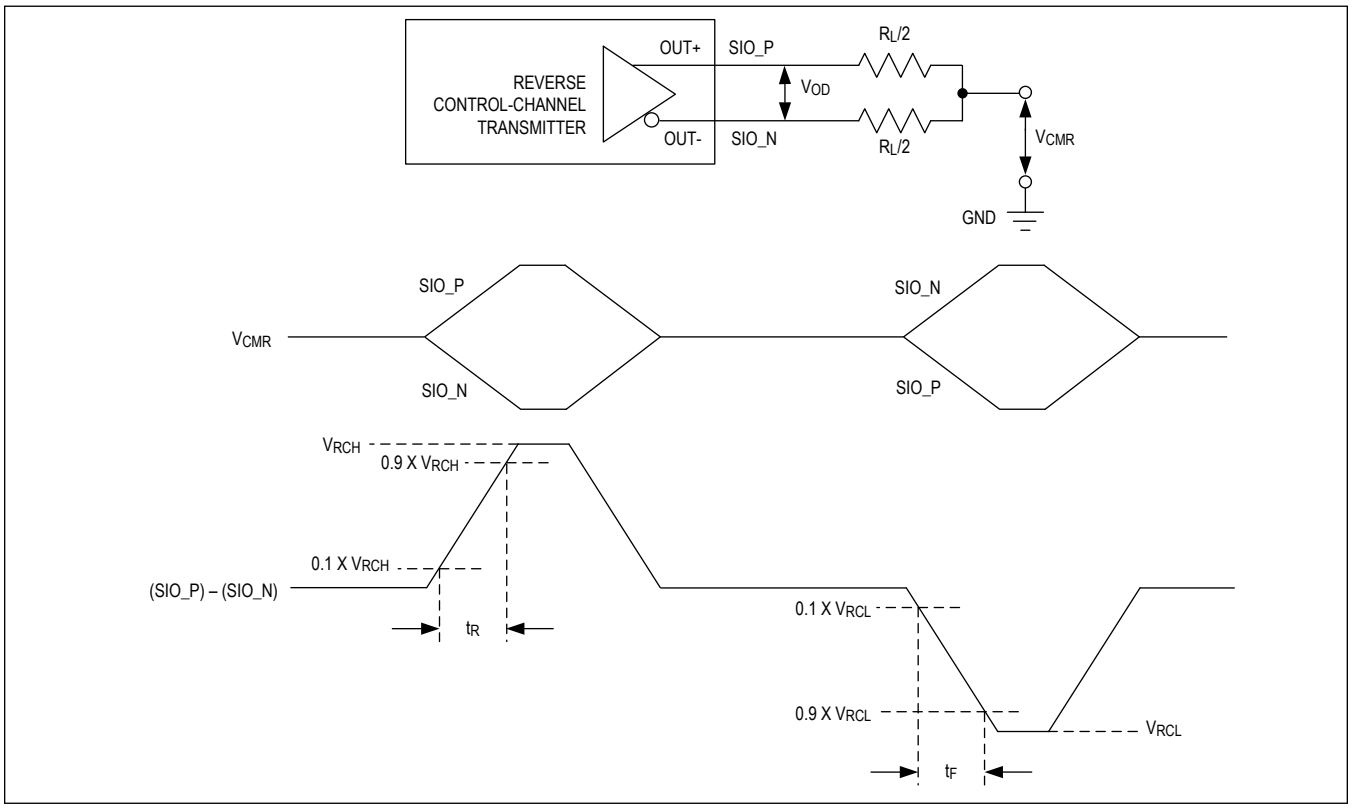


Figure 2. GMSL1 Reverse Channel Serial Outputs

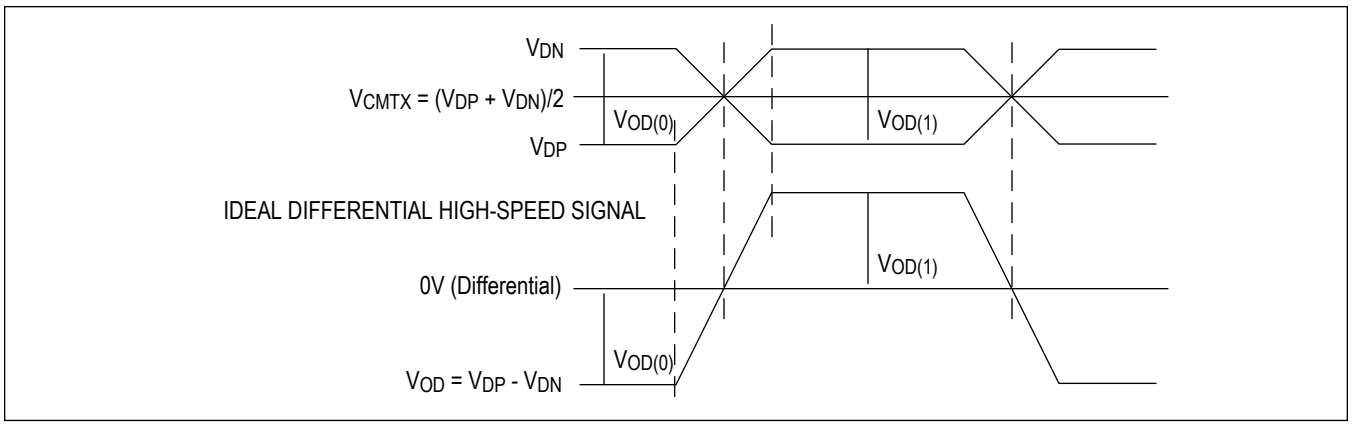


Figure 3. D-PHY Ideal Single-Ended and Resulting Differential HS Signals

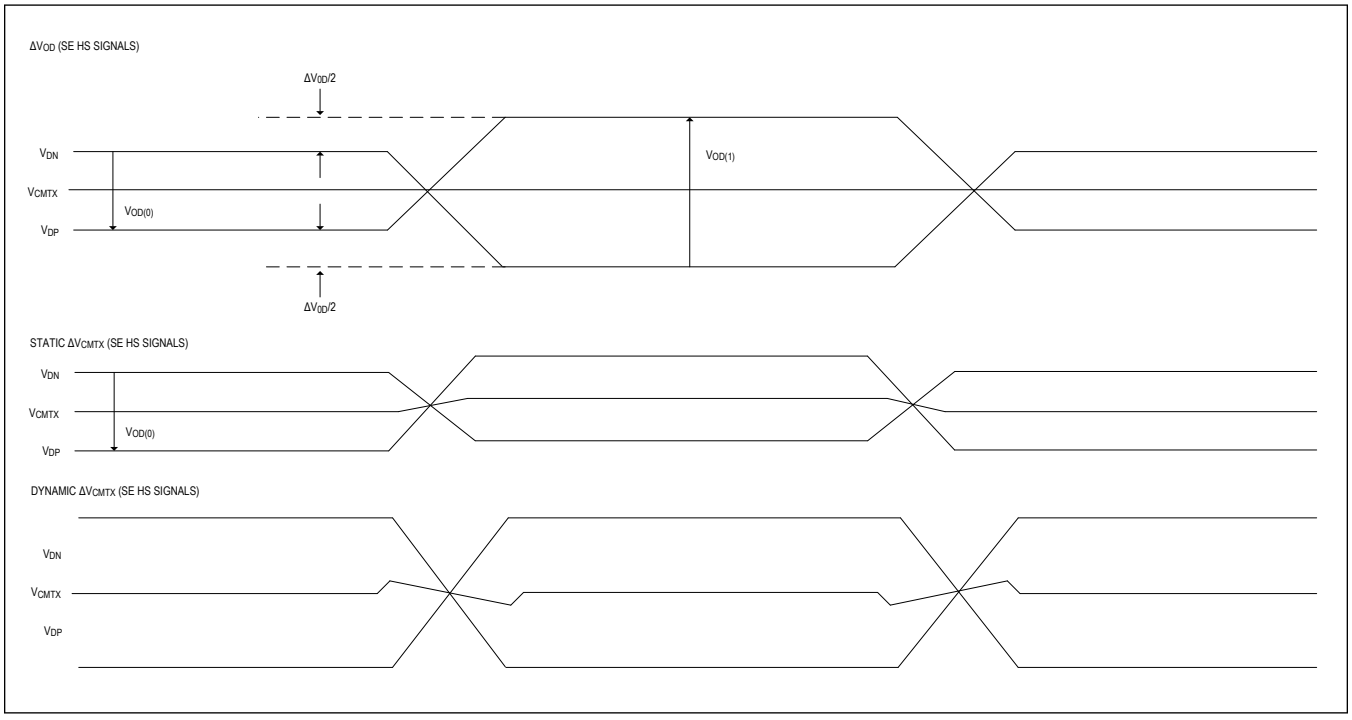


Figure 4. D-PHY Possible Delta V_{CMTX} and Delta V_{OD} Distortions of Single-Ended HS Signals

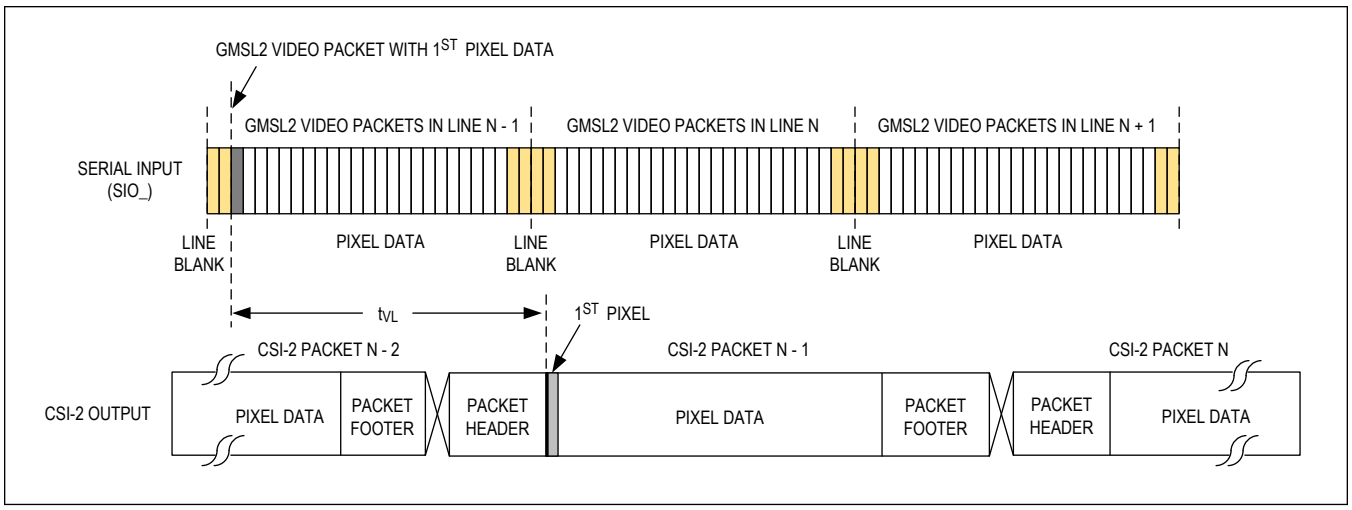


Figure 5. GMSL2 Video Latency

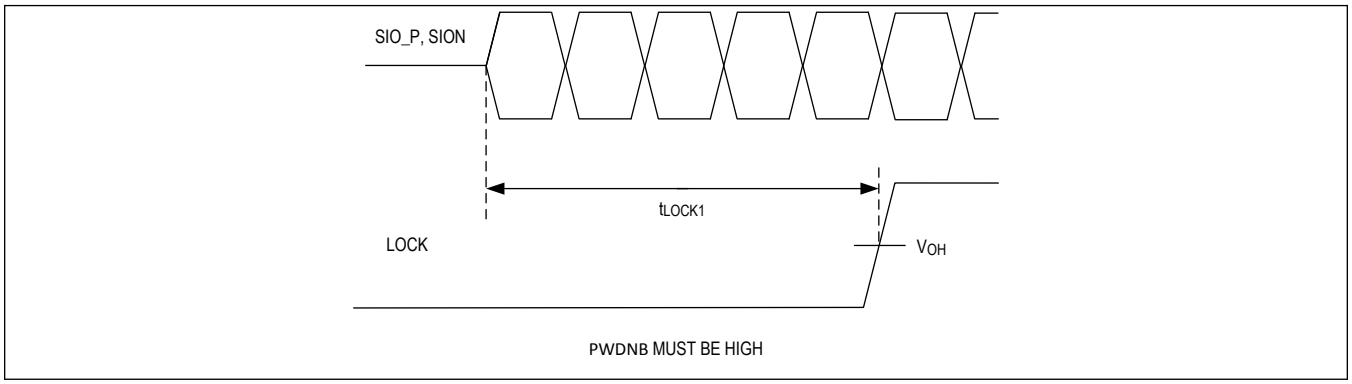


Figure 6. GMSL1 Lock Time

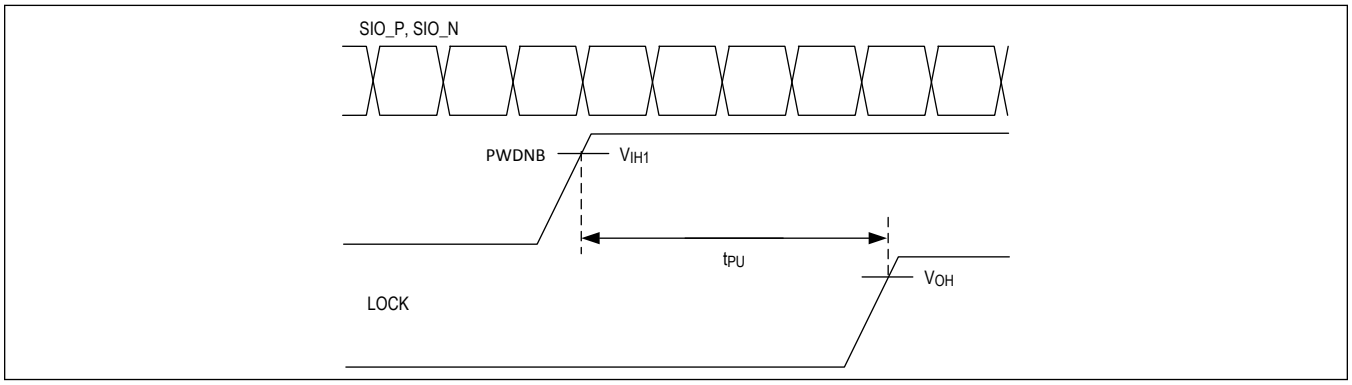


Figure 7. GMSL1 Power-Up Delay

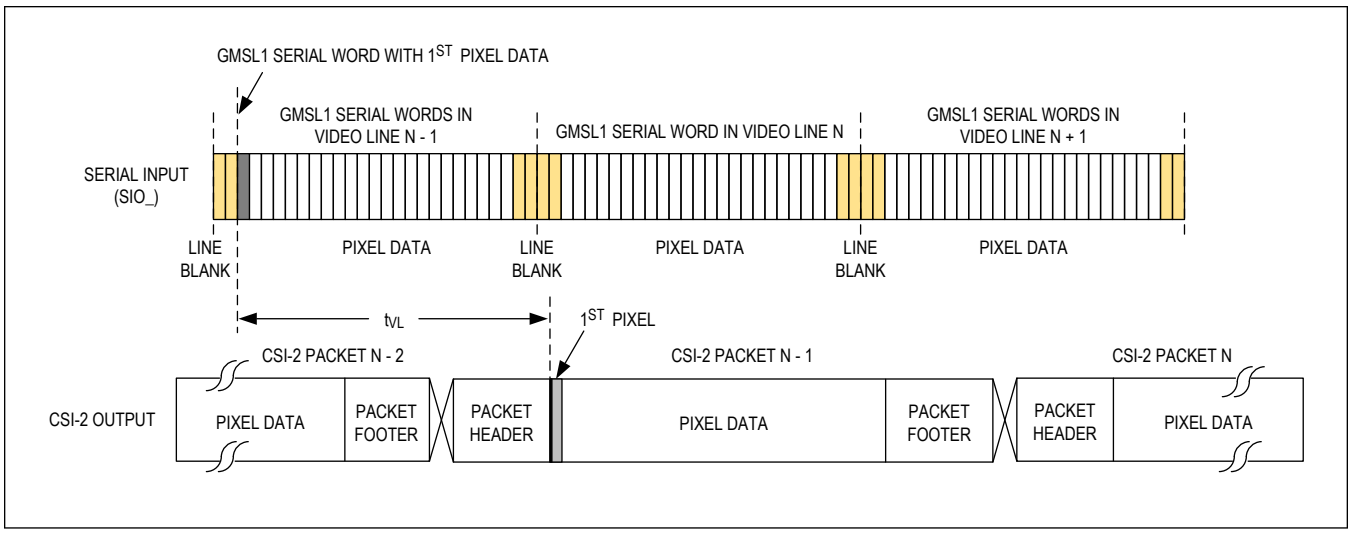


Figure 8. GMSL1 Video Latency

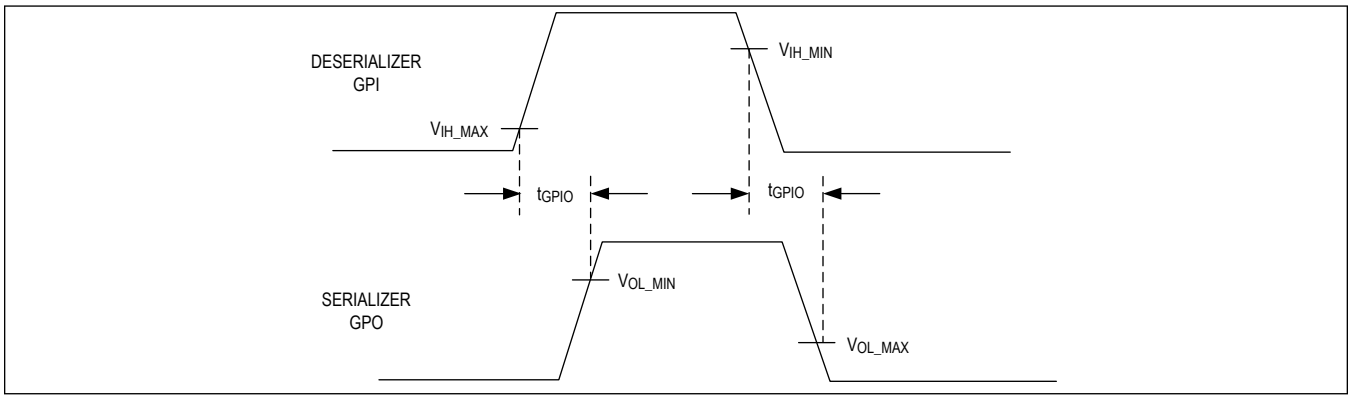


Figure 9. GSML1 GPI-to-GPO Delay

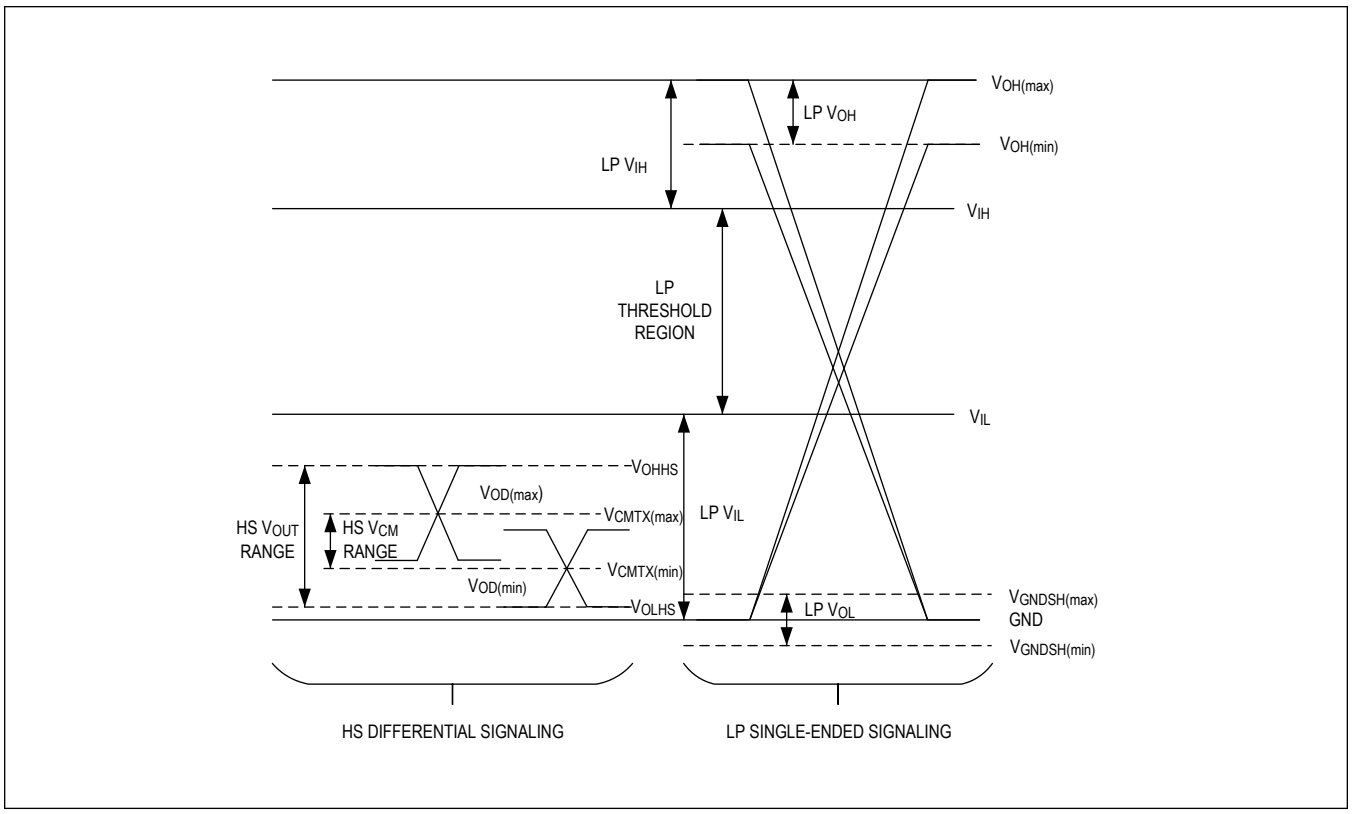


Figure 10. D-PHY Signaling Levels

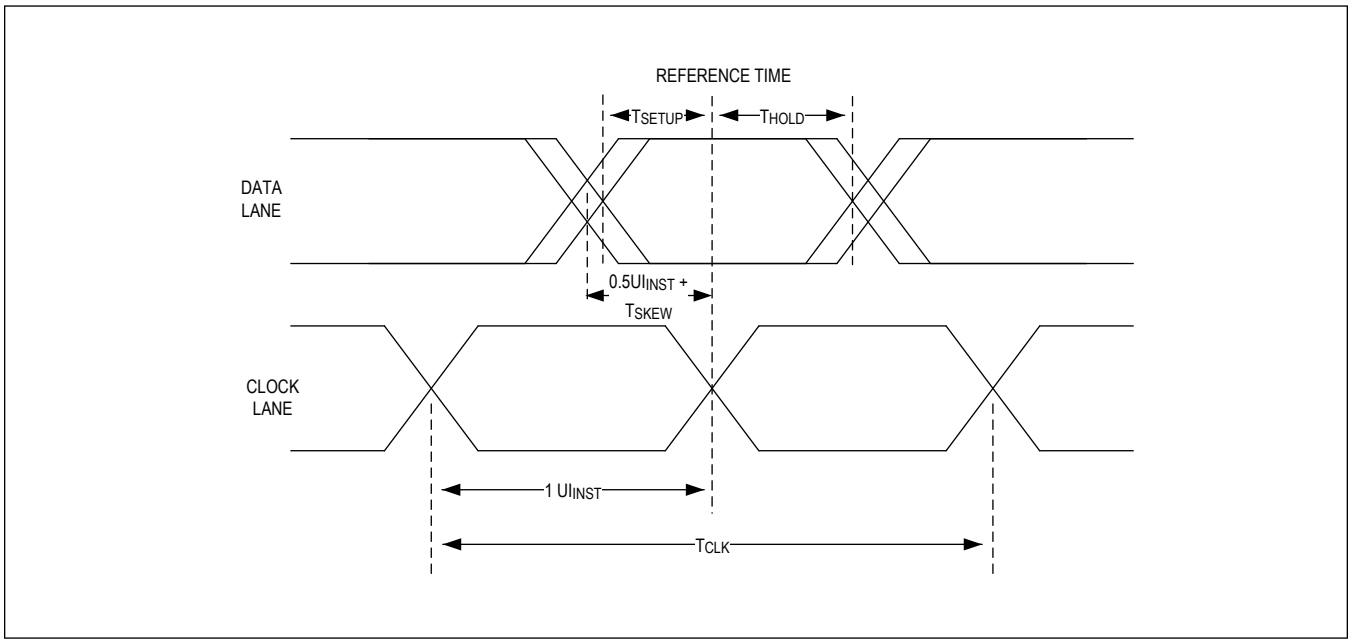


Figure 11. D-PHY Data Clock Timing

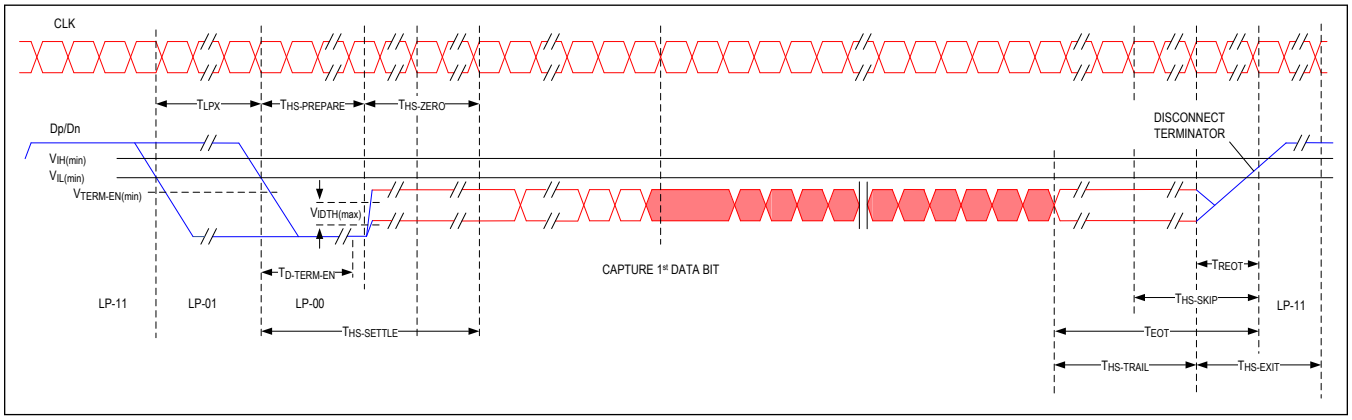


Figure 12. D-PHY Global Operation Timing (a)

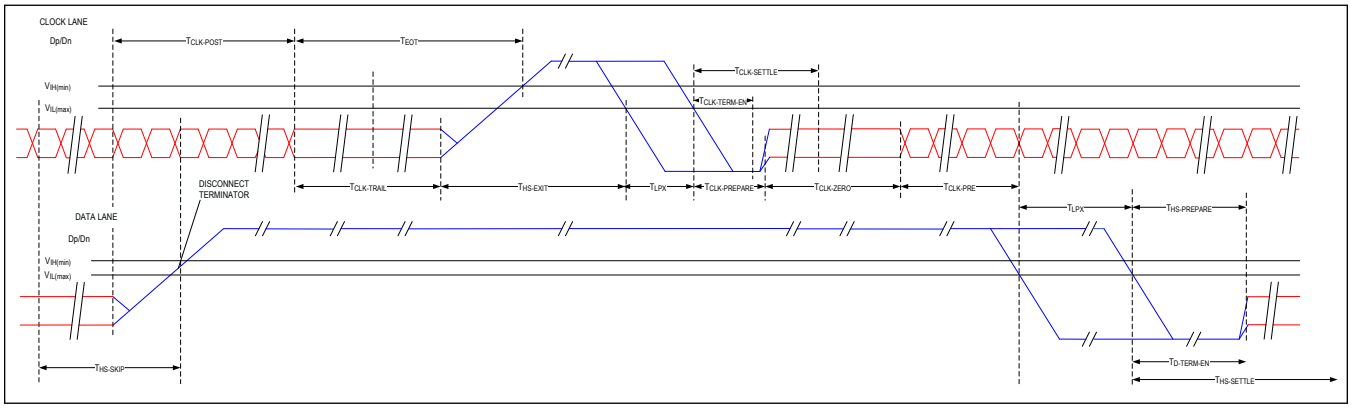


Figure 13. D-PHY Global Operation Timing (b)

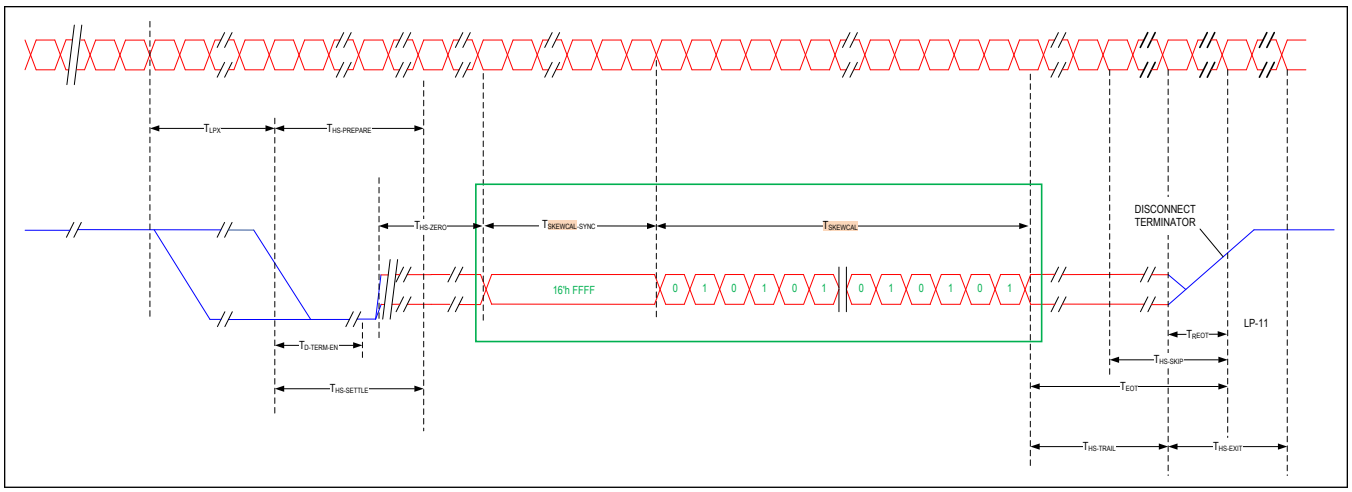


Figure 14. D-PHY High-Speed Skew Calibration

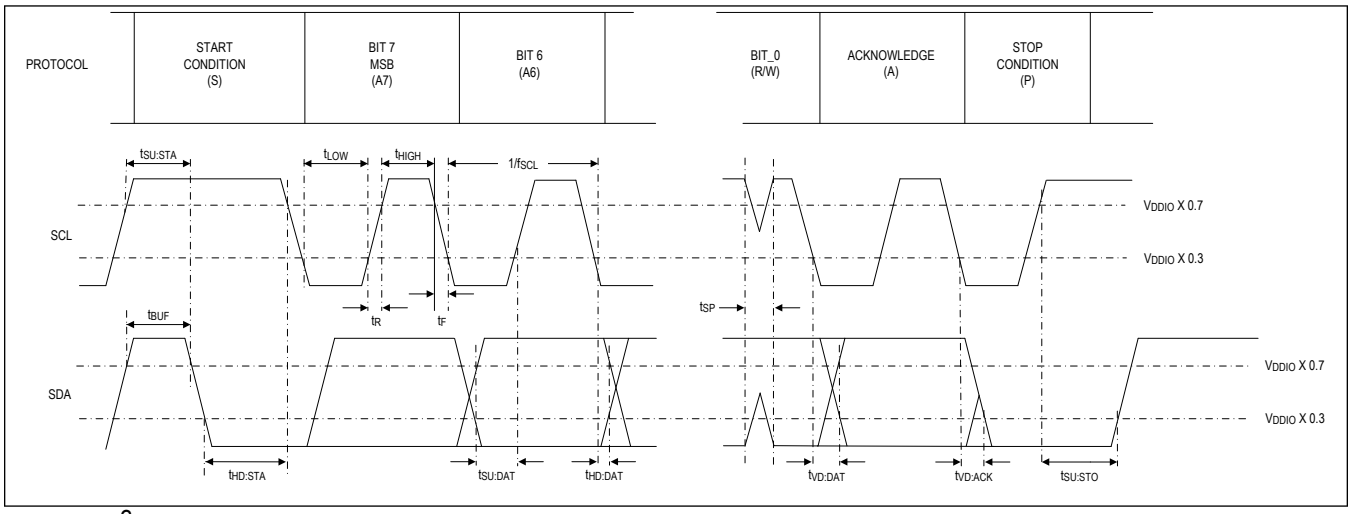


Figure 15. I^2C Timing Parameters

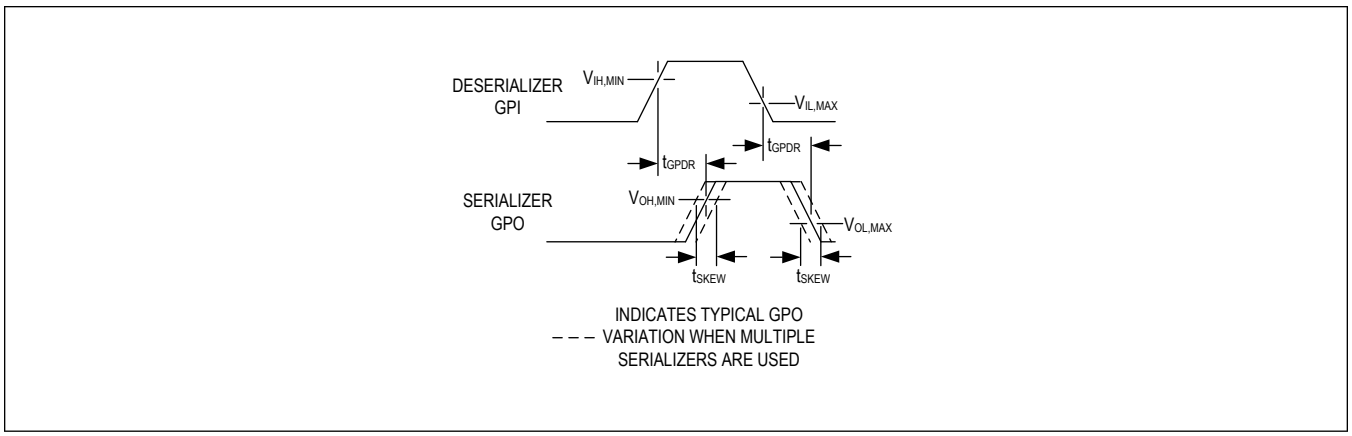


Figure 16. GMSL2 GPI-to-GPO Delay and Skew

Introduction

GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, bidirectional serial data transport. The MAX96714/F/R deserializers support two modes: the Pixel mode offers flexible and bandwidth-efficient data transfer, while the Tunnel mode provides end-to-end data integrity of both sensor data and side-channel data.

The MAX96714/F/R support up to 3Gbps or 6Gbps forward and 187.5Mbps reverse packetized data transmission over the fixed-speed link.

Product Overview

The MAX96714/F/R GMSL2 single-channel deserializers with GMSL1 backward compatibility connect to a serializer, which converts MIPI CSI-2 or parallel data to CSI-2 MIPI data output. It communicates to the serializer through the Control Channel using I^2C/UART. UART is not avaliable on the MAX96714R. The bidirectional data is communicated over low-cost 50Ω Coax or 100Ω STP cables that meet the GMSL2 channel specifications.

The MAX96714/F/R have a four-lane D-PHY v1.2 output port, which supports a data rate of 80Mbps to 2.5Gbps per lane. The MAX96714/F/R have four active D-PHY v1.2 lanes. The MAX96714/F/R support up to 16 virtual channels. In the Pixel mode, supported data types include RAW8/10/12/14/16/20, RGB565/666/888/YUV422 8-/10-bit, user-defined, EMB8, and generic long-packet data types. In the Tunnel mode, any CSI-2 data type is supported.

GMSL2/1 Block Diagram

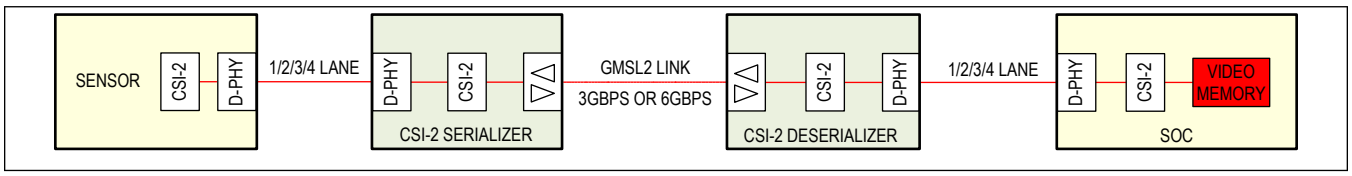


Figure 17. Single GMSL2 Link

The primary use-case is a single sensor with MIPI CSI-2 protocol and D-PHY output, as shown in Figure 17, with the sensor's output sent to an SoC in GMSL2 mode at a bit rate of 3Gbps or 6Gbps. The sensor data is output on the MAX96714/MAX96714F/MAX96714R CSI-2 port for capture by the SoC.

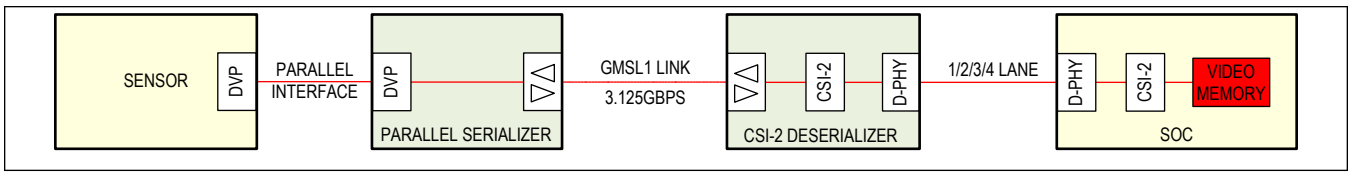


Figure 18. Single GMSL1 Link

GMSL2 Overview

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal/external oscillator. The link clock is not related to the video pixel clock beyond the natural constraint that the video bandwidth cannot exceed the available link bandwidth.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, the available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth. The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

GMSL2 provides a flexible broadband data link that can transport high-bandwidth bidirectional data between remotely located devices. The MAX96714/F/R are specifically designed to be an interface between a remotely located high-resolution camera or similar sensor. In addition to the core video/broadband streaming portion of the link, GMSL2 devices provide a variety of peripheral/auxiliary functions to enable flexible, robust system implementations.

GMSL2 provides extensive data integrity and safety features. Some of these features include CRC error detection that enables identification of errors in the video or control-data streams. In the case of control-channel CRC errors, automatic retransmission of the flagged packet maximizes control-channel speed and reliability. The internal video memory includes ECC protection to enable detection and correction of internally corrupted pixel data.

GMSL2 devices incorporate numerous link-margin optimization and monitoring functions that ensure high link margin and robust functionality. Continuous adaptive equalization occurs every second to optimize link margin to adapt to environmental changes and cable aging. An eye-opening monitor function provides continuous link-margin diagnosis and includes various threshold alarm levels that trigger run-time alerts whenever link degradation is detected.

GMSL2 Bandwidth Information and Calculation

The MAX96714/F/R forward links have a fixed link rate of 3Gbps or 6Gbps for the MAX96714/F/R. The reverse-link rate is fixed at 187.5Mbps. The GMSL2 protocol and channel coding overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction. Ensure that the worst-case use cases do not exceed the available throughput of the forward and reverse links. Maxim Integrated's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that can be used for initial bandwidth requirements estimates. It is recommended to consult the factory for high-bandwidth use cases to ensure error-free performance.

Table 4 provides rough estimates of the bandwidth utilization for each communication channel.

Table 4. Forward- and Reverse-Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	H x V x fps x bpp x (1+ (% horizontal blanking)/100 + (% vertical blanking)/100) x 1.14 Maximum bandwidth is limited by pixel clock rate PCLK. Pixel mode: GMSL PCLK = Received MIPI data rate/bpp Pixel mode (double pixel mode): PCLK = MIPI data rate/(2*bpp) Tunneling mode: GMSL PCLK = Received MIPI data rate/24 Maximum GMSL PCLK: 300MHz for 3Gbps link rate Maximum GMSL PCLK = 600MHz for 6Gbps link rate
I^2C	18 to 60 x I^2C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled

Table 4. Forward- and Reverse-Link Bandwidth Utilization (continued)

DATA	APPROXIMATE BANDWIDTH UTILIZATION
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = Horizontal resolution (active pixels)

V = Vertical resolution (active video lines)

fps = Frames per second

bpp = Bits per pixel

MIPI data rate = Aggregate data rate of all lanes in the MIPI interface

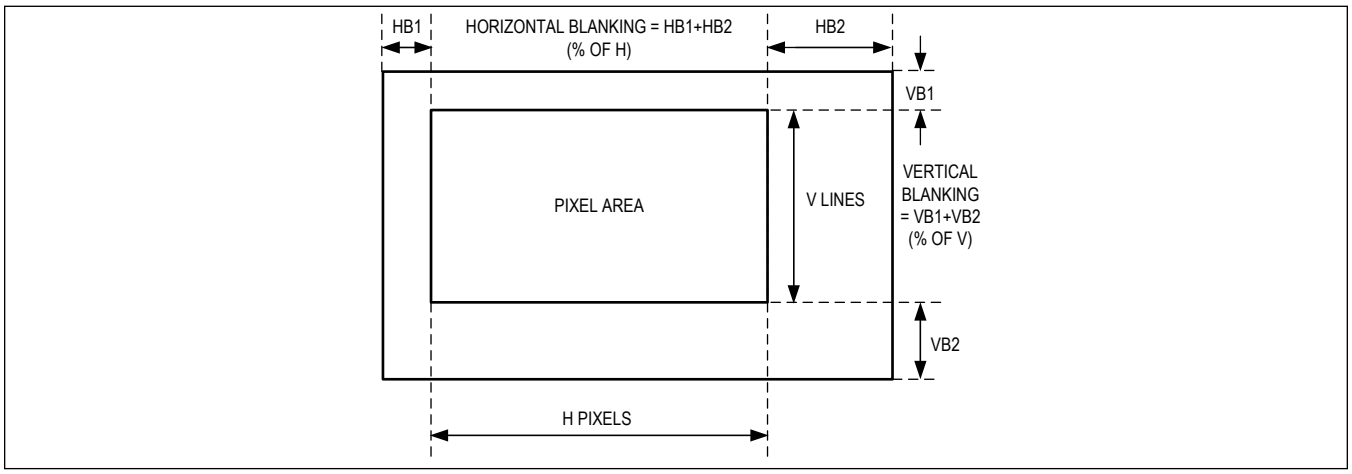


Figure 19. Video Frame Format for Bandwidth Calculation

GMSL2 Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or 300ns + 370UI (where UI is defined as the period of CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. Recommended vertical back porch is one video line.

Minimum vertical back porch in Pixel mode is the maximum of:

- 40 pixels
- 300ns + 370UI

Minimum vertical back porch in Tunneling mode is the maximum of:

- 40 pixels
- 200 PCLK periods + 233ns, where PCLK = total MIPI data rate/24
- 300ns + 370UI

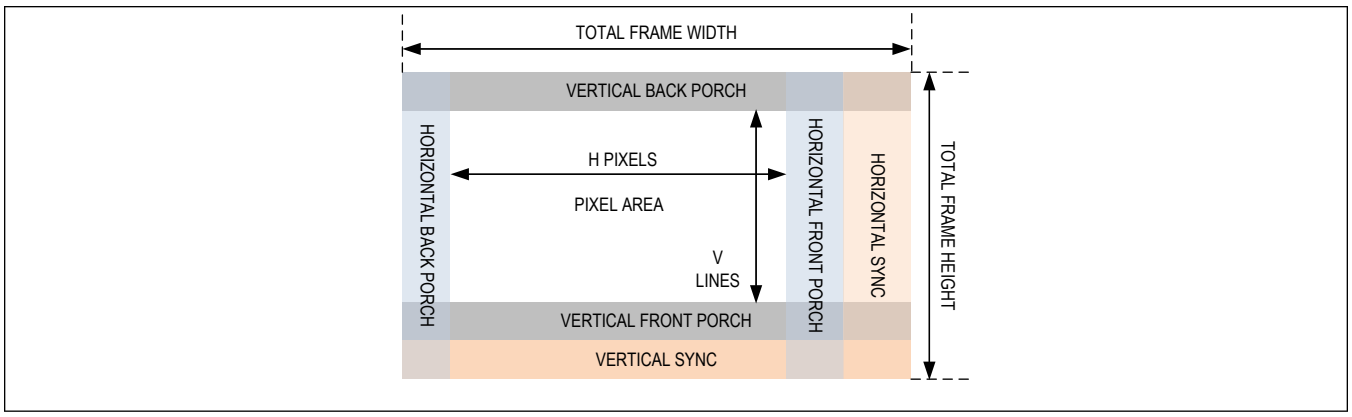


Figure 20. Video Timing

Auto-AEQ (Automatic Adaptive Equalization)

The GMSL2 devices automatically adapt the forward path receiver characteristics to compensate for insertion loss and return loss characteristics of the channel, which consist of the cables, connectors, temperature, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specifications. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then is invoked at every second to track temperature and voltage variations, all critical for a changing automotive safety application. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built-in eye-opening monitor.

Tunnel and Pixel Modes

The MAX96714/MAX96714F/MAX96714R is specifically designed for advanced driver assistance systems (ADAS) where data integrity is a key safety requirement. Prior GMSL2 solutions supported only Pixel mode for transporting received data from a MIPI CSI-2 interface over the GMSL link.

In Pixel mode, the received CSI-2 data is depacketized at the serializer's CSI-2 input interface. The received CSI-2 packet header includes an error correction code (ECC), which is checked and removed at the serializer input. The received CSI-2 packet footer contains the CSI-2 cyclic redundancy check (CRC), which is also checked and removed.

Video line pixel data and video routing information, such as data type and virtual channel, are received and extracted at the CSI-2 interface. Both video pixel data, control channel data and routing information are input to a scheduler in the serializer. The scheduler packetizes and encapsulates the data using GMSL protocol and sequences data transmission across the GMSL link. Video data transport across the GMSL link is protected by line CRCs that are part of the GMSL protocol.

The deserializer receives the GMSL packets and verifies the GMSL2 line CRCs. A CSI-2 interface at the deserializer output encapsulates each video line using CSI-2 protocol and outputs it in CSI-2 format across a CSI-2 interface to the SoC. See Figure 21.

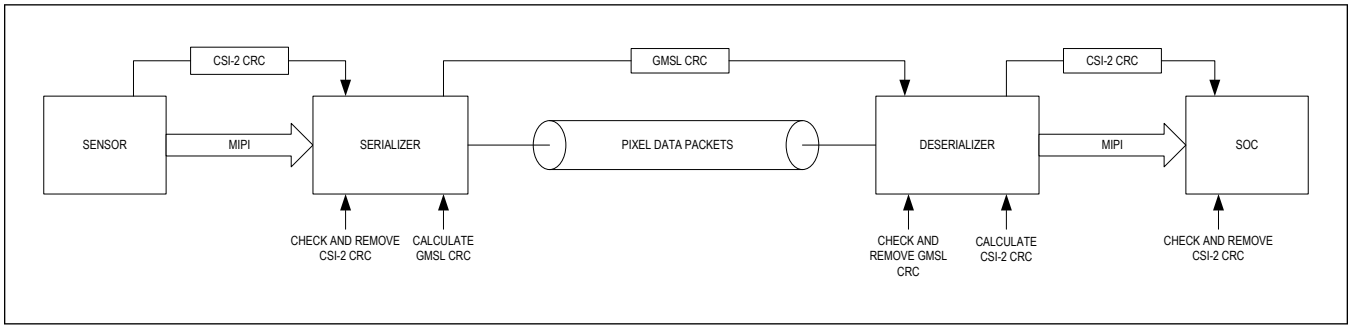


Figure 21. Pixel Mode

In Tunneling mode, the received CSI-2 ECC byte and CRC bytes are checked at the serializer input. These, as well as routing and pixel data, are received as a byte stream. The byte stream is split into smaller packets that are encapsulated using GMSL2 protocol.

The serializer adds a line CRC protecting transmission across the GMSL channel. This CRC covers the entire GMSL2 packetized byte stream for a video line. See Figure 22. The deserializer receives the transmitted GMSL2 packets and control channel packets, checks and removes the GMSL CRC, separates video data from control data, and reconstructs each received CSI-2 packet that is the output to the SoC on a CSI-2 interface. A CRC is calculated on the video data output on the CSI-2 interface. This CRC is compared by the deserializer to the original CRC received from the video source. This comparison guarantees that the entire data packet output on the standard MIPI interface is identical to that received at the serializer input. Tunneling mode is more bandwidth-efficient if multiple data types are being sent. Because data received at the serializer input and data output from the deserializer are verified to be identical, Tunneling mode does not allow for processing of the video data, such as watermarking or lossy data compression. Different data rate and lane count on serializer and deserializer are still possible.

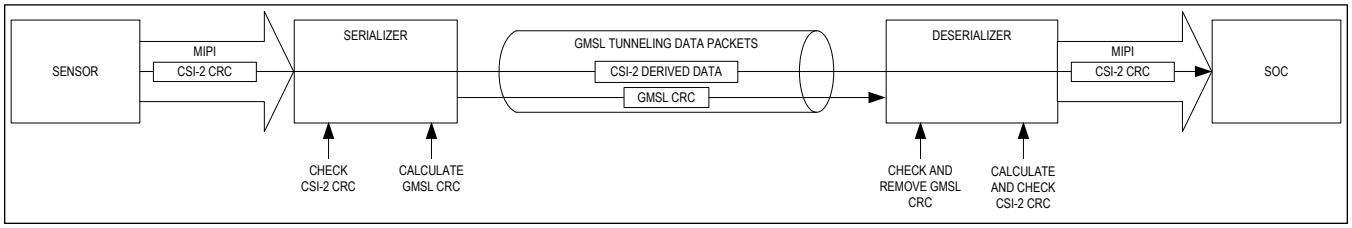


Figure 22. Tunnel Mode

Video Pipes - Stream Mode, Virtual Channel, Data Type, and Memory Information

In the GMSL2 Pixel mode, the transportation of video data is based on the concept of video pipes. Carrying data in pipes allows the GMSL2 to bridge different digital video interfaces (i.e., parallel YUV422 source to CSI-2 sink) and detection.

A pipe carries a video stream (or streams) and video synchronization data, and operates in one of three modes. In all the modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types as follows:

- Mode 1: Streams with constant Bits Per Pixel (BPP) of up to 24bpp. The BPP of the streams must be the same.
- Mode 2: Streams with 16bpp, 14bpp, 12bpp, 10bpp, or 8bpp. Streams less than 16bpp are padded with zeros.
- Mode 3: Streams with two different BPP rates. The BPP of one stream must be twice or triple that of the other stream. The higher BBP stream is 24bpp.

Modes 1 and 3 carry data at full bandwidth but put more restrictions on the BPP than Mode 2. Mode 2 allows streams with different BPP rates, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link (because of zero-padding). Mode 1 or 3 are sufficient for most applications. Mode 2 requires is more convenient if the application does not require maximum link bandwidth.

The MAX96714/F/R have one video pipe. The pipe has a dedicated video-line buffer that is 16k byte and has the capacity for a line length of up to 4096 24-bit pixels. Before the video data is sent out to the MIPI output port, the data is stored in the line buffer. In the Pixel mode, the line buffer stores a complete line of video data before the data is available for read-out by the Controller.

If the video source has a CSI-2 output, packet DT and VC can be left as-is or reassigned through register programming in pixel mode. There are two ways to change the VC/DT within the MAX96714/F/R.

1. Use of Destination and Source. This functionality is slightly more powerful than the override functionality mentioned below due to its capabilities. Up to 16 DT/VC incoming pairs can be mapped to 16 DT/VC outgoing pairs. Refer to the GMSL2 User Guide for functionality on this feature
2. Overriding the BPP/VC/DT can be done through the BACKTOP13 - VC override - BACKTOP15/6 - MIPI Software Data Type override - BACKTOP18 - BPP override if needed.

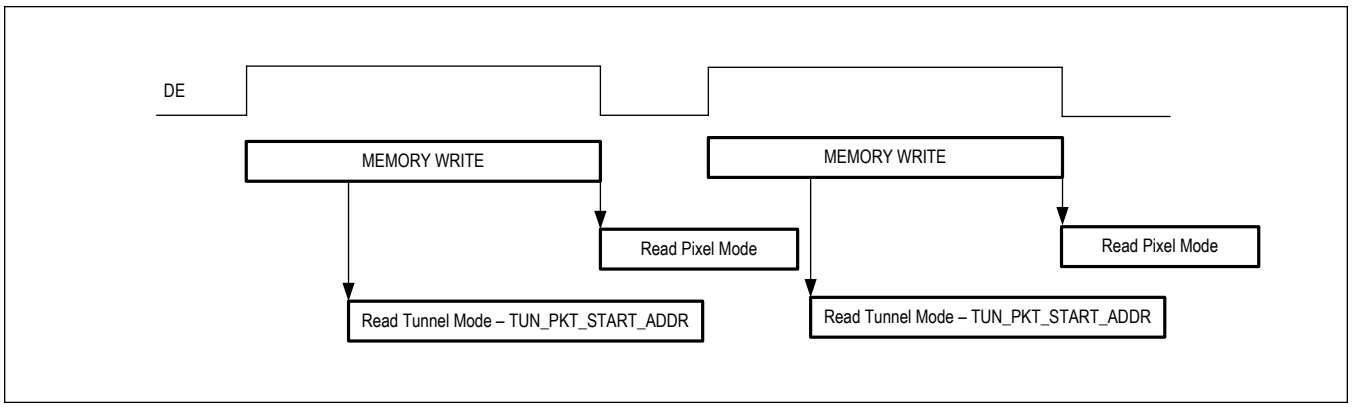


Figure 23. GMSL2 Memory Reading and Writing

The MAX96714/F/R support a new feature called 'cut-through' in the Tunnel mode that allows the controller to start reading from the memory sooner. Register TUN_PKT_START_ADDR can adjust when to start reading from memory after written to. This allows an extension to the video line memory for lines longer than 4096 pixels, and can also reduce latency, by allowing the ability to read the memory quicker. Once data is read out, it cannot be read out a second time. Figure 23 shows the MAX96714/F/R memory operation.

To prevent buffer overflow, the CSI-2 port data rate must be programmed to a equal to or greater rate than the incoming data rate. Programming the output rate to be faster than the bandwidth of the incoming video or data increases packet spacing (LP time between packets). The video memory has built-in overflow detection - BACKTOP11. This occurs when the video bandwidth is higher than the data going out on the MIPI port, not giving a chance to the memory to empty.

No reformatting of the data occurs in the Tunnel mode. It is a requirement for functional safety that the video data is unchanged, such that it can be compared against the tunneled CSI-2 CRC by the host.

After data exits a retiming buffer, it goes through a Data Type (DT) and Virtual Channel (VC) reassignment stage. If the video source has a CSI-2 output, packets DT and VC can each be left as-is,or reassigned by register programming.

The MAX96714/F/R - GMSL2 protocols allocate 24 bits of each packet for video content to effectively use the GMSL2 forward channel bandwidth. The serializer and MAX96714/F/R contain the double Pixel mode, which stuff x2 8bpp/10bpp/12bpp into the same packet. See bpp8dbly / bpp10dbly / bpp12db registers for more information.

Video Memory ECC Protection

The integrity of data propagating through the pipe's line memory is guaranteed by ECC, which enables correction of 1-bit errors and detection of 2-bit errors per 32 bits of video data. This functionality provides protection of data not protected by the CRCs of the incoming GMSL stream or the outgoing CSI stream, eliminating the possibility that internally generated silent bit errors might corrupt the outgoing CSI-2 stream. The state of the ERRB pin and error status register FS_INTR1 can be used to detect the presence of mempry ECC errors. Intentional memory error injection is available for diagnostic purposes. See register MEM_ECC0/1/2 for more information and to set up thresholds to detect these errors.

Video PRBS Generator/Checker

GMSL2 devices include built-in video PRBS generators/checkers for video link testing. For example, a serializer's PRBS generator can be used in conjunction with a deserializer's PRBS checker to test the GMSL2 video channel that connects the two devices. Here, the MAX96714/MAX96714F/MAX96714R's PRBS checker functionality compares the received PRBS stream with the predicted PRBS data to establish any errors. To run the video PRBS test, refer to the GMSL2 user guide for more information.

Frame Sync

In some camera applications, a frame-sync signal is required by the sensors to synchronize the output of a frame with the other cameras in the system. The MAX96714/F/R can generate FSYNC signal internally or receive an FSYNC signal from external SoC, and send it over to the sensor through the GMSL reverse channel. MFP0 or MFP2 is programmed to receive the external FSYNC signal and MAX96714/F/R are programmed as FSYNC subordinates. To generate the

internal FSYNC, the MAX96714/F/R are programmed as FSYNC mains. See register FSYNC_0 for details.

Vertical and Data Enable or Data Valid Sync Outputs

The MAX96714/MAX96714F/MAX96714R can output the Vertical Sync (VS) and Data Enable/Data Valid (DE/DV) of a video stream to monitor the video timing by a processor. This feature provides access to VS and DE/DV signals not available directly at the CSI-2 output. The VS and DE/DV output are alternate functions of MFP0 and MFP5.

Reverse Channel

A controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. The MAX96714/F/R support the following interfaces:

- Primary I^2C/UART - UART not present on MAX96714R
- Pass-Through I^2C/UART - Not present on MAX96714R
- GPIO

All the above interfaces can pass data through the GMSL2 link, but the GMSL2 device registers can be accessed and configured only through the primary I^2C/UART interface.

The reverse channel, with its various interfaces, is accessed using multifunction pins. Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 5 and Table 6 in the *Multifunction Pin Assignments* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Scheduler/Arbiter

The scheduler transmits packets with high-priority values before lower-priority values. Each communication transmit adapter sets a priority for the packet request before transmitting data to the remote side. The priority value is 2 bits, which allows for the following settings: 0 = Low, 1 = Normal, 2 = High, and 3 = Urgent - See TR0 for setting up priority. The scheduler, provided sufficient link bandwidth and chooses to transmit the packet with the highest priority among the pending active requests. Priority levels become more important as link bandwidth becomes scarce, and prioritization is assigned accordingly.

In most cases, each transmitter adapter should use the normal priority setting (priority = 1) to allow the scheduler to choose the transmission schedule based on recent bandwidth usage. Packet priority can be increased if packets require low latency or have waited for a specified period of time. For example, packets with requirements on maximum latency can have increased priority if the packet request is not serviced until half of the maximum latency requirement has elapsed. This can also be used for communications channels with continuous data flow (e.g., video). Priority can be increased when the transmit adapter data buffer approaches overflow. Conversely, register configuration allows the priority settings of each channel to be overridden. This option is useful if the host µC wants to prioritize one channel over the others.

Communications channels with very relaxed latency requirements can use the low-priority setting (priority = 0). These low-priority packets are not serviced by the scheduler if there are any pending requests of a higher priority setting. In this arrangement, link-bandwidth assignment can reach the theoretical maximum for video. Low-priority packets can then be transmitted during video horizontal-blanking time, during which the video-channel bandwidth usage drops considerably.

Primary and Pass-Through I^2C/UART

The primary I^2C/UART is located on the SDA_RX and SCL_TX pins. The I^2C (SDA, SCL) or UART (Tx, Rx) (not on the MAX96714R interface) is selected by the CFG0 pin voltage at power-up (see Table 8). The selected interface provides access to both the MAX96714/F/R registers and peripheral registers from either end of the link.

The main controller can reside on either end of the link (usually the deserializer side for camera applications). The MAX96714/F/R support dual main controllers, provided that software arbitration (such as token passing) is used to prevent packet collisions. The reverse channel allows only one main host to communicate at a time.

The MAX96714/F have a choice of two pass-through I^2C/UART channels that share the same MFPs. These channels do not have access to registers in either the GMSL2 serializer or the deserializer; they simply tunnel the I^2C or UART signal across the GMSL2 link. This allows I^2C channels to be separated so that no multi-main conflicts occur.

Message Counter

An additional functional safety feature of the MAX96714/F is the message counter, which can be used with the I2C/UART CRC feature. If enabled, the device expects a 2-byte message count from the host, indicating the number of writes being sent. The MAX96714/F count the number of read and write transactions. The writes are compared with the count sent by the host. If the two counts match, the write is accepted. If the two counts do not match, the write is rejected, a NACK is sent in return, and the error counter is incremented. A programmable threshold for the error counter asserts ERRB when reached.

For read transactions, the MAX96714/F send the message counter value to the host along with the requested data. The host should compare the sent message count against its stored value and accept the data if the counts match. Note that a read transaction has a repeated start condition, with the device address byte sent twice. This results in each read transaction incrementing the message counter twice, once for each device address byte. If the two message counter values do not agree, the data should be rejected. If a read is requested from the last used registers address, resulting in only one device address byte, the message counter is incremented once.

If the message counter values for the MAX96714/F and host do not agree, the device's message counter can be reset using a register write and the host's counter should also be reset. If the host is reset, or if its message counter is reset for any reason, the device's counter must be reset using a register write as well.

I2C Writes with CRC

To provide additional functional safety for ADAS applications, the MAX96714/F support the addition of a Cyclic Redundancy Check (CRC) to I2C transactions. When enabled, the µC must compute and send a CRC byte after each data byte. See Figure 24. For each single-byte or multibyte write, the deserializer first clears the CRC engine. The first CRC includes the Device Address byte, Register Address bytes, Message Counter bytes (when enabled), and first Data byte. For all the following data bytes, the CRC engine is reset and the CRC byte covers the additional data byte. When the message counter is disabled, the first CRC is calculated without the Message Counter bytes. See Figure 25 and Figure 26. The deserializer receives the data byte and calculates the CRC using an identical CRC engine, and verifies a match before accepting the data byte. If the CRCs do not match, a write is not accepted, a NACK is transmitted, and the error counter is triggered.

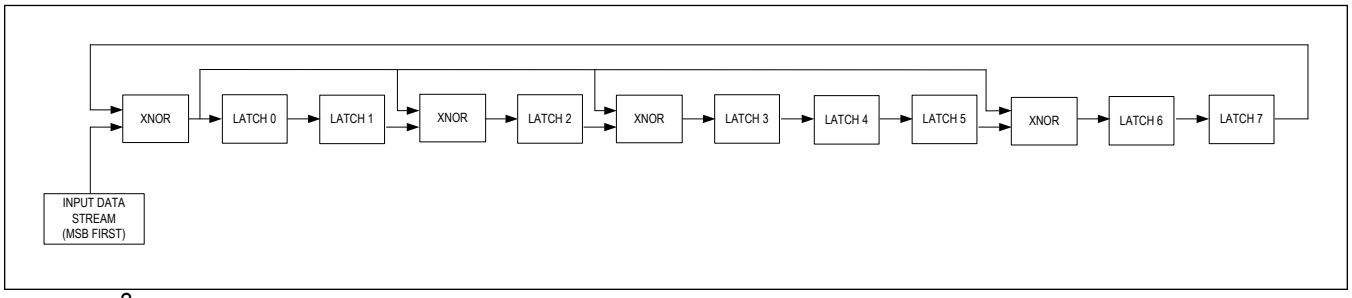


Figure 24. I2C CRC Engine

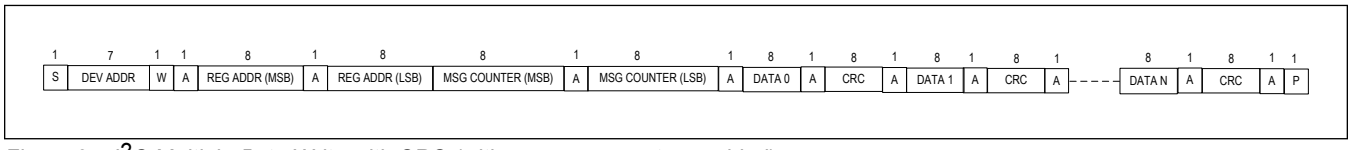


Figure 25. I2C Multiple-Byte Write with CRC (with message counter enabled)

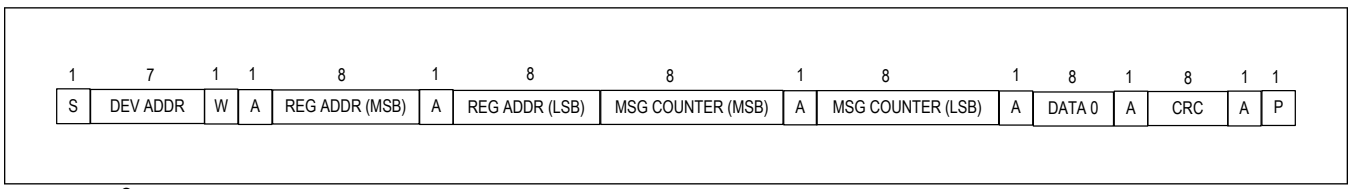


Figure 26. I2C Single-Byte Write with CRC (with message counter enabled)

I²C Reads with CRC

For I²C reads of the MAX96714/F registers, the device's CRC engine clears and then uses the outgoing Device Address byte(s), Register Address bytes, Message Counter bytes (when enabled), and first Data byte to calculate the first CRC byte. This is added to the data stream directly after the corresponding data byte. The CRC engine is subsequently cleared again for all other data bytes. When the message counter is disabled, the first CRC is calculated without the Message Counter bytes. See Figure 27 and Figure 28. When the host µC receives the I²C read data, the µC's CRC engine should calculate a CRC byte for each data byte and compare with the transmitted CRC byte.

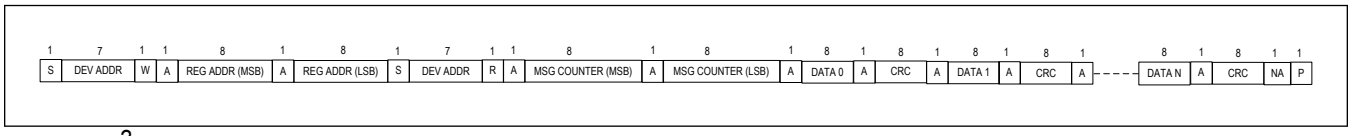


Figure 27. I²C Multiple-Byte Read with CRC (message counter enabled)

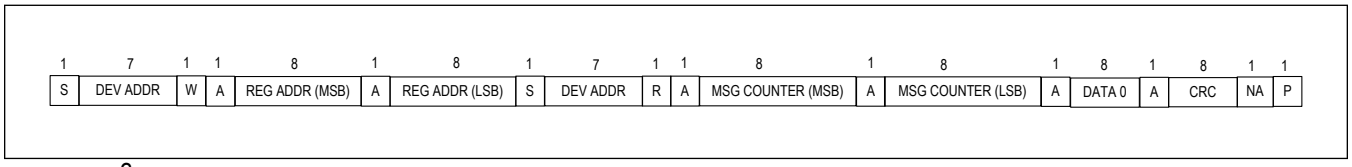


Figure 28. I²C Single-Byte Read with CRC (message counter enabled)

UART Writes with CRC

To provide additional functional safety for ADAS applications, the devices support the addition of a cyclic redundancy check (CRC) to UART transactions. When enabled, the µC must compute and send a CRC byte after each data byte. See Figure 29. For each single-byte or multi-byte write, the deserializer first clears the CRC engine. The first CRC includes the Sync Frame, Device Address byte, Register Address bytes, Message Counter bytes (when enabled), Byte Count, and first Data byte. All bytes are sent LSB first. For all following data bytes, the CRC engine is reset and the CRC byte covers the additional data byte. When the message counter is disabled, the first CRC is calculated without the Message Counter bytes. See Figure 30 and [[UART Single-Byte Write Transaction with CRC (message counter enabled)]]. The devices receive the data byte and calculates the CRC using an identical CRC engine, and verifies a match before accepting the data byte. If the CRCs do not match, a write is not accepted, a NACK is transmitted, and the error counter is triggered.

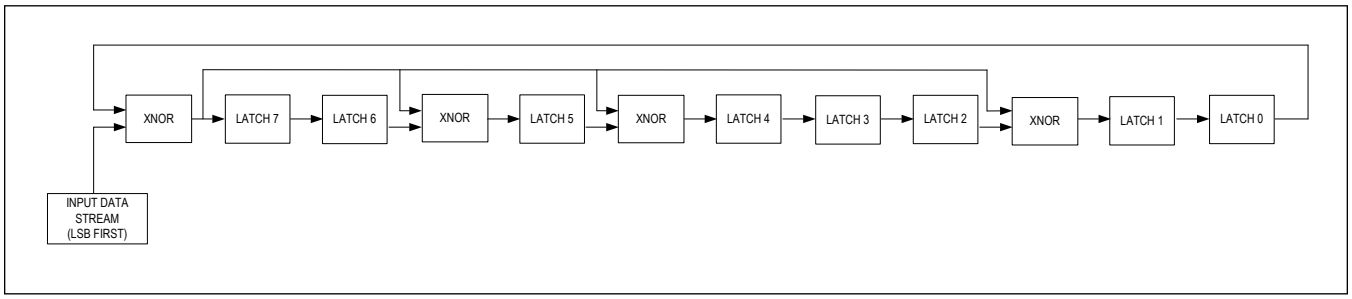


Figure 29. UART CRC Engine

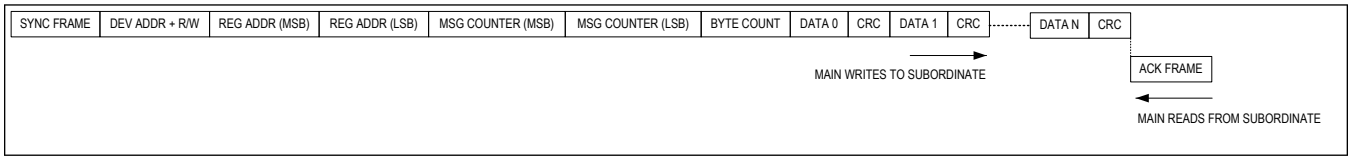


Figure 30. UART Multiple-Byte Write Transactions with CRC (message counter enabled)

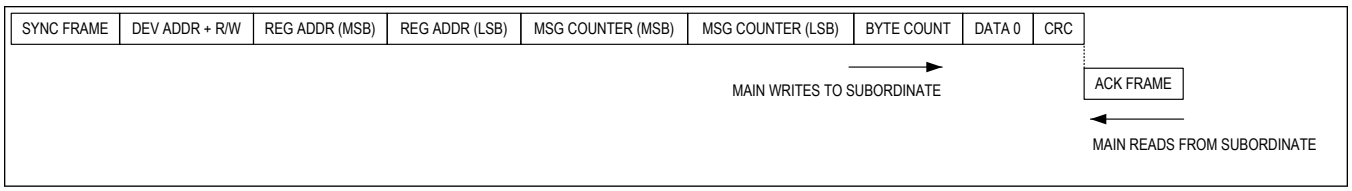


Figure 31. UART Single-Byte Write Transactions with CRC (message counter enabled)

UART Reads with CRC

For UART reads of registers, the device's CRC engine clears and then uses the outgoing Sync Frame, Device Address byte, Register Address bytes, Byte Count, Message Counter bytes (when enabled), and the first Data byte to calculate the first CRC byte. This is added to the data stream directly after the corresponding data byte. All bytes are sent LSB first. The CRC engine is subsequently cleared again for all other data bytes. When the message counter is disabled, the first CRC is calculated without the Message Counter bytes. See Figure 32 and Figure 33. When the host µC receives the UART read data, the µC's CRC engine should calculate a CRC byte for each data byte and compare with the transmitted CRC byte. The Ack Frame is not included in the CRC calculation because the µC is looking for the ACK value of 0xC3. If there is an error, the µC treats the frame as a NACK and rejects the data. Note that the read command from the µC does not include CRC.

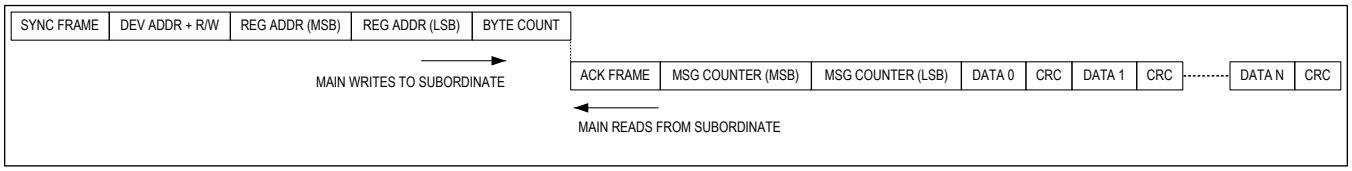


Figure 32. UART Multiple-Byte Read Transaction with CRC (message counter enabled)

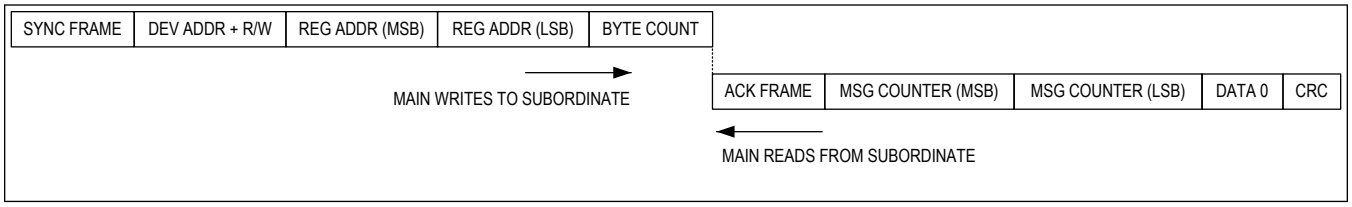


Figure 33. UART Single-Byte Read Transaction with CRC (message counter enabled)

Multifunction Pin Assignments

The MAX946714/F/R provide a range of peripheral I/O functions. These functions are mapped through the register control to an array of multifunction pins (MFP). Each MFP has several possible functions, but only one can be used at a time. A user selects an MFP function to suit their use-case by programming the appropriate registers: FRSYNC = FSYNC_0 | VS = CFG_0/1 | DE = CFG_2/4 |.

The *Pin Descriptions* table shows default and alternate functions for each MFP, listed in order of priority (highest priority listed first). A higher priority function must be disabled when a lower-priority function is enabled, both by register writes.

Table 5. GMSL2 Mode MFP Pin Function Map

PIN	I²C/UART MA96714/F	I²C MA96714R	GPIO	MONITOR	OTHER FUNCTIONS	POWER-UP DEFAULT MAX96714/F	POWER-UP DEFAULT MAX96714R	PIN SLEW DEFAULT
MFP0			GPIO0	VS, DE/ DV	MS*, FRSYNC	GPI0	GPI0	10
MFP1	SDA1/RX1*, SDA2/ RX2*	N/A	GPIO1			RX1	GPI1	11

Table 5. GMSL2 Mode MFP Pin Function Map (continued)

PIN	I²C/UART MA96714/F	I²C MA96714R	GPIO	MONITOR	OTHER FUNCTIONS	POWER-UP DEFAULT MAX96714/F	POWER-UP DEFAULT MAX96714R	PIN SLEW DEFAULT
MFP2	SCL1/TX1*, SCL2/ TX2*	N/A	GPIO2		MS*, FRSYNC	TX1	GPI2	11
MFP3	Primary SDA/RX*	SDA				SDA or RX	SDA	I²C
MFP4	Primary SCL/TX*	SCL				SCL or TX	SCL	I²C
MFP5			GPIO5	VS, DE/ DV	LOCK	LOCK	LOCK	10
MFP6			GPIO6	LMN0		GPI6	GPI6	11
MFP7			GPIO7	LMN1		GPI7	GPI7	11
MFP8			GPIO8		ERRB	ERRB	ERRB	11

Table 6. GMSL1 Mode MFP Pin Function Map

PIN	I²C/ UART	REGISTER PROGRAMMABLE GPIO	MONITOR	OTHER FUNCTIONS	CONTROL OUTPUT	POWER-UP DEFAULT	PIN SLEW DEFAULT
MFP0		GPIO0	VS, DE/ DV	MS*, FRSYNC	CNTL1	GPI0	10
MFP1		GPIO1		GPI	CNTL3	GPI	11
MFP2		GPIO2		MS*, FRSYNC	CNTL4	GPI2	11
MFP3	SDA/ RX*					SDA	I²C
MFP4	SCL/ TX*					SCL	I²C
MFP5		GPIO5	VS, DE/ DV	LOCK		LOCK	10
MFP6		GPIO6	LMN0		CNTL2	GPI6	11
MFP7		GPIO7	LMN1		CNTL0	GPI7	11
MFP8		GPIO8		ERRB		ERRB	11

* The MAX96714R does not have MS, UART, or Pass-through functionality.

Except for MFPs configured as I²C/UART or open-drain outputs, whose transition times are fixed, the transition time of each MFP can be changed from the default value by programming the PIO_SLEW registers.

Transition times depend on the PIO_SLEW_0/1/2 and V_{DDIO} supply voltage. See Table 7 for typical rise and fall times for each PIO_SLEW_0/1/2 setting. To change the transition time of an MFP, program PIO_SLEW_0/1/2 Table 7. For more information, see PIO_SLEW_0/1/2. When selected, the register control of transition time for these functions is automatically bypassed.

Table 7. MFP Pin Typical Output Rise and Fall Times

TRANSITION TIME SETTING (TTS)	RISE TIME (ns) (20% to 80%), C_L = 10pF		FALL TIME (ns) (80% to 20%), C_L = 10pF	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
00	1.0	0.6	0.8	0.5
01	2.1	1.1	2.0	1.1
10	4.0	2.3	4.3	2.3
11	9.0	5.0	10.0	5.0

Table 7. MFP Pin Typical Output Rise and Fall Times (continued)

I^2C	N/A	N/A	40	30

General Purpose Input and Output (GPIO)

The GPIO channel is used to transmit low-speed (<100Kbps) signals over the GMSL2 link. MFP pins can be programmed as GPI, GPO (push-pull output), or ODO (open-drain output). Each GPIO pin can be configured as an input, output, or input/output by programming the GPIO_TX_EN and GPIO_RX_EN register bits of each GPIO pin. Note that unwanted loop behavior is avoided for pins configured as input/output: when the pin is driven by a transition received from the remote side, the driven GPIO transition is not transmitted back. GPIO pins may alternately be controlled and read solely from registers. Most GPIO pins can be programmed for 1MΩ or 40kΩ pullup/pulldown/no pullup/pulldown, open drain, or push-pull output. See register GPIO_A/GPIO_B - MFP0 for configuration and programming.

A GPIO packet has 32 possible GPIO channel IDs. Each GPI is mapped to a channel ID according to the GPIO_TX_ID register. On the receiving end, each GPO outputs the received data with a programmed GPIO channel ID corresponding to the GPIO_RX_ID register for that pin. This provides flexibility in determining which GPIO input drives which GPIO output.

The GPIO channel is not bandwidth efficient and should be used for low-speed signals. Each GPIO transition uses 40-80 bits on the GMSL2 link for transmit and 40 bits to 60 bits on the reverse (due to received ACK packets).

Refer to the GMSL2 User Guide for more information on various configurations

GPIO Delay in Compensated vs. Non-Compensated Mode

In the Delay-Compensated mode, a timestamp value is transmitted in addition to the value of the transition and the GPIO channel ID. This timestamp is a high-resolution value sampled by an internal 600MHz clock that records when the GPIO transition is detected at the input. The remote-side chip uses the timestamp value to wait and output the GPIO transition after a total fixed delay from the GPIO input transition. This method mitigates possible variable latency issues by making the total GPIO input-to-output delay a precise, fixed value. GPIO_A - MFP0 enables this function and GPIO_REV_CDLY controls the bandwidth and delay multiplier for GPIOs.

In the Non-Compensated mode, the value of the transition is transmitted along with the GPIO channel ID. Note that GPIO channel latency is not fixed; the GMSL2 link has variable delay as a result of multiple communication channels sharing the link. A maximum latency limit is established by the GMSL2 bandwidth-sharing scheme, but significant fluctuation remains.

Reverse Channel Retransmission on Error

Automatic Repeat Request (ARQ)/Automatic Retransmission

Communications channels with control data (I^2C/UART, GPIO) are relatively low bandwidth but require the highest data-integrity protection. An optional automatic packet retransmission method, ARQ (Automatic Repeat reQuest), is employed here. ARQ works in conjunction with the 16-bit packet CRC to detect if packets are received without error.

Packets are appended with a 2-bit sequence number at the transmit side and an Acknowledge packet is sent from the receiver side upon successful receipt of each data packet. These packets are stored on the transmit side until they are acknowledged. If the Acknowledge packet does not arrive in a predetermined interval, or the sequence number of the Acknowledge packet does not match the expected value, the packet waiting at the top of the queue is automatically retransmitted.

The Acknowledge packet uses the same header field as low-bandwidth packets, but begins with a different special symbol to distinguish it from regular data packets. This simplified format keeps retransmission exchanges independent from the communication channel. Note that this smaller packet format contains no data, obviating the need for a full 16-bit CRC. Instead, the Header symbol is sent twice in the packet, and the instances are checked against each other to ensure a match. The Acknowledge packets also include a 2-bit sequence number that is the same sequence number of the correctly received data packet. The Data packet transmitter keeps track of which packets are acknowledged.

See ARQ0/1/2 registers for each feature GPIO/Control Channel/Pass-through 1 and 2 to configure the ARQ. By default, the ARQ is enabled for each function.

Functional Safety Features - POST/LBIST/MBIST - CRC

The MAX96714/F integrate a number of safety features, including the power-on self test (POST), which includes the logic built-in self test (LBIST) and memory built-in self test (MBIST). At power-up, the LBIST verifies that key logic blocks are correctly functioning and free of latent faults. The MBIST checks the line-buffer memory and other small memories in the deserializer to ensure that data is stored correctly prior to being sent to the MIPI output ports. The POST produces a pass/fail result that can be read through a register for each test. A failure does not prevent the device from operation but does assert ERRB.

Registers to read information on POST/LBIST/MBIST are contained in the REG_POST0 register.

The MAX96714/F contains the following CRCs. All CRCs require an enable and understanding on both sides of the link or communication host.

1. Forward Channel CRC - 6/3Gbps enable located in RX1 register. When enabling, select the correct pipe coming from the serializer.
2. Reverse Channel CRC - 187Mbps enable located in TR0 - Control channel CRC
3. External I^2C/UART CRC - This is a CRC for I^2C/UART connection leading from the MAX96714/F to the Host/ Main controller. To enable this feature, see I2C_UART_CRC7.
4. Info Frame Forward and Reverse channel CRC - FWD - Video info frames are low bandwidth packets sent after each line and each VSYNC. REV info monitors lock status. Both are enabled by default - TR0 - Info Frame CRC enable
5. Video Line CRC - Used to detect pixel corruption within the video lines - VIDEO_RX0
6. Video Packet CRC - When enabled, each packet carrying 36 pixels is protected by a CRC - INTR6 to enable
7. Tunnel Mode CRC - CSI-2 CRC byte - To enable, view MIPI_PHY16
8. GPIO Forward and Reverse channel CRC - To enable, view TR0 GPIO CRC
9. Pass-Through Forward and Reverse channel 1 and 2 CRC - To enable, view TR0 Pass-through 1 / 2
10. RBB Reverse Channel CRC - Fault that occurs in arbitration and scheduling of data is FAULT_OEN
11. Line Memory ECC - CRC cannot be trusted with the data coming in, so ECC is performed instead - FS_INTR0. Refer to the User Guide for further setup of the ECC thresholds.
12. Register Table CRC - Can use a rolling CRC to confirm if any register change has occurred. To enable, see REGCRC0/1/2/3. Refer to the User Guide for more information.
13. EFUSE CRC - Electrical fuse that contains chip configuration and test information. This feature is located in FS_INTR0
14. GMSL1 Video line CRC - GMSL1_1C
15. GMSL1 Reverse Channel CRC - GMSL1_18
16. GMSL1 Reverse Channel Packet CRC - GMSL1_19

All CRCs mentioned above are 16-bit except for Video line, which is 32-bit.

Other functional safety functions like overvoltage, undervoltage, overflow, etc., are found in other features that apply to that particular feature.

RoR (Reference over Reverse)

Reference Clock over Reverse Channel (RoR) is a GMSL clock operating mode where the serializer receives its reference clock from the deserializer over the GMSL link. RoR eliminates the need for a crystal oscillator on the serializer side of the link.

In RoR-mode, the serializer's timing reference is extracted from the signal sent on the reverse channel. The recovered clock coming from the deserializer is used by the serializer on-chip phase-locked loop (PLL) to synthesize the serializer output reference clock RCLKOUT.

RoR-mode is enabled by default on the MAX96714/F/R.

The removal of the crystal oscillator in RoR provides several advantages:

- Reduced system cost
- Increased reliability
- Reduced board area
- Simplified board layout

GMSL2 Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or 300ns + 370UI (where UI is defined as the period of CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. Recommended vertical back porch is one video line.

Minimum vertical back porch in Pixel mode is the maximum of:

- 40 pixels
- 300ns + 370UI

Minimum vertical back porch in Tunneling mode is the maximum of:

- 40 pixels
- 200 PCLK periods + 233ns, where PCLK = total MIPI data rate/24
- 300ns + 370UI

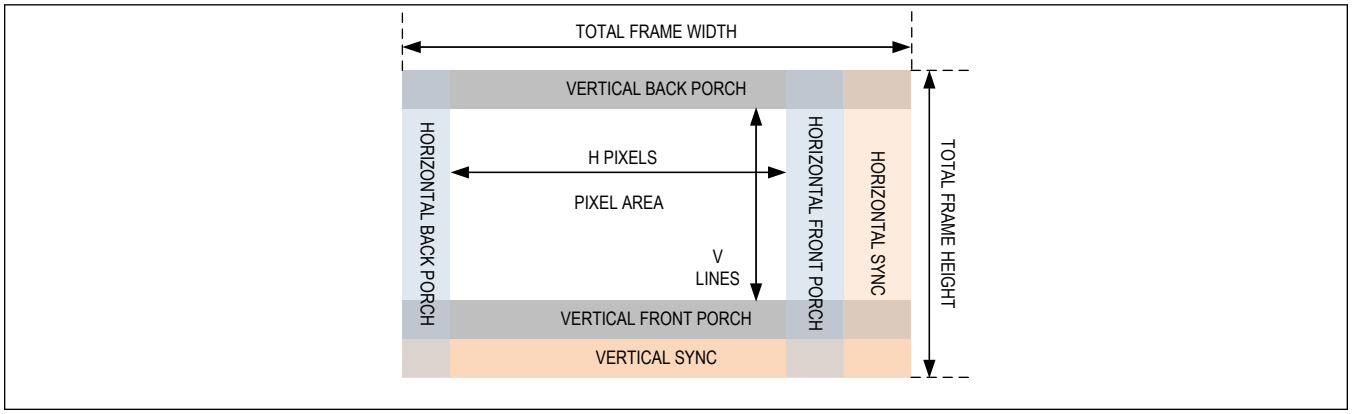


Figure 34. Video Timing

Link Error Generator

Each of the GMSL links includes a configurable error generator that injects errors into the outgoing data stream immediately prior to transmission. The deserializer injects errors into the reverse channel and the serializer injects errors into the forward channel. The receiving device detects, counts, and flags the errors, enabling a thorough validation of the system's response to error conditions of varying severity. See GMSL User Guide for more information on how to implement Link Error Generator.

Cabling Options

GMSL2 accommodates either 50Ω coaxial or 100Ω shielded-twisted pair (STP) cabling. Cables must have sufficient return and insertion loss characteristics for best full-duplex link performance. See GMSL2 Channel Specifications for more information.

Eye-Opening Monitor

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free, but have less link margin than desired. This allows the user to proactively react to deteriorating cable performance before any link errors occur. GMSL2 devices can measure the horizontal or vertical eye-opening of the equalizer's output. The measurement is activated automatically at a rate of approximately 1Hz once a link is active. The EOM block compares the data sampled at the center of the eye with a sample that is offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye-opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Line Fault

GMSL deserializers include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line fault monitor requires external resistors R_{EXT} and R_{PD} in Coax mode and STP mode connected to the LMN_ pins as detailed in the Figure 35. See Table 2 for referenced component values.

The line fault monitor is disabled by default, configuration options are available through registers, and status can be read by INTR2/3 and FAULT_STAT. Line fault detection CANNOT be used in conjunction with Power-over-Coax (PoC) or AC-coupled ground applications.

The line fault monitor pins offer flexible connection and programming in either Coax or STP applications.

Figure 35 illustrates the two configuration options for the location of line-fault detection. The Local-Side Serializer Configuration is typically used for display links and Local-Side Deserializer Configuration is typically used for camera links; however, either configuration can be used on any device serial link system. Additionally, either applies to Coax or STP mode.

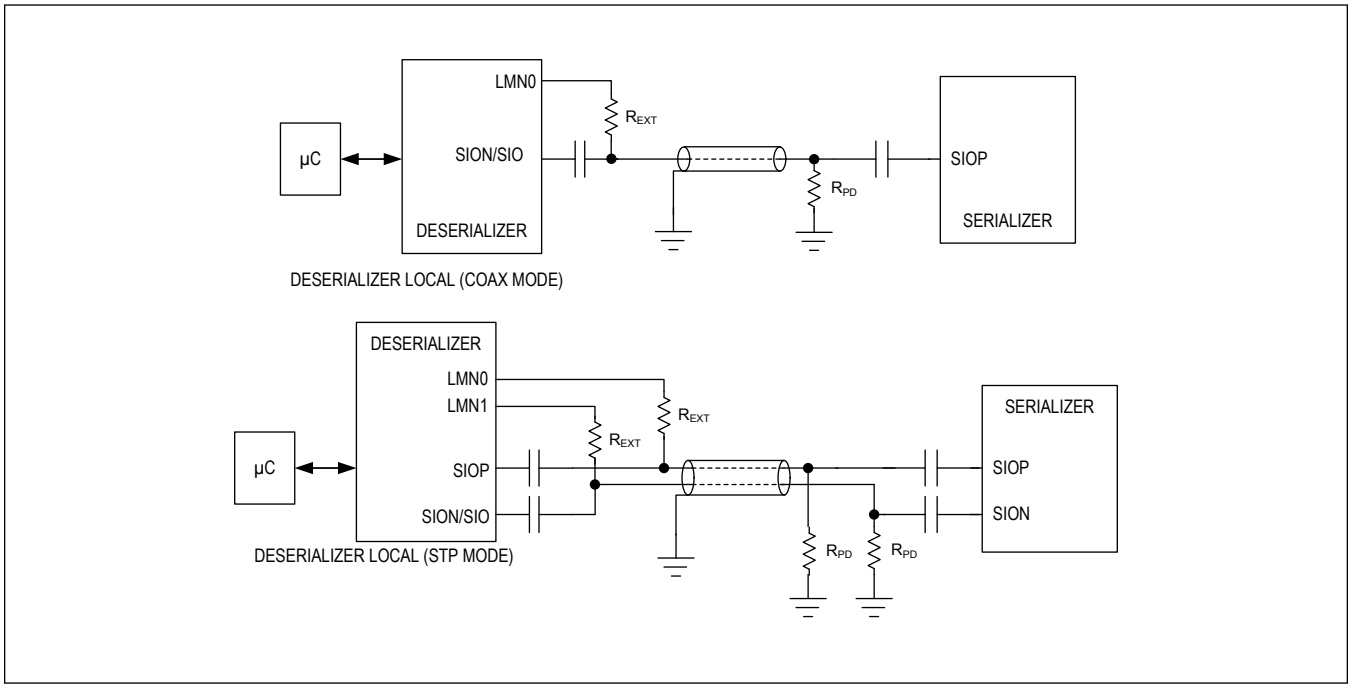


Figure 35. Line Fault Detection Location Options

Spread Spectrum

The MAX96714/F/R can accept the forward channel 6/3Gbps spread spectrum, which can be used to mitigate electromagnetic interference emitted from the device. Narrow frequency peaks are reduced by modulating the internal 6GHz clock at a rate of 25kHz with a saw-tooth profile. In order to keep consistent lock times, it is recommended not to enable spread spectrum. To enable this functionality, refer to the GMSL2 User Guide or contact the factory. Not all registers are visible to customers for this feature.

CSI-2 Output Interface

MIPI Lane Information

Video data is output through a unidirectional MIPI CSI-2 v1.3 output port. The D-PHY v1.2 interface supports four differential lanes. To ease the PCB layout, lane and polarity swapping is supported. See MIPI_PHY3 and MIPI_PHY5 for more information. The D-PHY output supports data rates up to 2.5Gbps each lane.

All MIPI related configurations are programmed before video streaming begins.

CSI-2 Virtual Channel

The device supports virtual channels, including virtual channel extension (VCX) introduced in CSI-2 v2.0, enabling up to 16 virtual channels.

MIPI CSI-2 Output Configuration

Due to limitations on the many host receiver controllers and PCB routing, the MAX96714/F/R have many MIPI optimizations that can be used to achieve optimal MIPI timing. See MIPI_PHY1/2/3/5/8/9 for various MIPI timing adjustments performed by the MAX96714/F/R. The MAX96714/F/R have the ability to fine-tune the MIPI output clock. See BACKTOP25. After the timing adjustments are made, a reset of the MIPI controller must be performed with the MIPI_PHY15.

The MAX96714/F/R support continuous D-PHY clock output. When the MAX96714/F/R receive the video stream, they start sending out the Start-of-Transmission(SOT) sequence on the MIPI clock lane, followed by continuous high-speed clock pulses. The D-PHY Receiver in SoC should be ready to receive the clock SOT transition before the video is transmitted because the SOT sequence on the clock lane is only sent out once. Once the MIPI enters the high-speed mode, the clock lane continues sending the high-speed signal until the MAX96714/F/R are reset or powered down.

The MAX96714/F/R facilitate MIPI PHY characterization by enabling the generation of PRBS output streams in the HS transmit mode directly from each D-PHY output lane. The available patterns are PRBS9, PRBS11, and PRBS18, and the resulting output data is a continuous stream not packetized by the CSI-2 controller.

MIPI Lane Deskew

The CSI-2 D-PHY interface supports interlane deskew by transmitting deskew patterns from the transmitter when the bit transmission rate is 1.5Gbps/lane and above. Deskew is optional for data rates lower than 1.5Gbps/lane.

The MAX96714/F/R support both initial and periodic deskew. Refer to MIPI_TX52 for more information. The user can program the length of the deskew patterns and the frequency of the periodic deskew output. Periodic deskew is automatically generated when enabled. The occurrence of the periodic deskew can be after Frame Start or Frame End. It can start every frame or after the number of frames specified by register MIPI_TX4[5:3].

In the Tunnel mode, additional deskew capabilities are added so that Deserializer's Tx deskew generation can track Serializer's received deskew pattern in occurrence and in deskew length. See DESKEW_INIT for more information.

CFG Latch at Power-Up Pins

At power-up or after reset, the voltages at the CFG0 and CFG1 pins are sampled. The sampled level is used to set the initial value of certain registers.

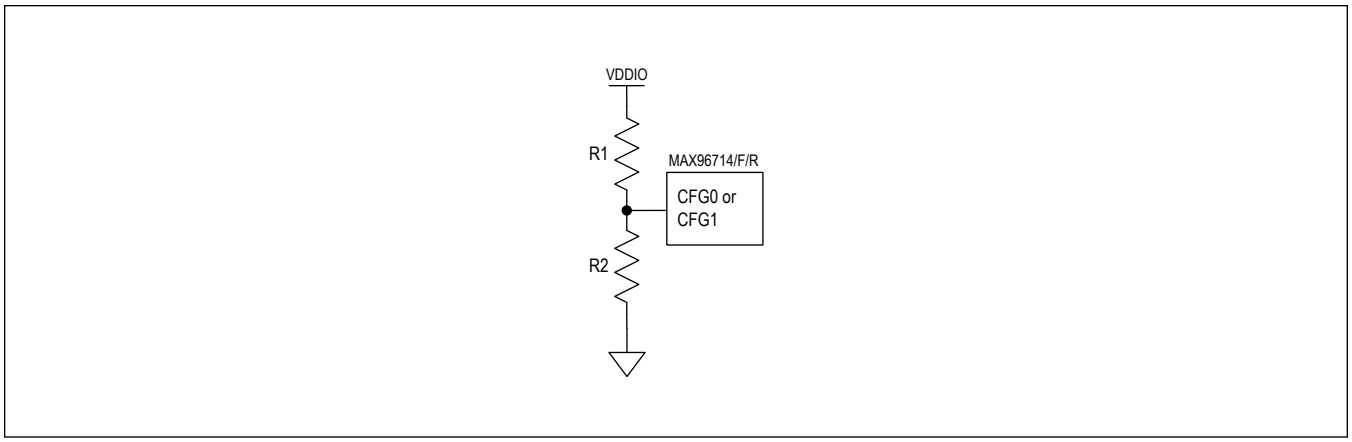


Figure 36. Configuration Pin Connection

The voltage level at each pin is set by an external precision resistor divider connected between V_{DDIO} and ground (Figure 36), or for some configurations, by a single resistor connected to V_{DDIO} or ground. Table 8 and Table 9 show the

recommended resistor values to select each configuration. The voltage level at the CFG pins is typically latched 11ms after all MAX96714/MAX96714F/MAX96714R supplies reach minimum levels required by the power-on-reset (POR) circuit. CFG pins must not be loaded with more than 10pF at power-up to ensure the proper voltage level.

Table 8. CFG0 Input Map

SPECIFICATION (Note a) (Percentage of V_{DDIO})			SUGGESTED RESISTOR VALUES (Notes b, c) (1% Tolerance)		MAPPED CONFIGURATION (Note d)		
MIN	**TYP**	**MAX**	**R1 (Ω)**	**R2 (Ω)**	**I²CSEL** MAX96714/F	I²CSEL MAX96714R	**Device Address**
0.0%	0.0%	11.7%	OPEN	10k	I²C	I²C	0x50
16.9%	20.2%	23.6%	80.6k	20.5k			0x54
28.8%	31.2%	35.5%	68.1k	32.4k			0x98
40.7%	44.0%	47.4%	56.2k	44.2k			0xD4
52.6%	56.0%	59.3%	44.2k	56.2k	UART	N/A	0xD4
64.5%	67.9%	71.2%	32.4k	68.1k			0x98
76.4%	79.8%	83.1%	20.5k	80.6k			0x54
88.3%	100%	100%	10k	OPEN			0x50

Table 9. CFG1 Input Map

SPECIFICATION (Note a) (Percentage of V_{DDIO})			SUGGESTED RESISTOR VALUES (Notes b, c) (1% Tolerance)		MAPPED CONFIGURATION (MAX96714)			MAPPED CONFIGURATION (MAX96714F/MAX96714R) (Note e)		
MIN	**TYP**	**MAX**	**R1 (Ω)**	**R2 (Ω)**	**Coax or Twisted Pair**	**MAX96714 Data Rate (Gbps)**	**Tunnel or Pixel Mode**	**Coax or Twisted Pair**	**GMSL1 or GMSL2 - 3Gbps**	**Tunnel or Pixel Mode**
0.0%	0.0%	11.7%	OPEN	10K	STP	RSVD	Tunnel	COAX	GMSL2	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		6			GMSL1, HIM	Pixel
28.8%	32.1%	35.5%	68.1k	32.4k		RSVD	Pixel		GMSL1, Legacy	
40.7%	44.0%	47.4%	56.2k	44.2k		6		STP	GMSL2	Tunnel
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	RSVD	Tunnel			Pixel
64.5%	67.95%	71.2%	32.4k	68.1k		6			GMSL1, HIM	
76.4%	79.8%	83.1%	20.5k	80.6k		RSVD	Pixel		GMSL1, Legacy	
88.3%	100%	100%	10k	OPEN		6		COAX	GMSL2	

Note a: Voltage divider resistor tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 or CFG1 input voltage to exceed the maximum or minimum limits.

Note b: Until the input voltage is latched, any load on CFG0 or CFG1 (other than R1 and R2) must be ≥ 25 x (R1 + R2). Load capacitance (including R1 and R2) must be lumped-load ≤ 10pF.

Note c: Each resistor in the voltage divider must be ≤ 100kΩ.

Note d: I²CSEL: I²C or UART interface select for SDA_RX and SCL_TX.

Note e: GMSL1 default BWS = 0 (24 bit).

GMSL1 Backwards Compatibility

The MAX96714/F/R are designed to pair with any GMSL1 serializer. However, some GMSL1 serializer features are not

supported. GMSL1 backwards compatibility is only supported with forward link rates from 500Mbps to 3.12Gbps and a reverse link rate of 1Mbps. When the MAX96714/F/R are paired with a legacy GMSL1-only serializer, they must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced to comply with the limitations of the specified GMSL1 serializer.

Table 10 specifies the availability of common GMSL2 features in GMSL2 devices operated in the GMSL1 mode. The MAX96714/F/R may not support all GMSL1 features in Table 10. Some GMSL2 features are only available in the GMSL2 mode, and thus, are not available in the GMSL1 mode. Disable the features not supported by both devices in a link.

Most features specified in Table 10 can be enabled/disabled by appropriate register configuration. Serializer and deserializer subsystems are responsible for implementing the configuration pin connections needed to achieve the desired settings. More information on how to connect to GMSL1 serializers can be found in the GMSL2 User Guide - pairing with GMSL1 serializer section.

Table 10. Feature Availability in GMSL1 Mode

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Bus Width Select (BWS)	Yes	Yes
High-Bandwidth Mode (HIBW)	Yes	Yes
Data Rate Select (DRS) (Low-Speed Mode)	Yes	Yes
DBL (Double Mode)	Yes	Yes
HSYNC/VSYNC Encoding	Yes	Yes
Pixel CRC (6 Bits per Pixel)	Yes	Yes
Video Line CRC (32 Bits per Line)	Yes	Yes
I^2C to I^2C	Yes	Yes
UART to UART	Yes	Yes
UART to I^2C	No	No
Pass-Through I^2C Channels	No	No
I^2C Address Translation	Yes	Yes
High-Immunity Mode	Yes	Yes
REV_FAST with HIBW Mode	Yes	Yes
Packet Control Channel with CRC	Yes	Yes
Packet CC Retransmission	Yes	Yes
Configuration Link	Yes	Yes
GPI to GPO on Reverse Channel	Yes	Yes
Frame Sync	Yes	Yes
Delay Compensated GPI/GPO	No	No
Line Fault	Yes	Yes
UART Base Mode	Yes	Yes
UART Bypass Mode	Yes	Yes
Spread Spectrum	Yes	Yes
Pre/Deemphasis	No	N/A
Legacy Programmable Equalization	N/A	No
Adaptive Equalization	N/A	Yes
Video Timing Generator	Yes	No
PRBS	Yes	Yes
CNTL0, 1, 2, 3 on Forward Channel	Yes	Yes

Table 10. Feature Availability in GMSL1 Mode (continued)

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
A/V Status Register Interrupt	No	No
HS/VS/DE Inversion	Yes	Yes

Power-Up and Link Startup

GMSL2 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer may power up in any order. After PWDNB is released and all power supplies are up, each device starts its power-up sequence and performs the following actions in sequence:

1. Set internal registers according to the selected configuration (selected by CFG0, CFG1).
2. Power-on self-test starts with MBIST followed by LBIST. Register REG_POST0 is updated after the POST completes. The chip is reset after the POST (only for MAX96714/F).
3. Device registers on local side are writable and readable through I^2C or UART.
4. GMSL2 PHYs perform link calibration, equalizer adaptation, and data-channel locking. Both chips set their LOCK pin high.
5. Device registers on remote side are writable and readable through GMSL channel.

Device Reset and Power Down

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. It resets all control registers to their defaults.
2. Setting RESET_LINK resets all GMSL PHY-related digital logic, and all data pipeline. After this bit is set, all control registers are still accessible through local reverse channel and their values are preserved. The link and data pipelines are held in RESET until RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related digital logic and all data pipeline and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Program registers that affect GMSL2 link operation (i.e., RX_RATE, CXTP, GMSL2) first, followed by RESET_ONESHOT, or set these registers when RESET_LINK = 1 and then set RESET_LINK = 0.

Asserting the PWDNB pin (active-low) places the device in power-down mode, and resets registers and device configurations to their power-up defaults. Any supply dropping below its internal threshold setting also places the device in power-down mode.

Link and Video Lock

GMSL2 Link Lock

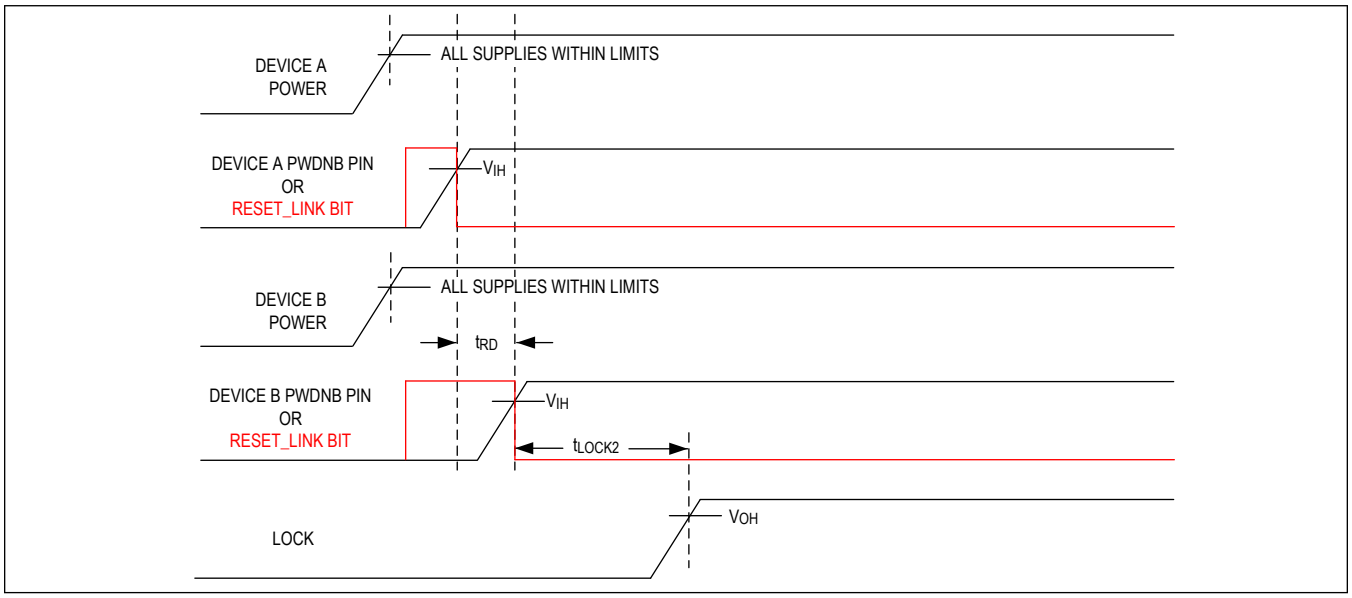


Figure 37. GMSL2 Lock Time

Figure 37 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C, GPIO) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in Note 9 of the Electrical Characteristics section. Contact the factory for guidance if this timing cannot be guaranteed.
7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.

8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register.

Error and Fault Condition Monitoring

The MAX96714/F/R have an open-drain, multipurpose error-reporting, and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers. So, the reason for assertion of ERRB can be determined by reading the register status. Errors can be automatically forwarded across the link from a serializer so that certain serializer errors, such as CSI-2 input-CRC errors, can be automatically flagged by the MAX96714/F/R's ERRB output.

Power Supplies Information, and Overvoltage and Undervoltage

There is no required sequence to bringing up the device power supplies. An on-chip power management block manages the power domains during power-up.

The MAX96714/F/R provides flexible power supply configurations.

The 1V core supply can be provided directly or through an internal low dropout (LDO) regulator. To minimize power dissipation, connect 1.0V ±5% to V_{DD}. If V_{DD} < 1.1V and CAP_VDD < 1.05V, the regulator is automatically disabled at power-up and low-resistance switches connect V_{DD} to the internal supply rails. For the internal regulator, connect 1.2V ±5% to V_{DD}. Following power-up, write REG_ENABLE = 1, then write REG_MNL = 1 as part of the device initialization to enable the internal LDO.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply. Connect 1.8V ±5%.

V_{TERM} is the D-PHY termination supply. Connect 1.2V ±5%.

Power supply ramp time recommendation: 20µs < ramp time < 2ms. Power supply ramps should be monotonic. Once the supply voltage has reached the minimum supply voltage limit, it should not be allowed to drop below the specification.

Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. See Table 2. See Table 1 for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

The MAX96714/F/R provides extensive power supply diagnostics capabilities. Overvoltage detection is also provided for all supply voltages except V_{DDIO}. As for undervoltage events, refer to the PWR0 register for information. An overvoltage (refer to INTR10 and PM_OV_STAT2/4 to enable) and undervoltage can be monitored with CMP_STATUS and V_{DDBAD}. The OV/UV situation can be reported by the ERRB pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an overvoltage situation, and the device continues to operate normally, although it may sustain damage depending on the duration and magnitude of the overvoltage event.

When relying on the ERRB pin to convey the occurrence of an undervoltage event, connect an external 1MΩ resistor between the ERRB pin and ground, because ERRB is not a power-up default MFP function. As a result, following a reset that is triggered by an undervoltage event, the ERRB MFP pin reverts to high impedance as opposed to ERRB. During an error state, the host device expects ERRB to drive logic-low, and the presence of the aforementioned resistor enables the appropriate logic level to be maintained following the reset, alerting the host device that attention is required.

PCB Layout Guidelines for GMSL

Proper circuit board design techniques are required for optimal GMSL link performance. This includes having at least a

four-layer board to provide a proper ground plane reference, adequate thermal impedance, DC supply pin bypassing, power-over-coax or line-fault design, and high-speed GMSL trace impedance matching. Refer to the GMSL2 Hardware Design Guide for more information.

Thermal Management

Power consumption of GMSL devices varies based on use case. The user must take care to provide sufficient heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedance.

System thermal management must keep the operating junction temperature below 125°C to avoid impacting device reliability.

Refer to Tutorial 4083, *Thermal Characterization of IC Packages* for guidance.

Register Map

Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

The GMSL2 equalizer requires register writes for optimal link margin.

Program the RLMS registers to optimize the link performance. After the register writes complete, perform a one-shot reset by writing bit RESET_ONESHOT=1 in register 0x10.

RLMS Register Setting for 6Gbps GMSL2 Rate: Required for all cable lengths.

- RLMS3F = 0x143F = 0x3D
- RLMS3E = 0x143E = 0xFD
- RLMS49 = 0x1449 = 0xF5
- RLMSA3 = 0x14A3 = 0x30
- RLMSD8 = 0x14D8 = 0x07
- RLMSA5 = 0x14A5 = 0x70

RLMS Register Setting for 3Gbps GMSL2 Rate: Required for all cable lengths.

- RLMS7F = 0x147F = 0x68
- RLMS7E = 0x147E = 0xA8
- RLMSA3 = 0x14A3 = 0x30
- RLMSD8 = 0x14D8 = 0x07
- RLMSA5 = 0x14A5 = 0x70

ADDRESS	NAME	MSB							LSB
DEV									
0x00	REG0[7:0]	DEV_ADDR[6:0]							CFG_BLOCK
0x01	REG1[7:0]	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	REG2[7:0]	–	–	VID_EN_Y	–	–	–	–	–
0x03	REG3[7:0]	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	–	–	–
0x05	REG5[7:0]	LOCK_EN	ERRB_EN	–	–	–	–	PU_LF1	PU_LF0
0x06	REG6[7:0]	–	GMSL2_A	–	I2CSEL	–	–	–	–
0x07	REG7[7:0]	CMP_VTERM_STATUS	–	–	–	–	–	–	–
0x0D	REG13[7:0]	DEV_ID[7:0]							
0x0E	REG14[7:0]	–	–	–	–	DEV_REV[3:0]			
0x26	REG26[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0x38	IO_CHK0[7:0]	PIN_DRV_EN_0[7:0]							
OVERLAP									

ADDRESS	NAME	MSB							LSB
TCTRL									
0x08	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x10	CTRL0[7:0]	RESET_ALL	RESET_LINK	RESET_ONESHOT	–	–	REG_ENABLE	–	–
0x11	CTRL1[7:0]	–	–	–	–	–	–	–	CXTP_A
0x12	CTRL2[7:0]	–	–	–	LDO_TEST	–	–	–	–
0x13	CTRL3[7:0]	–	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
0x18	INTR0[7:0]	–	–	–	LOCK_OEN	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x1A	INTR2[7:0]	–	–	–	–	LFLT_INT_OEN	IDLE_ERR_OEN	–	DEC_ERR_OEN_A
0x1B	INTR3[7:0]	–	–	REM_ERR_FLAG	–	LFLT_INT	IDLE_ERR_FLAG	–	DEC_ERR_FLAG_A
0x1C	INTR4[7:0]	–	EOM_ERR_OEN_A	–	–	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
0x1D	INTR5[7:0]	–	EOM_ERR_FLAG_A	–	–	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
0x1E	INTR6[7:0]	VDDCMP_INT_OEN	–	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
0x1F	INTR7[7:0]	VDDCMP_INT_FLAG	–	VDDBAD_INT_FLAG	FSYNC_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
0x21	INTR9[7:0]	ERR_RX_EN	ERR_RX_RECVED	–	ERR_RX_ID[4:0]				
0x22	CNT0[7:0]	DEC_ERR_A[7:0]							
GMSL									
0x29	TX1[7:0]	RSVD	–	–	ERRG_EN_A	–	–	–	–
0x2A	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2D	RX1[7:0]	LINK_PRBS_CHK	–	–	–	–	–	–	–
0x2F	RX3[7:0]	–	–	–	–	RSVD	–	–	–
0x30	GPIOA[7:0]	–	–	GPIO_FWD_CDLY[5:0]					
0x31	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC									
0x40	I2C_0[7:0]	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		

ADDRESS	NAME	MSB							LSB
0x48	UART_0[7:0]	–	–	REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x4C	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4D	I2C_PT_1[7:0]	–	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x4F	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	–	–	BITLEN_MAN_CFG_1	DIS_PAR_1	–	–
CFGH VIDEO_X									
0x50	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	–	–
CFGH VIDEO_Y									
0x51	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	–	–
CFGH VIDEO_Z									
0x52	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	–	–
CFGH VIDEO_U									
0x53	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	–	–
CFGI INFOFR									
0x60	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
CFGC CC									
0x70	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
0x75	ARQ0[7:0]	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
0x76	ARQ1[7:0]	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x77	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO									
0x78	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
0x7D	ARQ0[7:0]	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
0x7E	ARQ1[7:0]	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC IIC_X									
0x80	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x85	ARQ0[7:0]	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
0x86	ARQ1[7:0]	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC IIC_Y									
0x88	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
0x8D	ARQ0[7:0]	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
0x8E	ARQ1[7:0]	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_RX Y									
0x112	VIDEO_RX0[7:0]	LCRC_ERR	–	–	–	–	–	LINE_CRC_EN	–
0x118	VIDEO_RX6[7:0]	–	–	–	–	LIM_HEART	–	–	–
0x11A	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
0x11C	VIDEO_RX10[7:0]	VID_OVERFLOW	–	–	–	–	–	–	–
VIDEO_PIPE_SEL									
0x160	VIDEO_PIPE_EN[7:0]	–	–	–	–	–	–	VIDEO_PIPE_EN[1:0]	
0x161	VIDEO_PIPE_SEL[7:0]	–	–	–	–	–	VIDEO_PIPE_SEL_Y[2:0]		
VRX Y									
0x1E0	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1E1	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1E2	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1E3	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1E4	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1E5	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1E6	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				

ADDRESS	NAME	MSB							LSB
0x1E7	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1E8	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1E9	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1EA	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1EB	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1EC	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1ED	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1EE	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1EF	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1F0	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1F1	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1F2	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1F3	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1F4	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1F5	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1F6	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1F7	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1F8	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1F9	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1FA	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1FB	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1FC	VPRBS[7:0]	PATGEN_CLK_SRC	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x1FD	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1FE	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x1FF	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				

ADDRESS	NAME	MSB							LSB
VRX_PATGEN_0									
0x240	PATGEN_0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x241	PATGEN_1[7:0]	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
0x242	VS_DLY_2[7:0]	VS_DLY_2[7:0]							
0x243	VS_DLY_1[7:0]	VS_DLY_1[7:0]							
0x244	VS_DLY_0[7:0]	VS_DLY_0[7:0]							
0x245	VS_HIGH_2[7:0]	VS_HIGH_2[7:0]							
0x246	VS_HIGH_1[7:0]	VS_HIGH_1[7:0]							
0x247	VS_HIGH_0[7:0]	VS_HIGH_0[7:0]							
0x248	VS_LOW_2[7:0]	VS_LOW_2[7:0]							
0x249	VS_LOW_1[7:0]	VS_LOW_1[7:0]							
0x24A	VS_LOW_0[7:0]	VS_LOW_0[7:0]							
0x254	V2D_2[7:0]	V2D_2[7:0]							
0x255	V2D_1[7:0]	V2D_1[7:0]							
0x256	V2D_0[7:0]	V2D_0[7:0]							
0x257	DE_HIGH_1[7:0]	DE_HIGH_1[7:0]							
0x258	DE_HIGH_0[7:0]	DE_HIGH_0[7:0]							
0x259	DE_LOW_1[7:0]	DE_LOW_1[7:0]							
0x25A	DE_LOW_0[7:0]	DE_LOW_0[7:0]							
0x25B	DE_CNT_1[7:0]	DE_CNT_1[7:0]							
0x25C	DE_CNT_0[7:0]	DE_CNT_0[7:0]							
0x25D	GRAD_INCR[7:0]	GRAD_INCR[7:0]							
0x25E	CHKR_COLOR_A_L[7:0]	CHKR_COLOR_A_L[7:0]							
0x25F	CHKR_COLOR_A_M[7:0]	CHKR_COLOR_A_M[7:0]							
0x260	CHKR_COLOR_A_H[7:0]	CHKR_COLOR_A_H[7:0]							
0x261	CHKR_COLOR_B_L[7:0]	CHKR_COLOR_B_L[7:0]							
0x262	CHKR_COLOR_B_M[7:0]	CHKR_COLOR_B_M[7:0]							
0x263	CHKR_COLOR_B_H[7:0]	CHKR_COLOR_B_H[7:0]							
0x264	CHKR_RPT_A[7:0]	CHKR_RPT_A[7:0]							
0x265	CHKR_RPT_B[7:0]	CHKR_RPT_B[7:0]							
0x266	CHKR_ALT[7:0]	CHKR_ALT[7:0]							
GPIO0 0									
0x2B0	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B1	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B2	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				

ADDRESS	NAME	MSB							LSB
GPIO1 1									
0x2B3	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B4	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B5	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO2 2									
0x2B6	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B7	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B8	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO3 3									
0x2B9	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BA	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BB	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO4 4									
0x2BC	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BD	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BE	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO5 5									
0x2BF	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C0	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C1	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO6 6									
0x2C2	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C3	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C4	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO7 7									
0x2C5	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C6	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	NAME	MSB							LSB
0x2C7	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO8 8									
0x2C8	GPIO_A[7:0]	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C9	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CA	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
BACKTOP									
0x308	BACKTOP1[7:0]	–	–	CSIPLLY_LOCK	–	–	–	–	–
0x312	BACKTOP11[7:0]	–	–	cmd_overflow2	–	–	–	LMO_Y	–
0x313	BACKTOP12[7:0]	–	–	–	–	–	–	CSI_OUT_EN	–
0x314	BACKTOP13[7:0]	soft_vc_y[3:0]				–	–	–	–
0x316	BACKTOP15[7:0]	soft_dt_y_h[1:0]		–	–	–	–	–	–
0x317	BACKTOP16[7:0]	–	–	–	–	soft_dt_y_l[3:0]			
0x319	BACKTOP18[7:0]	–	–	–	soft_bpp_y[4:0]				
0x31C	BACKTOP21[7:0]	–	–	bpp8dbly	–	–	–	–	–
0x31D	BACKTOP22[7:0]	override_bpp_vc_dty	–	–	–	–	–	–	–
0x31F	BACKTOP24[7:0]	–	–	bpp8dbly_mode	–	–	–	–	–
0x320	BACKTOP25[7:0]	–	–	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
0x322	BACKTOP27[7:0]	–	–	yuv_8_10_mux_mode2	–	–	–	–	–
0x325	BACKTOP30[7:0]	BACKTOP_W_FRAME	–	–	–	–	–	–	–
0x327	BACKTOP32[7:0]	–	–	bpp10dbly_mode	–	–	–	bpp10dbly	–
MIPI_PHY									
0x330	MIPI_PHY0[7:0]	force_csi_out_en	–	–	–	–	–	–	–
0x331	MIPI_PHY1[7:0]	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
0x332	MIPI_PHY2[7:0]	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
0x333	MIPI_PHY3[7:0]	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x335	MIPI_PHY5[7:0]	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
0x338	MIPI_PHY8[7:0]	t_lpxesc[2:0]			–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x33F	MIPI_PHY15[7:0]	–	–	–	–	–	–	RST_MIPITX_LOC	–
0x340	MIPI_PHY16[7:0]	–	–	TUN_DATA_CRC_ERR_OEN	TUN_EC C_UNCORR_ERR_OEN	TUN_EC C_CORR_ERR_OEN	–	–	VID_OVERFLOW_OEN
0x341	MIPI_PHY17[7:0]	–	–	TUN_DATA_CRC_ERR	TUN_EC C_UNCORR_ERR	TUN_EC C_CORR_ERR	–	–	VID_OVERFLOW_FLAG
0x342	MIPI_PHY18[7:0]	–	–	–	–	csi2_tx1_pkt_cnt[3:0]			
0x344	MIPI_PHY20[7:0]	phy1_pkt_cnt[3:0]				–	–	–	–
FSYNC									
0x3E0	FSYNC_0[7:0]	–	–	FSYNC_OUT_PIN	–	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
0x3E1	FSYNC_1[7:0]	–	–	–	–	FSYNC_PER_DIV[3:0]			
0x3E2	FSYNC_2[7:0]	MST_LINK_SEL[2:0]			–	–	–	–	–
0x3E5	FSYNC_5[7:0]	FSYNC_PERIOD_L[7:0]							
0x3E6	FSYNC_6[7:0]	FSYNC_PERIOD_M[7:0]							
0x3E7	FSYNC_7[7:0]	FSYNC_PERIOD_H[7:0]							
0x3EF	FSYNC_15[7:0]	FS_GPIO_TYPE	FS_USE_XTAL	–	–	–	–	–	–
0x3F1	FSYNC_17[7:0]	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
0x3F6	FSYNC_22[7:0]	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	–	–	–	–	–	–
MIPI_TX 1									
0x441	MIPI_TX1[7:0]	MODE[7:0]							
0x442	MIPI_TX2[7:0]	STATUS[7:0]							
0x443	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x444	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x445	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x44A	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		–	–	CSI_VCX_EN	–	–	–
0x44B	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x44C	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x44D	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x44E	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x44F	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x450	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x451	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x452	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x453	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x454	MIPI_TX20[7:0]	MAP_DST_3[7:0]							

ADDRESS	NAME	MSB							LSB
0x455	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x456	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x457	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x458	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x459	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x45A	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x45B	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x45C	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x45D	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x45E	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x45F	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x460	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x461	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x462	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x463	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x464	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x465	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x466	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x467	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x468	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x469	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x46A	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x46B	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x46C	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x46D	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x46E	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x46F	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x470	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x472	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x473	MIPI_TX51[7:0]	TUN_WAIT_VS_START[2:0]			ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x474	MIPI_TX52[7:0]	TUN_NO_CORR	DESKEW_TUN[1:0]		–	–	–	–	TUN_EN
0x476	MIPI_TX54[7:0]	TUN_PKT_START_ADDR[7:0]							
MIPI_TX_EXT 1									
0x510	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x511	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x512	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x513	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–

ADDRESS	NAME	MSB							LSB
0x514	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x515	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x516	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x517	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x518	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x519	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x51A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x51B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x51C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x51D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x51E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x51F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MISC									
0x540	CFG_0[7:0]	VS_OUT 1	–	–	–	–	–	–	–
0x541	CFG_1[7:0]	VS_OUT 2	–	–	–	–	–	–	–
0x542	CFG_2[7:0]	HS_OUT 1	–	–	–	–	–	–	–
0x544	CFG_4[7:0]	HS_OUT 2	–	–	–	–	–	HVD_SYNC_LOCK_LOST_OEN	HVD_SYNC_LOCK_LOST
0x548	UART_PT_0[7:0]	BITLEN_PT_1_L[7:0]							
0x549	UART_PT_1[7:0]	–	–	BITLEN_PT_1_H[5:0]					
0x54A	UART_PT_2[7:0]	BITLEN_PT_2_L[7:0]							
0x54B	UART_PT_3[7:0]	–	–	BITLEN_PT_2_H[5:0]					
0x55A	BW_MEAS_1[7:0]	LFLT_STKY_INT	–	–	–	–	–	–	–
0x55C	CNT4[7:0]	VID_PXL_CRC_ERR0[7:0]							
0x569	UNLOCK_KEY[7:0]	UNLOCK_KEY[7:0]							
0x570	PIO_SLEW_0[7:0]	PIO03_SLEW[1:0]		PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
0x571	PIO_SLEW_1[7:0]	PIO07_SLEW[1:0]		–	–	–	–	–	–
0x572	PIO_SLEW_2[7:0]	PIO16_SLEW[1:0]		PIO12_SLEW[1:0]		PIO11_SLEW[1:0]		PIO08_SLEW[1:0]	
0x575	HS_VS_ACT_Y[7:0]	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
0x577	DP_ORSTB_CTL[7:0]	–	DP_RST_MIPI3_CHKB	DP_RST_STABLE_CHKB	DP_RST_MIPI2_CHKB	DP_RST_MIPI_CHKB	DP_RST_VP_CHKB	–	–
0x578	PM_OV_STAT2[7:0]	VTERM_OV_OEN	VREG_OV_OEN	–	–	–	–	–	–
0x579	PM_OV_STAT3[7:0]	VTERM_OV_FLAG	VREG_OV_FLAG	VDDIO_OV_FLAG	–	–	–	–	–
0x57A	PM_OV_STAT4[7:0]	VDDIO_OV_OEN	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x57B	FAULT_OEN[7:0]	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	GPIO_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
0x57C	FAULT_STAT[7:0]	LINE_INT_OPEN_FLAG	LINE_INT_L2LS_FLAG	LINE_INT_BAT_S_FLAG	LINE_INT_GND_S_FLAG	GPIO_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
CC_EXT									
0x808	UART_0[7:0]	–	–	REM_MS_EN_1	LOC_MS_EN_1	MS_LOC	BYPASS_TO_1[1:0]		BYPASS_EN_1
0x809	UART_1[7:0]	–	–	REM_MS_EN_2	LOC_MS_EN_2	–	BYPASS_TO_2[1:0]		BYPASS_EN_2
0x80E	I2C_PT_0[7:0]	–	I2C_REGSLV_0_TIMED_OUT	–	–	–	I2C_INTREG_SLV_TO[2:0]		
0x80F	I2C_PT_1[7:0]	I2C_REGSLV_2_TIMED_OUT	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]			I2C_INTREG_SLV_1_TO[2:0]		
GMSL1 A									
0xB04	GMSL1_4[7:0]	–	OUTENB	PRBSEN	CC_PORT_SEL[1:0]		–	REVCCEN	FWDCCEN
0xB05	GMSL1_5[7:0]	–	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xB06	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xB07	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xB08	GMSL1_8[7:0]	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xB0D	GMSL1_D[7:0]	I2C_LOC_ACK	–	–	–	–	–	–	–
0xB0E	GMSL1_E[7:0]	DET_THR[7:0]							
0xB0F	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xB10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xB11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xB12	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	–	–	LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xB13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xB14	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xB15	GMSL1_15[7:0]	DET_ERR[7:0]							

ADDRESS	NAME	MSB							LSB
0xB16	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xB17	GMSL1_17[7:0]	–	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xB19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xB1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xB1B	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xB1C	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xB1D	GMSL1_1D[7:0]	–	–	–	UNDER BOOST_DET	AEQ_BST[3:0]			
0xB96	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					–	CONV_GMSL1_EN	–
0xBA0	GMSL1_A0[7:0]	–	–	–	–	–	–	–	–
0xBA7	GMSL1_A7[7:0]	–	SHIFT_VID_HVD	–	–	–	–	–	–
0xBCB	GMSL1_CB[7:0]	–	–	–	–	–	–	–	LOCKED_G1
0xBD1	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1_COMMON									
0xF00	GMSL1_EN[7:0]	–	–	–	–	–	–	–	–
0xF02	COMMON1[7:0]	–	–	–	–	–	–	–	REM_ACK_ACKED_G1_A
0xF03	GMSL1_ERR_OEN[7:0]	–	–	–	–	–	–	–	G1_A_ERR_OEN
0xF04	GMSL1_ERR_FLAG[7:0]	–	–	–	–	–	–	–	G1_A_ERR_FLAG
0xF05	I2C_0[7:0]	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
0xF06	I2C_1[7:0]	EN_I2C_LOOPBACK	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
0xF0A	I2C_5[7:0]	–	–	–	–	–	–	–	–
RLMS A									
0x1403	RLMS3[7:0]	AdaptEn	–	–	–	–	–	–	–
0x1404	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	RLMS7[7:0]	EOM_DONE	EOM[6:0]						

ADDRESS	NAME	MSB							LSB
0x143E	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x143F	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x1449	RLMS49[7:0]	–	–	–	–	–	ErrChPwrUp	–	–
0x1464	RLMS64[7:0]	–	–	–	–	–	–	TxSSCMode[1:0]	
0x1470	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1471	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1473	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1475	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1476	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x147E	RLMS7E[7:0]	D2ErrChPhSecTA	D2ErrChPhSec[6:0]						
0x147F	RLMS7F[7:0]	D2ErrChPhPriTA	D2ErrChPhPri[6:0]						
0x1495	RLMS95[7:0]	TxAmplManEn	–	TxAmplMan[5:0]					
0x1498	RLMS98[7:0]	–	–	–	–	–	Rxhpf_cnt[2:0]		
0x14A3	RLMSA3[7:0]	DFEBST[3:0]				–	–	–	–
0x14A4	RLMSA4[7:0]	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x14A5	RLMSA5[7:0]	–	–	PHYC_WBLOCK_DLY[1:0]		–	–	–	–
0x14D8	RLMSD8[7:0]	–	–	–	–	sub_bst_trim[2:0]			sub_gain_ctrl
FUNC_SAFE									
0x3000	REGCRC0[7:0]	–	–	–	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
0x3001	REGCRC1[7:0]	CRC_PERIOD[7:0]							
0x3002	REGCRC2[7:0]	REGCRC_LSB[7:0]							
0x3003	REGCRC3[7:0]	REGCRC_MSB[7:0]							
0x3008	I2C_UART_CRC0[7:0]	–	–	–	–	–	–	–	RESET_MSGCNTR
0x3009	I2C_UART_CRC1[7:0]	MSGCNTR_ERR_THR[2:0]			CRC_ERR_THR[2:0]			RESET_MSGCNTR_ERR_CNT	RESET_CRC_ER_CNT
0x300A	I2C_UART_CRC2[7:0]	CRC_VAL[7:0]							
0x300B	I2C_UART_CRC3[7:0]	MSGCNTR_LSB[7:0]							
0x300C	I2C_UART_CRC4[7:0]	MSGCNTR_MSB[7:0]							
0x300D	I2C_UART_CRC5[7:0]	CRC_ERR_CNT[7:0]							

ADDRESS	NAME	MSB							LSB
0x300E	I2C_UART_CRC6[7:0]	MSGCNTR_ERR_CNT[7:0]							
0x300F	I2C_UART_CRC7[7:0]	–	–	–	MSGCNTR_PORT_SEL[1:0]		CC_MSGCNTR_EN	CC_CRC_EN	CC_CRC_MSGCNTR_OVR
0x3010	FS_INTR0[7:0]	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	EFUSE_CRC_ERR_OEN	REG_CRC_ERR_OEN
0x3011	FS_INTR1[7:0]	I2C_UART_MSGCNTR_ERR_INT	I2C_UART_CRC_ERR_INT	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	EFUSE_CRC_ERR_FLAG	REG_CRC_ERR_FLAG
0x3016	MEM_ECC0[7:0]	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
0x3017	MEM_ECC1[7:0]	MEM_ECC_ERR1_CNT[7:0]							
0x3018	MEM_ECC2[7:0]	MEM_ECC_ERR2_CNT[7:0]							
0x3020	REG_POST0[7:0]	POST_DONE	POST_MBIST_PASSED	POST_LBIST_PASSED	–	–	–	POST_RUN_MBIST	POST_RUN_LBIST
0x3030	REGCRC8[7:0]	SKIP0_LSB[7:0]							
0x3031	REGCRC9[7:0]	SKIP0_MSB[7:0]							
0x3032	REGCRC10[7:0]	SKIP1_LSB[7:0]							
0x3033	REGCRC11[7:0]	SKIP1_MSB[7:0]							
0x3034	REGCRC12[7:0]	SKIP2_LSB[7:0]							
0x3035	REGCRC13[7:0]	SKIP2_MSB[7:0]							
0x3036	REGCRC14[7:0]	SKIP3_LSB[7:0]							
0x3037	REGCRC15[7:0]	SKIP3_MSB[7:0]							
0x3038	REGCRC16[7:0]	SKIP4_LSB[7:0]							
0x3039	REGCRC17[7:0]	SKIP4_MSB[7:0]							
0x303A	REGCRC18[7:0]	SKIP5_LSB[7:0]							
0x303B	REGCRC19[7:0]	SKIP5_MSB[7:0]							
0x303C	REGCRC20[7:0]	SKIP6_LSB[7:0]							
0x303D	REGCRC21[7:0]	SKIP6_MSB[7:0]							
0x303E	REGCRC22[7:0]	SKIP7_LSB[7:0]							
0x303F	REGCRC23[7:0]	SKIP7_MSB[7:0]							
TCTRL_EXT									
0x5010	INTR10[7:0]	–	–	–	VDD18_OV_OEN	–	–	–	VDD_OV_OEN
0x5011	INTR11[7:0]	–	–	–	VDD18_OV_FLAG	–	–	–	VDD_OV_FLAG

Register Details

REG0 (0x0)

Device UART/I²C Address and Blocks UART/I²C Register Writes

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device I²C Address Default value is set by the CFG0 pin as follows: CFG0 Device Address 000 0b0101000 001 0b0101010 010 0b1001100 011 0b1101010 100 0b1101010 101 0b1001100 110 0b0101010 111 0b0101000	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 ... ... 0b1001000: I²C write/read address is 0x90/0x91 0b1001010: I²C write/read address is 0x94/0x95 0b1001100: I²C write/read address is 0x98/0x99 0b1101000: I²C write/read address is 0xD0/0xD1 0b1101010: I²C write/read address is 0xD4/0xD5 0b1101100: I²C write/read address is 0xD8/0xD9 0b0101000: I²C write/read address is 0x50/0x51 0b0101010: I²C write/read address is 0x54/0x55 ... ... 0b1111111: I²C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). Blocks writeable registers from being written. This bit can be used to freeze the chip configuration. After it is set, this bit becomes non-writable. To reset register to 'Not Blocked', the part is powered down or power cycled.	0b0: Not blocked 0b1: Blocked

REG1 (0x1)

GMSL Link Configuration

BIT	7	6	5	4	3	2	1	0
Field	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b00		0b10	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_2_EN	7	Enable pass-through I²C Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: I²C pass-through Channel 2 disabled 0b1: I²C pass-through Channel 2 enabled
IIC_1_EN	6	Enable pass-through I²C Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: I²C pass-through Channel 1 disabled 0b1: I²C pass-through Channel 1 enabled

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_CC	5	Disable control channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disable remote control channel Link A over GMSL2 connection from I2C/UART Channel 1 (SDA/RX, SCL/TX)	0b0: Remote control channel enabled 0b1: Remote control channel disabled
TX_RATE	3:2	Transmitter Rate When changed, becomes active after next link reset.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE	1:0	Receiver Rate When changed, becomes active after next link reset. Default value is set by configuration pins at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG2 (0x2)

Video Channel Y—GMSL2 Video Pipe Access

BIT	7	6	5	4	3	2	1	0
Field	–	–	VID_EN_Y	–	–	–	–	–
Reset	–	–	0b1	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_Y	5	Video Enable - Video switch used to access Pipe Y video flow.	0b0: Video transmit Pipe Y disabled 0b1: Video transmit Pipe Y enabled

REG3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	–	–	–
Reset	0b0	0b1	0b0	0b1	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	7	Configure LOCK pin behavior	0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started
PT_SWAP	6	Swap I2C/UART pass-through device pin assignments.	0b0: Do not swap pin assignments 0b1: Swap pin assignments
UART_2_EN	5	Enable pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Pass-through UART Channel 2 disabled 0b1: Pass-through UART Channel 2 enabled
UART_1_EN	4	Enable pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through UART Channel 1 disabled 0b1: Pass-through UART Channel 1 enabled

REG5 (0x5)

Enable LOCK/ERRB and Line Fault 0/1 Status

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	–	–	–	–	PU_LF1	PU_LF0
Reset	0b1	0b1	–	–	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enable LOCK output	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enable ERRB output	0b0: ERRB output disabled 0b1: ERRB output enabled
PU_LF1	1	Power up line-fault monitor 1	0b0: Line-fault monitor 1 disabled 0b1: Line-fault monitor 1 enabled
PU_LF0	0	Power up line-fault monitor 0	0b0: Line-fault monitor 0 disabled 0b1: Line-fault monitor 0 enabled

REG6 (0x6)

GMSL and UART/I^2C Configuration

BIT	7	6	5	4	3	2	1	0
Field	–	GMSL2_A	–	I2CSEL	–	–	–	–
Reset	–	0b1	–	0b0	–	–	–	–
Access Type	–	Write, Read	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL2_A	6	Bit is set according to the latched CFG pin value at power-up.	0x0: GMSL1 0x1: GMSL2
I2CSEL	4	I^2C/UART selection Bit is set according to the latched I2CSEL pin value at power-up.	0: UART 1: I^2C

REG7 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	CMP_VTERM_STATUS	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CMP_VTERM_STATUS	7	Power Manager V_{TERM} Comparator Status. Latched low when switched V_{TERM} supply < 1V. Cleared when the CMP_STATUS (Register 0x08) word is read and the switched V_{TERM} supply is > 1V.	0b0: V_{TERM} < 1V (latched low, read to clear) 0b1: V_{TERM} > 1V

REG13 (0xD)

Device Variant

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xC9							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device variant	0xC9: MAX96714 0xCA: MAX96714F 0xCB: MAX96714R

REG14 (0xE)

Device Revision

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DEV_REV[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision Starts with 0000; higher values indicate updated silicon. Contact factory for revision information.	0xX: Revision number

REG26 (0x26)

Line Fault Status

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line-fault status of wire connected to LMN1 pin.	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_0	2:0	Line-fault status of wire connected to LMN0 pin.	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

IO_CHK0 (0x38)

Video Pattern Generation PCLK Frequency Selection

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_EN_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_EN_0	7:0	Used to select Video Pattern Generation PCLK 0x2: 150MHz/375MHz, Use PATGEN_CLK_SRC (0x1FC, bit 7), to determine higher frequency PCLK	0x0: 25MHz PCLK 0x1: 75MHz PCLK 0x2: 150MHz/600MHz

PWR0 (0x8)

VDD, V_{DD18}, V_{DDIO}, and CAP_VDD undervoltage

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0b000			0b00000				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Switched 1V supply comparator status bits	0bXX1: Latched high when CAP_VDD < 0.82V 0bX1X: Latched high when CAP_VDD < 0.82V 0bX00: CAP_VDD > 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	V_{DD18}, V_{DDIO}, and CAP_VDD supply voltage comparator status bits	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when CAP_VDD < 0.82V 0bX0XXX: Reserved 0b0XXXX: Reserved 0bXX111: All supplies are at expected levels

CTRL0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	–	–	REG_ENABLE	–	–
Reset	0b0	0b0	0b0	–	–	0b0	–	–
Access Type	Write, Read	Write, Read	Write Clears All, Read	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Device Reset Writing a 1 to this bit resets the device including all blocks, and registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LINK	6	Link Reset Resets whole data path on Link A (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	One-Shot Link Reset Reset whole data path on Link A (keep register settings) in one-shot. Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path
REG_ENABLE	2	Enables V_{DD} LDO when set into manual LDO configuration. See LDO_TEST (0x12) to disable automatic LDO configuration.	0b0: V_{DD} LDO regulator disabled 0b1: V_{DD} LDO regulator enabled

CTRL1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CXTP_A
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_A	0	Coax/Twisted-pair cable select for Link A Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL2 (0x12)

LDO Override

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO_TEST	–	–	–	–
Reset	–	–	–	0b0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LDO_TEST	4	Enable LDO test to override LDO automatic detect.	0x0: Disable manual mode 0x1: Enable manual mode

CTRL3 (0x13)

GMSL2 LOCK, ERRB, CMU Clock Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL2 link locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	CMU Main Clock locked, crystal detection	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LOCK_OEN	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	–	–	–	0b0	0b0	0b000		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_OEN	4	Enables reporting of GMSL2 link lock status at ERRB pin.	0x0: Reporting disabled 0x1: Reporting enabled
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22), DEC_ERR_B (0x23) and IDLE_ERR (0x24) bitfields after ERRB pin is asserted for 1µs.	0b0: Autoreset disabled 0b1: Autoreset enabled
DEC_ERR_THR	2:0	Decoding and Idle-error Reporting Threshold. DEC_ERR_FLAG_A (0x1B) is asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR (0x18). IDLE_ERR_FLAG is asserted when IDLE_ERR ≥ DEC_ERR_THR (0x18).	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR2 (0x1A)

Line-Fault, Idle-Word, Decode-Error, and Memory Reporting

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LFLT_INT_OEN	IDLE_ERR_OEN	–	DEC_ERR_OEN_A
Reset	–	–	–	–	0b1	0b0	–	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OEN	3	Enables reporting of line-fault interrupt (LFLT_INT - 0x1B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_ OEN	2	Enables reporting of idle-word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_ OEN_A	0	Enable reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

0x1A Flags

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_ERR_ FLAG	–	LFLT_INT	IDLE_ERR_ FLAG	–	DEC_ERR_ FLAG_A
Reset	–	–	0b0	–	0b0	0b0	–	0b0
Access Type	–	–	Read Only	–	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_F LAG	5	Received remote side error status (inverse of remote side ERRB pin level)	0b0: No remote side error 0b1: Remote side error
LFLT_INT	3	Line-fault interrupt Asserted when either one of the line-fault monitors indicates a fault status. See LF_0 (0x26), LF_1 (0x26), and LFLT_STKY (0x55A) bitfields for more info. Is sticky if LFLT_STKY bit is set.	0b0: No line fault 0b1: Line fault
IDLE_ERR_F LAG	2	Idle word-error flag Asserted when IDLE_ERR ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_F LAG_A	0	Decoding error flag for Link A Asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	–	EOM_ERR_ OEN_A	–	–	MAX_RT_O EN	RT_CNT_O EN	PKT_CNT_ OEN	–
Reset	–	0b0	–	–	0b1	0b0	0b0	–
Access Type	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_ OEN_A	6	Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A - 0x1D) for Link A at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OE N	3	Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OEN	2	Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enable reporting of packet count flag (PKT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

EOM and ARQ Flags

BIT	7	6	5	4	3	2	1	0
Field	–	EOM_ERR_FLAG_A	–	–	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
Reset	–	0b0	–	–	0b0	0b0	0b0	–
Access Type	–	Read Only	–	–	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_A	6	Eye-opening is below configured threshold	0b0: No EOM error 0b1: EOM error
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag. Asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ retransmission event flag. Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet count flag, asserted when PKT_CNT (0x25) ≥ PKT_CNT_THR (0x19)	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)

V_{DD}, FSYNC, LCRC, V_{PRBS}, and Video Pixel CRC Reporting

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	–	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
Reset	0b0	–	0b0	0b1	0b1	0b1	–	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enable reporting of V_{DDCMP} interrupt (VDDCMP_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_INT_OEN	5	Enable reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
FSYNC_ERR_OEN	4	Enable reporting of frame sync errors (FSYNC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LCRC_ERR_OEN	3	Enable reporting of video line CRC errors (LCRC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VPRBS_ERR_OEN	2	Enable reporting of video PRBS errors (VPRBS_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VID_PXL_CRC_ERR_OEN	0	Video pixel CRC error counter interrupt output enable	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

V_{DD}, FSYNC, LCRC, V_{PRBS}, and Video Pixel CRC Flag

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	–	VDDBAD_INT_FLAG	FSYNC_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
Reset	0b0	–	0b0	0b0	0b0	0b0	–	0b0
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	V_{DDCMP} interrupt flag	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	V_{DD} status interrupt	0b0: Flag not asserted 0b1: Flag asserted
FSYNC_ERR_FLAG	4	Frame sync error flag Asserted when FSYNC_ERR_CNT (0x3F0) ≥ FSYNC_ERR_THR (0x3F1).	0b0: Flag not asserted 0b1: Flag asserted
LCRC_ERR_FLAG	3	Video line CRC error flag Asserted when a video line CRC error is detected.	0b0: Flag not asserted 0b1: Flag asserted
VPRBS_ERR_FLAG	2	Video PRBS error flag Asserted when VPRBS_ERR (register PRBS_ERR) > 0	0b0: Flag not asserted 0b1: Flag asserted
VID_PXL_CRC_ERR	0	Video pixel CRC error counter interrupt	0b0: Error counter interrupt output not enabled 0b1: Error counter interrupt output enabled

INTR9 (0x21)

GPIO ID, Remote, and Serializer Errors

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	ERR_RX_RECVED	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0b11111				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Enable receiving of serializer error status to deserializer side through available GPIO on deserializer.	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_RECVED	6	Received serializer error	0x0: Error detected 0x1: No error
ERR_RX_ID	4:0	Set GPIO ID to not conflict with other MFP pin GPIO_IDs already in use. There ARE 32 available GPIO IDs that can be used.	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

Decoding Errors

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected. Reset after reading or with the rising edge of LOCK.	0xXX: Number decoding errors detected

TX1 (0x29)

GMSL Reverse-Channel Link Error Generator

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN_A	–	–	–	–
Reset	0b0	–	–	0b0	–	–	–	–
Access Type	Write, Read	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Enable link PRBS-7 generator	
ERRG_EN_A	4	Random GMSL Reverse channel link-error injection,causes GMSL link errors, refer to 0x2A.	0b0: Link A error generator disabled 0b1: Link A error generator enabled

TX2 (0x2A)

Reverse-Channel Link Error Settings

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit-error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Error generator burst-error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error-distribution selection	0b0: Pseudorandom 0b1: Periodic

RX1 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_CHK	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
LINK_PRBS_CHK	7	Enable link PRBS-7 checker

RX3 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	–	–	–
Reset	–	–	–	–	0b0	–	–	–
Access Type	–	–	–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION
RSVD	3	Link PRBS is synced to incoming data

GPIOA (0x30)

GPIO Forward-Channel Delay Compensation

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_FWD_CDLY[5:0]					
Reset	–	–	0b000001					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)

GPIO Reverse-Channel Bandwidth Utilization

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwdith usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)

I²C Clock Stretching for Various GMSL Configurations

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I²C-to-I²C subordinate-setup and hold-time setting. Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate.	0b00: Set for I²C Fast-mode Plus speed (1Mb/s) 0b01: Set for I²C Fast-mode speed (400kb/s) 0b10: Set for I²C standard-mode speed (100kb/s) 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO	2:0	I²C-to-I²C subordinate timeout setting. Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

UART_0 (0x48)

Bypass for UART

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	–	–	0b0	0b0	0b0	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN	5	Enables UART Bypass Mode Control by Remote GPIO Pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN	4	Enables UART CC Port bypass mode control by local MFP pin (the MS function). Please see MS_LOC register field for MFP pin selection of MS function (at address 0x808). Set to enable MS pin for UART CC Port (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode. **Note:** Only one UART port may use the MS function at any given time. Mulitple UART ports are NOT simultaneously supported.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART Soft-Bypass Timeout Duration When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled

BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_EN	0	Enable UART Soft-Bypass Mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for the selected duration (configured by BYPASS_TO bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

I2C_PT_0 (0x4C)

I²C Subordinate Pass-Through Speed and Timeout Selection

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-through I²C-to-I²C Subordinate Setup and Hold Time Setting (Setup, Hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate.	0b00: Set for I²C Fast-mode Plus speed (1Mb/s) 0b01: Set for I²C Fast-mode speed (400kb/s) 0b10: Set for I²C Standard-mode speed (100kb/s) 0b11: Reserved
SLV_TO_PT	2:0	Pass-Through I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_1 (0x4D)

I²C Subordinate Pass-Through Speed and Timeout Selection

BIT	7	6	5	4	3	2	1	0
Field	–	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	–	0b101			–	0b110		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT	6:4	Pass-Through I2C-to-I2C Main Bit-Rate Setting Configures the I2C bit rate used by the internal I2C main (in the device on the remote side from the external I2C main). Set according to the I2C speed mode.	0b000: 9.92Kbps - Set for I2C Standard mode speed 0b001: 33.2Kbps - Set for I2C Standard mode speed 0b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 0b011: 123Kbps - Set for I2C Fast-mode speed 0b100: 203Kbps - Set for I2C Fast-mode speed 0b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I2C Fast-mode Plus speed 0b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_PT	2:0	Pass-Through I2C-to-I2C Main Timeout Setting Internal GMSL2 I2C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

UART_PT_0 (0x4F)

UART Custom Bit Rate

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	–	–	BITLEN_MAN_CFG_1	DIS_PAR_1	–	–
Reset	0b1	0b0	–	–	0b1	0b0	–	–
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Use the custom UART bit rate (selected by the BITLEN_PT_2_L - 0x548 and BITLEN_PT_2_H - 0x549 bitfields) in pass-through UART Channel 2.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disable parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
BITLEN_MAN_CFG_1	3	Use the custom UART bit rate (selected by the BITLEN_PT_1_L - 0x54A and BITLEN_PT_1_H - 0x54B bitfields) in pass-through UART Channel 1.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disable parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled

RX0 (0x50)

CRC for Forward-Channel GMSL Link

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	GMSL Video packet CRC Utilizes GMSL 6Gbps bandwidth, refer to CRC section for bandwidth information. Pipe X serializer side (default)	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled

RX0 (0x51)

CRC for Forward-Channel GMSL Link Default

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	GMSL Video packet CRC Utilizes GMSL 6Gbps bandwidth, refer to CRC section for bandwidth information Pipe Y serializer side (default)	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled

RX0 (0x52)

CRC for Forward-Channel GMSL Link Default

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	GMSL Video packet CRC Utilizes GMSL 6Gbps bandwidth, refer to CRC section for bandwidth information Pipe Z serializer side (default)	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled

RX0 (0x53)

CRC for Forward-Channel GMSL Link Default

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	GMSL Video packet CRC Utilizes GMSL 6Gbps bandwidth, refer to CRC section for bandwidth information Pipe U serializer side (default)	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled

TR0 (0x60)

Info Frame—CRC Setup

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Reverse-channel Info frame ACK CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	Forward-channel Info frame CRC enable	0b0: Receive CRC disabled 0b1: Receive CRC enabled

TR0 (0x70)

PRIMARY CC—CRC Setup

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Reverse channel Control Channel CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	Forward channel Control Channel CRC enable	0b0: Receive CRC disabled 0b1: Receive CRC enabled

ARQ0 (0x75)

PRIMARY CC—ARQ Enable

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
Reset	–	–	–	–	0b1	0b0	–	–
Access Type	–	–	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RETX	2	Disable retransmission due to receiving same acknowledge twice.	0b0: Enabled 0b1: Disabled

ARQ1 (0x76)

PRIMARY CC—ARQ Setup

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - 0x616) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x77)

PRIMARY CC—ARQ Count

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x78)

GPIO—CRC Setup

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Reverse channel GPIO CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	Forward channel GPIO CRC enable	0b0: Receive CRC disabled 0b1: Receive CRC enabled

ARQ0 (0x7D)

GPIO—ARQ Enable

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
Reset	–	–	–	–	0b1	0b0	–	–
Access Type	–	–	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RETX	2	Disable retransmission due to receiving same acknowledge twice.	0b0: Enabled 0b1: Disabled

ARQ1 (0x7E)

GPIO—ARQ Setup

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - 0x616) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x7F)

GPIO—ARQ Setup

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x80)

Pass-Through 1 CC—CRC Setup

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Reverse Channel Pass-Through Channel 1 CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	Forward Channel Pass-Through Channel 1 CRC enable	0b0: Receive CRC disabled 0b1: Receive CRC enabled

ARQ0 (0x85)

Pass-Through 1—ARQ Enable

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
Reset	–	–	–	–	0b1	0b0	–	–
Access Type	–	–	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RETX	2	Disable retransmission due to receiving same acknowledge twice.	0b0: Enabled 0b1: Disabled

ARQ1 (0x86)

Pass-Through 1—ARQ Setup

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - 0x616) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87)

Pass-Through 1—ARQ Count

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x88)

Pass-Through 2 CC—CRC Setup

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Reverse Channel Pass-Through Channel 2 CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	Forward Channel Pass-Through Channel 2 CRC enable	0b0: Receive CRC disabled 0b1: Receive CRC enabled

ARQ0 (0x8D)

Pass-Through 2—ARQ Enable

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN	DIS_DBL_ACK_RETX	–	–
Reset	–	–	–	–	0b1	0b0	–	–
Access Type	–	–	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RETX	2	Disable retransmission due to receiving same acknowledge twice.	0b0: Enabled 0b1: Disabled

ARQ1 (0x8E)

Pass-Through 2—ARQ Setup

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - 0x616) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x8F)

\Pass-Through 2—ARQ Count

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

VIDEO_RX0 (0x112)

Video Line CRC

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	–	–	–	–	–	LINE_CRC_EN	–
Reset	0b0	–	–	–	–	–	0b1	–
Access Type	Read Clears All	–	–	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag	0b0: No video line CRC detected 0b1: Video line CRC detected
LINE_CRC_EN	1	Video Line CRC Enable	0b0: Video line CRC disabled 0b1: Video line CRC enabled

VIDEO_RX6 (0x118)

Heartbeat

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LIM_HEART	–	–	–
Reset	–	–	–	–	0b0	–	–	–
Access Type	–	–	–	–	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LIM_HEART	3	Disable heartbeat during blanking	0b0: Heartbeat enabled during blanking 0b1: Heartbeat disabled during blanking

VIDEO_RX8 (0x11A)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Read Clears All	Read Only	Read Only	Read Clears All	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx block-length error detected	0b0: No error detected 0b1: Video Rx block-length error detected
VID_LOCK	6	Video pipeline locked	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Sufficient video Rx packet throughput detected	0b0: Not enough throughput 0b1: Sufficient throughput detected
VID_SEQ_ERR	4	Video Rx sequence error has occurred	0b0: No error detected 0b1: Error detected

VIDEO_RX10 (0x11C)

BIT	7	6	5	4	3	2	1	0
Field	VID_OVERFLOW	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VID_OVERFLOW	7	Sticky bit for overflow detected in video Rx buffers, read to clear.	0: No error detected 1: Error detected

VIDEO_PIPE_EN (0x160)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VIDEO_PIPE_EN[1:0]	
Reset	–	–	–	–	–	–	0b01	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_EN	1:0	it 0 enables/disables PIPE Y. Bit 1 is reserved.	0b00: Disable pipe Y 0b01: Enable Pipe Y (Defailt) 0b1X: Reserved (Do not use)

VIDEO_PIPE_SEL (0x161)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	VIDEO_PIPE_SEL_Y[2:0]		
Reset	–	–	–	–	–	0b010		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_Y	2:0	Bits [1:0] select the video stream that is routed to video pipe Y (des). Bit [2] is reserved.	0b000: Select Stream 0 0b001: Select Stream 1 0b010: Select Stream 2 (default) 0b011: Select Stream 3 0b1XX: Reserved (do not use)

CROSS_0 (0x1E0)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

CROSS_1 (0x1E1)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0b0	0b0	0b00001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x1E2)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0b0	0b0	0b00010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x1E3)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0b0	0b0	0b00011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

CROSS_4 (0x1E4)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0b0	0b0	0b00100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS4_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x1E5)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0b0	0b0	0b00101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x1E6)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0b0	0b0	0b00110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

CROSS_7 (0x1E7)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0b0	0b0	0b00111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x1E8)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0b0	0b0	0b01000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x1E9)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0b0	0b0	0b01001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

CROSS_10 (0x1EA)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0b0	0b0	0b01010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10	0bXXXXX: Incoming bit position

CROSS_11 (0x1EB)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0b0	0b0	0b01011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x1EC)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0b0	0b0	0b01100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

CROSS_13 (0x1ED)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0b0	0b0	0b01101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x1EE)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0b0	0b0	0b01110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x1EF)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0b0	0b0	0b01111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

CROSS_16 (0x1F0)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0b0	0b0	0b10000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x1F1)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0b0	0b0	0b10001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x1F2)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0b0	0b0	0b10010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

CROSS_19 (0x1F3)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0b0	0b0	0b10011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x1F4)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0b0	0b0	0b10100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x1F5)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0b0	0b0	0b10101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

CROSS_22 (0x1F6)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0b0	0b0	0b10110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x1F7)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0b0	0b0	0b10111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

CROSS_HS (0x1F8)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
Reset	–	0b0	0b0	0b11000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_HS_I	6	Invert CROSS_HS	0b0: Do not invert bit 0b1: Invert bit
CROSS_HS_F	5	Force CROSS_HS to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_HS	4:0	Map selected internal signal to HS	0bXXXXX: Incoming bit position

CROSS_VS (0x1F9)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
Reset	–	0b0	0b0	0b11001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_VS_I	6	Invert CROSS_VS	0b0: Do not invert bit 0b1: Invert bit
CROSS_VS_F	5	Force CROSS_VS to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_VS	4:0	Map selected internal signal to VS	0bXXXXX: Incoming bit position

CROSS_DE (0x1FA)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
Reset	–	0b0	0b0	0b11010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_DE_I	6	Invert CROSS_DE	0b0: Do not invert bit 0b1: Invert bit
CROSS_DE_F	5	Force CROSS_DE to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_DE	4:0	Map selected internal signal to DE	0bXXXXX: Incoming bit position

PRBS_ERR (0x1FB)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS error counter, clears on read	0xXX: Number of video PRBS errors since last read

VPRBS (0x1FC)

BIT	7	6	5	4	3	2	1	0
Field	PATGEN_CLK_SRC	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
Reset	0b1	–	0b0	0b0	–	–	–	0b0
Access Type	Write, Read	–	Read Only	Write, Read	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PATGEN_CLK_SRC	7	Pattern-generator clock source for video checkerboard, and gradient patterns	0x0: 150MHz 0x1: 600MHz (default)
VPRBS_FAIL	5	Video PRBS check pass/fail	0b0: Video PRBS check passed 0b1: Video check failed
VPRBS_CHK_EN	4	Enable video PRBS checker	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled
VIDEO_LOCK	0	Video channel is locked and outputting valid video data	0b0: Video channel not locked 0b1: Video channel locked

CROSS_27 (0x1FD)

BIT	7	6	5	4	3	2	1	0
Field	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	0b0	0b0	0b0	0b11011				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_CROSSBAR	7	Selects whether to use the crossbar in the VRX block or the alternative crossbar in the RDP.	0x0: Use crossbar in VRX block 0x1: Use crossbar in RDP
CROSS27_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Map selected internal signal to CrossX	0bXXXXX: Incoming bit position

CROSS_28 (0x1FE)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0b0	0b0	0b11100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28	4:0	Map selected internal signal to CrossX	0bXXXXX: Incoming bit position

CROSS_29 (0x1FF)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0b0	0b0	0b11101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Map selected internal signal to CrossX	0bXXXXX: Incoming bit position

PATGEN_0 (0x240)

Pattern Generator Control

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Invert VSYNC output of video-timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Invert HSYNC output of video-timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Invert DE output of video-timing generator	0b0: Do not invert DE 0b1: Invert DE

BITFIELD	BITS	DESCRIPTION	DECODE
VTG_MODE	1:0	Video interface timing generation mode. 00 = VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After the VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or power-up, the next VS input edge is assumed to be the right VS edge. 01 = VS one-trigger mode One VS input edge triggers the generation of ONE frame of VSO/HSO/DEO. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO. 10 = Auto-repeat mode (default) The VS input edge triggers the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO. 11 = Free-running mode	0b00: VS tracking mode VS input's period (VS_HIGH + VS_LOW) is tracked. After the VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or at power-up, the next VS input edge is assumed to be the right VS edge. 0b01: VS one-trigger mode One VS input edge triggers the generation of one frame of VSO/HSO/DEO. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time point of the rising edge of the newly generated VSO/HSO/DEO. 0b10: Auto-repeat mode VS input edge triggers the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time point of the rising edge of the newly generated VSO/HSO/DEO. 0b11: Free-running mode Automatically starts generating the pattern relying on VS input.

PATGEN_1 (0x241)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
Reset	0b0	–	0b00		–	–	–	0b0
Access Type	Write, Read	–	Write, Read		–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	7	Gradient Pattern-Generator Mode	0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00
PATGEN_MODE	5:4	Pattern-Generator Mode	0b00: Pattern generator disabled - use video from the serializer input (default) 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved
VS_TRIG	0	Select VS trigger edge	0b0: Falling edge 0b1: Rising edge

VS_DLY_2 (0x242)

VSYNC Delay

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VSYNC Delay Enable GEN_VS (0x240) to use VSYNC delay feature. Each bit enabled delays the VSYNC by 1 PCLK. Following examples delay VSYNC by 257 PCLKs: 0x242: 0x00000000 [MSB], 0 PCLK 0x243: 0x00000001, 256 PCLK 0x244: 0x00000001 [LSB], 1 PCLK	0xXX: Most significant byte of VS delay

VS_DLY_1 (0x243)

VSYNC Delay

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VSYNC Delay Enable GEN_VS (0x240) to use VSYNC delay feature. Each bit enabled delays the VSYNC by 1 PCLK. Following examples delay VSYNC by 257 PCLKs: 0x242: 0x00000000 [MSB], 0 PCLK 0x243: 0x00000001, 256 PCLK 0x244: 0x00000001 [LSB], 1 PCLK	0xXX: Middle significant byte of VS delay

VS_DLY_0 (0x244)

VSYNC Delay

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VSYNC Delay Enable GEN_VS (0x240) to use VSYNC delay feature. Each bit enabled delays the VSYNC by 1 PCLK. Following examples delay VSYNC by 257 PCLKs: 0x242: 0x00000000 [MSB], 0 PCLK 0x243: 0x00000001, 256 PCLK 0x244: 0x00000001 [LSB], 1 PCLK	0xXX: Least significant byte of VS delay

VS_HIGH_2 (0x245)

VSYNC High Period to PCLK Cycles [24:16] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS high period

VS_HIGH_1 (0x246)

VSYNC High Period to PCLK Cycles [15:8] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS high period

VS_HIGH_0 (0x247)

VSYNC High Period to PCLK Cycles [7:0] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS high period

VS_LOW_2 (0x248)

VSYNC Low Period to PCLK Cycles [24:16] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS low period

VS_LOW_1 (0x249)

VSYNC Low Period to PCLK Cycles [15:8] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS low period

VS_LOW_0 (0x24A)

VSYNC Low Period to PCLK Cycles [7:0] Bits

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS low period

V2D_2 (0x254)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS edge to first DE

V2D_1 (0x255)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS edge to first DE

V2D_0 (0x256)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([23:16])	0xXX: Least significant byte of VS edge to first DE

DE_HIGH_1 (0x257)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles ([15:8])	0xXX: Most significant byte of DE high period

DE_HIGH_0 (0x258)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of DE high period

DE_LOW_1 (0x259)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles ([15:8])	0xXX: Most significant byte of DE low period

DE_LOW_0 (0x25A)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of DE low period

DE_CNT_1 (0x25B)

Data Enable Count—Used for Pattern Generation

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame ([15:8])	0xXX: Most significant byte of DE pulses per frame

DE_CNT_0 (0x25C)

Data Enable Count—Pattern Generation Function

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame ([7:0])	0xXX: Least significant byte of DE pulses per frame

GRAD_INCR (0x25D)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INCR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INCR	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)	0xXX: Gradient increment base

CHKR_COLOR_A_L (0x25E)

Refer to User Guide for Information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_L	7:0	Checkerboard mode Color A low byte	0xXX: Least significant byte of checkerboard mode Color A

CHKR_COLOR_A_M (0x25F)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_M	7:0	Checkerboard mode Color A middle byte	0xXX: Middle significant byte of checkerboard mode Color A

CHKR_COLOR_A_H (0x260)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_H	7:0	Checkerboard mode Color A high byte	0xXX: Most significant byte of checkerboard mode Color A

CHKR_COLOR_B_L (0x261)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_L	7:0	Checkerboard mode Color B low byte	0xXX: Least significant byte of checkerboard mode Color B

CHKR_COLOR_B_M (0x262)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_M	7:0	Checkerboard mode Color B middle byte	0xXX: Middle significant byte of checkerboard mode Color B

CHKR_COLOR_B_H (0x263)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_H	7:0	Checkerboard mode Color B high byte	0xXX: Most significant byte of checkerboard mode Color B

CHKR_RPT_A (0x264)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode Color A repeat count	0xXX: Repeat count of checkerboard mode Color A

CHKR_RPT_B (0x265)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode Color B repeat count	0xXX: Repeat count of checkerboard mode Color B

CHKR_ALT (0x266)

Refer to User Guide for information

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

GPIO_A (0x2B0)

GPIO Configuration for MFP0

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2B1)

GPIO Output Type and Tx ID for MFP0

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No Pullup/Pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2B2)

GPIO Link A RX ID for MFP0

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00000				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set, use RES_CFG and PULL_UPDN_SEL	0b0: Non-override configuration 0b1: Override default configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B3)

GPIO Configuration for MFP1

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2B4)

GPIO Output Type and Tx ID for MFP1

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00001				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Enabled 0b1: Disabled
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2B5)

GPIO Link A RX ID for MFP1

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00001				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B6)

GPIO Configuration for MFP2

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2B7)

GPIO Output Type and Tx ID for MFP2

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00010				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2B8)

GPIO Link A Rx ID for MFP2

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00010				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B9)

GPIO Configuration for MFP3

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2BA)

GPIO Output Type and Tx ID for MFP3

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00011				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2BB)

GPIO Link A Rx ID for MFP3

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00011				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BC)

GPIO Configuration for MFP4

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2BD)

GPIO Output Type and Tx ID for MFP4

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2BE)

GPIO Link A Rx ID for MFP4

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00100				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BF)

GPIO Configuration for MFP5

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2C0)

GPIO Output Type and Tx ID for MFP5

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00101				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2C1)

GPIO Link A Rx ID for MFP5

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00101				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C2)

GPIO Configuration for MFP6

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2C3)

GPIO Output Type and Tx ID for MFP6

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00110				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2C4)

GPIO Link A Rx ID for MFP6

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00110				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C5)

GPIO Configuration for MFP7

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2C6)

GPIO Output Type and Tx ID for MFP7

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00111				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2C7)

GPIO Link A Rx ID for MFP7

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b00111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C8)

GPIO Configuration for MFP8

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	GPIO internal resistor value selection	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enable GPIO Delay compensation	0b0: Enabled 0b1: Disabled
GPIO_OUT	4	GPIO FORCED output value when GPIO_RX_EN = 0	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_IN	3	GPIO - value reported at Deserializer pin	0b0: GPIO = 0 0b1: GPIO = 1
GPIO_RX_EN	2	GPIO Receive Control This bit is used to receive GPIO transmission from serializer.	0b0: Disabled 0b1: Enabled
GPIO_TX_EN	1	GPIO Transmit Control This bit is used to control GPIO transmission to serializer.	0b0: Disabled 0b1: Enabled
GPIO_OUT_DIS	0	Disable GPIO0 Output Driver When ENABLED output can be driven from deserializer When DISABLED output can NOT be driven from deserializer	0b0: Enabled 0b1: Disabled

GPIO_B (0x2C9)

GPIO Output Type and Tx ID for MFP8

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	GPIO internal resistor configuration	0b00: No pullup/pulldown 0b01: Pullup 0b10: Pulldown 0b11: RSVD
OUT_TYPE	5	GPIO Internal Driver Selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	Transmit ID for GPIO to Map GPIO to appropriate MFP pins on serializer	0bXXXXX: Default MFP0 transmit ID is set to 0x000000

GPIO_C (0x2CA)

GPIO Link A Rx ID for MFP8

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0b0	–	–	0b01000				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Used to override default internal resistor configuration value. When set use RES_CFG and PULL_UPDN_SEL.	0b00: Non-override configuration 0b01: Override default Configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

BACKTOP1 (0x308)

CSI Controller Lock Indication

BIT	7	6	5	4	3	2	1	0
Field	–	–	CSIPLLY_LOCK	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLLY_LOCK	5	CSI controller clock status	0b0: CSI controller not locked 0b1: CSI controller locked

BACKTOP11 (0x312)

Memory Overflow

BIT	7	6	5	4	3	2	1	0
Field	–	–	cmd_overflow2	–	–	–	LMO_Y	–
Reset	–	–	0b0	–	–	–	0b0	–
Access Type	–	–	Read Only	–	–	–	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow2	5	Occurs when MIPI clock is not set correctly or too "slow" • Occurs when MIPI data is routed to the wrong CSI controller	0x0: No Command FIFO overflow 0x1: Command FIFO overflow detected
LMO_Y	1	Video Pipe Overflow • Occurs when video bandwidth is too high compared to MIPI output • Also occurs when line is over 4086 pixels	0b0: Pipeline Y no line memory overflow 0b1: Pipeline Y line memory overflow

BACKTOP12 (0x313)

CSI Output Enable

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CSI_OUT_EN	–
Reset	–	–	–	–	–	–	0b1	–
Access Type	–	–	–	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
CSI_OUT_EN	1	Enables/Disables all MIPI Outputs and puts MIPI into LP11 state. • Start - Does not wait for MIPI Frame Start or Frame End, sends data on the next received video line • Stop - Occurs immediately	0b0: CSI output disabled 0x1: CSI output enabled

BACKTOP13 (0x314)

Software Virtual Channel Override

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_y[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_y	7:4	Software virtual channel override • Setting to 0 = Virtual Channel 0 • To allow override of software VC's, override_bpp_vc_dty (0x31D) needs to be enabled.	0xX: Software-defined virtual channel for Pipeline Y

BACKTOP15 (0x316)

MIPI Software Data Type Override (high bits)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_y_h[1:0]		–	–	–	–	–	–
Reset	0b00		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_y_h	7:6	Combine with register soft_dt_y_l (0x317) (low bits for data type) Example: RAW12 = 0x2C Soft_dt_y_h = 0x80 Soft_dt_y_l = 0x0C To allow override of software data type, override_bpp_vc_dty (0x31D) needs to be enabled.	0bXX: High bits of software-defined data type for Pipeline Y

BACKTOP16 (0x317)

MIPI Software Data Type Override (low bits)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	soft_dt_y_l[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
soft_dt_y_l	3:0	Combine with register soft_dt_y_h (0x316) (high bits for data type) Example: RAW12 = 0x2C Soft_dt_y_h = 0x80 Soft_dt_y_l = 0x0C To allow override of software data type - override_bpp_vc_dty (0x31D) needs to be enabled.

BACKTOP18 (0x319)

MIPI Software BPP Override

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	soft_bpp_y[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_y	4:0	Software-defined bpp for Video Pipe Example: 0x8 - used for 8-bit data type, 0x2A (RAW8) 0x10-12 (EMB8) 0xA - used for 10-bit data type, 0x2B(RAW10) To allow override of software bpp - override_bpp_vc_dty (0x31D) needs to be enabled.	0x8: Data types = 0x2A, 0x10-12, 0x31-37 0xA: Data types = 0x2B 0xC: Data types = 0x2C 0xE: Data types = 0x2D 0x10: Data types = 0x22, 0x1E, 0x2E, 0x12: Data types = 0x23 0x14: Data types = 0x1F, 0x2F 0x18: Data types = 0x24, 0x30 Others: Reserved

BACKTOP21 (0x31C)

Double Pixel Mode - Used for Pixel Mode

BIT	7	6	5	4	3	2	1	0
Field	–	–	bpp8dbly	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbly	5	Used to pack two 8-bit pixels into 1, GMSL pixel clock See bpp8dbly_mode (0x31F) for more info. See ALT_MEM_MAP8 (0x473) for more info. **Note:** Needs to also be set on GMSL2 serializer to enable feature	0b0: Disabled 0b1: Enabled

BACKTOP22 (0x31D)

Enable for Software Override for BPP, VC, and Data Type

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dty	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dty	7	Software-override enable for BPP, VC, and DT. **Note:** Overrides all three functions when enabled; BPP, VC, and DT.	0b0: Disabled 0x1: Enabled

BACKTOP24 (0x31F)

Double Pixel BPP Mode 8-Bit

BIT	7	6	5	4	3	2	1	0
Field	–	–	bpp8dbly_mode	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbly_mode	5	Used to reassign 8bpp before writing to video line memory See ALT_MEM_MAP8 (0x473) for more info. **Note:** Needs to also be set on GMSL2 serializer to enable feature	0b0: Disabled 0x1: Enabled

BACKTOP25 (0x320)

MIPI Clock

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
Reset	–	–	0b1	0b01111				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY1 software-override disable for frequency fine-tuning	fine-tuning 0b0: Software override for frequency fine tuning enabled 0x1: Software override for frequency fine-tuning disabled

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_predef_freq	4:0	Determines CSI PHY1 output frequency in multiples of 100Mbps/lane. Default is 1500Mbps/lane.	0x0: 80Mbps/lane 0x1: 100Mbps/lane 0x2: 200Mbps/lane 0x3: 300Mbps/lane 0x4: 400Mbps/lane 0x5: 500Mbps/lane 0x6: 600Mbps/lane 0x7: 700Mbps/lane 0x8: 800Mbps/lane 0x9: 900Mbps/lane 0xA: 1000Mbps/lane 0xB: 1100Mbps/lane 0xC: 1200Mbps/lane 0xD: 1300Mbps/lane 0xE: 1400Mbps/lane 0xF: 1500Mbps/lane 0x10: 1600Mbps/lane 0x11: 1700Mbps/lane 0x12: 1800Mbps/lane 0x13: 1900Mbps/lane 0x14: 2000Mbps/lane 0x15: 2100Mbps/lane 0x16: 2200Mbps/lane 0x17: 2300Mbps/lane 0x18: 2400Mbps/lane 0x19: 2500Mbps/lane others: 1500Mbps/lane

BACKTOP27 (0x322)

Used for YUV422 MUXED Mode

BIT	7	6	5	4	3	2	1	0
Field	–	–	yuv_8_10_mux_mode2	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode2	5	Enable YUV422 8-/10-bit muxed mode support	0x0: Disabled 0x1: Enabled

BACKTOP30 (0x325)

MIPI Start of Frame

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP_W_FRAME	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP_W_FRAME	7	When register is enabled, MIPI port waits to send data until the start of a New Frame is received, before outputting MIPI data.	0x0: Disabled 0x1: Enabled

BACKTOP32 (0x327)

Double Pixel BPP Mode 10-bit

BIT	7	6	5	4	3	2	1	0
Field	–	–	bpp10dbly_mode	–	–	–	bpp10dbly	–
Reset	–	–	0b0	–	–	–	0b0	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbly_mode	5	Used to reassign 10bpp before writing to video line memory. **Note:** Needs to also be set on GMSL2 serializer to enable feature.	0b0: Disabled 0b1: Enabled
bpp10dbly	1	bpp = 10 processed as 20-bit color	0b0: Do not process bpp = 10 as 20-bit color 0b1: Process bpp = 10 as 20-bit color

MIPI_PHY0 (0x330)

BIT	7	6	5	4	3	2	1	0
Field	force_csi_out_en	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Force CSI output clock for use in MIPI loopback test or pattern generator use.	0b0: CSI output clock not enabled for MIPI loopback test or pattern generation 0b1: CSI output clock enabled for MIPI loopback test or pattern generation

MIPI_PHY1 (0x331)

MIPI Timing Configurations

BIT	7	6	5	4	3	2	1	0
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_przero	7:6	Typical DPHY data lane HS_prep + HS_zero timing	0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing See t_clk_prep (0x335) for MIPI clock modification .	0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI
t_clk_trail	3:2	Typical DPHY clock HS_trail timing	0b00: 160ns 0b01: 167ns 0b10: 173ns 0b11: 180ns
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing	0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns

MIPI_PHY2 (0x332)

MIPI Timing Configurations

BIT	7	6	5	4	3	2	1	0
Field	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
Reset	0xF				0b01		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
phy_Stdby_n	7:4	Put PHY into standby mode if not used to save power.	0bXX0X: Put PHY1 in standby mode 0bXX1X: Put PHY1 not in standby mode
t_lpx	3:2	Typical DPHY T_{LPX} timing	0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing	0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI

MIPI_PHY3 (0x333)

MIPI Lane Swapping

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	Lane mapping for Data Lane 2 and 3	0bXX00: D2P/N is assigned to Data Lane 0 0bXX01: D2P/N is assigned to Data Lane 1 0bXX10: D2P/N is assigned to Data Lane 2 (default) 0bXX11: D2P/N is assigned to Data Lane 3 0b00XX: D3P/N is assigned to Data Lane 0 0b01XX: D3P/N is assigned to Data Lane 1 0b10XX: D3P/N is assigned to Data Lane 2 0b11XX: D3P/N is assigned to Data Lane 3 (default)
phy0_lane_map	3:0	Lane mapping for Data Lane 0 and 1	0bXX00: D0P/N is assigned to Data Lane 0 (default) 0bXX01: D0P/N is assigned to Data Lane 1 0bXX10: D0P/N is assigned to Data Lane 2 0bXX11: D3P/N is assigned to Data Lane 3 0b00XX: D1P/N is assigned to Data Lane 0 0b01XX: D1P/N is assigned to Data Lane 1 (default) 0b10XX: D1P/N is assigned to Data Lane 2 0b11XX: D1P/N is assigned to Data Lane 3

MIPI_PHY5 (0x335)

MIPI Timing and Polarity Configuration

BIT	7	6	5	4	3	2	1	0
Field	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
Reset	0b00		0b000			0b000		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing See t_hs_prep (0x331) for MIPI data lane modification	0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns
phy1_pol_map	5:3	MIPI Clock and Data Lane 2/3 polarity configuration Normal: P - positive polarity Normal: N - negative polarity Swapped: P - negative polarity Swapped: N - positive polarity	0bXX0: Normal polarity D2P/N 0bXX1: Swapped polarity D2N/P 0bX0X: Normal polarity D3P/N 0bX1X: Swapped polarity D3N/P 0b0XX: Normal polarity CKP/N 0b1XX: Swapped polarity CKN/P
phy0_pol_map	2:0	MIPI Data Lane 0/1 polarity configuration Normal: P - positive polarity Normal: N - negative polarity Swapped: P - negative polarity Swapped: N - positive polarity	0bXX0: Normal polarity D0P/N 0bXX1: Swapped polarity D0N/P 0bX0X: Normal polarity D1P/N 0bX1X: Swapped polarity D1N/P 0b0XX: Reserved 0b1XX: Reserved

MIPI_PHY8 (0x338)

MIPI Timing Configuration

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]			–	–	–	–	–
Reset	0b000			–	–	–	–	–
Access Type	Write, Read			–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
t_lpxesc	7:5	Typical DPHY T_{LPX} timing in escape mode	0b000: 66.67ns 0b001: 80ns 0b010: 100ns 0b011: 133ns 0b100: 200ns 0b101: 400ns 0b110: 1000ns 0b111: 2000ns

MIPI_PHY15 (0x33F)

MIPI Controller Reset

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RST_MIPITX_LOC	–
Reset	–	–	–	–	–	–	0b0	–
Access Type	–	–	–	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
RST_MIPITX_LOC	1	MIPI Controller reset to initial set To enable, DP_RST_MIPI_CHKB needs to be assertedTo disable, write register to 0	0x0: Normal operation 0x1: Reset set MIPI controller - 0x577 include info

MIPI_PHY16 (0x340)

Tunnel Mode ECC and CRC/Video Overflow ERRB Reporting

BIT	7	6	5	4	3	2	1	0
Field	–	–	TUN_DATA_CRC_ERR_OEN	TUN_ECC_UNCORR_ERR_OEN	TUN_ECC_CORR_ERR_OEN	–	–	VID_OVERFLOW_OEN
Reset	–	–	0b0	0b0	0b0	–	–	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_DATA_CRC_ERR_OEN	5	Tunnel mode - DPHY CSI CRC error reporting enable See TUN_DATA_CRC_ERR (0x341) for more info.	0x0: Disabled 0x1: Enabled
TUN_ECC_UNCORR_ERR_OEN	4	Tunnel mode - DPHY CSI ECC uncorrectable error reporting enable See TUN_ECC_UNCORR_ERR (0x341) for more info.	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_ECC_CORR_ERR_OEN	3	Tunnel mode - DPHY CSI ECC correctable error reporting enable See TUN_ECC_CORR_ERR (0x341) for more info.	0x0: Disabled 0x1: Enabled
VID_OVERFLOW_OEN	0	Enable reporting of video pipe overflow (VID_OVERFLOW) at ERRB pin See VID_OVERFLOW_FLAG (0x341) for more info.	0x0: Disabled 0x1: Enabled

MIPI_PHY17 (0x341)

Tunnel Mode ECC and CRC/Video Overflow Errors (Refer to 0x442 to clear)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TUN_DATA_CRC_ERR	TUN_ECC_UNCORR_ERR	TUN_ECC_CORR_ERR	–	–	VID_OVERFLOW_FLAG
Reset	–	–	0b0	0b0	0b0	–	–	0b0
Access Type	–	–	Read Only	Read Only	Read Only	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_DATA_CRC_ERR	5	For tunneling mode, DPHY/CPHY data CRC errors Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear. The loss of video lock also clears this bit.	0b0: No Error 0b1: Error
TUN_ECC_UNCORR_ERR	4	For tunneling mode, uncorrectable errors on DPHY ECC or CPHY header CRC Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear. The loss of video lock also clears this bit.	0b0: No Error 0b1: Error
TUN_ECC_CORR_ERR	3	For tunneling mode, correctable errors on DPHY ECC or CPHY header CRC. Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear. The loss of video lock also clears this bit.	0b0: No Error 0b1: Error
VID_OVERFLOW_FLAG	0	Combined error status of all video pipe overflow (VID_OVERFLOW) bits. Read individual VID_OVERFLOW bits to clear.	0b0: No Error 0b1: Error

MIPI_PHY18 (0x342)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	csi2_tx1_pkt_cnt[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_tx1_pkt_cnt	3:0	Packet Count sent out of CSI2 Controller 1.	0bXXXX: Number of packets out

MIPI_PHY20 (0x344)

BIT	7	6	5	4	3	2	1	0
Field	phy1_pkt_cnt[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Read Only				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:4	Packet Count out of of MIPI PHY1	0bXXXX: Number of packets out

FSYNC_0 (0x3E0)

MFP FSYNC Output

BIT	7	6	5	4	3	2	1	0
Field	–	–	FSYNC_OUT_PIN	–	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
Reset	–	–	0b0	–	0b11		0b10	
Access Type	–	–	Write, Read	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_OUT_PIN	5	Select pin to output frame sync signal (effective only when FSYNC_MODE = 01) See MFP priority table to confirm FSYNC has proper priority.	0x0: MFP0 0x1: MFP2
FSYNC_MODE	3:2	MFP Frame Sync Generation Enable	**GMSL1** 0b00: Frame sync generation is on. FSYNC pin is High-Z. 0b01: Frame sync generation is on. FSYNC pin drives a subordinate device. 0b10: Frame sync generation is off. FSYNC pin is driven by a main device. 0b11: Frame sync generation is off. GPI-to-GPO channel can be used for frame sync. **GMSL2** 0b00: Frame sync generation is on. GPIO is not used as FSYNC output. 0b01: Frame sync generation is on. GPIO is used as FSYNC output and drives a subordinate device. 0b10: Frame sync generation is off. GPIO is not used as FSYNC output. 0b11: Frame sync generation is off. GPIO is not used as FSYNC output.
FSYNC_METH	1:0	Frame Sync Method Auto: Adjusts FSYNC timing based on VSYNC signals Manual: Does not rely on VSYNC signal to generate FSYNC timing	0b00: Manual 0b01: Reserved 0b10: Auto 0b11: Reserved

FSYNC_1 (0x3E1)

FSYNC to VSYNC Period

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	FSYNC_PER_DIV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	FSYNC to VSYNC output ratio - works only when FSYNC_MODE = 0b00/0b01. FSYNC waits for the specified VSYNC periods to output FSYNC signal.	0x0: 1 0x1: 2 0x2: 3 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

FSYNC_2 (0x3E2)

Video Pipe FSYNC Generation

BIT	7	6	5	4	3	2	1	0
Field	MST_LINK_SEL[2:0]			–	–	–	–	–
Reset	0b101			–	–	–	–	–
Access Type	Write, Read			–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	MAIN link select for FSYNC generation MUST SET to 0b001 - Pipe Y. Currently set to RSVD configuration	0b000: RSVD 0b001: Pipe Y 0b010: RSVD 0b011: RSVD 0b100: RSVD 0b101: RSVD (default) 0b110: RSVD 0b111: RSVD

FSYNC_5 (0x3E5)

FSYNC Manual Mode Low Byte

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_L	7:0	MST_LINK_SEL (0x3E2): When set to Pipe Y, PCLK source = PCLK from serializer. FS_USE_XTAL (0x3EF): Enable to source crystal for FYSNC generation, is based on the 25MHz crystal frequency.	0xXX: Low byte of PCLK cycles in frame period

FSYNC_6 (0x3E6)

FSYNC Manual Mode Middle Byte

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_M	7:0	MST_LINK_SEL (0x3E2): When set to Pipe Y, PCLK source = PCLK from serializer. FS_USE_XTAL (0x3EF): Enable to source crystal for FYSNC generation, is based on the 25MHz crystal frequency.	0xXX: Middle byte of PCLK cycles in frame period

FSYNC_7 (0x3E7)

FSYNC Manual Mode High Byte

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_H	7:0	MST_LINK_SEL (0x3E2): When set to Pipe Y, PCLK source = PCLK from serializer. FS_USE_XTAL (0x3EF): Enable to source crystal for FYSNC generation, is based on the 25MHz crystal frequency.	0xXX: High byte of PCLK cycles in frame period

FSYNC_15 (0x3EF)

FSYNC GMSL and Clock Source Selection

BIT	7	6	5	4	3	2	1	0
Field	FS_GPIO_TYPE	FS_USE_XTAL	–	–	–	–	–	–
Reset	0b1	0b0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FS_GPIO_TYPE	7	Select the type of FSYNC signal to output from GPIO This bit is not automatically set.	0x0: GSML1 type 0x1: GMSL2 type

BITFIELD	BITS	DESCRIPTION	DECODE
FS_USE_XTAL	6	Enable crystal/oscillator clock for generating frame sync signal. This bit, when enabled, overrides incoming video PCLK to use a 25MHz clock source for FSYNC generation.	0x0: Disabled 0x1: Enabled

FSYNC_17 (0x3F1)

FSYNC GPIO ID and FSYNC Error Threshold

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
Reset	0b11110					0b000		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal to serializer used only in GMSL2 mode. Do not conflict with other GPIO IDs.	0bXXXXX: GPIO ID
FSYNC_ERR_THR	2:0	Frame Sync Error Threshold Reporting FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT (0x3F0) ≥ FSYNC_ERR_THR.	0bXXX: Frame sync error reporting threshold

FSYNC_22 (0x3F6)

FSYNC LOCK

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type	Read Clears All	Read Only	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_LOSS_OF_LOCK	7	Frame Synchronization Lost Lock Flag Cleared when read.	0b0: Frame sync lock not lost 0b1: Frame sync lock lost
FSYNC_LOCKED	6	Frame Synchronization Lock Flag	0b0: Frame sync not locked 0b1: Frame sync locked

MIPI_TX1 (0x441)

MIPI Frame ID Short Packet

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI Tx Mode Bits 7:1: RSVD Bit 0: Enables MIPI Frame ID to Frame Start and Frame End short packet	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MIPI_TX2 (0x442)

Individual MIPI PHY Status (Refer to 0x342 for overall)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx Status The register is split into decode segments: bit[0] SYNC mode enable. bit[1] Video sync flag bit[2] Loss of video sync flag bit[3] Tunneling mode: DPHY ECC or CPHY header CRC error (correctable) bit[4] Tunneling mode: DPHY ECC or CPHY header CRC error (uncorrectable) bit[5] Tunneling mode: DPHY/CPHY data CRC error	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0bXXXXX0XX: No loss of video sync 0bXXXXX1XX: Video sync lost after last read of this register or RESET. 0bXXXX0XXX: No tunneling ECC correctable error 0bXXXX1XXX: Tunneling ECC correctable error after last read of this register or RESET. 0bXXX0XXXX: No tunneling ECC uncorrectable error 0bXXX1XXXX: Tunneling ECC uncorrectable error after last read of this register or RESET. 0bXX0XXXXX: No tunneling data CRC error 0bXX1XXXXX: Tunneling data CRC error after last read of this register or RESET.

MIPI_TX3 (0x443)

MIPI Initial Deskew Calibration

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY Deskew Initial Calibration Control The register is split into six decode segments: bit[7] Selects auto-initial deskew calibration on or off bit[6] Reserved bit[5] Any bit change initiates an initial calibration if bit 4 = 1 bit[4] Selects manual initial on or off bit[3] Reserved bits[2:0] Selects initial deskew width.	0bXXXXX000: Reserved 0bXXXXX001: Initial deskew width = 2 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX010: Initial deskew width = 3 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX011: Initial deskew width = 4 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX100: Initial deskew width = 5 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX101: Initial deskew width = 6 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX110: Initial deskew width = 7 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX111: Initial deskew width = 8 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on

MIPI_TX4 (0x444)

MIPI Periodic Deskew Calibration

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY Periodic Deskew Calibration Control The register is split into four decode segments: bit[7] Selects periodic deskew calibration on or off bit[6] Selects generation on rising or falling edge of VS bits[5:3] Selects periodic interval bits[2:0] Selects periodic deskew width.	0bXXXXX000: Reserved 0bXXXXX001: Periodic deskew width = 2k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX010: Periodic deskew width = 3k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX011: Periodic deskew width = 4k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX100: Periodic deskew width = 5k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX101: Periodic deskew width = 6k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX110: Periodic deskew width = 7k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXXXXX111: Periodic deskew width = 8k UI - (t_lpx+t_hs_przero)[UI] - 16 UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodic deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x445)

CSI Tpre Data Adjustment

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of MIPI byte clocks to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX10 (0x44A)

MIPI Number of Data Lanes, VC Extension, CSI Wakeup (high bits)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		–	–	CSI_VCX_EN	–	–	–
Reset	0b11		–	–	0b0	–	–	–
Access Type	Write, Read		–	–	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
CSI_VCX_EN	3	Enable VC Extension	0x0: Extended VC not supported 0x1: Extended VC supported

MIPI_TX11 (0x44B)

DST and SRC for Mapping for VC and Data Type 0-7

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping Enable Low Byte [7:0] Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_0 (0x44D) and MAP_DST_0 (0x44E) bitfields 0xX2: Enable MAP_SRC_1 (0x44F) and MAP_DST_1 (0x450) bitfields 0xX4: Enable MAP_SRC_2 (0x451) and MAP_DST_2 (0x452) bitfields 0xX8: Enable MAP_SRC_3 (0x453) and MAP_DST_3 (0x454) bitfields 0x1X: Enable MAP_SRC_4 (0x455) and MAP_DST_4 (0x456) bitfields 0x2X: Enable MAP_SRC_5 (0x457) and MAP_DST_5 (0x458) bitfields 0x4X: Enable MAP_SRC_6 (0x459) and MAP_DST_6 (0x45A) bitfields 0x8X: Enable MAP_SRC_7 (0x45B) and MAP_DST_7 (0x45C) bitfields

MIPI_TX12 (0x44C)

DST and SRC for Mapping for VC and Data Type 0-7

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping Enable High Byte [15:8] Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	ValueEnumerationDecode 0xX1: Enable MAP_SRC_8 (0x45D) and MAP_DST_8 (0x45E) bitfields 0xX2: Enable MAP_SRC_9 (0x45F) and MAP_DST_9 (0x460) bitfields 0xX4: Enable MAP_SRC_10 (0x461) and MAP_DST_10 (0x462) bitfields 0xX8: Enable MAP_SRC_11 (0x463) and MAP_DST_11 (0x464) bitfields 0x1X: Enable MAP_SRC_12 (0x465) and MAP_DST_12 (0x466) bitfields 0x2X: Enable MAP_SRC_13 (0x467) and MAP_DST_13 (0x468) bitfields 0x4X: Enable MAP_SRC_14 (0x469) and MAP_DST_14 (0x46A) bitfields 0x8X: Enable MAP_SRC_15 (0x46B) and MAP_DST_15 (0x46C) bitfields

MIPI_TX13 (0x44D)

VC and DT Source Mapping 0

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX14 (0x44E)

VC and DT Destination Mapping 0

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Destination DT and VC that is routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX15 (0x44F)

VC and DT Source Mapping 1

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX16 (0x450)

VC and DT Destination Mapping 1

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX17 (0x451)

VC and DT Source Mapping 2

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX18 (0x452)

VC and DT Destination Mapping 2

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX19 (0x453)

VC and DT Source Mapping 3

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX20 (0x454)

VC and DT Destination Mapping 3

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX21 (0x455)

VC and DT Source Mapping 4

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX22 (0x456)

VC and DT Destination Mapping 4

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX23 (0x457)

VC and DT Source Mapping 5

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX24 (0x458)

VC and DT Destination Mapping 5

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX25 (0x459)

VC and DT Source Mapping 6

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX26 (0x45A)

VC and DT Destination Mapping 6

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX27 (0x45B)

VC and DT Source Mapping 7

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX28 (0x45C)

VC and DT Destination Mapping 7

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX29 (0x45D)

VC and DT Source Mapping 8

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX30 (0x45E)

VC and DT Destination Mapping 8

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX31 (0x45F)

VC and DT Source Mapping 9

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX32 (0x460)

VC and DT Destination Mapping 9

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX33 (0x461)

VC and DT Source Mapping 10

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX34 (0x462)

VC and DT Destination Mapping 10

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX35 (0x463)

VC and DT Source Mapping 11

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX36 (0x464)

VC and DT Destination Mapping 11

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX37 (0x465)

VC and DT Source Mapping 12

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX38 (0x466)

VC and DT Destination Mapping 12

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX39 (0x467)

VC and DT Source Mapping 13

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX40 (0x468)

VC and DT Destination Mapping 13

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX41 (0x469)

VC and DT Source Mapping 14

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX42 (0x46A)

VC and DT Destination Mapping 14

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX43 (0x46B)

VC and DT Source Mapping 15

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Source DT and VC (present in the corresponding pipe) mapped to the corresponding destination DT and VC and routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX44 (0x46C)

VC and DT Destination Mapping 15

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	Bit [7:6]: Virtual channel Bit [5:0]: Data type

MIPI_TX45 (0x46D)

Controller 1 Mapping of DST and SRC 0-3

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_2	5:4	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_1	3:2	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_0	1:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved

MIPI_TX46 (0x46E)

Controller 1 Mapping of DST and SRC 7-4

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_6	5:4	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_5	3:2	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_4	1:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved

MIPI_TX47 (0x46F)

Controller 1 Mapping of DST and SRC 11-8

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_10	5:4	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_9	3:2	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_8	1:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved

MIPI_TX48 (0x470)

Controller 1 Mapping of DST and SRC 15-12

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_14	5:4	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_13	3:2	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved
MAP_DPHY_DEST_12	1:0	Destination DT and VC routed to the PHY configured in MIPI_TX45-48.	0b00: Reserved 0b01: Map to Controller 1 0b10: Reserved 0b11: Reserved

MIPI_TX50 (0x472)

VC Periodic Deskew Adjustment

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic Deskew Select Register The register is split into three decode segments: bit[7]: Select periodic deskew calibration for one or all virtual channels bits[6:5]: Reserved bits[4:0]: Virtual channel to generate periodic deskew calibration when only 1 channel is selected by bit 7	0b0XXXXXXX: Generate periodic calibration deskew calibration on all Virtual Channels 0b1XXX0000: Periodic deskew calibration generated by Virtual Channel 0 0b1XXX0001: Periodic deskew calibration generated by Virtual Channel 1 0b1XXX0010: Periodic deskew calibration generated by Virtual Channel 2 0b1XXX0011: Periodic deskew calibration generated by Virtual Channel 3 0b1XXX0100: Periodic deskew calibration generated by Virtual Channel 4 0b1XXX0101: Periodic deskew calibration generated by Virtual Channel 5 0b1XXX0110: Periodic deskew calibration generated by Virtual Channel 6 0b1XXX0111: Periodic deskew calibration generated by Virtual Channel 7 0b1XXX1000: Periodic deskew calibration generated by Virtual Channel 8 0b1XXX1001: Periodic deskew calibration generated by Virtual Channel 9 0b1XXX1010: Periodic deskew calibration generated by Virtual Channel 10 0b1XXX1011: Periodic deskew calibration generated by Virtual Channel 11 0b1XXX1100: Periodic deskew calibration generated by Virtual Channel 12 0b1XXX1101: Periodic deskew calibration generated by Virtual Channel 13 0b1XXX1110: Periodic deskew calibration generated by Virtual Channel 14 0b1XXX1111: Periodic deskew calibration generated by Virtual Channel 15

MIPI_TX51 (0x473)

Data Type Memory Mapping and VS Frame Wait (TUN Mode)

BIT	7	6	5	4	3	2	1	0
Field	TUN_WAIT_VS_START[2:0]			ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	0x0			0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_WAIT_VS_START	7:5	Number of VS frames to wait before sending MIPI packet Used for Tunnel mode only.	0x0: No wait Others: Number of frames to wait
ALT2_MEM_MAP8	4	Alternative memory read mapping enable for 8-bit DT when sharing the same video pipe with RAW16	0b0: Disabled 0b1: Enabled
MODE_DT	3	Select 24-bit mode for user-defined data types See data sheet for more information	0b0: Disabled 0b1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_ MAP10	2	Alternative memory map enable for 10-bit DT	0b0: Disabled 0b1: Enabled
ALT_MEM_ MAP8	1	Alternative memory map enable for 8-bit DT	0b0: Disabled 0b1: Enabled
ALT_MEM_ MAP12	0	Alternative memory map enable for 12-bit DT	0b0: Disabled 0b1: Enabled

MIPI_TX52 (0x474)

Deskew CSI Tunnel Mode Adjustment and TUN Mode Enable

BIT	7	6	5	4	3	2	1	0
Field	TUN_NO_C ORR	DESKEW_TUN[1:0]		–	–	–	–	TUN_EN
Reset	0b0	0x0		–	–	–	–	0b0
Access Type	Write, Read	Write, Read		–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_C ORR	7	Do not enable header error correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled
DESKEW_T UN	6:5	Deskew Mode for CSI2 Tunneling	0b00: Periodic deskew using deserializer DESKEW_PER register 0b01: Periodic deskew follows what Serializer receives with small offset adjustment by DESKEW_TUN_OFFSET. 0b10: Periodic deskew occurrence follows Serializer but width determined by register DESKEW_PER 0b11: Reserved
TUN_EN	0	Tunneling Enable The configuration pin 1 sets this value initially, and further register writes to this register changes the value.	0b0: Tunneling disabled 0b1: Tunneling enabled

MIPI_TX54 (0x476)

Tunnel Mode MIPI Memory Read Adjustment

BIT	7	6	5	4	3	2	1	0
Field	TUN_PKT_START_ADDR[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_PKT_S TART_ADDR	7:0	Specifies the start address of the long packet in tunneling mode. 0x00: 0x01: 0xFF: MIPI outputs the packet after 32640 bytes are written to memory. Advanced feature - Consult factory for usage.	0x00: Disabled. The MIPI does not output the packet until the whole video line is written to memory. 0x01: MIPI outputs the packet after 128 bytes are written to memory. ... 0xFF: MIPI outputs the packet after 32,640 bytes are written to memory.

MIPI_TX_EXT0 (0x510)

Extended Virtual Channels for SRC and DST 0

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_0_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_0_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT1 (0x511)

Extended Virtual Channels for SRC and DST 1

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_1_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_1_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT2 (0x512)

Extended Virtual Channels for SRC and DST 2

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_2_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_2_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT3 (0x513)

Extended Virtual Channels for SRC and DST 3

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_3_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_3_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT4 (0x514)

Extended Virtual Channels for SRC and DST 4

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_4_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_4_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT5 (0x515)

Extended Virtual Channels for SRC and DST 5

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_5_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_5_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT6 (0x516)

Extended Virtual Channels for SRC and DST 6

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_6_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_6_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT7 (0x517)

Extended Virtual Channels for SRC and DST 7

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_7_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_7_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT8 (0x518)

Extended Virtual Channels for SRC and DST 8

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_8_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_8_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT9 (0x519)

Extended Virtual Channels for SRC and DST 9

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_9_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_9_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT10 (0x51A)

Extended Virtual Channels for SRC and DST 10

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_10_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_10_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT11 (0x51B)

Extended Virtual Channels for SRC and DST 11

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_11_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_11_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT12 (0x51C)

Extended Virtual Channels for SRC and DST 12

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_12_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_12_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT13 (0x51D)

Extended Virtual Channels for SRC and DST 13

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_13_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_13_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT14 (0x51E)

Extended Virtual Channels for SRC and DST 14

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_14_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_14_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

MIPI_TX_EXT15 (0x51F)

Extended Virtual Channels for SRC and DST 15

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_15_H	7:5	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).
MAP_DST_15_H	4:2	Extended bits of Virtual channel This bit gets combined with the 0x44D whenever extended Virtual channel is enabled, CSI_VCX_EN (0x44A).

CFG_0 (0x540)

VSYNC Output to MFP0

BIT	7	6	5	4	3	2	1	0
Field	VS_OUT1	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_OUT1	7	Output VSYNC from MFP0 See MFP priority table to confirm if other functions have higher priority.	0x0: Disabled 0x1: Output VSYNC from MFP0

CFG_1 (0x541)

VSYNC Output to MFP5

BIT	7	6	5	4	3	2	1	0
Field	VS_OUT2	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_OUT2	7	Output VSYNC from MFP5 See MFP priority table to confirm if other functions have higher priority.	0x0: Disabled 0x1: Output VSYNC from MFP5

CFG_2 (0x542)

DE Output to MFP0

BIT	7	6	5	4	3	2	1	0
Field	HS_OUT1	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HS_OUT1	7	DE output to MFP0 See MFP priority table to confirm if other functions have higher priority.	0x0: Disabled 0x1: Output DE/DV from MFP0

CFG_4 (0x544)

DE Output to MFP5 and HS/VS/DE ERR Reporting

BIT	7	6	5	4	3	2	1	0
Field	HS_OUT2	–	–	–	–	–	HVD_SYNC_LOCK_LOST_OEN	HVD_SYNC_LOCK_LOST
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Write, Read	–	–	–	–	–	Write, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HS_OUT2	7	DE output to MFP5 See MFP priority table to confirm if other functions have higher priority.	0x0: Disabled 0x1: Output DE/DV from MFP5
HVD_SYNC_LOCK_LOST_OEN	1	HS, VS, and DE tracking lock lost reporting enable to ERRB pin HS/VS/DE tracking must be enabled Htracken/Vtracken/Dtracken	0b0: Reporting disabled 0b1: Reporting enabled
HVD_SYNC_LOCK_LOST	0	HS, VS, and DE Tracking Lock Lost Read this bitfield to clear.	0b0: Flag not asserted 0b1: Flag asserted

UART_PT_0 (0x548)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Custom UART bit length for pass-through UART Channel 1 Set BITLEN_MAN_CFG_1 (0x4F) to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits)	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x549)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set BITLEN_MAN_CFG_1 (0x4F) to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x54A)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 2. Set BITLEN_MAN_CFG_2 (0x4F) to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

UART_PT_3 (0x54B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	High byte of custom UART bit length for pass-through UART Channel 2. Set BITLEN_MAN_CFG_2 (0x4F) to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

BW_MEAS_1 (0x55A)

BIT	7	6	5	4	3	2	1	0
Field	LFLT_STKY_INT	–	–	–	–	–	–	–
Reset	0x1	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_STKY_INT	7	Sets value in 0x57C to hold value until read or automatically erases after line-fault error no longer exists. Otherwise, if disabled, the value is not held.	0x0: Disabled 0x1: Enabled

CNT4 (0x55C)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR0[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR0	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK. Also, include 9b10b decoding errors that are checked regardless of whether or not pixel CRC is enabled.	0xXX: Total number of video pixel CRC errors detected in video stream Y

UNLOCK_KEY (0x569)

BIT	7	6	5	4	3	2	1	0
Field	UNLOCK_KEY[7:0]							
Reset	0xAA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
UNLOCK_KEY	7:0	Register must be at unlock value to enable write access to port control pins DIS_LOCAL_CC, IIC_1_EN, IIC_2_EN, UART_1_EN, UART_2_EN Defaults to unlocked.	0xAA: Unlock write access Others: Lock write access

PIO_SLEW_0 (0x570)

BIT	7	6	5	4	3	2	1	0
Field	PIO03_SLEW[1:0]		PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
Reset	0b11		0b11		0b11		0b10	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PIO03_SLEW	7:6	Rise and fall time speed setting for MFP3 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO02_SLEW	5:4	Rise and fall time speed setting for MFP2 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO01_SLEW	3:2	Rise and fall time speed setting for MFP1 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO00_SLEW	1:0	Rise and fall time speed setting for MFP0 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate

PIO_SLEW_1 (0x571)

BIT	7	6	5	4	3	2	1	0
Field	PIO07_SLEW[1:0]		–	–	–	–	–	–
Reset	0b10		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PIO07_SLEW	7:6	Rise and fall time speed setting for MFP4 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate

PIO_SLEW_2 (0x572)

BIT	7	6	5	4	3	2	1	0
Field	PIO16_SLEW[1:0]		PIO12_SLEW[1:0]		PIO11_SLEW[1:0]		PIO08_SLEW[1:0]	
Reset	0b11		0b11		0b11		0b10	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PIO16_SLEW	7:6	Rise and fall time speed setting for MFP8 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO12_SLEW	5:4	Rise and fall time speed setting for MFP7 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO11_SLEW	3:2	Rise and fall time speed setting for MFP6 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate
PIO08_SLEW	1:0	Rise and fall time speed setting for MFP5 output 00 value is the fastest rise and fall time, and 11 value is the slowest. See Multifunction Pin Assignments section in data sheet.	0x0: Fastest Slew Rate 0x1: Faster Slew Rate 0x2: Slower Slew Rate 0x3: Slowest Slew Rate

HS_VS_ACT_Y (0x575)

Pipe Y DE/VS/HS and VS/HS Polarity

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_Y	6	DE activity is detected	0x0: DE is not detected 0x1: DE is detected
VS_DET_Y	5	VS activity is detected	0x0: VS is not detected 0x1: VS is detected
HS_DET_Y	4	HS activity is detected	0x0: HS is not detected 0x1: HS is detected
VS_POL_Y	1	Detected VS polarity	0x0: Active low 0x1: Active high
HS_POL_Y	0	Detected HS polarity	0x0: Active low 0x1: Active high

DP_ORSTB_CTL (0x577)

MIPI/FIFO/Control Register Reset Enables

BIT	7	6	5	4	3	2	1	0
Field	–	DP_RST_MIPI3_CHKB	DP_RST_STABLE_CHKB	DP_RST_MIPI2_CHKB	DP_RST_MIPI_CHKB	DP_RST_VP_CHKB	–	–
Reset	–	0b1	0b1	0b0	0b0	0b0	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI3_CHKB	6	Select reset mode to MIPI controllers	0x0: Legacy 0x1: Enable auto reset of command FIFO read pointer in MIPI TX
DP_RST_STABLE_CHKB	5	Select reset mode when changing register values	0x0: Legacy 0x1: Prevent resets while control register values are changing
DP_RST_MIPI2_CHKB	4	Select reset mode to MIPI controllers	0x0: Legacy 0x1: Independent reset functionality. Enable auto reset of MIPI controllers.
DP_RST_MIPI_CHKB	3	Select reset mode to MIPI controllers	0x0: Legacy 0x1: Independent reset functionality. This enables RST_MIPITX_LOC[3:0] (0x33F) to reset controllers individually.
DP_RST_VP_CHKB	2	Select reset mode to VIDEO_RX, VRX blocks	0x0: Legacy 0x1: Independent reset functionality

PM_OV_STAT2 (0x578)

BIT	7	6	5	4	3	2	1	0
Field	VTERM_OV_OEN	VREG_OV_OEN	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VTERM_OV_OEN	7	V_{TERM} overvoltage status on ERRB, 1.35V threshold	0b0: Reporting disabled 0b1: Reporting enabled
VREG_OV_OEN	6	V_{REG} overvoltage status on ERRB, 1.35V threshold	0b0: Reporting disabled 0b1: Reporting enabled

PM_OV_STAT3 (0x579)

V_{TERM}/V_{REG}/V_{DDIO} Sticky Enable

BIT	7	6	5	4	3	2	1	0
Field	VTERM_OV_FLAG	VREG_OV_FLAG	VDDIO_OV_FLAG	–	–	–	–	–
Reset	0b0	0b0	0b0	–	–	–	–	–
Access Type	Read Clears All	Read Clears All	Read Clears All	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VTERM_OV_FLAG	7	Sticky status value for V_{TERM} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VREG_OV_FLAG	6	Sticky status value for V_{REG} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VDDIO_OV_FLAG	5	Sticky status value for VDDIO overvoltage	0b0: Flag not asserted 0b1: Flag asserted

PM_OV_STAT4 (0x57A)

V_{DDIO} Overvoltage ERRB Reporting, 3.685V Threshold

BIT	7	6	5	4	3	2	1	0
Field	VDDIO_OV_OEN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VDDIO_OV_OEN	7	Enable VDDIO overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled

FAULT_OEN (0x57B)

Line Fault/Short Reporting and CRC Reporting

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	GPIO_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OPEN_OEN	7	Enables reporting of line-fault open interrupt (LFLT_INT_OPEN) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_L2LS_OEN	6	Enables reporting of line to line short interrupt (LFLT_INT_L2LS) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_BAT_S_OEN	5	Enable CC packet CRC error	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_GND_S_OEN	4	Enables reporting of short to ground line-fault interrupt (LFLT_INT) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
GPIO_CRC_ERR_OEN	3	Enable GPIO CRC error (GPIO_CRC_ERR_FLAG) status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
RBB_CC_CRC_ERR_OEN	2	Enable RBB CC CRC error (RBB_CC_CRC_ERR_FLAG) status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
PT2_CRC_ERR_OEN	1	Enable PT2 CRC error (PT2_CRC_ERR_FLAG) status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
PT1_CRC_ERR_OEN	0	Enable PT1 CRC error (PT1_CRC_ERR_FLAG) status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled

FAULT_STAT (0x57C)

Line Fault/Short Flags and CRC Flags

BIT	7	6	5	4	3	2	1	0
Field	LINE_INT_OPEN_FLAG	LINE_INT_L2LS_FLAG	LINE_INT_BAT_S_FLAG	LINE_INT_GND_S_FLAG	GPIO_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_INT_OPEN_FLAG	7	Line-fault interrupt. Asserted when either one of line-fault monitors indicate an open fault status. See LF_0 and LF_1 bitfields for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behaviour.	0b0: Flag not asserted 0b1: Flag asserted
LINE_INT_L2LS_FLAG	6	Line-fault interrupt. Asserted when either one of line-fault monitors indicate a line to line short fault status. See LF_0 and LF_1 bitfields for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behaviour.	0b0: Flag not asserted 0b1: Flag asserted
LINE_INT_BAT_S_FLAG	5	Line-fault interrupt. Asserted when either one of line-fault monitors indicate a short to battery fault status. See LF_0 and LF_1 bitfields for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behaviour.	0b0: Flag not asserted 0b1: Flag asserted
LINE_INT_GND_S_FLAG	4	Line-fault interrupt. Asserted when either one of line-fault monitors indicate a short to ground fault status. See LF_0 and LF_1 bitfields for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behaviour.	0b0: Flag not asserted 0b1: Flag asserted
GPIO_CRC_ERR_FLAG	3	GPIO CRC error flag. Asserted when GPIO CRC error count > 0. Read GPIO_CRC_ERR to clear.	0b0: Flag not asserted 0b1: Flag asserted
RBB_CC_CRC_ERR_FLAG	2	RBB CC CRC error flag. Asserted when RBB CC CRC error count > 0. Read RBB_CC_CRC_ERR to clear.	0b0: Flag not asserted 0b1: Flag asserted
PT2_CRC_ERR_FLAG	1	PT1 CRC error flag. Asserted when PT2 CRC error count > 0. Read PT2_CRC_ERR to clear.	0b0: Flag not asserted 0b1: Flag asserted

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_CRC_ERR_FLAG	0	PT1 CRC error flag. Asserted when PT1 CRC error count > 0. Read PT1_CRC_ERR to clear.	0b0: Flag not asserted 0b1: Flag asserted

UART_0 (0x808)

Bypass for UART1 Pass-Through

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_MS_EN_1	LOC_MS_EN_1	MS_LOC	BYPASS_TO_1[1:0]		BYPASS_EN_1
Reset	–	–	0b0	0b0	0x0	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_1	5	Enable UART bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_1	4	Enables UART Port 1 bypass mode control by local MFP pin (the MS function). Please see MS_LOC register field for MFP pin selection of MS function. Set to enable MS pin for UART Port 1 (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode. **Note:** Only one UART port may use the MS function at any given time. Mulitple UART ports are NOT simultaneously supported.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
MS_LOC	3	Selects which MFP to use for MS function. **Note:** Only one UART port may use the MS function at any given time. Mulitple UART ports are NOT simultaneously supported.	0x0: Use MFP0 as MS function 0x1: Use MFP2 as MS function
BYPASS_TO_1	2:1	UART soft-bypass timeout duration. When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN_1	0	Enable UART soft-bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO (0x48) bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_1 (0x809)

Bypass for UART2 Pass-Through

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_MS_EN_2	LOC_MS_EN_2	–	BYPASS_TO_2[1:0]		BYPASS_EN_2
Reset	–	–	0b0	0b0	–	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_2	5	Enable UART bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_2	4	Enables UART Port 2 bypass mode control by local MFP pin (the MS function). See MS_LOC (0x808) bitfield for MFP pin selection of MS function. Set to enable MS pin for UART Port 2 (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode. **Note:** Only one UART port may use the MS function at any given time. Multiple UART ports are NOT simultaneously supported.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_TO_2	2:1	UART soft-bypass timeout duration. When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN_2	0	Enable UART soft-bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO (0x48) bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

I2C_PT_0 (0x80E)

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_REGSLV_0_TIMED_OUT	–	–	–	I2C_INTREG_SLV_TO[2:0]		
Reset	–	0x0	–	–	–	0x6		
Access Type	–	Read Only	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_0_TIMED_OUT	6	Internal I²C-to-Register subordinate for Port 0 has timed out while waiting for the main or the internal register access FSM.	0x0: Internal I²C-to-Register subordinate for Port 0 has not timed out 0x1: Internal I²C-to-Register subordinate for Port 0 has timed out
I2C_INTREG_SLV_TO	2:0	I²C-to-Internal Register Subordinate 0 Timeout Setting Internal register I²C subordinate 0 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I²C Port 0.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

I2C_PT_1 (0x80F)

BIT	7	6	5	4	3	2	1	0
Field	I2C_REGSLV_2_TIMED_OUT	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]			I2C_INTREG_SLV_1_TO[2:0]		
Reset	0x0	0x0	0x6			0x6		
Access Type	Read Only	Read Only	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_2_TIMED_OUT	7	Internal I²C-to-Register subordinate for Port 2 has timed out while waiting for the main or the internal register access FSM.	0x0: Internal I²C-to-Register subordinate for Port 2 has not timed out 0x1: Internal I²C-to-Register subordinate for Port 2 has timed out
I2C_REGSLV_1_TIMED_OUT	6	Internal I²C-to-Register subordinate for Port 1 has timed out while waiting for the main or the internal register access FSM.	0x0: Internal I²C-to-Register subordinate for Port 1 has not timed out 0x1: Internal I²C-to-Register subordinate for Port 1 has timed out
I2C_INTREG_SLV_2_TO	5:3	I²C-to-Internal Register Subordinate 2 timeout setting Internal register I²C subordinate 2 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I²C Port 2.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled
I2C_INTREG_SLV_1_TO	2:0	I²C-to-Internal Register Subordinate 1 Timeout Setting Internal register I²C subordinate 1 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I²C Port 1.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

GMSL1_4 (0xB04)

FWD/REV/PORT Enable/Disable and PRBS Enable

BIT	7	6	5	4	3	2	1	0
Field	–	OUTENB	PRBSEN	CC_PORT_SEL[1:0]		–	REVCCEN	FWDCCEN
Reset	–	0b0	0b0	0b00		–	0b1	0b1
Access Type	–	Write, Read	Write, Read	Write, Read		–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OUTENB	6	Disable outputs	0b0: Outputs enabled 0b1: Outputs disabled
PRBSEN	5	PRBS test enable (In HIBW mode set PRBS_TYPE = 0)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	4:3	Select which I^2C/UART port is connected to this link	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
REVCCEN	1	Enable reverse control channel from deserializer	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
FWDCCEN	0	Enable forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0xB05)

EQ and I^2C Settings

BIT	7	6	5	4	3	2	1	0
Field	–	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
Reset	–	0b0	0b1	0b1	0x9			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
NO_REM_MST	6	Serializer Main Select mode	0x0: I^2C main on serializer side 0x1: No I^2C main on serializer side
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full periodic HV tracking
EN_EQ	4	Enable equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization
EQTUNE	3:0	Equalizer boost level at 750MHz (effective when Adaptive EQ is turned off)	0b0000: 1.6dB manual EQ setting 0x0001: 2.1dB manual EQ setting 0x0010: 2.8dB manual EQ setting 0x0011: 3.5dB manual EQ setting 0x0100: 4.3dB manual EQ setting 0x0101: 5.2dB manual EQ setting 0x0110: 6.3dB manual EQ setting 0x0111: 7.3dB manual EQ setting 0x1000: 8.5dB manual EQ setting 0x1001: 9.7dB manual EQ setting 0x1010: 11dB manual EQ setting 0x1011: 12.2dB manual EQ setting 0x1100: Reserved 0x1101: Reserved 0x1110: Reserved 0x1111: Reserved

GMSL1_6 (0xB06)

HIM, HV_VSYNC, Packet-Based, and GPI Settings

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
Reset	0b0	0b1	0b1	0b0	0b1	0b111		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit 0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I^2C retransmission enable	0b0: Disable I^2C retransmission 0b1: Enable I^2C retransmission enable
GPI_COMP_EN	4	GPI skew compensation enable	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission
HV_SRC	2:0	HV_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.125Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

GMSL1_7 (0xB07)

DBL, DRS, BWS, HIBW, HVEN, and PXL_CRC Settings

BIT	7	6	5	4	3	2	1	0
Field	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	High-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN=0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_8 (0xB08)

GPI, FSYNC_TX, PCKT_CC, Control-Channel CRC

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
Reset	–	–	0b1	0b0	–	0b0	0b01	
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_EN	5	Enable GPI-to-GPO signal transmission to serializer	0b0: Disable GPI-to-GPO transmission 0b1: Enable GPI-to-GPO transmission
EN_FSYNC_TX	4	Enable frame sync signal transmission	0x0: Disable 0x1: Enable
PKTCC_EN	2	Packet based control channel mode enable	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LENGTH	1:0	Control channel CRC length	0b00: 1-bit CRC 0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

GMSL1_D (0xB0D)

I^2C Local Acknowledge

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enable I^2C-to-I^2C subordinate local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available

GMSL1_E (0xB0E)

Error Detection Threshold

BIT	7	6	5	4	3	2	1	0
Field	DET_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_THR	7:0	Threshold for detected errors	0xXX: Number of errors for detected error threshold

GMSL1_F (0xB0F)

DE/HS/VS—Glitch Filters/PRBS Type Select/DE Processing

BIT	7	6	5	4	3	2	1	0
Field	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
Reset	–	0b0	0b0	0b0	0b1	–	–	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DE_FILT	6	Enable glitch filtering on DE	0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering
EN_HS_FILT	5	Enable glitch filtering on HS	0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering
EN_VS_FILT	4	Enable glitch filtering on VS	0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering
DE_EN	3	Enable processing separate HS and DE signals	0b0: Disable processing HS and DE signals 0b1: Enable processing HS and DE signals
PRBS_TYPE	0	PRBS type select (in HIBW mode, set PRBS_TYPE = 0)	0b0: GMSL1 legacy video PRBS test 0b1: GMSL1 legacy link PRBS test

GMSL1_10 (0xB10)

PCKT Based REV CH Error Generator CFG and EN

BIT	7	6	5	4	3	2	1	0
Field	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
Reset	0b00		0b0	0x1				0b0
Access Type	Write, Read		Write, Read	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (Effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (Effective when RCEG_TYPE = 0x)	0xX: Number of errors generated per request
RCEG_EN	0	Enable reverse channel error generator	0b0: Disable reverse channel error generator 0b1: Enable reverse channel error generator enabled

GMSL1_11 (0xB11)

PCKT Based REV CH Error Generator CFG

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
Reset	0xF				0b00		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG\_ERR\_RATE+3)}$. (Effective when RCEG_TYPE = 0x)	0x0: Rate is 2^{-3} 0x1: Rate is 2^{-4} 0x2: Rate is 2^{-5} ... ... 0xF: Rate is 2^{-18}
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150µs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

GMSL1_12 (0xB12)

PCKT Based REV CH CFG/Video Line CRC/ERR CFG/Reporting

BIT	7	6	5	4	3	2	1	0
Field	UNDERBST_DET_EN	CC_CRC_ERR_EN	–	–	LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
Reset	0b0	0b1	–	–	0b0	–	0b1	0b0
Access Type	Write, Read	Write, Read	–	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBST_DET_EN	7	Allow underboost detection driving ERRORB pin	0b0: Disable underboost detection driving ERRORB pin 0b1: Enable underboost detection driving ERROR pin

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERR_EN	6	Enable reporting of (CC_CRC_ERR_CNT > 0) on the ERRORB pin	0b0: Disable reporting of errors on ERRB 0b1: Enable reporting of errors on ERRB
LINE_CRC_EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0x1: Enable video line CRC
MAX_RT_ERR_EN	1	Enable reflection of maximum retransmission error on the ERRB pin	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR_PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

GMSL1_13 (0xB13)

BIT	7	6	5	4	3	2	1	0
Field	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
Reset	0b1	0b1	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EN_G1	7	Eye-opening monitor enable	0b0: Disable EOM 0x1: Enable EOM
EOM_PER_MODE_G1	6	Eye-opening monitor periodic mode select	non-periodic 0b0: Set EOM to use nonperiodic mode 0x1: Set EOM to use periodic mode
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger EOM 0x1: Manually trigger the EOM
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRORB pin	0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% 0b11111: 100%

GMSL1_14 (0xB14)

AEQ Settings

BIT	7	6	5	4	3	2	1	0
Field	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
Reset	0b1	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization enable	0b0: Disable AEQ 0x1: Enable AEQ

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use nonperiodic mode 0x1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Adaptive equalizer manual fine-tune request enable. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger AEQ fine-tuning 0x1: Manually trigger the AEQ fine-tuning
EOM_PER_THR	4:0	Eye-opening threshold to trigger a fine-tune operation	Eye-opening 0b00000: Eye-opening threshold is disabled 0b10000: 50% eye-opening triggers fine-tune operation OTHER: Reserved

GMSL1_15 (0xB15)

Decode ERR

BIT	7	6	5	4	3	2	1	0
Field	DET_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_ERR	7:0	Number of decode errors detected	0xXX: Number of detected errors

GMSL1_16 (0xB16)

PRBS ERR

BIT	7	6	5	4	3	2	1	0
Field	PRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_ERR	7:0	PRBS error counter	0xXX: Number of detected PRBS errors

GMSL1_17 (0xB17)

Retransmit I^2C/GPI—GPI Status/PRBS Status

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
Reset	–	0b0	0b0	0b0	0b0	–	–	–
Access Type	–	Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_I2C	6	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_OK	5	MAX9271/73 compatible PRBS test for the link is completed normally. Check PRBS_ERR register for the PRBS success. For other SERDES read PRBS_ERR registers.	0b0: No MAX9271/MAX9273-compatible PRBS test completed 0b1: MAX9271/MAX9273-compatible PRBS test completed normally
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ERR_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_19 (0xB19)

Packet CRC Errors Detected

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control channel CRC error counter	0xXX: Number of control channel CRC errors

GMSL1_1A (0xB1A)

CC ERR Generator Counter

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_CNT	7:0	Control channel number of generated errors	0xXX: Number of control channel generated errors

GMSL1_1B (0xB1B)

Video Line CRC Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LINE_CRC_ERR	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error - cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

GMSL1_1C (0xB1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EOM_EYE_WIDTH[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured Eye-opening. Opening width = EOM_EYE_WIDTH/63 * 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% ... ... 0b11111: Width is 63/63 x 100%

GMSL1_1D (0xB1D)

Underboost and AEQ Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Underboost detected	0b0: Normal Operation 0x1: Underboost (at maximum AEQ gain) detected
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 750MHz	0b0000: 1.6dB EQ setting 0x0001: 2.1dB EQ setting 0x0010: 2.8dB EQ setting 0x0011: 3.5dB EQ setting 0x0100: 4.3dB EQ setting 0x0101: 5.2dB EQ setting 0x0110: 6.3dB EQ setting 0x0111: 7.3dB EQ setting 0x1000: 8.5dB EQ setting 0x1001: 9.7dB EQ setting 0x1010: 11dB EQ setting 0x1011: 12.2dB EQ setting 0x1100: Reserved 0x1101: Reserved 0x1110: Reserved 0x1111: Reserved

GMSL1_96 (0xB96)

Data Type Conversion for GMSL1 to GMSL2

BIT	7	6	5	4	3	2	1	0
Field	CONV_GMSL1_DATATYPE[4:0]					–	CONV_GMSL1_EN	–
Reset	0b00000					–	0b0	–
Access Type	Write, Read					–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_GMSL1_DATATYPE	7:3	Convert from GMSL1 color format mapping to GMSL2 CSI transmitter color format	0x0: RGB888 OLDI 0x1: RGB565 0x2: RGB666 0x3: YUV 422 8-bit Mux mode (use yuv_8_10_mux_mode) 0x4: YUV 422 10-bit Mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined Generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined Generic 8-bit 0xC 0xD 0xE 0xF 0x10: RGB888 VESA® 0x11 0x12 0x13: YUV 422 8-bit Normal mode 0x14: YUV 422 10-bit Normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F
CONV_GMSL1_EN	1	Enable conversion from GMSL1 color format mapping to GMSL2 CSI transmitter	

GMSL1_A7 (0xBA7)

HSYNC/VSYNC Conversion for GMSL1 to GMSL2

BIT	7	6	5	4	3	2	1	0
Field	–	SHIFT_VID_HVD	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
SHIFT_VID_HVD	6	Shift video bits to make sure that the HS, VS does not appear on pixel data

GMSL1_CB (0xBCB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOCKED_G1
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
LOCKED_G1	0	Link locked

GMSL1_D1 (0xBD1)

CTRL Pin Configuration and Enable

BIT	7	6	5	4	3	2	1	0
Field	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
Reset	0x0			0b00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_OUT_ORD	7:5	Internal CNTL_OUT order to pins CNTL4 to CNTL0	0x0: 4,3,2,1,0 0x1: 3,2,1,0,4 0x2: 2,1,0,4,3 0x3: 1,0,4,3,2 0x4: 0,1,2,3,4 0x5: 1,2,3,4,0 0x6: 2,3,4,0,1 0x7: 3,4,0,1,2
CNTL_OUT_EN	4:0	CNTL output enable for CNTL 0,1,2,3,4	

COMMON1 (0xF02)

GMSL1 I^2C Remote ACK Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	REM_ACK_ACKED_G1_A
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ACK_ACKED_G1_A	0	Remote ACK acknowledged	0b0: Remote ACK not acknowledged 0b1: Remote ACK acknowledged

GMSL1_ERR_OEN (0xF03)

ERRB Reporting Enabling

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	G1_A_ERR_OEN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
G1_A_ERR_OEN	0	Enable reporting of GMSL1 Link A errors (G1_A_ERR_FLAG - 0xF03) at ERRB pin

GMSL1_ERR_FLAG (0xF04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	G1_A_ERR_FLAG
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
G1_A_ERR_FLAG	0	GMSL1 Link A error flag. When PRBS test is enabled, it is asserted when at least one PRBS error has been detected. When PRBS test is not enabled, it is asserted when any of these conditions is true: 1) Number of detected decoding errors are greater than the detected error threshold (DET_ERR > DET_THR) 2) Measured eye-opening is less than or equal to eye-opening threshold (EOM_EYE_WIDTH ≤ EOM_MIN_THR_G1) 3) Adaptive EQ has detected under boost 4) Video Line CRC error is detected 5) Exceeded maximum retransmission count in PKTCC communication 6) CRC errors detected in PKTCC communication

I2C_0 (0xF05)

GMSL1 I^2C Subordinate Setup and Timeout Configuration

BIT	7	6	5	4	3	2	1	0
Field	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SLV_SH	5:4	GMSL1 I2C-to-I2C subordinate setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I2C subordinate. Set this according to the I2C speed mode: Fast-mode Plus = 00 Fast-mode = 01 Standard-mode = 10 See register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b00: Set for I2C Fast-mode Plus speed (1Mbps) 0b01: Set for I2C Fast-mode speed (400Kbps) 0b10: Set for I2C standard-mode speed (100Kbps) 0b11: Reserved
G1_SLV_TO	2:0	GMSL1 I2C-to-I2C subordinate timeout setting Internal GMSL1 I2C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from remote device. See register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0xF06)

GMSL1 I2C Main Setup and Timeout Configuration

BIT	7	6	5	4	3	2	1	0
Field	EN_I2C_LOOPBACK	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type	Write, Read	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
EN_I2C_LOOPBACK	7	Enable I2C loopback between links in G1 + G2 or G1 + G1 aggregation mode. When I2C loopback is enabled, the I2C transactions generated at the leaf-end of one link are reflected to the leaf-end of the other link	0x0: Disable loopback 0x1: Enable loopback

BITFIELD	BITS	DESCRIPTION	DECODE
G1_MST_BT	6:4	GMSL1 I2C-to-I2C main bit rate setting Configures the I2C bit rate used by the internal I2C main (in the device on remote side from the external I2C main) Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010 See register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b000: 9.92Kbps - Set for I2C Standard mode speed 0b001: 33.2Kbps - Set for I2C Standard mode speed 0b010: 99.2Kbps - Set for I2C standard or Fast-mode speed 0b011: 123Kbps - Set for I2C Fast-mode speed 0b100: 203Kbps - Set for I2C Fast-mode speed 0b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I2C Fast-mode Plus speed 0b111: 980Kbps - Set for I2C Fast-mode Plus speed
G1_MST_TO	2:0	GMSL1 I2C-to-I2C main timeout setting Internal GMSL1 I2C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. See register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

RLMS3 (0x1403)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt process enable	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x1404)

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye-monitor window. N is used in the equation: Observations = $6.29 \times 10^{(N+2)}$	0xX: N factor

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_ THR	3:2	Eye-opening monitor number of error bits allowed in a measurement window	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
EOM_PER_ MODE	1	Eye-Opening Monitor Periodic Mode Enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-Opening Monitor Enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405)

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN _TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_ TRG_REQ	7	Eye-Opening Monitor Manual Trigger For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_T HR	6:0	The eye-opening monitor minimum threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: Eye-opening monitor minimum threshold factor

RLMS6 (0x1406)

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_ MODE	EOM_RST_THR[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_M ODE	7	Eye-opening is measured vertically or horizontally	0b0: Vertical opening mode 0b1: Horizontal opening mode
EOM_RST_T HR	6:0	The eye-opening monitor refresh threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: EOM refresh threshold factor

RLMS7 (0x1407)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-Opening Monitor Measurement Done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed EOM observation	0bXXXXXXX: EOM measurement result

RLMS3E (0x143E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0b1	0x03						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	The phase interpolator command to align the error sampling channel and the secondary data channel to optimize 6G GMSL2 channel link margin	0: Reserved 1: Set value to '1'
ErrChPhSec	6:0	The phase interpolator command to align the error sampling channel and the secondary data channel to optimize 6G GMSL2 channel link margin	0x7D: Set value to 0x7D Others: Reserved

RLMS3F (0x143F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0b0	0x43						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	The phase interpolator command to align the error sampling channel and the primary data channel to optimize 6G GMSL2 channel link margin	0: Set value to '0' 1: Reserved
ErrChPhPri	6:0	The phase interpolator command to align the error sampling channel and the primary data channel to optimize 6G GMSL2 channel link margin	0x3D: Set value to 0x3D Others: Reserved

RLMS49 (0x1449)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ErrChPwrUp	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error channel power up. Set this bit = 1 to force the Error Channel always to powered up	0: Normal operation 1: Force Error Channel powered up

RLMS64 (0x1464)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCMode[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx Spread Spectrum Mode	00: No spread spectrum (manual phase) 01: Reserved 10: Reserved 11: Center spread

RLMS70 (0x1470)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx SSC modulation frequency control	0x07: SSC 268ppm 0x06: SSC 580ppm 0x03: SSC 970ppm 0x01: SSC 1750ppm 0x01: SSC 2530ppm others: Reserved

RLMS71 (0x1471)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx SSC center spread starting phase	0x02: SSC 268ppm 0x02: SSC 580ppm 0x02: SSC 970ppm 0x02: SSC 1750ppm 0x02: SSC 2530ppm others: Reserved
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx SSC frequency prescaler low	0xC9: SSC 26ppm 0xAB: SSC 580ppm 0xAB: SSC 970ppm 0xF9: SSC 1750ppm 0xAB: SSC 2530ppm others: Reserved

RLMS73 (0x1473)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx SSC frequency prescaler high	0x02: SSC 268ppm 0x00: SSC 580ppm 0x00: SSC 970ppm 0x00: SSC 1750ppm 0x00: SSC 2530ppm others: Reserved

RLMS74 (0x1474)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx SSC phase accumulator increment low	0xF9: SSC 268ppm 0x63: SSC 580ppm 0x63: SSC 970ppm 0x2C: SSC 1750ppm 0x63: SSC 2530ppm others: Reserved

RLMS75 (0x1475)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx SSC phase accumulator increment high	0x01: SSC 268ppm 0x07: SSC 580ppm 0x07: SSC 970ppm 0x05: SSC 1750ppm 0x07: SSC 2530ppm others: Reserved

RLMS76 (0x1476)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx SSC phase starting phase quadrant	0x00: SSC 268ppm 0x00: SSC 580ppm 0x00: SSC 970ppm 0x00: SSC 1750ppm 0x00: SSC 2530ppm others: Reserved

RLMS7E (0x147E)

BIT	7	6	5	4	3	2	1	0
Field	D2ErrChPhSecTA	D2ErrChPhSec[6:0]						
Reset	0b1	0x5A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
D2ErrChPhSecTA	7	The phase interpolator command to align the error sampling channel and the secondary data channel to optimize 3G GMSL2 channel link margin	0: Reserved 1: Set value to '0'

BITFIELD	BITS	DESCRIPTION	DECODE
D2ErrChPhSec	6:0	The phase interpolator command to align the error sampling channel and the secondary data channel to optimize 3G GMSL2 channel link margin	0x28: Set value to 0x28 Others: Reserved

RLMS7F (0x147F)

BIT	7	6	5	4	3	2	1	0
Field	D2ErrChPhPriTA	D2ErrChPhPri[6:0]						
Reset	0b0	0x1B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
D2ErrChPhPriTA	7	The phase interpolator command to align the error sampling channel and the primary data channel to optimize 3G GMSL2 channel link margin	0: Set value to '0' 1: Reserved
D2ErrChPhPri	6:0	The phase interpolator command to align the error sampling channel and the primary data channel to optimize 3G GMSL2 channel link margin	0x68: Set value to 0x68 Others: Reserved

RLMS95 (0x1495)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	–	TxAmplMan[5:0]					
Reset	0b0	–	0b101001					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	TX amplitude manual override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMS98 (0x1498)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	Rxhpf_cnt[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
Rxhpf_cnt	2:0	Rxhpf_cnt value during RLMS (MSB = Enable)	0bXXXXXX: Rx high pass filter setting

RLMSA3 (0x14A3)

BIT	7	6	5	4	3	2	1	0
Field	DFEBST[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DFEBST	7:4	Enable DFE boost to increase the bandwidth	0x3: Set value to 0x3 Others: Reserved

RLMSA4 (0x14A4)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0b10		0b111101					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier	00: 1ms 01: 4ms 10: 16ms 11: 64ms
AEQ_PER	5:0	Adaptive EQ period Periodic adaptation is disabled when value is 0 Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT)	

RLMSA5 (0x14A5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PHYC_WBLOCK_DLY[1:0]		–	–	–	–
Reset	–	–	0b10		–	–	–	–
Access Type	–	–	Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PHYC_WBLOCK_DLY	5:4	PHY controller word boundary lock start delay	00: 1 ms 01: 2 ms 10: 4 ms 11: 8 ms

RLMSD8 (0x14D8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	sub_bst_trim[2:0]			sub_gain_ctrl
Reset	–	–	–	–	0b000			0b0
Access Type	–	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
sub_bst_trim	3:1	Subtractor boost trim	0x3: Set value to 3 Others: Reserved
sub_gain_ctrl	0	Enable Subtractor gain control	0: Reserved 1: Set value to '1'

REGCRC0 (0x3000)

Register CRC for Configuration

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_ROLLING_CRC	4	Calculate CRC using additional 2-bit counter, so CRC value cycles every four invocations.	
I2C_WR_COMPUTE	3	Execute CRC computation after every I^2C register write.	0b0: Disabled 0b1: Enabled
PERIODIC_COMPUTE	2	Register CRC computation period enable Refer to REGCRC1 (0x3001) - to change the timing period	0b0: Disabled 0b1: Enabled
CHECK_CRC	1	Register CRC check enable - This compares the previous CRC value and if the CRC value does not match an error occurs. This error is mapped to ERRB.	0b0: Disabled 0b1: Enabled
RESET_CRC	0	Reset for Register CRC This is required when enabling the Register CRC. If an error occurs, a reset is done to re-enable the Register CRC.	0b0: Normal State 0b1: Reset

REGCRC1 (0x3001)

Register CRC Occurrence

BIT	7	6	5	4	3	2	1	0
Field	CRC_PERIOD[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_PERIOD	7:0	Period for CRC occurrence - to enable see REGCRC0	0b00: 2msecs 0b01: 4msecs ... 0bFF: 512msecs

REGCRC2 (0x3002)

Register Table CRC Calculated Value

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_LSB	7:0	CRC result LSB This is used to prove Rolling CRC is effectively working

REGCRC3 (0x3003)

Register Table CRC Calculated Value

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_MSB	7:0	CRC result MSB This is used to prove Rolling CRC is effectively working

I2C_UART_CRC0 (0x3008)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RESET_MSGCNTR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_MSGCNTR	0	Reset Message Counter Value to 0	0b0: Reset deasserted 0b1: Reset asserted

I2C_UART_CRC1 (0x3009)

I2C/UART Message Counter CRC

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_THR[2:0]			CRC_ERR_THR[2:0]			RESET_MSGCNTR_ERR_CNT	RESET_CRC_ERR_CNT
Reset	0b0			0b0			0b0	0b0
Access Type	Write, Read			Write, Read			Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_ERR_THR	7:5	Decoding and idle-error reporting threshold. MSGCTR_ERR_FLAG_A is asserted when MSGCTR_ERR_A ≥ MSGCTR_ERR_THR MSGCTR_ERR_FLAG_B is asserted when MSGCTR_ERR_B ≥ MSG_ERR_THR IDLE_ERR_FLAG is asserted when IDLE_ERR ≥ DEC_ERR_THR	
CRC_ERR_THR	4:2	Decoding and idle-error reporting threshold CRC_ERR_FLAG_A is asserted when CRC_ERR_A ≥ CRC_ERR_THR CRC_ERR_FLAG_B is asserted when CRC_ERR_B ≥ CRC_ERR_THR IDLE_ERR_FLAG is asserted when IDLE_ERR ≥ DEC_ERR_THR	
RESET_MSGCNTR_ERR_CNT	1	Reset Message Counter Error Count to 0	0b0: Reset deasserted 0b1: Reset asserted
RESET_CRC_ERR_CNT	0	Reset CRC Error Count to 0	0b0: Reset deasserted 0b1: Reset asserted

I2C_UART_CRC2 (0x300A)

Primary I²C/UART CRC value

BIT	7	6	5	4	3	2	1	0
Field	CRC_VAL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VAL	7:0	Calculated CRC value for the last write transaction	0xXX: Calculated CRC value

I2C_UART_CRC3 (0x300B)

Primary I²C/UART Message Counter LSB Value

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_LSB	7:0	Bits 7:0 of current message counter value	0xXX: Bits 7:0 of current message counter value

I2C_UART_CRC4 (0x300C)

Primary I2C/UART Message Counter MLSB Value

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_MSB	7:0	Bits 7:0 of current message counter value	0xXX: Bits 15:8 of current message counter value

I2C_UART_CRC5 (0x300D)

BIT	7	6	5	4	3	2	1	0
Field	CRC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_ERR_CNT	7:0	Number of CRC errors observed	0xXX: Number of CRC errors observed

I2C_UART_CRC6 (0x300E)

Primary I2C/UART Message Counter Error Count

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_ERR_CNT	7:0	Number of message counter errors observed	0xXX: Number of message counter errors observed

I2C_UART_CRC7 (0x300F)

MSG Counter and CRC Enables

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MSGCNTR_PORT_SEL[1:0]		CC_MSGCNTR_EN	CC_CRC_EN	CC_CRC_MSGCNTR_OVR
Reset	–	–	–	0x0		0b1	0b1	0b0
Access Type	–	–	–	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_PORT_SEL	4:3	Selects the current message/CRC counter Selects between the ports for values read from MSGCCNTR_LSB/MSB, MSGCNTR_ERR_CNT, CRC_VAL, and CRC_ERR_CNT.	0b00: Primary I^2C/UART 0b01: Pass-through 1 I^2C/UART 0b10: Pass-through 2 I^2C/UART
CC_MSGCNTR_EN	2	Enable I^2C/UART message counter override when set to 1 Only active when CC_CRC_MSGCNTR_OVR = 1.	0b0: Reporting disabled 0b1: Reporting enabled
CC_CRC_EN	1	Enable I^2C/UART CRC override when set to 1 Only active when CC_CRC_MSGCNTR_OVR = 1.	0b0: Reporting disabled 0b1: Reporting enabled
CC_CRC_MSGCNTR_OVR	0	Enable I^2C/UART CRC or message counter override when set to 1 When 0, eFuse controls CRC and message counter options.	0b0: Reporting disabled 0b1: Reporting enabled

FS_INTR0 (0x3010)

MSG, I^2C/UART CRC, ECC, EFUSE, REG CRC—ERRB Reporting

BIT	7	6	5	4	3	2	1	0
Field	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	EFUSE_CRC_ERR_OEN	REG_CRC_ERR_OEN
Reset	0b1	0b1	0b1	0b0	–	–	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_UART_MSGCNTR_ERR_OEN	7	Enable reporting of decoding errors (I2C_UART_MSGCNTR_ERR) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
I2C_UART_CRC_ERR_OEN	6	Enable reporting of decoding errors (I2C_UART_CRC_ERR) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_ECC_ERR2_OEN	5	Enable reporting of memory ECC 2-bit uncorrectable errors at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_ECC_ERR1_OEN	4	Enable reporting of memory ECC 1-bit correctable errors at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
EFUSE_CRC_ERR_OEN	1	Enable reporting eFuse CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
REG_CRC_ERR_OEN	0	Enable reporting register CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

FS_INTR1 (0x3011)

MSG, I2C/UART CRC, ECC, EFUSE, REG CRC—Flag Reporting

BIT	7	6	5	4	3	2	1	0
Field	I2C_UART_MSGCNTR_ERR_INT	I2C_UART_CRC_ERR_INT	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	EFUSE_CRC_ERR_FLAG	REG_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_UART_MSGCNTR_ERR_INT	7	Decoding error flag for Link A, asserted when MSTCNTR_ERR_CNT ≥ MSGCNTR_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_CRC_ERR_INT	6	Decoding error flag for Link A, asserted when CRC_ERR_CNT ≥ CRC_ERR_THR	0b0: Flag not asserted 0b1: Flag asserted
MEM_ECC_ERR2_INT	5	Decoding error flag for 2-bit uncorrectable memory ECC errors, asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.	0b0: Flag not asserted 0b1: Flag asserted
MEM_ECC_ERR1_INT	4	Decoding error flag for 1-bit correctable memory ECC errors, asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.	0b0: Flag not asserted 0b1: Flag asserted
EFUSE_CRC_ERR_FLAG	1	An error occurred on the eFuse CRC calculation	0b0: Flag not asserted 0b1: Flag asserted
REG_CRC_ERR_FLAG	0	An error occurred on the register CRC calculation	0b0: Flag not asserted 0b1: Flag asserted

MEM_ECC0 (0x3016)

Memory ECC Threshold and Reset

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
Reset	0b0			0b0			0b0	0b0
Access Type	Write, Read			Write, Read			Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR2_THR	7:5	Decoding and error reporting threshold. MEM_ECC_ERR2 is asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR1_THR	4:2	Decoding and error reporting threshold MEM_ECC_ERR1 is asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.
RESET_MEM_ECC_ERR2_CNT	1	Reset memory ECC 2-bit error count to 0
RESET_MEM_ECC_ERR1_CNT	0	Reset memory ECC 1-bit error count to 0

MEM_ECC1 (0x3017)

Memory ECC 1-Bit Count

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR1_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR1_CNT	7:0	Number of 1-bit correctable memory ECC errors observed

MEM_ECC2 (0x3018)

Memory ECC 2-Bit Count

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR2_CNT	7:0	Number of 2-bit uncorrectable memory ECC errors observed

REG_POST0 (0x3020)

POST/MBIST/LBIST

BIT	7	6	5	4	3	2	1	0
Field	POST_DONE	POST_MBIST_PASSED	POST_LBIST_PASSED	–	–	–	POST_RUN_MBIST	POST_RUN_LBIST
Reset	0b0	0b0	0b0	–	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
POST_DONE	7	POST has been run
POST_MBIST_PASSED	6	MBIST passed during POST
POST_LBIST_PASSED	5	LBIST passed during POST
POST_RUN_MBIST	1	Indicates the chip runs MBIST during POST.

BITFIELD	BITS	DESCRIPTION
POST_RUN_LBIST	0	Indicates the chip runs LBIST during POST.

REGCRC8 (0x3030)

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP0_LSB	7:0	Address 0 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC9 (0x3031)

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP0_MSB	7:0	Address 0 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC10 (0x3032)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP1_LSB	7:0	Address 1 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC11 (0x3033)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP1_MSB	7:0	Address 1 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC12 (0x3034)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP2_LSB	7:0	Address 2 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC13 (0x3035)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP2_MSB	7:0	Address 2 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC14 (0x3036)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP3_LSB	7:0	Address 3 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC15 (0x3037)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP3_MSB	7:0	Address 3 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC16 (0x3038)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP4_LSB	7:0	Address 4 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC17 (0x3039)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP4_MSB	7:0	Address 4 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC18 (0x303A)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP5_LSB	7:0	Address 5 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC19 (0x303B)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP5_MSB	7:0	Address 5 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC20 (0x303C)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP6_LSB	7:0	Address 6 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC21 (0x303D)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP6_MSB	7:0	Address 6 to skip (MSB)	0xXX: MSB of Address to skip

REGCRC22 (0x303E)

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP7_LSB	7:0	Address 7 to skip (LSB)	0xXX: LSB of Address to skip

REGCRC23 (0x303F)

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP7_MSB	7:0	Address 7 to skip (MSB)	0xXX: MSB of Address to skip

INTR10 (0x5010)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VDD18_OV_OEN	–	–	–	VDD_OV_OEN
Reset	–	–	–	0b0	–	–	–	0b0
Access Type	–	–	–	Write, Read	–	–	–	Write, Read

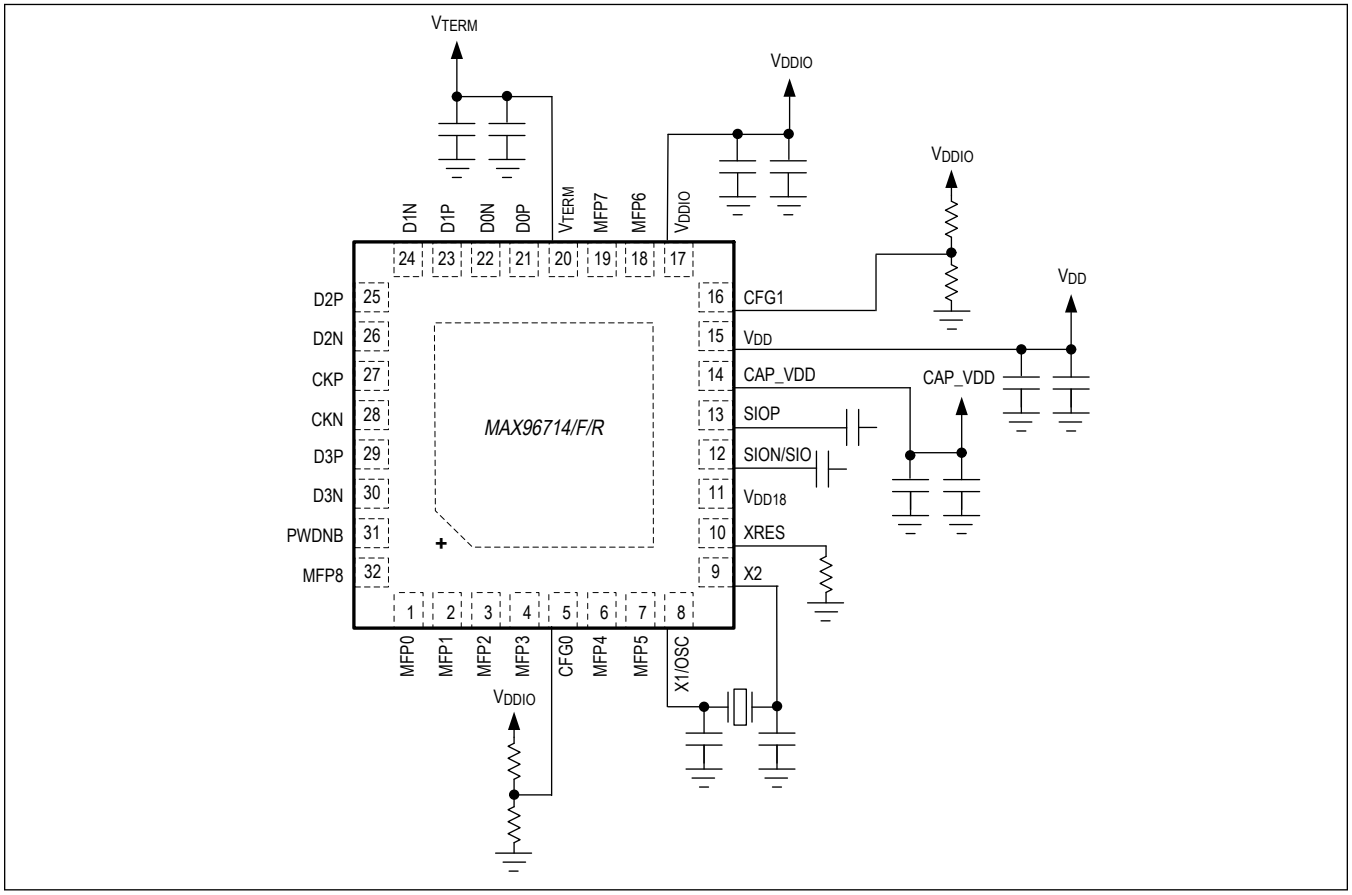
BITFIELD	BITS	DESCRIPTION	DECODE
VDD18_OV_OEN	4	Enable V_{DD18} overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
VDD_OV_OEN	0	Enable V_{DD} overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled

INTR11 (0x5011)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VDD18_OV_FLAG	–	–	–	VDD_OV_FLAG
Reset	–	–	–	0b0	–	–	–	0b0
Access Type	–	–	–	Read Clears All	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VDD18_OV_FLAG	4	Sticky status value for V_{DD18} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VDD_OV_FLAG	0	Sticky status value for V_{DD} overvoltage flag	0b0: Flag not asserted 0b1: Flag asserted

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	ASIL
MAX96714GTJ/VY+	-40°C to +105°C	32-Pin TQFN-SW-EP	B
MAX96714GTJ/VY+T	-40°C to +105°C	32-Pin TQFN-SW-EP	B
MAX96714FGTJ/VY+	-40°C to +105°C	32-Pin TQFN-SW-EP	B
MAX96714FGTJ/VY+T	-40°C to +105°C	32-Pin TQFN-SW-EP	B
MAX96714FGTJ/V+	-40°C to +105°C	32-Pin TQFN-EP	B
MAX96714FGTJ/V+T	-40°C to +105°C	32-Pin TQFN-EP	B
MAX96714RGTJ/VY	-40°C to +105°C	32-Pin TQFN-SW-EP	QM
MAX96714RGTJ/VY+T	-40°C to +105°C	32-Pin TQFN-SW-EP	QM
MAX96714RGTJ/V+	-40°C to +105°C	32-Pin TQFN-EP	QM
MAX96714RGTJ/V+T	-40°C to +105°C	32-Pin TQFN-EP	QM

/V = Automotive qualified product

Y = Wettable flank

+ = Lead(Pb)-free/RoHS-compliant package

T = Tape and Reel

EP = Exposed Pad

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—
1	8/21	Added RoR section	1, 44
2	6/23	Replace Master/Slave with Main/Subordinate Replace Main I2C/UART with Primary I2C/UART Add RoR to MAX96714R Package information: Note Add "in still air" PWDNB Hold time: Increase from 1ms to 1us ESD Protection: Moved to Reccomeneded operating table Pin Description: Removed Oscillator connections from GMSL1 mode Added instructions for 1V VDD mode Detailed Description: Tunnel mode: Updated the description Device Reset and Power Donw: Remove references to multiple links Link and video Lock: Swap reference from Serialzer to deserializer Power Supplies Infomration and Overview: Updated the description to include 1V operation Thermal Management: Include note to keep Juction below 125C Ordering Information: added MAX96714RGTJ/VY+ and MAX69714RGTJ/VY+T Register Map: add CMP_VTERM_STATUS, Remove PORZ_INT_OEN PORZ_INT_FLAG, add Adapt Enable, TX_AMPL_MAN, TX_AMPL_MAN_EN, RXHPF_CNT, REV TRFMANEN, REVTRFMAN, REVLEMMANEN, REVFLENMAN, AEQ_PER, AEQ_PER_MULT, TX TRF REGCRC8, REGCRC9 Update Descriptions GRAD_MODE, PATGEN_MODE, PIO_SLEW_, PRBS_TYPE	1, 6, 10, 15, 20, 35, 37, 38, 40, 43, 44, 50, 51, 53, 54, 66, 71, 72, 74, 76, 77, 78, 80, 85, 105, 106, 125, 130, 131, 133, 134, 139, 140, 141, 144, 145, 146