MAX96751

GMSL2 Serializer with HDMI 2.0 Input

General Description

The MAX96751 serializer converts HDMI® to single or dual GMSL™ serial protocol. It also sends and receives side-channel and peripheral control data, enabling full-duplex, single-wire, transmission of video and bidirectional data. Each GMSL2 link operates at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in the reverse direction.

The MAX96751 supports RGB888 video at up to 215MHz PCLK per GMSL2 link.

For designs supporting two displays, see the New Designs Supporting Two Displays section of Detailed Descriptions for more information.

The GMSL2 concurrent control channel operates in I^2C or UART mode. Two additional pass-through I^2C or UART channels and a pass-through SPI channel are provided for peripheral control. The bidirectional audio channel supports I^2S stereo and up to 8 channels in Time-Division Multiplexing (TDM) mode.

Data can be transmitted over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 Channel Specification. Contact the factory to receive the GMSL2 Channel Specification document.

Table 1. **Typical Maximum Cable Length**

	3.2mm Ø 50Ω Coax, Foam Dielectric	**2.7mm Ø 50Ω Coax, Solid Dielectric**	**100Ω Shielded Twisted Pair, AWG26**
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°C**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Applications

- Navigation and Touch-Panel Displays
- Digital Instrument Clusters and Heads-Up Displays
- Rear-Seat and Passenger Infotainment Displays
- Consumer HDMI Port Applications

Benefits and Features

- HDMI v1.4b/v2.0a Input Interface
- 3Gbps or 6Gbps Forward-Link Rates
- 187.5Mbps Reverse-Link Rate
- Full-Duplex Capability Over a Single Wire
- Ideal for High-Definition Video Applications
  - Up to 215MHz PCLK per Link
  - Up to 430MHz PCLK in Dual-Link Mode
- Uses Low-Cost 50Ω Coax or 100Ω STP Cables
- Forward and Reverse I^2S or 7.1 TDM Audio
- Video Pattern Generator Provides Fast Link Validation
- Line-Fault Monitor Detects Serial I/O Shorted Together, to Ground, to Battery or Open
- ASIL-Relevant Functional Safety Features
  - ASIL B Compliant
  - 16-Bit CRC Protection of Control-Channel Data (I^2C, UART, SPI, GPIO, Audio)
  - Retransmission on Error of all Control-Channel Data and Audio Data Upon Error Detection
  - Optional 32-Bit Video-Line CRC
  - Selectable Interrupts for Fault Detection
  - Video Watermark Generation
- Performance Tools Ensure High Link Margin
  - Continuous Adaptive Equalization on GMSL Links
  - Built-In Forward- and Reverse-Channel PRBS Generator for BER Testing of Serial I/O Links
  - Eye-Opening Monitor for Link Diagnosis
- Concurrent Control Channel for Device Configuration and Communication with Remote Peripherals
  - Primary and Pass-Through I^2C/UART, SPI, and Tunneled or Register-Programmable GPIO
  - Settable Priority Levels
  - Eight Hardware Programmable Device Addresses
  - Up to 20 Programmable GPIO
  - Sleep Mode with Register State Retention
- Operation Specified Over the -40°C to +105°C Automotive Temperature Range
- AEC-Q100 Qualified
- Compact 8mm x 8mm TQFN with an Exposed Pad

This product contains licensed HDMI technology. Customers must be HDMI adopters listed at HDMI.org.

***Ordering Information** appears at end of the datasheet.*

19-101780; Rev 0; 4/24

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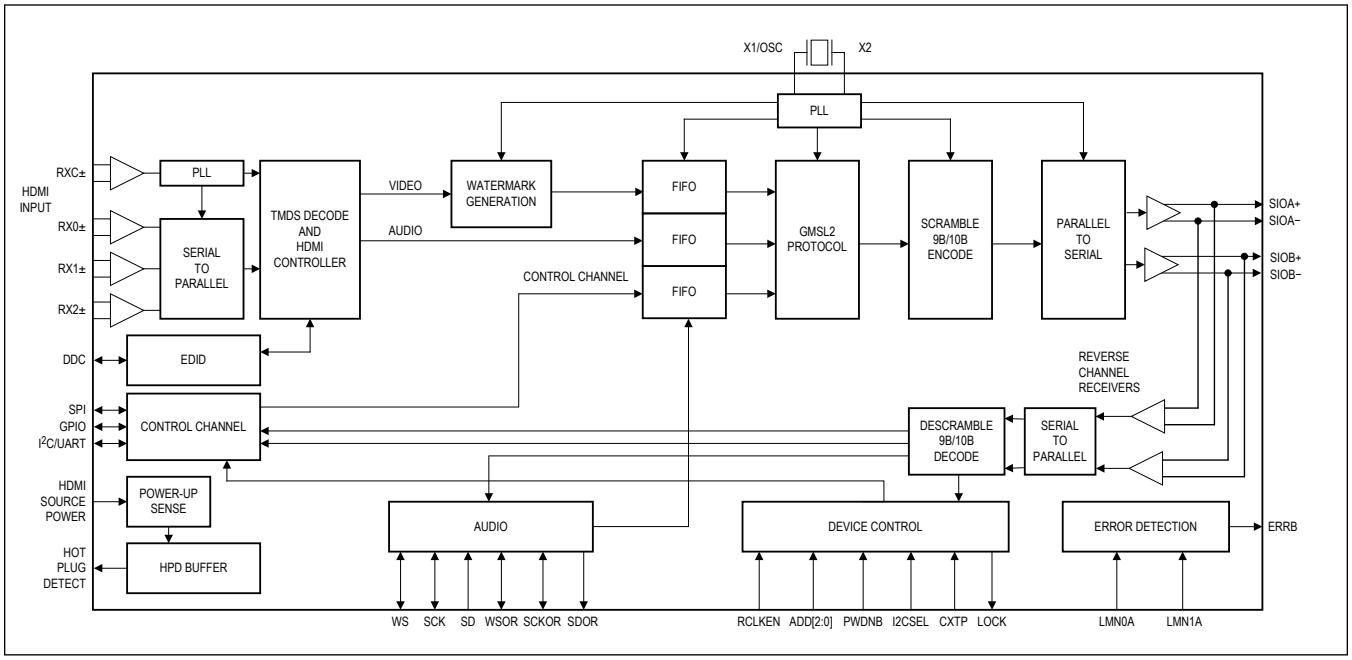
Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DDD}, V_{DDA} ..... -0.3V to +1.1V
V_{DD33} ..... -0.3V to +3.9V
Rx__ ..... -0.3V to +3.9V
SIO__ (Active State) (*Note a*) ..... (V_{DD18} - 1.1V) to V_{DD18}
SIO__ (Inactive State) (*Note a*) ..... -0.3V to +1.1V
RX_, RXC_ ..... (V_{DD33} - 1.3V) to (V_{DD33} + 0.3V)
LMN_ ..... -0.3V to +2.0V
XRES, X2, AUX± ..... -0.3V to V_{DD18} + 0.3V
All Other Pins (*Note b*) ..... -0.3V to V_{DDIO} + 0.3V
Continuous Power Dissipation (T_A = +70ºC) TQFN (Multilayer board, derate 40mW/ºC above +70ºC) 2200mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note a: Active state means the device is powered up and not in Sleep or Power-down mode. Inactive means the device is not powered up or is powered up but in Sleep or Power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56-Pin TQFN

Package Code	T5688+6
Outline Number	21-0135
Land Pattern Number	90-100041
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1°C/W

56-Pin TQFN-SW (Side-Wettable)

Package Code	T5688Y+6
Outline Number	21-100046
Land Pattern Number	90-100048
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 SERIALIZER FORWARD CHANNEL SERIAL OUTPUTS (SIO__) SEE Figure 1						
Output Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, (V_{OH} - V_{OL}) for all four outputs	300	400	500	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage	600	800	1000	mV_{P-P}
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$			25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state	V_{DD18} - 0.65	V_{DD18} - 0.45	V_{DD18} - 0.25	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$			25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / HDMI DIFFERENTIAL INPUTS (Rx[2:0]±, RxC±) SEE Figure 2						
Differential Input Voltage Swing	V_{IDIFF}	Differential, peak-to-peak measurement (*Note 2*)	150		1200	mV
Input Common-Mode Voltage	V_{ICM1}	TMDS clock ≤ 165MHz, DC coupled (*Note 2*)	V_{DD33} - 300		V_{DD33} - 37.5	mV
		165MHz < TMDS clock ≤ 340MHz, DC coupled (*Note 2*)	V_{DD33} - 400		V_{DD33} - 37.5	
		3.4Gbps < R_{BIT} ≤ 6Gbps, DC coupled (*Note 2*)	V_{DD33} - 700		V_{DD33} - 37.5	
	V_{ICMS2}	AC coupled	V_{DD33} − 10		V_{DD33} + 10	
Termination Resistance	R_T	Any pin to V_{DD33}	45	50	55	Ω
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-Up/Pull-Down Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level, Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-Up Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pull-Down Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE FAULT DETECTION INPUTS (LMN0A, LMN1A, LMN0B, LMN1B)						
Open Pin Voltage	V_{O0}	LMN0A or LMN0B		1.25		V
	V_{O1}	LMN1A or LMN1B		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)						
X1 Input Capacitance	C_{IN_X1}			5.5		pF
X2 Input Capacitance	C_{IN_X2}			4		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_m			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V
Low-Level Input Voltage	V_{IL}				0.4	V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				5.5		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY							
Supply Current (*Note 3*)	I_{DD}	Dual 6Gbps links, 198MHz PCLK on each link, color bar pattern	V_{DD33}, HDMI V_{CM} apprx. -180mV (*Note 4*)		30	35	mA
			V_{DD18}		155	180	
			V_{DDD}		280	630	
			V_{DDA}		0.1	2	
		Single 6Gbps link, 198MHz PCLK, color bar pattern	V_{DD33}, HDMI V_{CM} apprx. -180mV (*Note 4*)		30	35	
			V_{DD18}		90	105	
			V_{DDD}		240	600	
			V_{DDA}		0.1	2	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per GPIO toggling at 50 MHz, C_L = 10pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DD33} at 3.47V	T_A = +25ºC		2.7		µA
			T_A = +105ºC		4		
		V_{DDIO} at 3.6V	T_A = +25ºC		4.1		
			T_A = +105ºC		5		
		V_{DD18} at 1.9V	T_A = +25ºC		1.1		
			T_A = +105ºC		17		
		V_{DDD} at 1.05V	T_A = +25ºC		8		
			T_A = +105ºC		47		
		V_{DDA} at 1.05V	T_A = +25ºC		2.6		
			T_A = +105ºC		16		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current	I_{DD}	V_{DD33} at 3.47V	T_A = +25ºC		3.2		µA
			T_A = +105ºC		4		
		V_{DDIO} at 3.6V	T_A = +25ºC		4		
			T_A = +105ºC		6		
		V_{DD18} at 1.9V	T_A = +25ºC		18		
			T_A = +105ºC		30		
		V_{DDD} at 1.05V	T_A = +25ºC		12		
			T_A = +105ºC		50		
		V_{DDA} at 1.05V	T_A = +25ºC		2.4		
			T_A = +105ºC		17		

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS							
Serial Output Rise Time	t_R	20% to 80%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Serial Output Fall Time	t_F	80% to 20%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Total Serial Output Jitter	t_{TSOJ2}	PRBS7, single-ended or differential output			0.15		UI (p-p)
Deterministic Serial Output Jitter	t_{DSOJ2}	PRBS7, single-ended or differential output			0.10		UI (p-p)
Lock Time	t_{LOCK}	(*Note 5*, *Note 9*)			45		ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from when video is applied to input to when the first video packet appears at GMSL2 outputs, assuming the link is already established.			1.1 + 17,000 x t_{PCLK}		ms
Maximum Video Latency	t_{SL}	Time from TMDS input to SIO± output in GMSL2 packet	Single-link mode		120 x t_{PCLK}		s
			Dual-view splitter mode		4120 x t_{PCLK}		
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held low to reset the chip.			1		ms
AC ELECTRICAL CHARACTERISTICS / HDMI DIFFERENTIAL INPUT (Rx[2:0]±, RxC±) (*Note 2*) (*Note 6*)							
Minimum Differential Sensitivity				150			mV_{P-P}
Video Pixel Clock Frequency	f_{PCLK}	Single-Link mode				215	MHz
		Dual-Link mode				430	
TMDS Clock-Jitter Tolerance	t_{JTMDS}	Relative to ideal recovery clock		0.3			T_{BIT}
Intra-Pair Skew	t_{INTRA_SKEW}	HDMI 1.4, TMDS clock ≤ 222.75MHz		0.4			T_{BIT}
		HDMI 1.4, TMDS clock > 222.75MHz		0.15 x T_{BIT} + 112			ps
		HDMI 2.0, 3.4Gbps < R_{BIT} ≤ 6.0Gbps		0.15 x T_{BIT} + 112			
Inter-Pair Skew	t_{INTER_SKEW}			0.2 x $T_{CHARACTER}$ + 1.78			ns
AC ELECTRICAL CHARACTERISTICS / I²C/UART PORT TIMING							
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pull-up to V_{DDIO} (*Note 2*)		20 x V_{DDIO}/5.5V		150	ns

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C/UART Wake Time		From power-up or rising edge of PWDNB to local register access; for remote register access, I^2C/UART wake time is the same as Lock Time (t_{LOCK}).		1.1	4	ms
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I^2C MST_BT = 010, I^2C SLV_SH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I^2C MST_BT = 101, I^2C SLV_SH = 01)	100		400	
		High f_{SCL} range: (I^2C MST_BT = 111, I^2C SLV_SH = 00)	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B				100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MAIN (*Note 7*) (SEE Figure 6)						
Operating Frequency	f_{MCK}		0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(*Note 2*)	$t_{MCK}/2$ - 3	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge (*Note 2*)	-2.3		+2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sample edge (*Note 2*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sample edge (*Note 2*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SUBORDINATE (*Note 7*) (SEE Figure 7)						
Operating Frequency	f_{SCK}				25	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MISO Data Output Delay	t_{SOD}	After SCLK falling edge (*Note 2*)	-1.5		11.3	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge	3			ns
AC ELECTRICAL CHARACTERISTICS / I^2S/TDM MAIN TIMING (*Note 2*) (*Note 8*)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times$ (2 or 8)	0.512		49.152	MHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns
SD, WS Valid Time Before SCK	t_{SET}	$t_{SCK} = 1/f_{SCK}$	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{HOLD}	$t_{SCK} = 1/f_{SCK}$	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
AC ELECTRICAL CHARACTERISTICS / I^2S/TDM SUBORDINATE TIMING (*Note 2*) (*Note 8*)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, V_{DD33} = 3.14V to 3.47V, T_A = −40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, V_{DD33} = 3.3V, T_A = +25°C, unless otherwise noted.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$	0.512		49.152	MHz
SD, WS Setup Time	t_{SET}		4			ns
SD, WS Hold Time	t_{HOLD}		4			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2) (*Note 2*)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1, X2 UNCONNECTED) (*Note 2*)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		Forward data rate = 6Gbps, sinusoidal jitter < 1MHz (rising edge)			600	ps p-p
Input Duty Cycle	T_{DUTY}		40		60	%
Input Fall Time	T_F	80% to 20%			4	ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK OUTPUT (RCLKOUT)						
Frequency	f_{REF}	Crystal or reference clock input		25		MHz
Rise Time	t_R	20% to 80%, C_L = 10pF, 25MHz divided by 1, 2, or 4 (*Note 2*)			2	ns
Fall Time	t_F	80% to 20%, CL = 10pF, 25MHz divided by 1, 2, or 4 (*Note 2*)			2	ns
Jitter Generation	t_J			200		ps

Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: Color bar pattern.

Note 4: HDMI input common mode voltage is relative to V_{DD33}. Due to the 50Ω input termination resistors, V_{DD33} current is highly dependent on the HDMI common mode voltage. See the *HDMI Receiver* section.

Note 5: From power-up, release of RESET_LINK, or rising edge of PWDNB pin to rising edge of the LOCK pin. t_{RD} must be <90ms. For more information, see the *Link Lock* section.

Note 6: For more details, refer to the HDMI Version 1.4 and 2.0 specifications. HDMI 1.4 testing was done at a PCLK of 297MHz.

Note 7: Measured at 25MHZ.

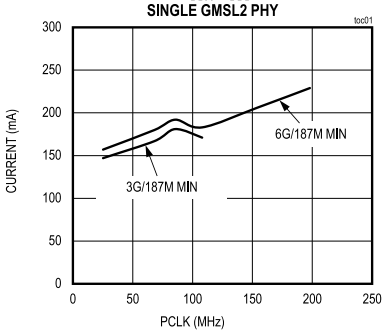
Note 8: Measured at 50MHZ.

Note 9: Production tested using ECS ECS-250-18-33Q-DS crystal.

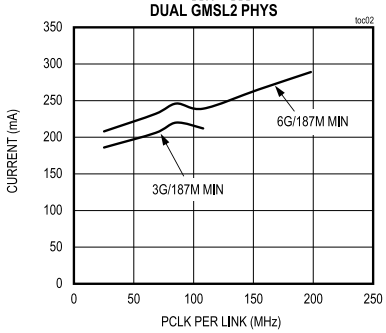
Typical Operating Characteristics

(T_A = +25°C, 6G/187M MIN = 6Gbps FWD, 187.5Mbps REV, one GPIO (100kHz). 3G/187M MIN = 3Gbps FWD, 187.5Mbps REV, one GPIO (100kHz), DUAL GMSL2 PHY = two GMSL2 PHYs; SINGLE GMSL2 PHY = one GMSL2 PHY.)

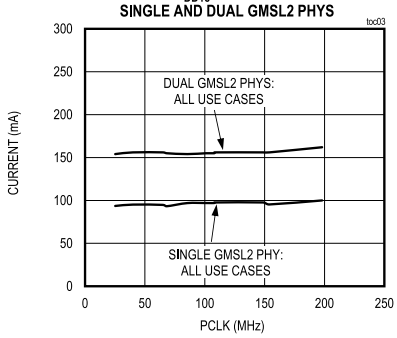
COMBINED V_{DDA}+V_{DDD} CURRENT
SINGLE GMSL2 PHY



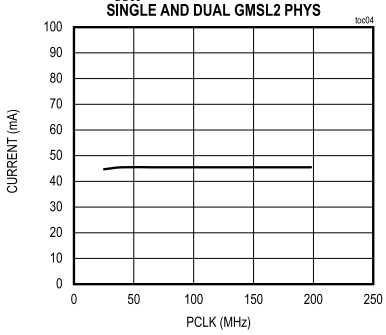
COMBINED V_{DDA}+V_{DDD} CURRENT
DUAL GMSL2 PHYS



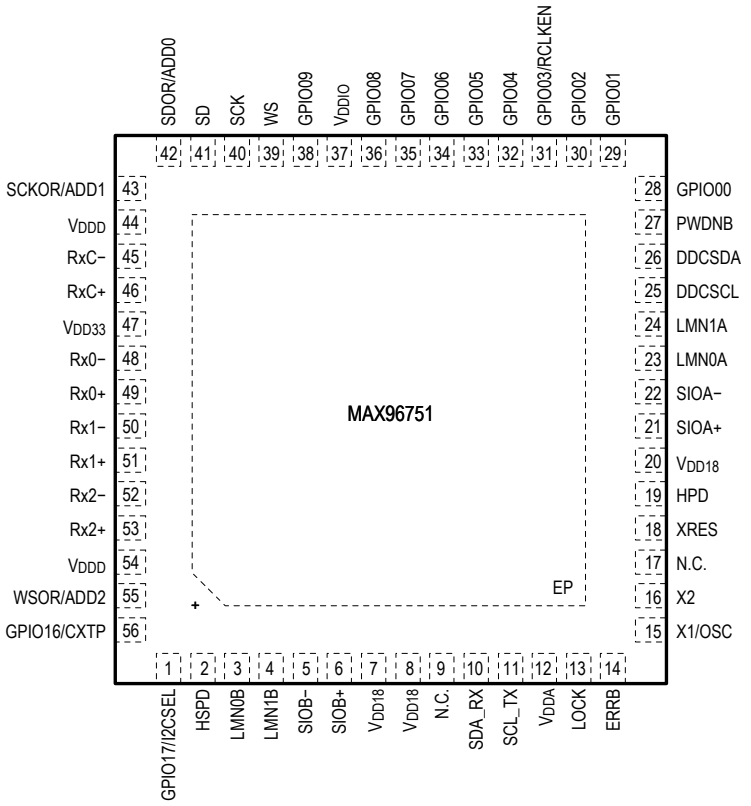
V_{DD18} CURRENT
SINGLE AND DUAL GMSL2 PHYS



V_{DD33} CURRENT ALL USE CASES
SINGLE AND DUAL GMSL2 PHYS



Pin Configuration



Pin Description

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL NAME	
GMSL2 SERIAL LINK			
21	SIOA+	SIOA+	Noninverting Coax/Twisted-Pair Serial-Data Output 1
22	SIOA-	SIOA-	Inverting Twisted-Pair Serial-Data Output 1
6	SIOB+	SIOB+	Noninverting Coax/Twisted-Pair Serial-Data Output 2
5	SIOB-	SIOB-	Inverting Twisted-Pair Serial-Data Output 2
23	LMN0A	LMN0A	Line-Fault Monitor Input
24	LMN1A	LMN1A	Line-Fault Monitor Input
3	LMN0B	LMN0B	Line-Fault Monitor Input
4	LMN1B	LMN1B	Line-Fault Monitor Input
HDMI INTERFACE			
2	HSPD	HSPD	HDMI Source Power-Detect Input with an Internal 1MΩ Pull-Down to Ground. Connect a voltage-divider to divide the 5V HDMI voltage down to V_{DDIO}.
19	HPD	HPD	HDMI Hot-Plug Detect Output
25	DDCSCL	DDCSCL	DDC I^2C Serial-Clock Open-Drain Input/Output with Internal 40kΩ Pull-Up to V_{DDIO}. Used by the HDMI source to read the EDID.

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL NAME	
26	DDCSDA	DDCSDA	DDC I^2C Serial-Data Open-Drain Input/Output with Internal 40kΩ Pull-Up to V_{DDIO}. Used by the HDMI source to read the EDID.
45	RxC-	RxC-	Inverting HDMI Clock Input with Internal 50Ω Termination to V_{DD33}
46	RxC+	RxC+	Noninverting HDMI Clock Input with Internal 50Ω Termination to V_{DD33}
48	Rx0-	Rx0-	Inverting HDMI Data0 Input with Internal 50Ω Termination to V_{DD33}
49	Rx0+	Rx0+	Noninverting HDMI Data0 Input with Internal 50Ω Termination to V_{DD33}
50	Rx1-	Rx1-	Inverting HDMI Data1 Input with Internal 50Ω Termination to V_{DD33}
51	Rx1+	Rx1+	Noninverting HDMI Data1 Input with Internal 50Ω Termination to V_{DD33}
52	Rx2-	Rx2-	Inverting HDMI Data2 Input with Internal 50Ω Termination to V_{DD33}
53	Rx2+	Rx2+	Noninverting HDMI Data2 Input with Internal 50Ω Termination to V_{DD33}
CONTROL AND GPIO (*DENOTES DEFAULT AFTER POWER-UP)			
28	GPIO00	GPIO00* SDA1_RX1	GPIO00: Configurable General-Purpose Input or Output. Configured as an open-drain output with an internal 40kΩ pull-up to V_{DDIO} at power-up. By default, this outputs the GPO0 value received from the deserializer. SDA1_RX1: Pass-Through I^2C1 Serial-Data Input/Output or UART1 Receive. Internal 40kΩ pull-up to V_{DDIO}. SDA1: I^2C Serial Data Input/Open-Drain Output. RX1: UART Input.
29	GPIO01	GPIO01* SCL1_TX1	GPIO01: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground at Power-Up. By default, this is a GPI1 input transmitted to the deserializer to be output from GPO1. SCL1_TX1: Pass-Through I^2C1 Serial-Clock Input/Output or UART1 Transmit. Internal 40kΩ pull-up to V_{DDIO}. SCL1: I^2C Clock Input/ Open-Drain Output. TX1: UART Open-Drain Output.
30	GPIO02	GPIO02* MS SDA2_RX2	GPIO02: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground. MS: UART Mode Select with an Internal 1MΩ Pull-Down to Ground. Set MS low to select Base mode. Set MS high to select Bypass mode. The MS state can also be temporarily overwritten by a register write. SDA2_RX2: Pass-Through I^2C2 Serial-Data Input/Output or UART2 Receive. Internal 40kΩ pull-up to V_{DDIO}. SDA2: I^2C Serial Data Input/Open-Drain Output. RX2: UART Input.
31	GPIO03/RCLKEN	RCLKEN GPO03* RCLKOUT	RCLKEN: Reference Clock Enable with an Internal 1MΩ Pull-Down to Ground. The state of RCLKEN latches at power-up. If RCLKEN is high, drives external reference clock (RCLKOUT). If RCLKEN is low, it is a configurable general-purpose input or output. GPO03: Configurable General-Purpose Output RCLKOUT: 25MHz Reference Clock Push-Pull Output.

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL NAME	
32	GPIO04	GPIO04* SCL2_TX2	GPIO04: General-Purpose Input/Output. Configured as open drain with an internal 40kΩ pull-up to V_{DDIO} at power-up. SCL2_TX2: Pass-Through I^2C2 Serial-Clock Input/Output or UART2 Transmit. Internal 40kΩ pull-up to V_{DDIO}. SCL2: I^2C Clock Input/ Open-Drain Output. TX2: UART Open-Drain Output.
33	GPIO05	GPIO05* BNE SS1	GPIO05: General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground BNE: Buffer Not Empty. When configured as a subordinate, push-pull output. When BNE is high, indicates SPI data is available. SS1: SPI Subordinate Select 1. When configured as a main, subordinate select 1 is a push-pull output.
34	GPIO06	GPIO06* RO SS2	GPIO06: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground RO: When configured as a subordinate, the SPI mode-select input with internal 1MΩ pull-down to ground. When RO is high, enables main read from MISO. When RO is low, enables main write to MOSI. SS2: SPI Subordinate Select 2. When configured as a main, subordinate select 2 is a push-pull output.
35	GPIO07	GPIO07* MISO	GPIO07: Configurable General-Purpose Input or Output with Internal 1MΩ Pull-Down to Ground MISO: SPI Main In Subordinate Out. When configured as the main, a push-pull output drives data to an external subordinate. When configured as a subordinate, the input with an internal 1MΩ pull-down to ground receives data from the external main.
36	GPIO08	GPIO08* MOSI	GPIO08: Configurable General-Purpose Input or Output with Internal 1MΩ Pull-Down to Ground MOSI: SPI Main Out Subordinate In. When configured as the main, a push-pull output drives data to an external subordinate. When configured as a subordinate, an input with an internal 1MΩ pull-down to ground receives data from the external main.
38	GPIO09	GPIO09* SCLK	GPIO09: Configurable General-Purpose Input or Output with Internal 1MΩ Pull-Down to Ground. SCLK: SPI Clock: When configured as a main, it is a push-pull clock output. When configured as a subordinate, it is a clock input with an internal 1MΩ pull-down to ground.
39	WS	WS* GPIO10	WS: I^2S/TDM Word-Select Input with Internal 1MΩ Pull-Down to Ground. Supports forward audio from serializer to deserializer. GPIO10: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground.
40	SCK	SCK* GPIO11	SCK: I^2S/TDM Serial Clock Input with Internal 1MΩ Pull-Down to Ground. Supports forward audio from serializer to deserializer. GPIO11: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground.

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL NAME	
41	SD	SD* GPIO12	SD: I²S/TDM Serial-Data Input with an Internal 1MΩ Pull-Down to Ground. Supports forward audio from serializer to deserializer. GPIO12: Configurable General-Purpose Input or Output with an Internal 1MΩ Pull-Down to Ground
42	SDOR/ADD0	ADD0 SDOR* GPO13	ADD0: Address Selection Input with Internal 1MΩ Pull-Down to Ground. Latched on power-up. SDOR: I²S/TDM Serial Data Push-Pull Output. Supports reverse-channel audio from deserializer to serializer. GPO13: Configurable General-Purpose Output.
43	SCKOR/ADD1	ADD1 SCKOR* GPO14	ADD1: Address Selection Input with Internal 1MΩ Pull-Down to Ground. Latched on power-up. SCKOR: I²S/TDM Clock Push-Pull Output. Supports reverse-channel audio from deserializer to serializer. GPO14: Configurable General-Purpose Output.
55	WSOR/ADD2	ADD2 WSOR* GPO15	ADD2: Address Selection Input with Internal 1MΩ Pull-Down to Ground. Latched on power-up. WSOR: I²S/TDM Word Select Push-Pull Output. Supports reverse-channel audio from deserializer to serializer. GPO15: Configurable General Purpose Output.
56	GPIO16/CXTP	CXTP GPO16* HS	CXTP: Coax/Twisted-Pair Select Input with an Internal 1MΩ Pull-Down to Ground. State is latched on power-up. Set CXTP high for coax cable drive. Set CXTP low for twisted-pair cable. GPO16: Configurable General-Purpose Output. HS: Horizontal Sync Push-Pull Output.
1	GPIO17/I2CSEL	I2CSEL GPO17* VS	I2CSEL: Control-Channel Interface Select for Primary I²C/UART with an Internal 1MΩ Pull-Down to Ground. Set I2CSEL high to select the I²C interface. Set I2CSEL is low to select the UART interface. GPO17: Configurable General-Purpose Output. VS: Vertical Sync Push-Pull Output.
10	SDA_RX	SDA_RX* GPIO18	SDA_RX: I²C Serial-Data Input/Output or UART Receive. Internal 40kΩ pull-up to V_{DDIO}. SDA: I²C serial data input/open-drain output. RX: UART input. GPIO18: Configurable General-Purpose Input or Open-Drain Output. Function available only if the MAX96751 is being programmed over the GMSL2 link and not locally. Internal 40kΩ pull-up to V_{DDIO}.

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
11	SCL_TX	SCL_TX*	SCL_TX: I^2C Serial-Clock Input/Output or UART Transmit. Internal 40kΩ pull-up to V_{DDIO}. SCL: I^2C clock input/open-drain output. TX: UART open-drain output. GPIO19: Configurable General-Purpose Input or Open-Drain Output. This function is available only if the MAX96751 is programmed over the GMSL2 link and not locally. Internal 40kΩ pull-up to V_{DDIO}.
13	LOCK	LOCK	Open-Drain Lock Indication Output with an Internal 40kΩ Pull-Up to V_{DDIO}
14	ERRB	ERRB	Open-Drain Error Indication Output with an Internal 40kΩ Pull-Up to V_{DDIO}. Low ERRB indicates a data error or interrupt is detected. ERRB is high when PWDNB is low.
27	PWDNB	PWDNB	Active-Low, Power-Down Input with Internal 1MΩ Pull-Down to Ground. Set PWDNB low to enter power-down mode.
MISCELLANEOUS - SEE Table 3			
15	X1/OSC	X1/OSC	Crystal/Oscillator Input. Connect to either a 25MHz crystal or a 25MHz external clock source.
16	X2	X2	Crystal Input. Connect to one terminal of a 25MHz crystal and connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used).
18	XRES	XRES	Used to calibrate SIO output driver swings. Connect an external 402Ω resistor between XRES and ground.
9, 17	RSVD	RSVD	Reserved. Make no electrical connection to these pins.
POWER SUPPLIES - SEE Table 3			
44, 54	V_{DDD}	V_{DDD}	Core Supply. Connect a 1.0V ±5% external power supply.
12	V_{DDA}	V_{DDA}	1.0V Analog Supply. Connect a 1.0V ±5% external power supply.
37	V_{DDIO}	V_{DDIO}	1.8V to 3.3V I/O Power Supply
7, 8, 20	V_{DD18}	V_{DD18}	1.8V I/O Supply
47	V_{DD33}	V_{DD33}	3.3V HDMI Supply
—	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Recommended Operating Conditions, External Components and ESD Protection

Table 2. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DDD}, V_{DDA}		0.95	1.0	1.05	V
	V_{DDIO}	1.8V	1.7	1.8	1.9	V
		3.3V	3.0	3.3	3.6	V
	V_{DD33}		3.14	3.3	3.47	V
Maximum Supply Noise	V_{DD18}			25		mV_{P-P}
	V_{DDD}, V_{DDA}			25		mV_{P-P}
	V_{DDIO}	1.8V		50		mV_{P-P}
		3.3V		100		mV_{P-P}
	V_{DD33}			100		mV_{P-P}
Operating Junction Temperature, T_J			-40		+125	°C

Note: Supply noise < 1MHz.

See Figure 22 and Figure 23.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R_{XRES}		402 ±1%, use a single resistor	Ω
Line Fault Pull-Down Resistor	R_{PD}		49.9 ±1%	kΩ
Line Fault Series Resistor	R_{EXT}	LMN0A, LMN0B – STP mode	42.2 ±1%	kΩ
		LMN0A, LMN0B – Coax mode	48.7 ±1%	kΩ
		LMN1A, LMN1B – STP/Coax mode	48.7 ±1%	kΩ
Link Isolation Capacitors	C_{LINK}	Place close to the SIO pins (21, 22, 6, 5) used in the application.	0.1	µF
Termination Resistors for Unused GMSL2 Outputs in Coax Mode	R_{TERM}	Place close to the Link Isolation Capacitor(s) for the unused SIO output(s) in Coax mode. See Figure 22.	49.9 ±1%	Ω
Crystal		Place as close as possible to pins 15 and 16.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 15 (X1/OSC) and 16 (X2).		
V_{DDIO} Decoupling Capacitors (Note 10)		Place a 0.01µF capacitor as close as possible to pin 37. Include a minimum of 10µF bulk decoupling on the PCB.	0.01 + 10	µF

Table 3. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
V_{DD18} Decoupling Capacitors (Note 10)		Place a 0.01µF capacitor as close as possible to pin 20. Place another 0.01µF capacitor as close as possible to pins 7 and 8. Run separate traces from each pin to the capacitor. Include a minimum of 10µF bulk decoupling on the PCB.	(2x) 0.01 + 10	µF
V_{DD33} Decoupling Capacitors (Note 10)		Place a 0.01µF capacitor as close as possible to pin 47. Include a minimum of 10µF bulk decoupling on the PCB.	0.01 + 10	µF
V_{DDD} and V_{DDA} Decoupling Capacitors		Place 0.01µF capacitors as close as possible to pins 12, 44, and 54. Include a minimum of 10µF bulk decoupling on the PCB that can be shared if the same supply is used for V_{DDD} and V_{DDA}. (Note 11)	(3x) 0.01 + 10	µF
Open-Drain Pull-Up Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.		
HSPD Resistor Divider		Connect a resistor divider between the HDMI +5V supply and ground. Connect the midpoint to pin 2. Select the resistors such that the HSPD voltage is equal to V_{DDIO} x 0.9. See the *HSPD Input Circuit* section.		

Note 10: Power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Note 11: With a 10µF decoupling capacitor, a V_{DD} supply voltage sag may be observed when coming out of Power-down or Sleep mode. The device will function correctly internally. If the V_{DD} sag affects other devices on the board, use 47µF instead.

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, Coax Configuration		±8		
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Functional Diagrams

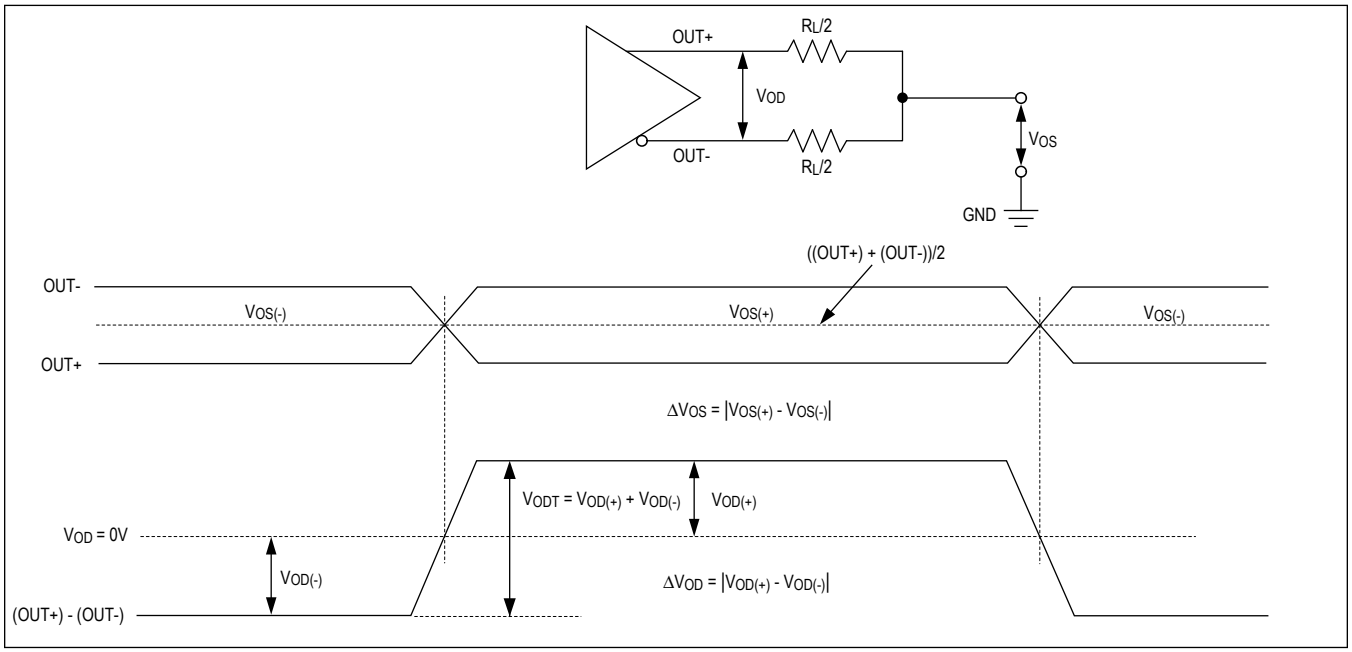


Figure 1. Serial Output Parameters

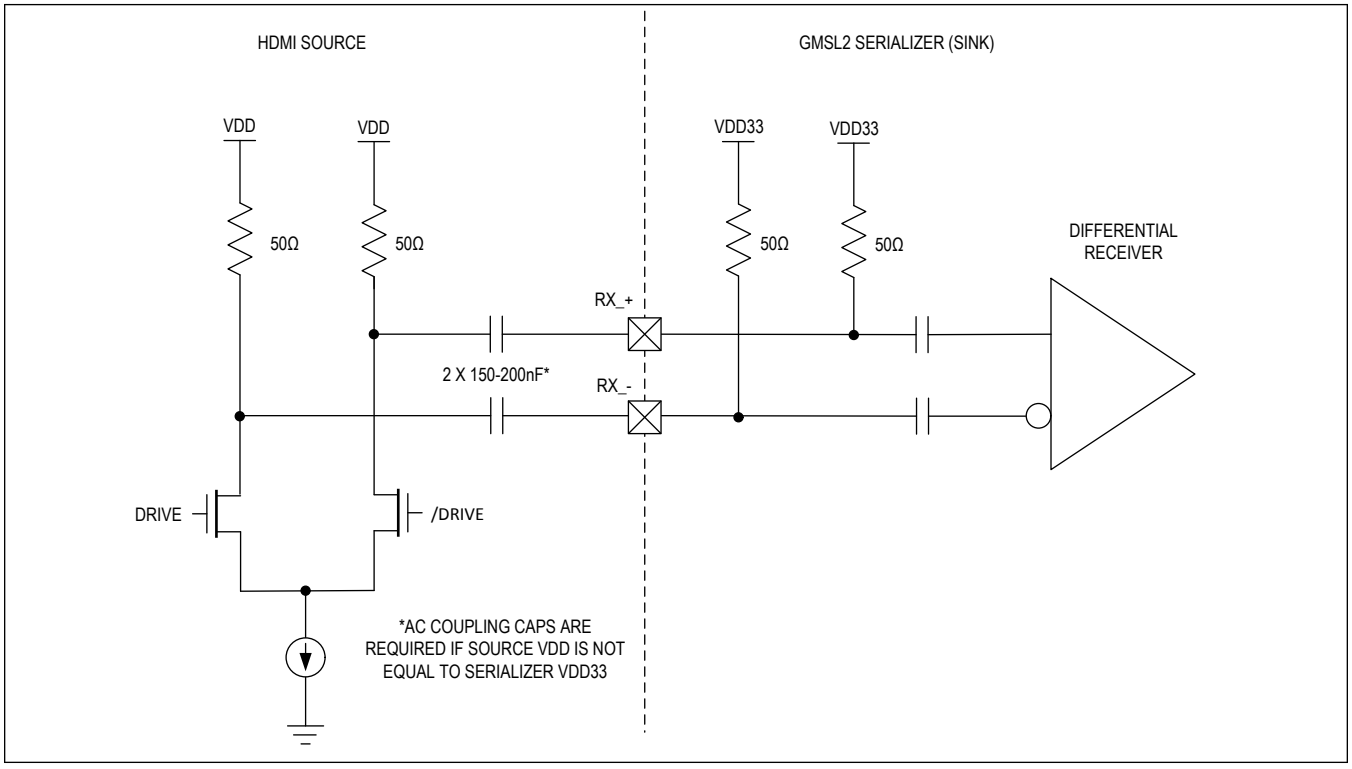


Figure 2. HDMI Differential Input

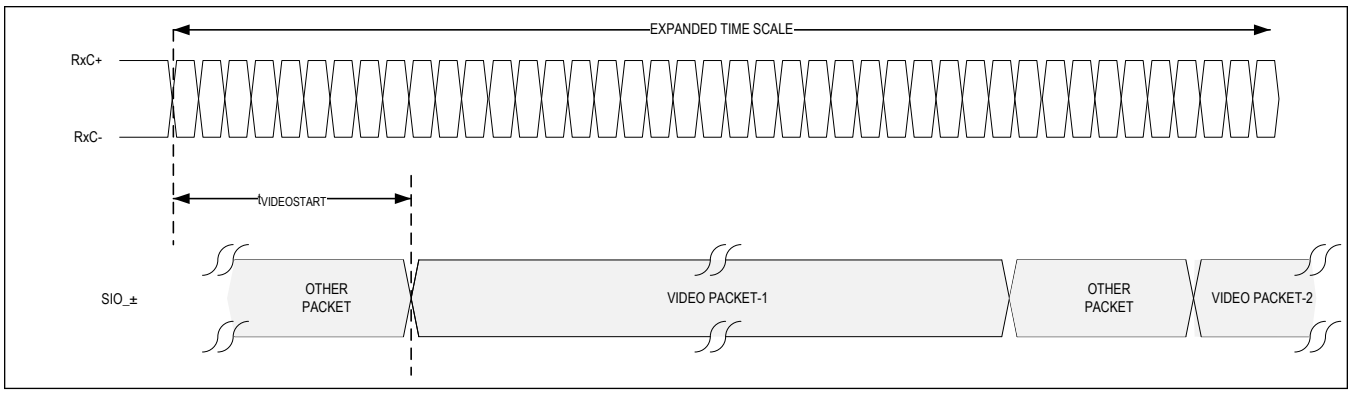


Figure 3. Video Initialization Time

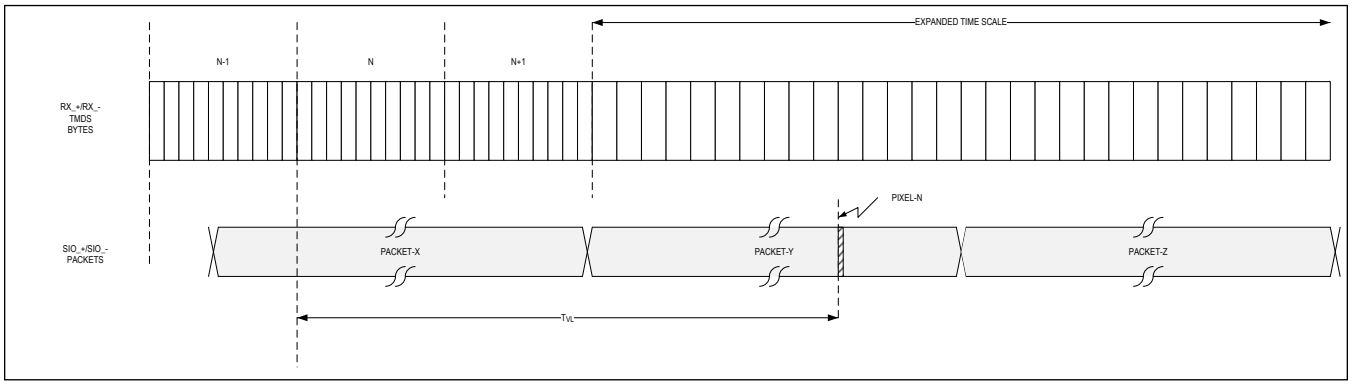


Figure 4. Video Latency

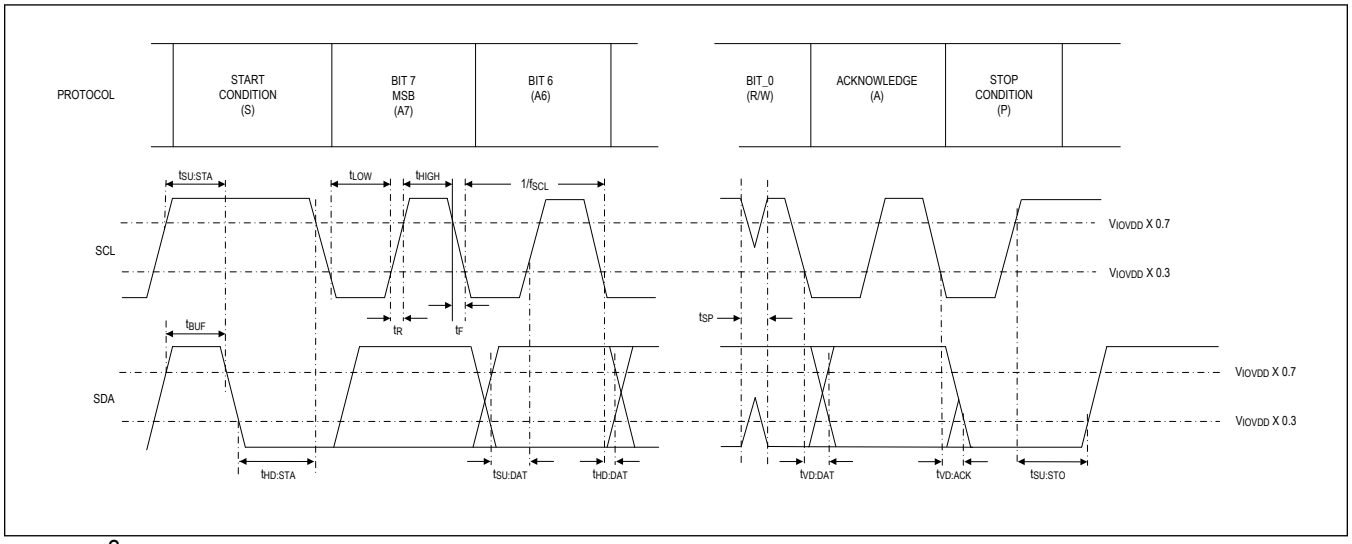


Figure 5. I^2C Timing Parameters

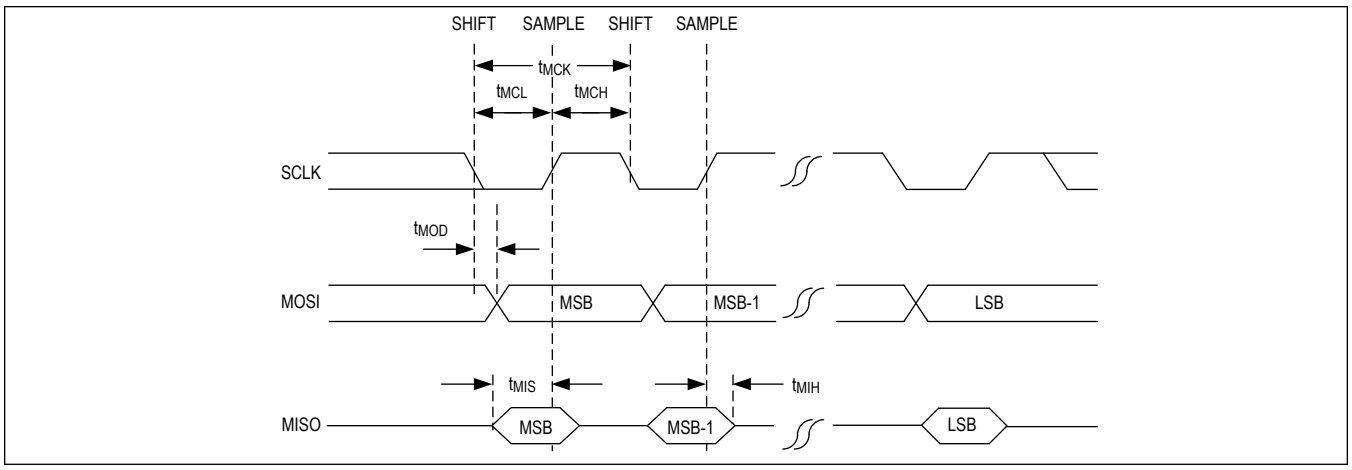


Figure 6. SPI Main Mode Timing Parameters

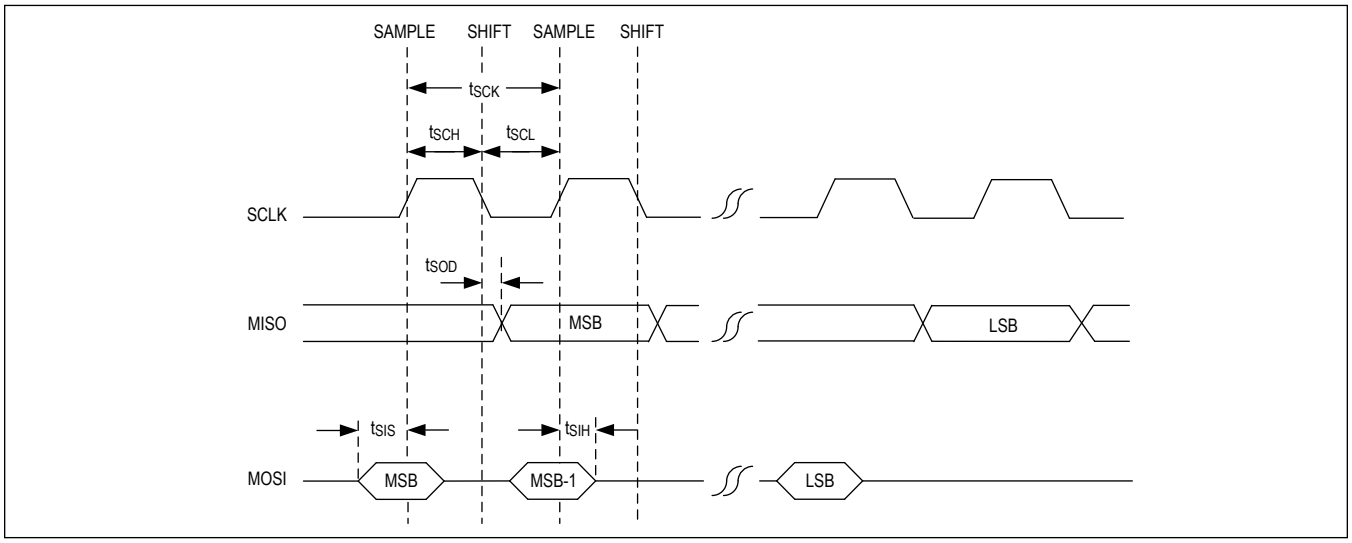


Figure 7. SPI Subordinate Mode Timing Parameters

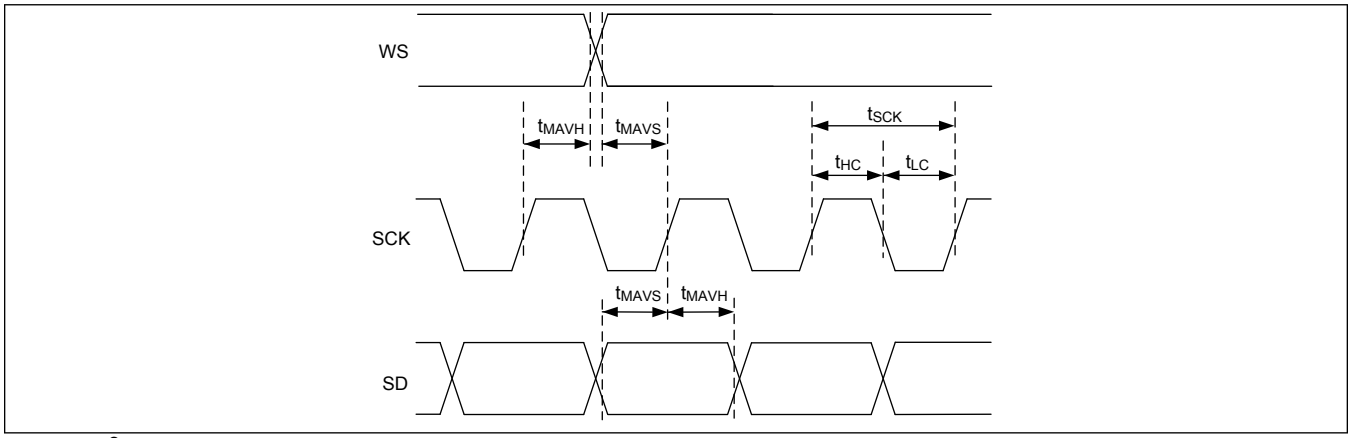


Figure 8. I^2S Main Timing Diagram

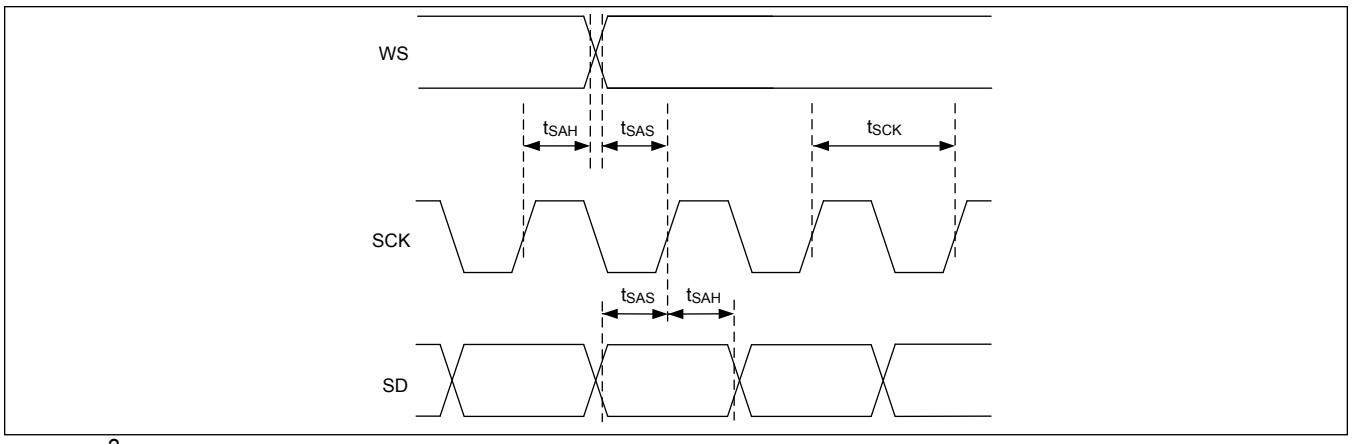


Figure 9. I^2S Subordinate Timing Diagram

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews, and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, a selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- The **MAX96751 User Guide** contains detailed programming guidelines for MAX96751 device features.
- **Errata sheets** contain deviations from published device specifications and are specific to part number and revision ID.

Contact the factory to receive these documents and for additional guidance on MAX96751 features.

New Designs Supporting Two Displays

Although the MAX96751 device supports using both GMSL2 links at the same time, Analog Devices does not recommend this device for new designs supporting two displays.

In modes using both GMSL2 links (Splitter or Replication modes), if one link loses lock (display turned off, damaged link, etc.) then both links will lose lock. The MAX96751 device repeatedly attempts to re-establish lock on both links. In the event that the cause of the loss of lock is permanent (i.e., broken link or similar), then neither link is able to re-establish lock without specific software intervention from the head unit.

If the disturbance to the other display is unacceptable, our recommendation is to not use these devices for designs supporting two displays. Contact the factory for recommended alternatives.

Note that in Dual-link mode, in which the two links drive a single deserializer, loss of one link causes the display to blank.

The MAX96751 device is robust in single-link applications and continues to be recommended for new designs.

Contact the factory for recommended software workarounds and further details relative to use cases supporting two displays.

Introduction

Analog Devices' GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total capacity of 12Gbps forward and 375Mbps reverse in specific configurations.

The following sections provide a brief overview of the device functions and features. Contact factory for additional information and details on configuration of each function and feature.

Product Overview

The MAX96751 converts an HDMI v1.4/v2.0 input to single or dual GMSL2 output. It supports up to 215MHz PCLK per link, enabling transmission of 2560x1080, 24-bit color, 60Hz video or equivalent on each GMSL2 link. The MAX96751 provides 187.5Mbps reverse-link bandwidth.

HDMI Video

The MAX96751 is set to high-speed (>340MHz) HDMI version 2.0 by default. Registers CDR_CTL1_REG, DPLL_CFG1, and DPLL_CFG6 must be configured to disable the default CDR mode for high-speed (>340MHz) HDMI 2.0 and to enable DPLL mode for low-speed (<340MHz) HDMI 1.4.

Video Input Formats

The MAX96751 HDMI input can accept RGB888 single-stream video as well as dual-view video in either side-by-side (full) or uniquely pixel-interleaved formats as detailed in Figure 10 through Figure 13.

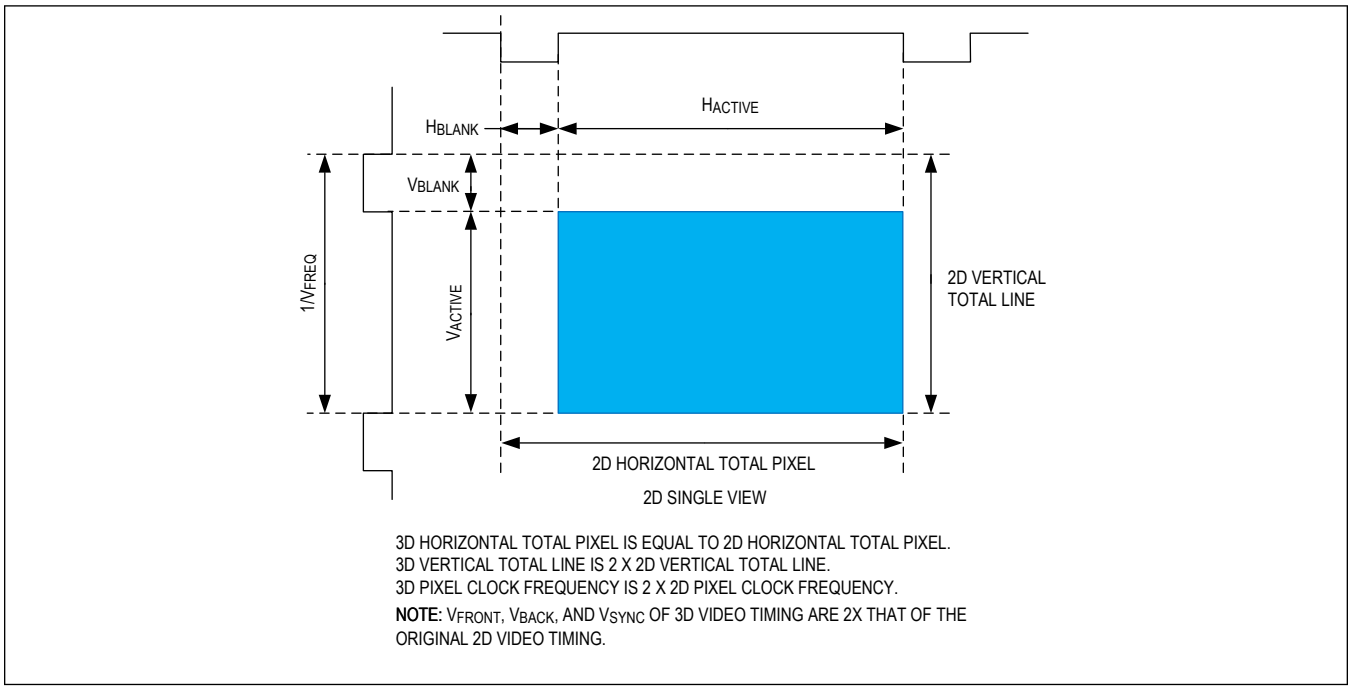


Figure 10. Single-Stream HDMI Interface Format

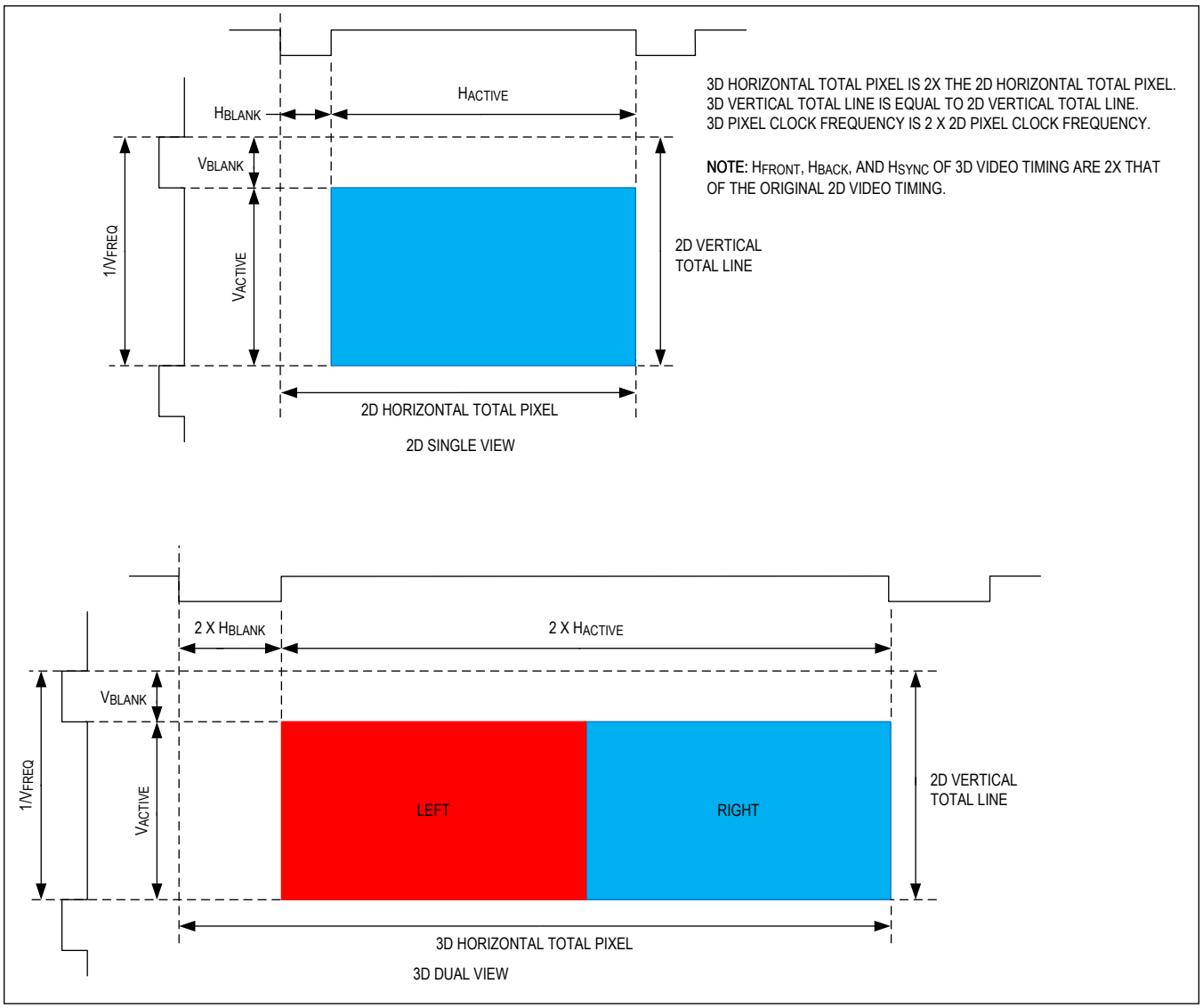


Figure 11. Dual-View Side-by-Side (Full) HDMI Interface Format

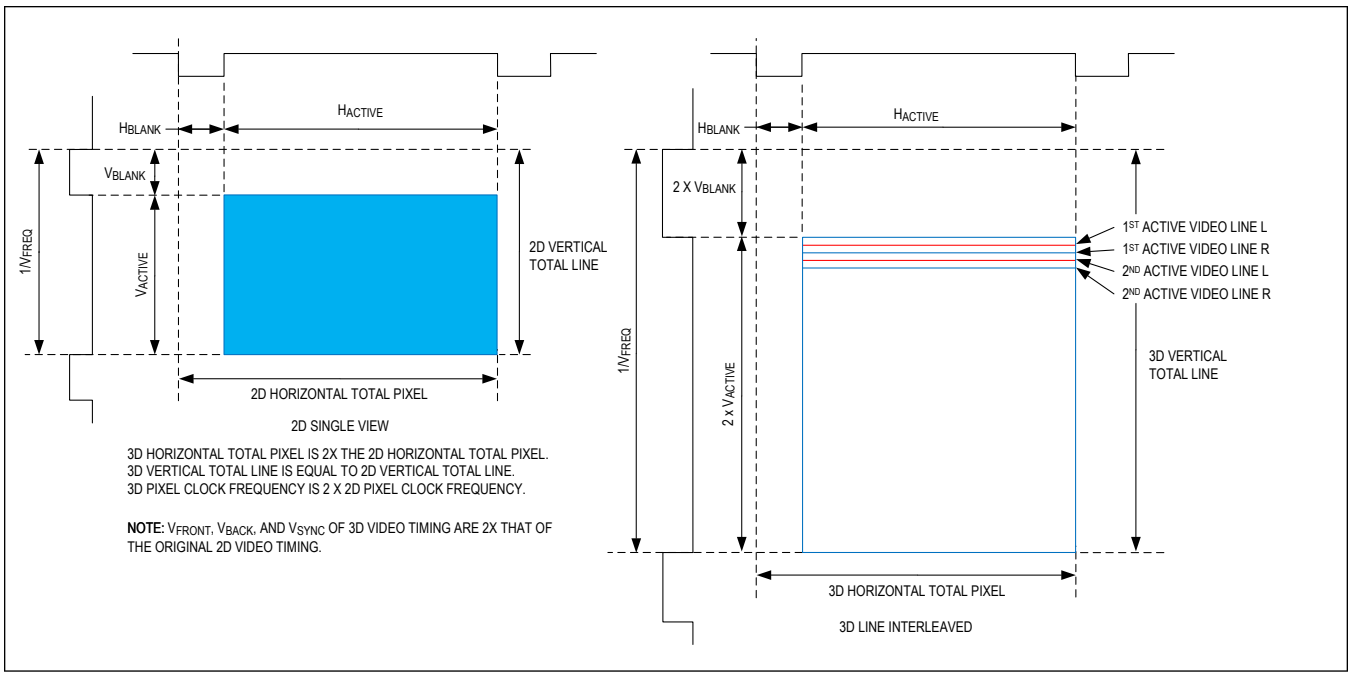


Figure 12. Dual-View Line Interleaved HDMI Interface Format

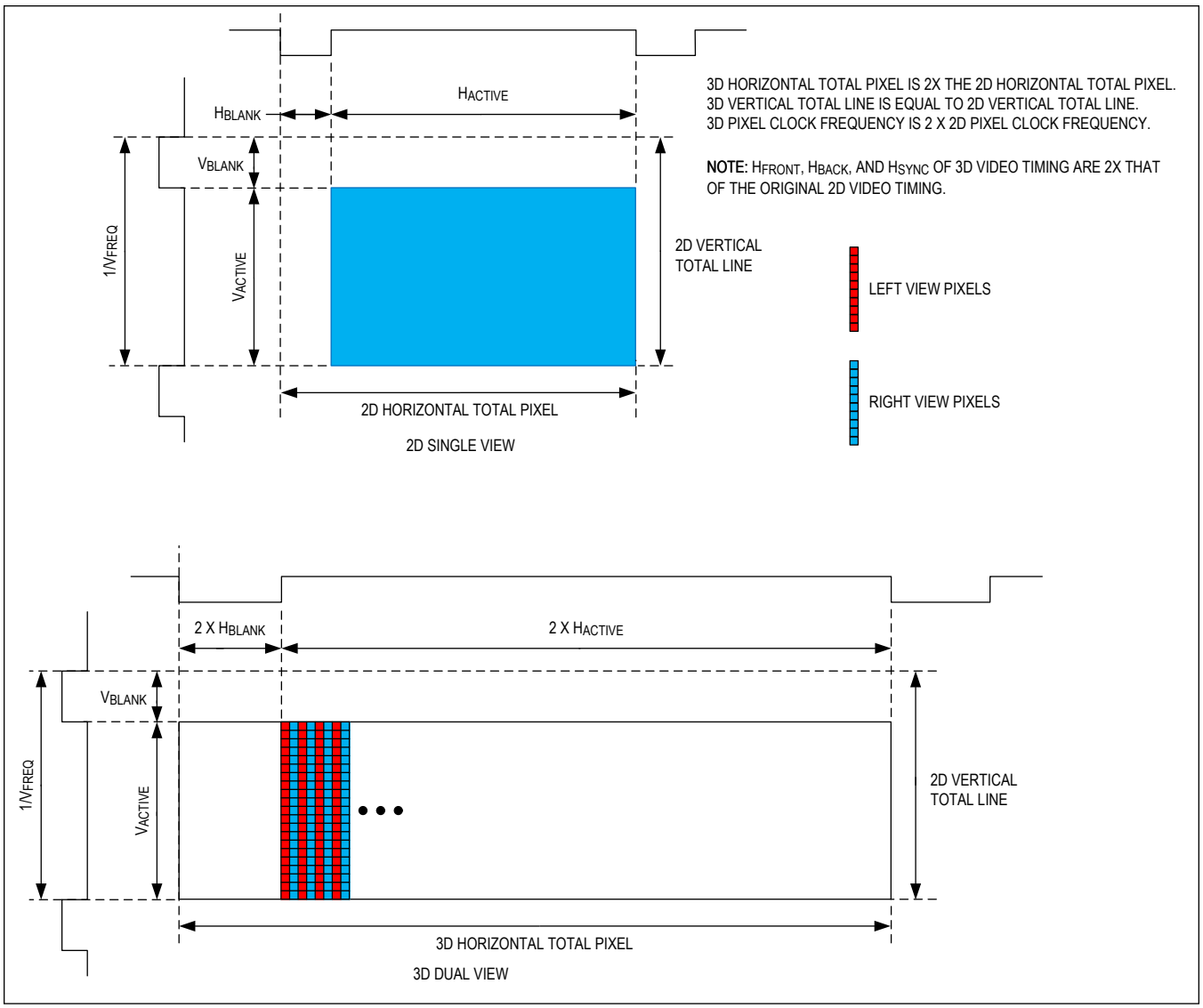


Figure 13. Dual-View Column (Pixel) Interleaved HDMI Interface Format

Serializer Modes

The MAX96751 has two video pipes, video replication, and dual-view splitter technology that enable a single serializer to support up to four displays as illustrated in Figure 14 through Figure 21. The user can configure each video pipeline to be routed to either GMSL2 SIO output or to both outputs for replication and dual-view splitter applications.

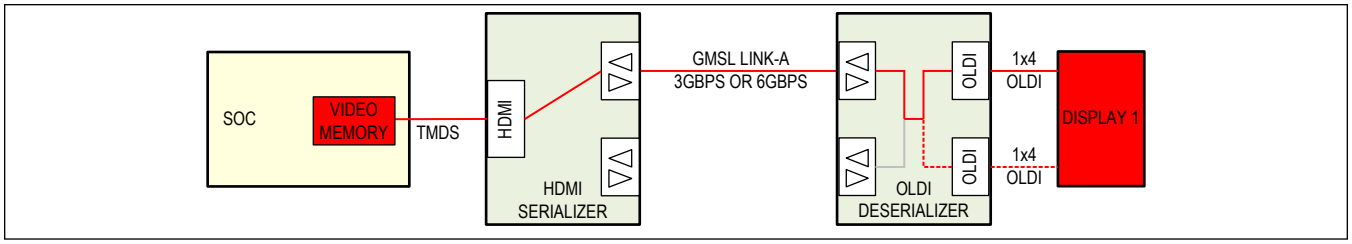


Figure 14. Single Video Stream, Single GMSL2 Link at Either 3Gbps or 6Gbps, OLDI Deserializer with Single or Dual OLDI Outputs

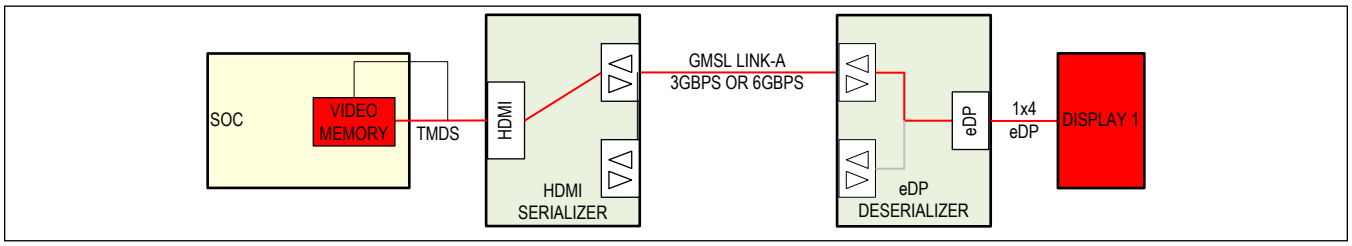


Figure 15. Single Video Stream, Single GMSL2 Link at Either 3Gbps or 6Gbps, eDP Deserializer (One, Two, or Four Lanes)

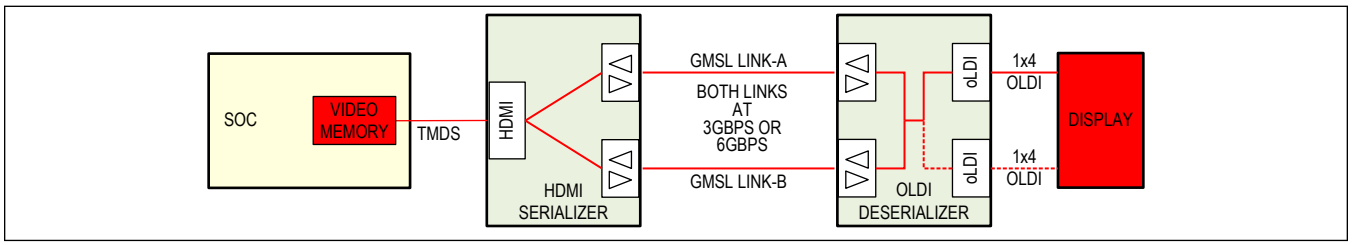


Figure 16. Single Video Stream, Dual GMSL2 Links with Both at Either 3Gbps or 6Gbps, OLDI Deserializer with Single or Dual OLDI Outputs

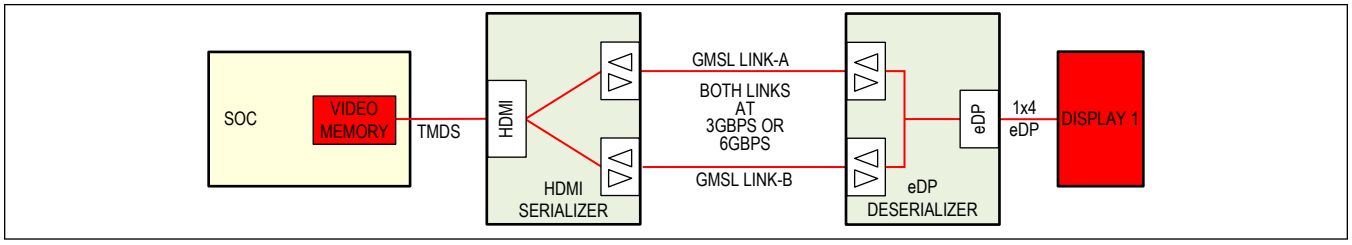


Figure 17. Single Video Stream, Dual GMSL2 Links with Both at Either 3Gbps or 6Gbps, eDP Deserializer (One, Two, or Four Lanes)

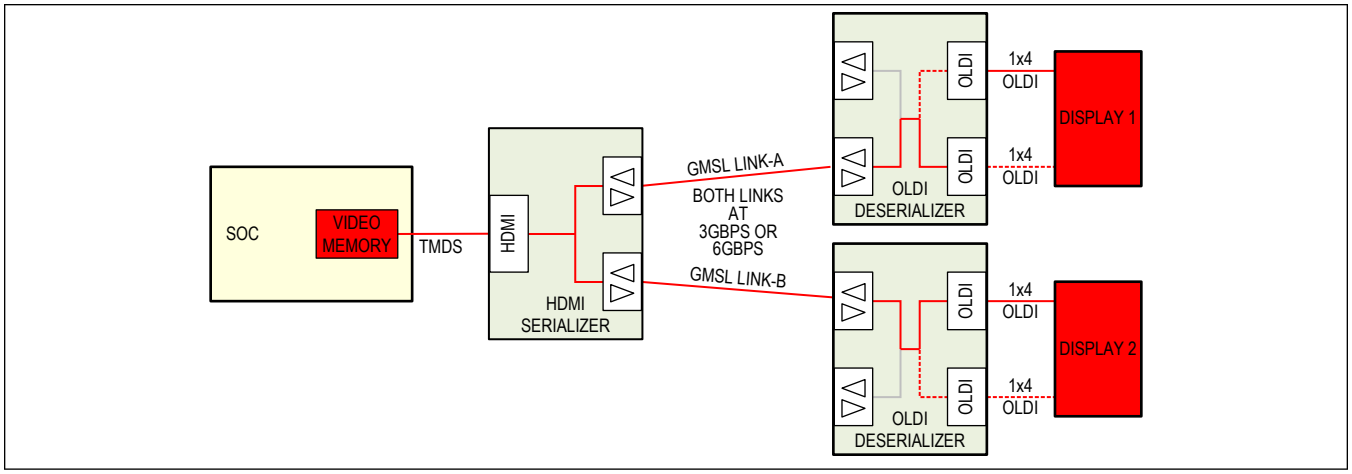


Figure 18. Serializer Single-Stream Replication, Dual GMSL2 Links, OLDI Deserializers with Single or Dual OLDI Outputs, Can Also Be Done with eDP Deserializers

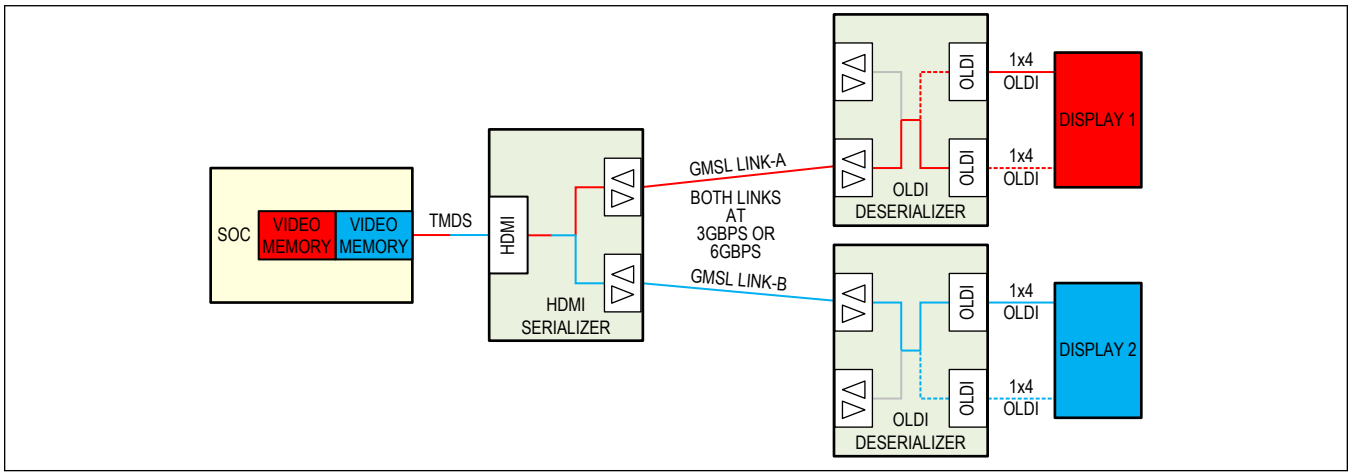


Figure 19. Serializer Dual-View Splitter Mode, Dual GMSL2 Links, Dual OLDI Deserializers with Single or Dual OLDI Outputs, Can Also Be Done with Dual eDP Deserializers, and Each Video Stream (View) Must Have Identical Timing

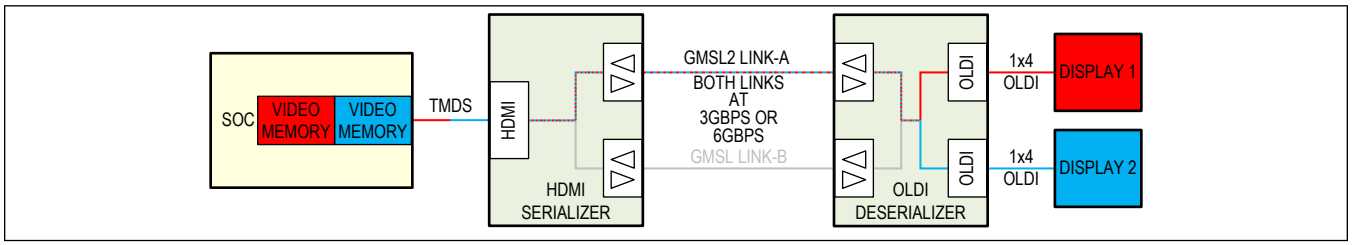


Figure 20. Serializer Dual-View Splitter Mode, Convert Dual-View to Pixel Interleave, Send Dual-Views Down Single GMSL2 Link, Dual OLDI Deserializer Splits Pixel Interleaved Dual View, Each Video Stream (View) Must Have Identical Timing, Can Also Be Done in Dual GMSL2 Link Mode

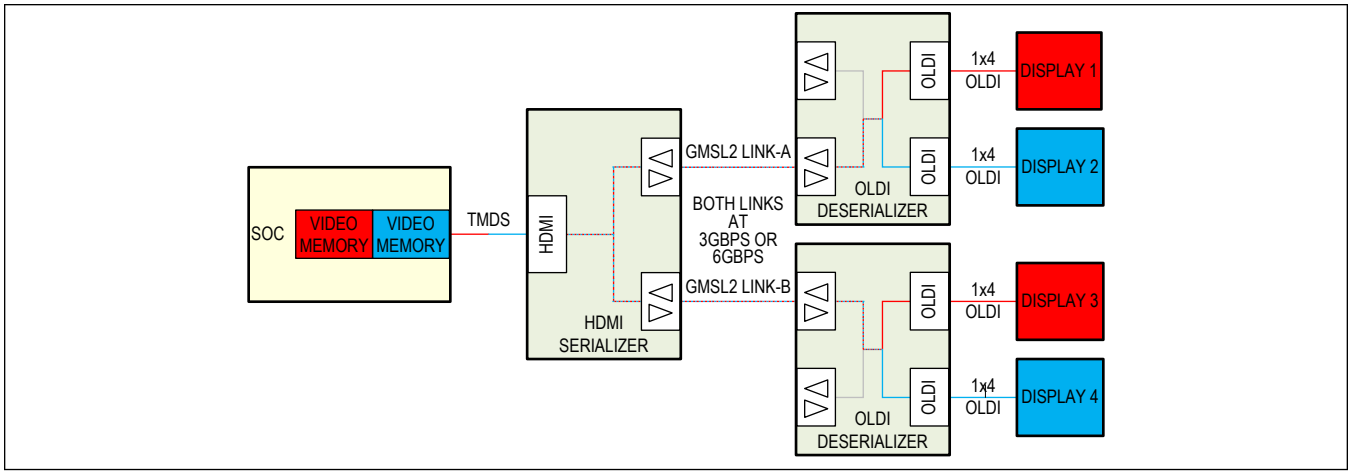


Figure 21. Serializer Dual-View Splitter Mode, Convert Dual View to Pixel Interleave, Replicate Pixel-Interleaved Streams, Send Dual Views Down Both GMSL2 Links, Dual OLDI Deserializer Splits Pixel-Interleaved Dual View, Each Video Stream (View) Must Have Identical Timing

Other Functions

The GMSL2 serializers and deserializers have a primary I^2C/universal asynchronous receiver-transmitter (UART) control channel interface that a microcontroller (µC) uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through I^2C/UART channels available for local or remote peripheral control. The pass-through I^2C/UART channels do not have access to serializer and deserializer registers.

The MAX96751 supports both forward (serializer to deserializer) and reverse (deserializer to serializer) audio channels. The forward channel supports audio from either the HDMI source or the local I^2S interface. The audio channels support I^2S stereo and up to 8 channels in time-division multiplexing (TDM) mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 bits to 32 bits.

Additionally, the MAX96751 includes a serial peripheral interface (SPI) main/subordinate interface, including two subordinate select pins, for peripheral control. The SPI enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices (a GMSL2 device can be configured as a SPI main or subordinate).

The MAX96751 provides up to 20 GPIOs, dependent on device feature utilization. GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction.

The device includes a video crossbar and watermark generation or detection. The crossbar can be used to reorder the color and sync signals. It can also be used for HDMI TMDS lane remapping and phase inversion if desired. The watermark generation and detection is used for verifying that the video image is not frozen.

The GMSL2 devices incorporate numerous link margin optimization and monitoring functions to ensure high link margin. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link margin diagnosis with various threshold alarm levels is available for run-time alerts of link degradation. Pseudorandom binary (bit) sequence (PRBS) checking verifies correct link and video channel operation.

GMSL2 Protocol

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or external reference frequency. The link clock does not have any relation to the video pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to

prevent a single channel from utilizing the link bandwidth for an extended time. In most available cases, link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels and for both video and control-channel data.

GMSL2 Physical Layer

Analog Devices' GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, enabling full-duplex operation on a single wire. A single cable between the serializer and deserializer transmits data from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data transmitted from the deserializer to the serializer.

Forward rate options are fixed at 3Gbps or 6Gbps, with defaults of 6Gbps in coax mode and 3Gbps in STP mode. The MAX96751 reverse-link rate is fixed at 187.5Mbps. Both forward and reverse rates are doubled in a dual-link configuration, in which a serializer and paired deserializer are connected using two links.

Cabling Options

GMSL2 supports operation with either 50Ω coaxial or 100Ω shielded-twisted pair (STP) cabling.

Cables must have sufficient return and insertion loss characteristics for best full-duplex link performance. The available link rates and GMSL2 dynamic link optimization enable support of a wide range of cabling options. Contact the factory for insertion and return loss guidelines.

Coax or STP operation is determined by the state of CXTP at power-up. Set CXTP high for coax cable drive (single-ended with default 6Gbps link rate). Set CXTP low for STP mode (differential with default 3Gbps link rate). See the *Latch-On-Power-Up Pins* section.

In Coax mode, use only the noninverted SIO pin. In STP configurations, both the noninverted and inverted SIO pins are enabled by default. Any unused SIO pins should be AC terminated with 50Ω to ground.

The GMSL2 channel specification must be adhered to. It provides guidance on maximum lengths for the coax and STP cable types commonly used in the automotive industry. The guidelines assume two inline connectors in addition to the end-point connectors, and 25mm of PCB trace at each end. In general, any physical channel implementation that is compliant with the GMSL2 channel specification can be used with reliable results. Contact the factory for details regarding the GMSL2 channel specification.

A 100nF AC-coupling capacitor is normally used for GMSL2 links.

Line Fault

The GMSL2 serializers include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line-fault monitor requires external resistors R_{EXT} and R_{PD} connected to the LMN pins as shown in Figure 22 and Figure 23.

By default, only LMN0 is enabled in MAX96751. Configuration options are available through registers. Its status can be read by register. If unmasked, a line-fault condition asserts ERRB. Line-fault detection cannot be used in conjunction with power over coax (POC).

The line-fault monitor pins offer flexible connection and programming. On parts with multiple GMSL2 links, either pair (i.e., LMN1A/LMN0A) can be used with either link (i.e., SIOA+/SIOA-). In addition, the pins within each pair can be assigned to either polarity of the link.

The line-fault circuit does not work in floating GND applications.

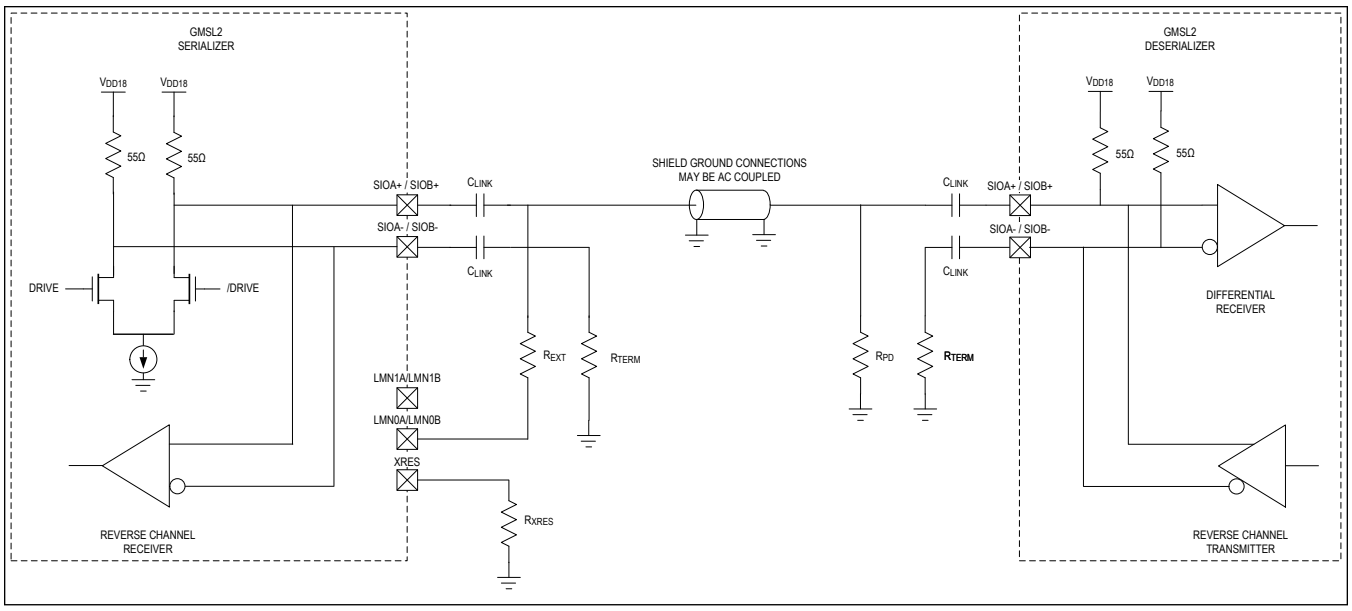


Figure 22. Typical GMSL2 Link Application Circuit for Coax Cable

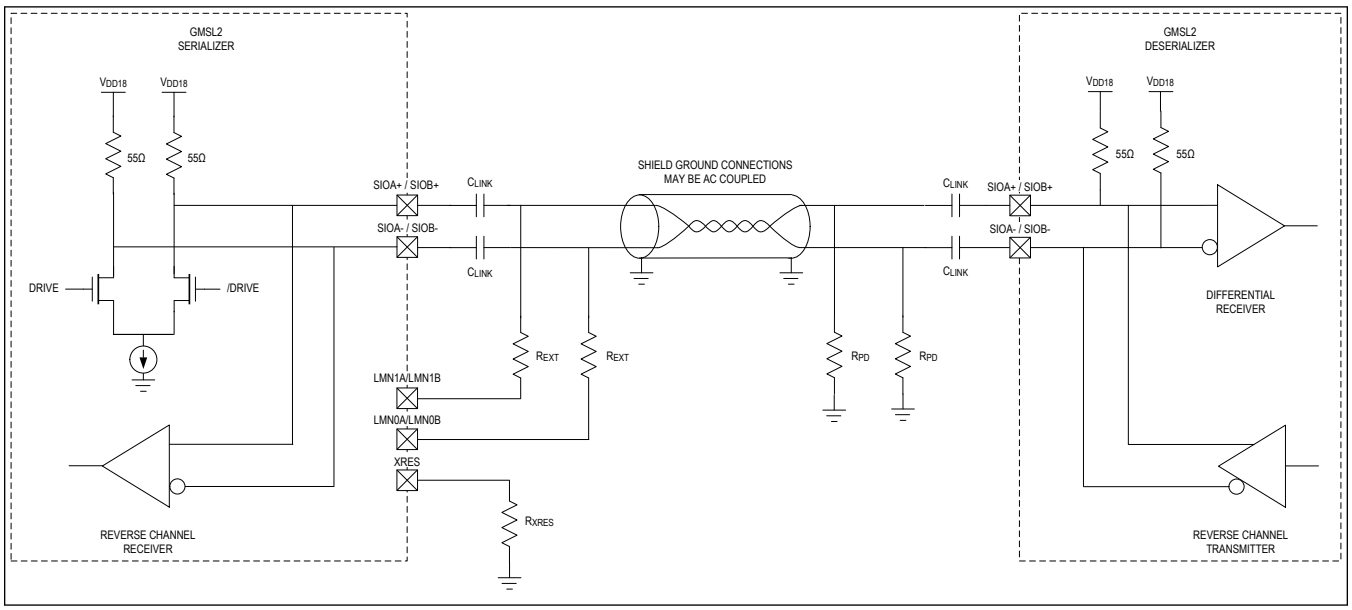


Figure 23. Typical GMSL2 Link Application Circuit for Twisted Pair

Line Fault in AC-Coupled Ground Applications

Use of the line fault function is not recommended in applications with a floating cable shield. Contact the factory for details.

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared between video, the I^2C/UART control channel, pass-through I^2C/UARTs, I^2S/TDM audio, SPI, and GPIOs, plus various protocol specific data exchanges (i.e., info frames, sync, and acknowledgements). The reverse channel bandwidth is also shared with all of the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

Link bandwidth is shared flexibly between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation; if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent one single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Users need to ensure that the worst-case use cases do not exceed the available throughput of the forward and reverse links. Analog Devices' evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that can be used for initial bandwidth requirements estimates. Analog Devices also has other tools that are useful for calculating link bandwidth utilization. It is recommended to consult the factory for high bandwidth use cases to ensure error-free performance.

Table 5 provides rough estimates of the bandwidth utilization for each of the communication channels.

Table 5. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Display Video (Forward Path Only)	PCLK x (bpp + 0.5 + packet_CRC) x 10/9 x 2048/2047
I^2C	13 to 40 x I^2C clock rate
UART	6 x UART bit rate
SPI	1.7 to 3.1 x SPI rate, depending on SPI byte length
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled
I^2S/TDM	BW = sample_rate x 20 x (roundup (channelcnt x sample_depth/18 + 0.5) + 2)

Definitions:

PCLK = Total horizontal pixels x total vertical lines x frame rate. Total horizontal includes blanking pixels, and total vertical includes blanking lines.

bpp = bits per pixel (typically 24)

packet_CRC = 0.5 when packet CRC is enabled, = 0 when packet CRC is disabled. Packet CRC is disabled by default.

sample_rate = audio sample rate (samples per second)

sample_depth = bits per sample per audio channel (must be the same for all channels)

channelcnt = number of audio channels

Power Supplies

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the MAX96751. V_{DD18} is the primary analog supply and is fixed at 1.8V. The 3.3V V_{DD33} supply provides power to the HDMI interface. The analog V_{DDA} and the digital V_{DDD} require a 1.0V power supply. Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. See *Table 3* for external components requirements. See *Table 2* for power supply tolerances. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Power supply ramp-time recommendation: 20µs < ramp time < 2ms. Power supply ramps should be monotonic. Once the supply voltage has reached the minimum supply voltage limit, it should not be allowed to drop below the specification.

Analog Devices provides power management ICs (PMICs) optimized for supporting serial link devices. Contact the factory for information.

Thermal Management

Power consumption of GMSL2 devices varies based on their use case. Care must be taken by the user to provide sufficient heat dissipation with proper board and cooling design techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to meet electrical specifications and avoid impacting device reliability.

For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Primary I^2C/UART (internal access)
- Pass-through I^2C/UART
- SPI
- GPIO

Some GMSL2 devices also support the following interface:

- I^2S/TDM audio

Data from all these interfaces tunnel through the GMSL2 link, but it is only through the primary I^2C/UART interface that the GMSL2 device registers can be accessed and configured.

The side channel, with its various interfaces, is accessed through multifunction GPIO pins (MFPs on some devices). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 8 and the *Pin Description* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Primary I^2C/UART

The primary I^2C/UART is located on the SDA_RX and SCL_TX pins of each GMSL2 device. The I^2C (SDA, SCL) or UART (Tx, Rx) interface is selected by the I2CSEL configuration pin state at power-up (see the *Latch-On-Power-Up Pins* section). The selected interface provides main access to GMSL2 registers, as well as peripheral device registers, from either end of the link.

The main µC can be located on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). Dual main µCs are supported, wherein DIS_REM_CC settings in register I2C_6 for each link can disable the remote Control Channel communications on that link. Optionally, software arbitration (such as token passing) can be used to prevent packet collisions.

To configure peripheral devices over the link, the GMSL2 serializer and deserializer must use the same control channel interface (both I^2C or both UART). Unlike GMSL1 devices, there is no I^2C-to-UART conversion capability. I^2C/UART outputs are open drain and require appropriately-sized external pull-up resistors for proper operation.

For detailed primary channel programming information, see the Control Channel Programming section under *Applications Information*.

Pass-Through I^2C/UART

GMSL2 devices have two pass-through I^2C/UART channels. These channels do not have access to registers in either the GMSL2 serializer or the deserializer; they simply tunnel the I^2C or UART signal through the GMSL2 link. This can be useful for separating I^2C channels so that multi-main conflicts do not occur. The I^2C/UART outputs are open drain and require appropriately sized external pull-up resistors for proper operation.

SPI

GMSL2 enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. Communication can be in either direction across the GMSL2 link. Although multiple SPI peripherals may be

connected, it is recommended that only one be communicated with at a time. Contact the factory for guidance on configuring SPI connections.

The SPI clock range is 600kHz to 25MHz. Care must be taken to meet setup and hold time requirements when using at speeds higher than 20MHz.

I²S/TDM Audio

GMSL2 devices for display applications support I²S stereo and up to 8 channels of audio in TDM mode. In GMSL2 mode, most devices have two audio channels: forward direction and reverse direction. Sample rates of 8kHz to 192kHz and sample depths of 8- to 32-bits are supported. In GMSL2 mode, the maximum SCK frequency is 49.152MHz. For system flexibility, GMSL2 devices can act as either the subordinate or the main at either end of the link.

Table 6. Typical Control Channel Latencies

FUNCTION	FORWARD (µS)	REVERSE (µS)	NOTES
I²C	< 10	< 10	—
UART	< 10	< 10	—
Audio	< 100	< 100	For typical use cases
SPI	< 10	< 10	Round trip

General-Purpose Inputs and Outputs (GPIOs)

The GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link and can be set up in forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based; a GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The GPIO multifunction pins can be programmed as GPI (input), GPO (push-pull or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pull-up or pull-down (or none). Although an internal pull-up is provided, high-speed open-drain outputs require an appropriate value external pull-up resistor to V_{DDIO}. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pull-up or pull-down programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) set to the same pin ID. By default, the ID mapping is GPIO0-GPIO0, GPIO1-GPIO1, GPIO2-GPIO2, etc. However, the GPIO mapping can be arbitrarily changed through register settings.

GPI transitions can be transmitted in two modes: Delay-compensated and Non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease. Delay compensation is only available on MAX96751 Link-A.

The state of each GPIO can be read or written by register either locally or remotely over the GMSL2 link by a µC using the control channel I²C/UART interface.

In Non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

Note: Reverse GPIO with delay compensation can be used on Link-A, but it cannot be used on Link-B.

Typical GMSL2-only device delays for 6Gbps forward and 187Mbps reverse-link rates are shown in Table 7.

Table 7. Typical GPIO Delays for Forward and Reverse Link Transmission

LINK TRANSMISSION	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	6µs
	1	15µs

Multifunction Pin Assignments

Multiple functions are assigned to each multifunction pin. They cannot be used simultaneously. The user must decide which function to use for each pin. The *Pin Description* indicates the function modes for each multifunction pin, listed in order of priority. Higher priority modes must be turned off when lower-priority modes are enabled, both through register writes. Table 8 indicates how latch-on power-up, I²C/UART, audio, SPI, and other functions are mapped to the GPIO pins. All GPIOs have rise and fall times that support the highest speed applications. Any pins configured for I²C/UART operation automatically switch to the I²C pin speed.

Table 8. GPIO Pin Function Map

PIN	LATCH ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO
GPIO00		Pass-Through 1 SDA/RX				GPIO00
GPIO01		Pass-Through 1 SCL/TX				GPIO01
GPIO02		MS/Pass-Through 2 SDA/RX				GPIO02
GPIO03	RCLKEN				RCLKOUT	GPIO03
GPIO04		Pass-Through 2 SCL/TX				GPIO04
GPIO05				BNE, SS1		GPIO05
GPIO06				RO, SS2		GPIO06
GPIO07				MISO		GPIO07
GPIO08				MOSI		GPIO08
GPIO09				SCLK		GPO09
GPIO10			Fwd Path WS			GPIO10
GPIO11			Fwd Path SCK			GPO11
GPIO12			Fwd Path SD			GPO12
GPIO13	ADD0		Rev Path SD			GPO13
GPIO14	ADD1		Rev Path SCK			GPIO14
GPIO15	ADD2		Rev Path WS			GPIO15
GPIO16	CXTP				HS	GPIO16
GPIO17	I2CSEL				VS	GPIO17
GPIO18		Primary Channel SDA/RX				GPIO18
GPIO19		Primary Channel SCL/TX				GPIO19

Table 9. Control and Side Channel Rise and Fall Times

PIN	TYPICAL RISE TIME*		TYPICAL FALL TIME**	
V_{DD18}	1.8V	3.3V	1.8V	3.3V
ERRB, LOCK	1.0ns	0.6ns	0.8ns	0.5ns
All GPIO pins	1.0ns	0.6ns	0.8ns	0.5ns
I²C	*	*	40ns	30ns

*20% to 80%, 10pF load. Rise time is for push-pull output configuration. Rise time for open-drain outputs depends on the external pull-up resistor value.

**80% to 20%, 10pF load.

Latch-On Power-Up Pins

Upon power-up, logic states are latched at specific configuration input pins. These states set initial register values and functional modes that cannot be easily programmed through I²C or UART after the IC powers up.

Bias the pins to V_{DDIO} for a logic 1 or GND for a logic 0 using sufficiently high-value resistors (up to 10kΩ). Make sure

that the voltage seen at the pin is at a valid logic level to ensure proper latching.

All latch-on power-up pins also double as GPO only pins after power-up. Before the pin states are latched, the chip does not drive the pin. It is highly recommended to use the GPIO pins only as outputs that function doubly as latch-on power-up pins, unless the user can guarantee that the proper pin logic state is present at the pin at power-up. When the pin is used as an output, it should not be driven externally. The power-up state is solely determined by the external resistor.

The following is a list and descriptions of latch-on power-up bits:

ADD2, ADD1, ADD0: These bits set the device address (DEV_ADDR) that is used as the subordinate address by I^2C and UART. They also set the default value of the TX_SRC_ID registers of each low bandwidth channel (audio, info frame, I^2C, UART, SPI, GPIO). Device addresses can be changed after power-up by writing to the DEV_ADDR register. See Table 10.

CXTP: This bit sets the device into coaxial or twisted-pair mode with the value reflected in both register bits CXTP_A and CXTP_B. This bit can be changed after power-up, since one link can be set as coax and the other as twisted pair. CXTP = 0 sets the differential mode operation at 3Gbps GMSL2 forward link rate, while CXTP = 1 sets single-ended coax operation at 6Gbps GMSL2 forward link rate. The default reverse channel rate is set to 187.5Mbps independent of CXTP setting.

I2CSEL: This bit selects either I^2C or UART mode for internal register access and remote (over GMSL2 link) control channel communication. Set I2CSEL = 0 for UART or I2CSEL = 1 for I^2C.

RCLKEN: This bit sets the default value of the RCLKEN register. If RCLKEN = 1, the chip outputs the 25MHz reference clock from RCLKOUT.

Table 10. Device Addresses

ADDRESS BITS ADD[2:0]	DEVICE ADDRESS
000	0x80
001	0x84
010	0x88
011	0xC0
100	0xC4
101	0xC8
110	0x40
111	0x44

Power-Up and Link Startup

GMSL2 devices are in power-down mode when PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies are up, each device starts its power-up sequence and performs these actions in sequence:

1. Set the latch-on-power-up pins register. Set the internal registers according to the selected configuration: I2CSEL, CXTP, ADD0, ADD1, ADD2, RCLKEN (if available).
2. The control channel (I^2C or UART) is functional on the local side. The device registers are writable and readable.
3. The link is established based on the following settings:
   a. Single Link Auto Selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish a GMSL2 link by periodically trying to handshake using PHY A and PHY B. Note: AUTO_LINK = 1 is the default and recommended setting to optimize lock time in single link mode.
   b. Single Link Manual Selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish a link using PHY A. If LINK_CFG = 2, establish a link using PHY B.
   c. Dual Link mode (LINK_CFG = 0): Establish a link using both PHYs.
   d. Splitter (serializer)/Aggregator (deserializer) mode (LINK_CFG = 3): Establish a link using both PHYs (for specific applications only).
4. Each enabled PHY performs link calibration, equalizer adaptation, and data channel locking. Both devices set their

LOCK pins high.
5. The control channel is available from remote side.

The link-up process, from the time that the last part's PWDNB input is brought high, typically takes approximately 45ms for any channel meeting the GMSL2 Lock Time t_{RD} timing (noted in *Link Lock* section) and the GMSL2 channel specification.

After the devices are linked, they can be configured. This can be done locally or over the control channel by a µC on either the serializer side or the deserializer side.

Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks, including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. Note: If Sleep mode is being used, do not use RESET_ALL as it returns the device to Sleep mode.
2. Setting RESET_LINK resets all GMSL PHY-related digital logic and data pipelines. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related digital logic and data pipelines, then automatically clears itself. This is similar to setting and clearing RESET_LINK. RESET_ONESHOT should only be used when GMSL link lock is active.

Program the registers that affect the GMSL2 link operation first (example, TX_RATE, RX_RATE, CXTP_A/B, AUTO_LINK, LINK_CFG, GMSL2), followed by RESET_ONESHOT, or set these registers when RESET_LINK = 1, then set RESET_LINK = 0. Setting LINK_CFG = 3 is a special case that requires writing LINK_CFG = 3 and RESET_ONESHOT = 1 in the same register byte.

Clocking

GMSL Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both the serializer and deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

Spread-Spectrum Clocking

Analog Devices' GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and interconnections and provide additional margin.

SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25KHz sawtooth modulation profile, programmable to deviate up to ±2500ppm from the center frequency.

Reference Clock Generation

The MAX96751 can share a crystal by utilizing a reference clock output. RCLKOUT can be used as a reference clock by another serializer in close proximity. This arrangement eliminates the need for an additional external crystal or oscillator for the second serializer.

Link and Video Lock

GMSL Link Lock

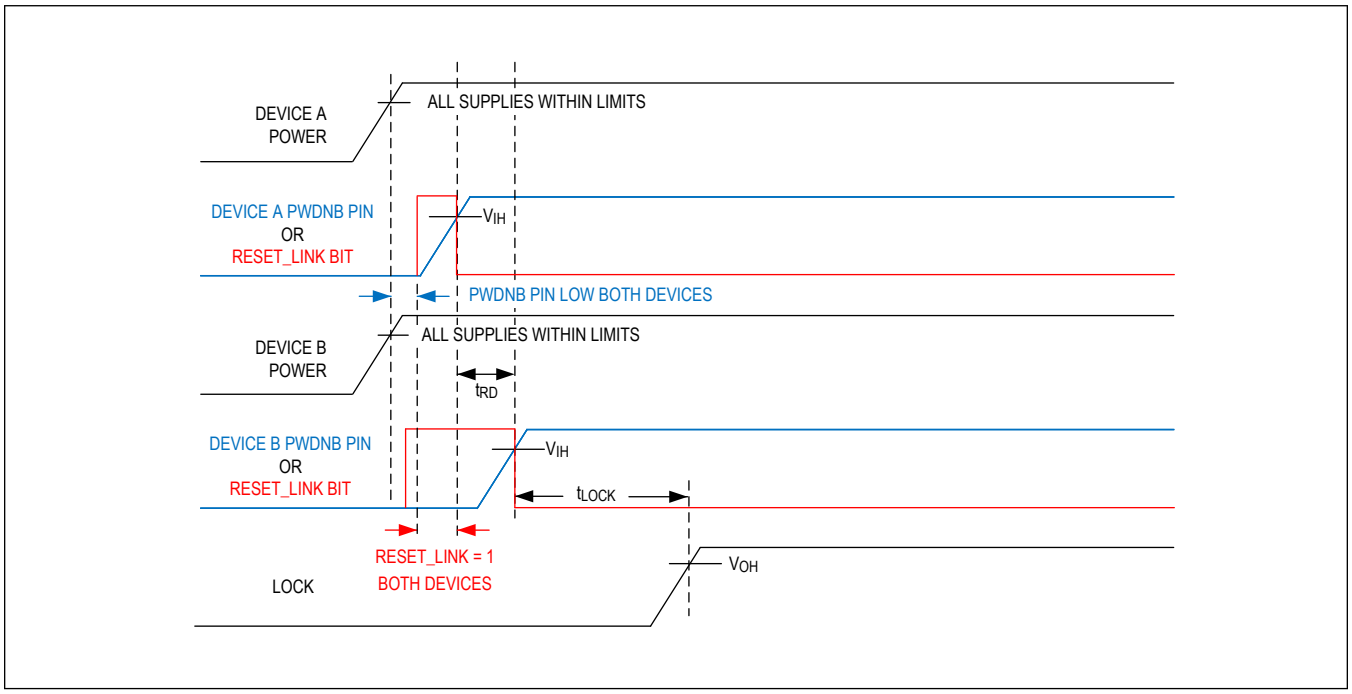


Figure 24. GMSL2 Lock Time

Figure 24 illustrates the sequence used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C/UART, SPI, GPIO, audio) can be used immediately after link lock is asserted.

The device establishes single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in, and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

Dual-link and splitter configurations require additional user programming. For guidance on enabling these configurations and optimizing the lock time, contact the factory.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links. So, a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in *Note 5*. Contact the factory for guidance if this timing cannot be

guaranteed.

7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This minimizes any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

Power Standby and Sleep Mode

A power manager block is present in all GMSL2 devices. Its primary function is to monitor supply voltages and control power-down (standby) and sleep modes. V_{DD18} must remain stable to provide continuous power to the data retention memory, and it is recommended that all supplies be maintained in their nominal operating range.

There are two ways to go into low power mode while all power supplies are active: assert the PWDNB pin or invoke the sleep state. Both states offer very low power supply currents.

Asserting the PWDNB pin (active low) places the device in standby power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in power-down mode.

The sleep state provides preservation of critical register settings and configurations. The register table includes an asterisk (*) for registers that are retained. The device can be put into the sleep state through an I^2C/UART command. The resume state restores the device back to the presleep condition without the need for additional register writes. There are two ways to wake up from Sleep mode:

- Local Wake-Up: Local wake-up entails the local host processor initiating a dummy control channel transaction, which briefly wakes up the device. In I^2C mode, the initial temporary wake-up requires four falling edges on SDA. Depending on the device address used, the host may need to issue multiple consecutive dummy transactions to achieve the required four SDA falling edges. The dummy transaction(s) must immediately be followed by the host processor setting SLEEP=0 to permanently exit Sleep mode. The device automatically returns to Sleep mode if SLEEP remains set to 1.
- Remote Wake-Up: All GMSL devices include wake-up detectors to observe GMSL link activity and briefly turn on the device when activity is detected. The link can then lock, providing an opportunity for a remote host to disable Sleep mode (setting SLEEP=0). The device automatically reverts to Sleep mode if SLEEP remains set to 1.

All GPIO pins are Hi-Z in power-down and sleep states.

Error and Fault Condition Monitoring

Both the serializer and deserializer have an open-drain, multipurpose error reporting, and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for assertion of ERRB can be determined by reading the register status.

Remote Error Monitoring

If REM_ERR_OEN is enabled on the remote device before link lock, there is a ~1 µs glitch on the remote ERRB upon link lock if there are no errors on both sides of the link. See Figure 25. REM_ERR_OEN is not enabled by default on this device.

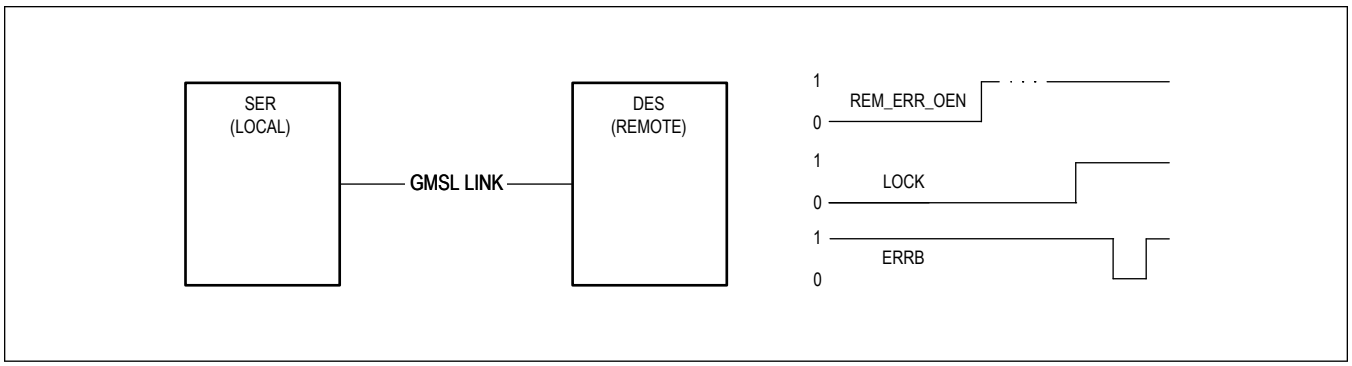


Figure 25. REM_ERR_OEN on the remote device is enabled before Link Lock

To ensure proper operation of REM_ERR_OEN, enable REM_ERR_OEN on the remote device only after link lock is established. See Figure 26.

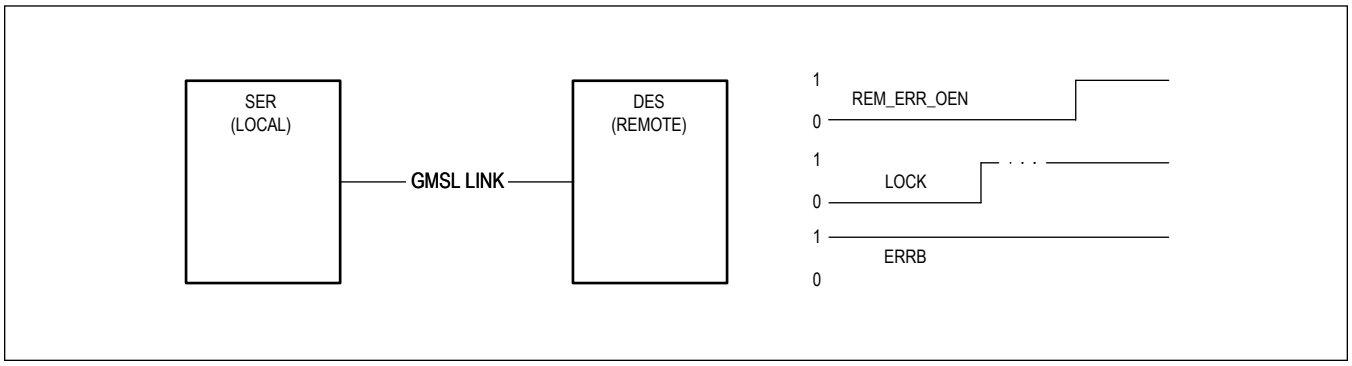


Figure 26. REM_ERR_OEN on the remote device is enabled after Link Lock

If REM_ERR_OEN=1 on the remote device before link lock, and the µC is on the remote device:

1. Disable ERR_RX_EN on the local device before link lock.
2. Wait for link lock.
3. Disable ERR_TX_EN on the remote device.
4. Enable ERR_RX_EN on the local device.
5. Enable ERR_TX_EN on the remote device.

If REM_ERR_OEN=1 on the remote device before link lock, and the µC is on the current device:

1. Disable ERR_TX_EN on the local device before link is down.
2. Wait for link lock.
3. Enable ERR_RX_EN on the remote device.
4. Enable ERR_TX_EN on the local device.
5. Disable ERR_TX_EN on the local device.
6. Enable ERR_TX_EN on the local device.

Adaptive Equalization (AEQ)

The GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then is invoked at a ~1Hz rate to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built in eye-opening monitor.

Video Pipeline

The video pipeline receives data and timing signals from the HDMI port. Video flows through the design as described in the following sections and is output on the GMSL link(s).

The MAX96751 has two video pipes to support Dual-view Splitter mode.

Video Timing Generator

The video timing generator (VTG) is an auxiliary block that can substitute HS, VS, and DE signals with the signals that it generates as defined by the configuration registers. The VTG can generate almost any type of SYNC signal set pattern in various modes by using the sync signals from the peripheral input as the trigger for starting the generated patterns.

RGB888 Video Pattern Generator

The RGB888 video pattern generator (VPG) is also an auxiliary block that can be used for various purposes. If desired, video from the peripheral can be replaced by the video pattern generated by the VPG. The VPG generates various patterns when configured from the configuration registers. The VPG creates RGB888 data only.

Tx Crossbar

Data from the video input is captured and optionally multiplexed with the generated patterns from the VTG or VPG. Final data goes into a crossbar multiplexer that allows any input bit to be mapped to any output bit using the configuration registers.

Video Line CRC

A CRC32 polynomial is used to generate an optional 32-bit code at the end of each DE or HS pulse. This code is transferred to the receiver side using info frames. The CRC checker generates the same code on the receiver side and validates if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE on the receiver side, even if the info frame is not received.

Eye-Opening Monitor

The eye-opening monitor (EOM) enables the GMSL2 devices to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free, but have less link margin than desired. This allows the customer to proactively react to deteriorating cable performance before any link errors occur. GMSL2 devices can measure the horizontal or vertical eye opening of the equalizer's output. The measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Watermarking

The watermarking block allows users to detect a frozen frame failure in a frame-based processing system between the generator and detector. This feature is specifically targeted to detect frozen frames caused by SOCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector.

GMSL2 devices contain both a watermark generator and a watermark detector. This allows both serializers and deserializers to insert a watermark or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark. If it fails to see all the generated watermarks, this indicates a frozen frame in the frame-based processing system between the generator and detector. For this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe state in less than 500ms.

PRBS

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer for testing the video

channel operation. The video PRBS generator can work with the recovered PCLK received from the video source. An external PCLK can also be provided to a designated GPIO pin to run the video PRBS generator. Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link that does not cause a video PRBS error.

Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker on the receiver side for testing the audio channel operation. The audio PRBS generator can operate using the incoming I^2S SCK and WS signals or using an internally generated reference clock. The detected audio channel bit errors are reported through a status register.

HDMI Receiver

The HDMI v1.4 and v2.0 compliant receiver provides audio and video serializer data. High-bandwidth video streams can require dual links or video compression to deliver streams to the deserializer. HDMI audio from a user input port can be output for local use. HDMI receiver interrupts are accessible after register configuration, and the consolidated HDMI receiver interrupt can be connected to the ERRB pin to observe events such as cable disconnect, cable connect, and sync detect. In the HDMI serializer, there are two video-transmit paths. Only the first video pipeline has the watermark function. The second video path is enabled when the video is split using the dual-view controller. The dual-view controller can optionally convert a side-by-side, dual-view superframe to a column-interleaved, dual-view format. Additionally, it can split columns of video data into two streams for transmission using two separate transmit paths by observing DE or HS signals for even/odd alignment.

Effectively, the split and convert functions of the dual-view block allow the user to transport side-by-side or column-interleaved HDMI video to two separate displays on two different deserializers or through the two video output ports of the same deserializer.

The OLDI deserializer is a special case as it can only split even and odd pixels from the same video stream to OLDI output ports. Therefore, when paired with an OLDI deserializer, the split needs to be done on the deserializer side while just providing a single column interleaved stream from the serializer side. The conversion function should be used to make sure that the incoming HDMI video is converted to column interleaved format.

Note: The HPD pin output logic levels are referenced to V_{DDIO}. For the most robust operation, use the same supply voltage for the HDMI source and serializer V_{DDIO}. If different supply voltages are used, a level-shifting circuit may be required.

HSPD Input Circuit

HDMI source power detect (HSPD) must simultaneously be driven to a valid logic-high voltage and stay within its absolute maximum voltage under all conditions. To accomplish this, provide a resistive divider between the +5V HDMI supply and ground, with the midpoint connected to HSPD. See Figure 27. The target voltage at HSPD is 90% of the nominal V_{DDIO} voltage.

The R2 resistor effective value must be calculated with the 1MΩ internal pull-down resistor in parallel. Use a 24.9kΩ, 1% resistor for R2. Higher values are not recommended, due to the cumulative tolerances of the relevant voltages and resistances. Table 11 provides the required R1 value when using 24.9kΩ for R2.

Note that the ESD diode provides a path for the HDMI +5V to power up the V_{DDIO} circuits when the V_{DDIO} supply is off. This can potentially result in the MAX96751 power manager recognizing all supplies as valid if the V_{DDIO} and V_{DD} supplies are powered up, even though V_{DDIO} is not.

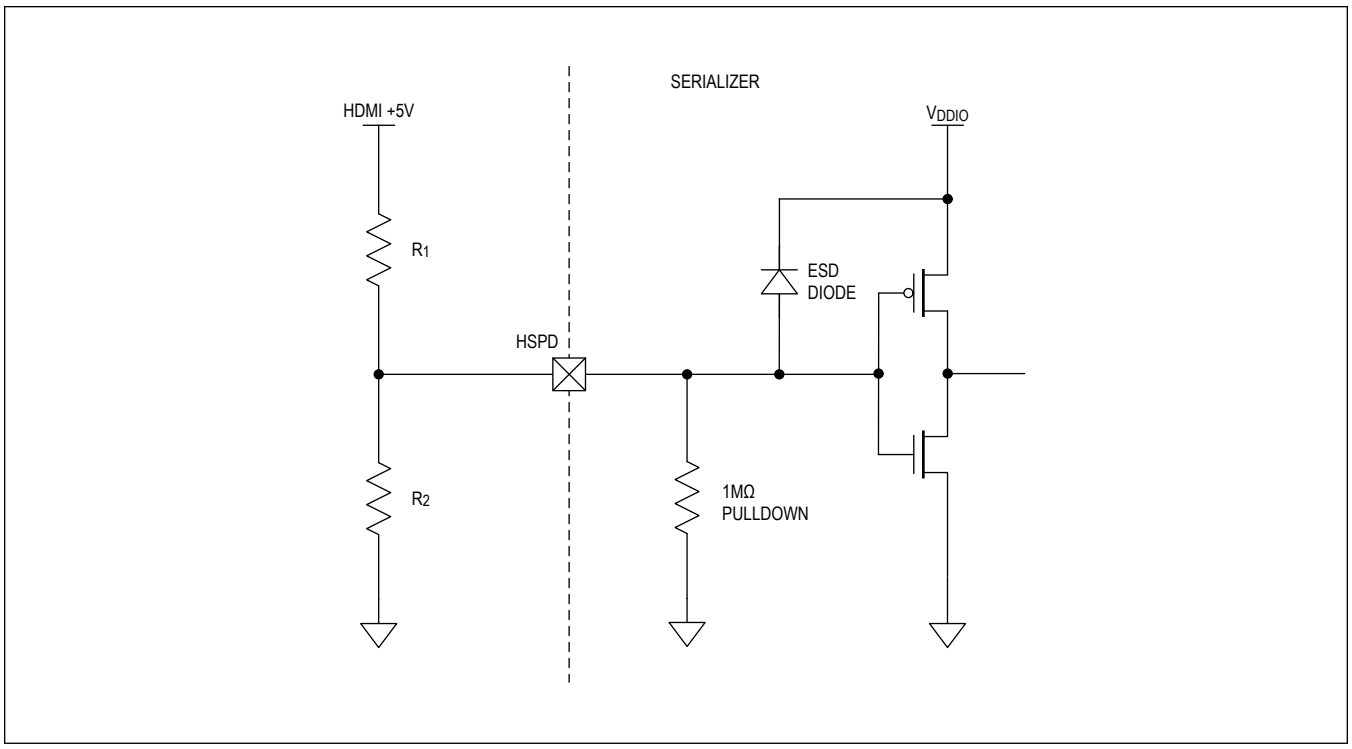


Figure 27. HSPD Input Circuit

Table 11. HSPD Resistor Value

V_{DDIO} VOLTAGE FUNCTION	1.8V	2.5V	3.3V
R1 Value	50.5kΩ	29.8kΩ	16.5kΩ

Applications Information

Software Programming Model

Analog Devices' automotive serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control channel accesses, such as the ASIL safety measures and interrupt handling, the following programming model should be followed:

1. Set the impacted functional blocks to Disabled or Reset mode. A general method used to place the part in IDLE state is to stop all side channel and video traffic followed by a register write (RESET_LINK=1) in order to stop the GMSL link.
2. It is required that the settings for each feature are fully configured before it is enabled.
3. Establish the link by setting RESET_LINK=0 and wait for link to lock.
4. Start video and side channel traffic.

If changing the configuration of a feature is required during operation of other features, disable the feature to be reconfigured, change its settings, and re-enable it.

Programming Notes

Make the following register writes to ensure proper operation of the MAX96751. Without these writes, the operation of the device specified in the data sheet cannot be guaranteed

Mandatory Register Programming

There are no mandatory register writes for MAX96751.

Control-Channel Programming

GMSL device registers can only be accessed and configured through the I^2C/UART interface in either I^2C mode or UART mode. By default, the primary I^2C/UART control channel is also sent to the remote-side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multimain configurations, with µCs connected to both the serializer and deserializer, disabling the remote control channel through register settings is recommended to prevent bus contention.

SDA and SCL lines operate as both an input and an open-drain output. Pull-up resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a main, followed by the device's 7-bit subordinate address, plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

Device Address

Each device on the I^2C/UART control channel must have a unique address. The MAX96751 GMSL2 device address is set to one of eight 7-bit addresses according to the logic states of pins ADD[2:0] at power-up. Note that the device address can be changed after power-up by writing to the DEV_ADDR register.

Primary I^2C Host-to-GMSL2 Device Communication

The host I^2C main has access to the GMSL2 serializer and deserializer registers. The host can program GMSL2 device registers to configure the pass-through I^2C/UART interfaces as I^2C or UART.

I^2C Programming

Each device has an internal I^2C subordinate for register access. The internal registers can be written and read according to the I^2C protocol using the packet formats in Figure 28 and Figure 29.

I²C Write-Packet Format

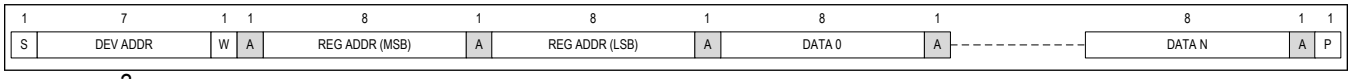


Figure 28. I²C Write-Packet Format

I²C Read-Packet Format

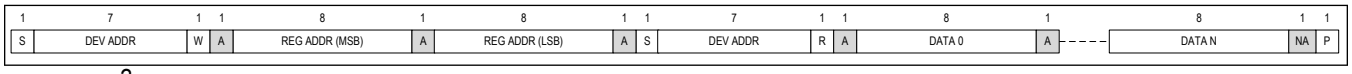


Figure 29. I²C Read-Packet Format

Host-to-Peripheral Primary I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, primary and pass-through I²C operation is the same. An I²C tunnel across the GMSL2 link connects the host's I²C main to the remote I²C subordinate. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C main connects to a GMSL2 device I²C subordinate, and the peripheral I²C subordinate connects to a GMSL2 device I²C main. For example, when the host I²C main transacts on one side of the link (local side), data is forwarded to the other side (remote side) by the I²C subordinate of the local side GMSL2 device. Data is then received by the I²C main of the remote side GMSL2 device, which in turn generates the same I²C transaction with the peripheral subordinate I²C. The remote side GMSL2 device sends back any I²C data expected by the local side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between main and subordinate and to allow time for data to be forwarded and received across the serial link. The host I²C main and peripheral I²C subordinate must support clock stretching by the GMSL2 device.

The host can program the GMSL2 device registers to independently configure the pass-through I²C/UART interfaces as either I²C or UART.

UART Programming

When the primary I²C/UART interface is configured as UART, there are two operating modes: Base and Bypass.

UART Base Mode

Base mode is the means of µC communication with the serializer and deserializer, in which, registers in these devices as well as peripheral devices, can be accessed. Base mode is enabled by default at power-up. In Base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in Base mode (through INTTYPE register settings). The device addresses of the serializer and deserializer in this mode are programmable.

In Base mode, serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol.

Figure 30 shows the UART protocol for writing and reading in Base mode.

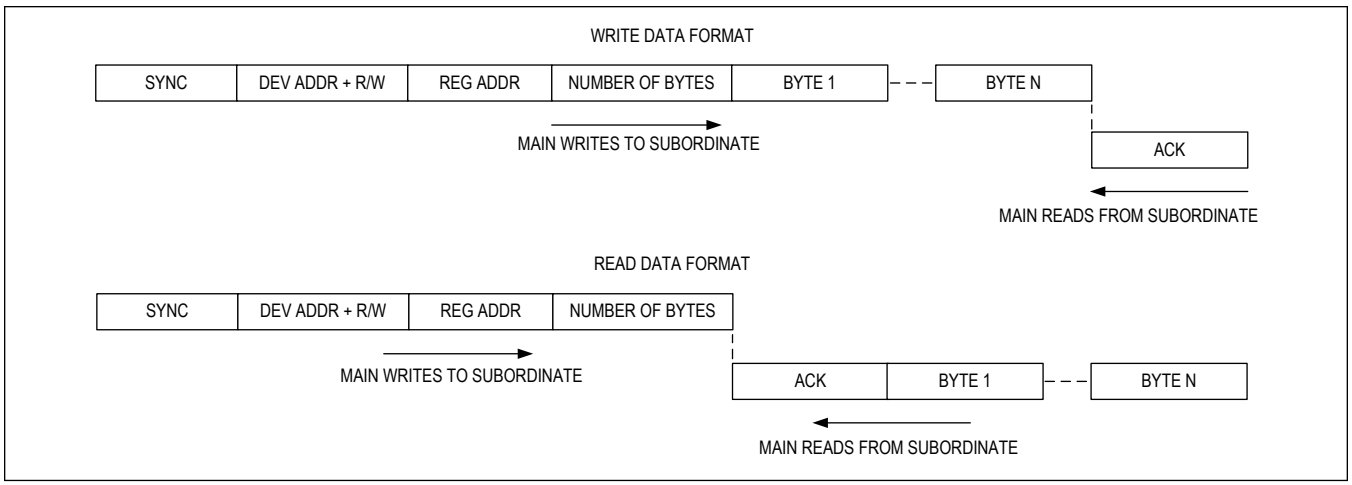


Figure 30. GMSL2 UART Protocol for Base Mode

UART Bypass Mode

In Bypass mode, the serializer/deserializer ignore UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between Base and Bypass mode: programming the register and using the MS pin.

When programmed by register, Bypass mode is only active when there is UART activity. When there is no UART activity for a selected timeout, both devices exit Bypass mode, and the bit is automatically cleared.

When set by the MS pin, a high pin level puts the device into Bypass mode, and a low level puts the device into Base mode. MS is set on the fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and is finished with a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd; otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be no more than 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet is discarded, starting from the frame with the error. The start of each frame is always a high-to-low transition (i.e., the stop bit is high, and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of 1 UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In Bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions, and the recipient of the data must perform error checking. The parity bit (which is enabled by default in Bypass mode) can be disabled before entering Bypass mode. Note that the bit rate in Bypass mode must be the same bit rate last used in Base mode.

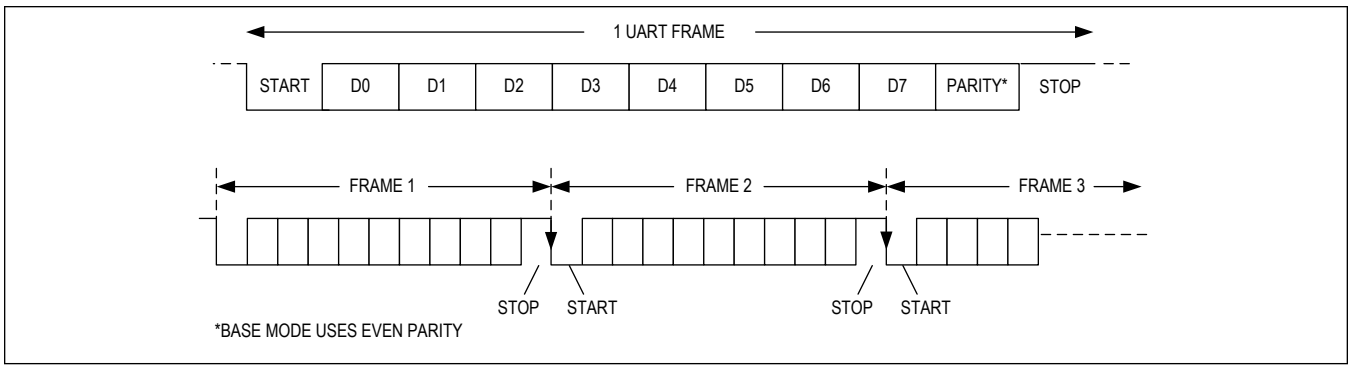


Figure 31. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. A sync frame (that is, a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset, and the framer begins waiting for the next sync frame.

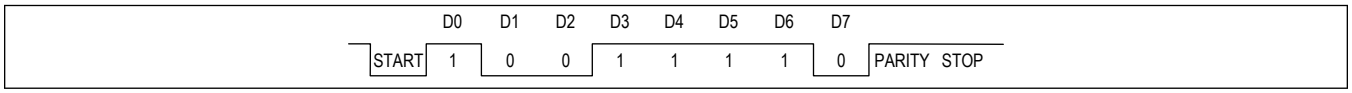


Figure 32. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors are detected in the transmitted packet, and it is recognized as valid. This is sent after the last bit of a successfully recognized packet is received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

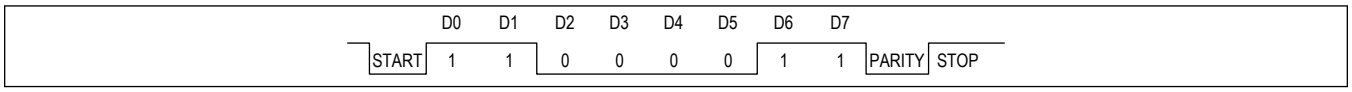


Figure 33. UART Acknowledge Frame

Write Packet

Write packets consist of a 5-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSb of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors are detected while receiving the write packet, and the write packet is valid. Byte count indicates the number of data bytes to be written, and it cannot be 0.

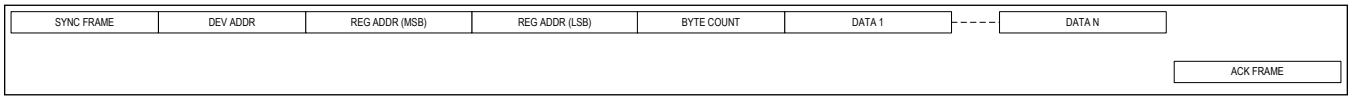


Figure 34. UART Write-Packet Format

Read Packet

Read packet consists of 5 bytes. The LSb of the device address frame is 1 for read packets. If no errors are detected while receiving the read packet, and the packet is valid, the addressed device responds with an acknowledge frame followed by one or more data bytes. Byte count indicates the number of data bytes to be read, and it cannot be 0.

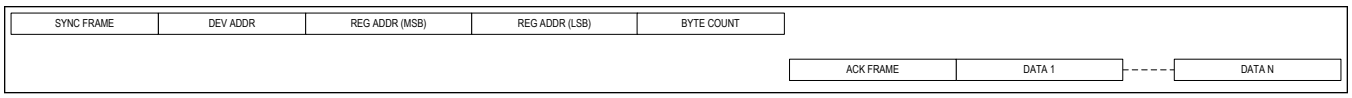


Figure 35. UART Read-Packet Format

Ordering Information

Part Number	Temp Range	Pin-Package
MAX96751GTN/V+	-40°C to +105°C	56-lead TQFN-EP*
MAX96751GTN/V+T	-40°C to +105°C	56-lead TQFN-EP*
MAX96751GTN/VY+	-40°C to +105°C	56-lead TQFN-SW-EP*
MAX96751GTN/VY+T	-40°C to +105°C	56-lead TQFN-SW-EP*

V Denotes an automotive qualified part

+ Denotes a lead(Pb)-free/RoHS-compliant package

EP Denotes Exposed Pad*

Register Map

Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. All bits not explicitly defined in the register table should be treated as reserved and should not be written to. If a write is required to a register with both defined and undefined register bits, read out the register's contents, change the defined bits, and write the new values back to the register.

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Note: * Indicates that the register is stored when entering Sleep mode and is restored upon exit from Sleep mode.

To ensure proper device operation, see the Mandatory Register Programming section (based on the existing Errata documentation) and the Device-specific User Guide.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x80	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x48	REG1[7:0]*	HDMI_AUTOS	RSVD	IIC_2_EN	IIC_1_EN	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	0x47	REG2[7:0]*	AUD_RX_SRC	RSVD	DIS_LOCAL_CC	DIS_REM_CC	AUD_TX_EN_Y	AUD_TX_EN_X	RSVD	RSVD
0x03	0x00	REG3[7:0]*	RSVD	–	RCLKEN	I2CSEL	UART_2_EN	UART_1_EN	RCLKSEL[1:0]	
0x04	0x1A	REG4[7:0]*	LF_1_M	LF_0_M	PU_LF1	PU_LF0	LF_1[1:0]		LF_0[1:0]	
0x05	0x0A	REG5[7:0]*	LF_3_M	LF_2_M	PU_LF3	PU_LF2	LF_3[1:0]		LF_2[1:0]	
0x0D	0x83	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x00	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
0x0F	0x00	REG15[7:0]	RSVD	RSVD	SPEED_CPBL[1:0]		DV_CPBL_N	DUAL_CPBL_N	SPLTR_CPBL_N	RSVD
0x39	0x00	IO_CHK1[7:0]	PIN_DRV_EN_1[7:0]							
0x3A	0x00	IO_CHK2[7:0]	PIN_DRV_SEL	–	PIN_DRV_EN_2[5:0]					
0x3C	0x00	IO_CHK4[7:0]	PIN_IN_1[7:0]							
0x3D	0x00	IO_CHK5[7:0]	–	–	PIN_IN_2[5:0]					
OVERLAP										
TCTRL										
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x0C	0x1A	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	RSVD	WAKE_EN_A	RSVD[3:0]			
0x10	0x11	CTRL0[7:0]*	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
0x11	0x22	CTRL1[7:0]*	–	–	RSVD	CXTP_B	RSVD	RSVD	RSVD	CXTP_A
0x13	0x10	CTRL3[7:0]	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–

ADDRESS	RESET	NAME	MSB							LSB
0x18	0xA0	INTR0[7:0]*	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x0B	INTR2[7:0]*	RSVD	RSVD	REM_ERR_OEN	HDMI_INT_OEN	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG	HDMI_INT	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x09	INTR4[7:0]*	RSVD	RSVD	MEM_INT_ERR_OEN	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	0x00	INTR5[7:0]	RSVD	RSVD	MEM_INT_ERR_FLAG	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	0x0F	INTR6[7:0]*	–	–	–	–	VDDCMP_INT_OEN	RSVD	APRBS_ERR_OEN	VDDBAD_INT_OEN
0x1F	0xC0	INTR7[7:0]	RSVD[1:0]		RSVD	RSVD	VDDCMP_INT_FLAG	RSVD	APRBS_ERR_FLAG	VDDBAD_INT_FLAG
0x20	0x1F	INTR8[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	0x5F	INTR9[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x22	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x23	0x00	CNT1[7:0]	DEC_ERR_B[7:0]							
0x24	0x00	CNT2[7:0]	IDLE_ERR[7:0]							
0x25	0x00	CNT3[7:0]	PKT_CNT[7:0]							
GMSL										
0x29	0x00	TX1[7:0]*	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
0x2A	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	0x44	TX3[7:0]*	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x2C	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x30	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
0x31	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	I2C_0[7:0]*	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	I2C_2[7:0]*	SRC_A[6:0]							–

ADDRESS	RESET	NAME	MSB							LSB
0x43	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x44	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x45	0x00	I2C_5[7:0]*	DST_B[6:0]							–
0x46	0x08	I2C_6[7:0]*	–	–	–	–	I2C_AUTO_CFG	I2C_SRC_CNT[2:0]		
0x47	0x00	I2C_7[7:0]	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
0x48	0x42	UART_0[7:0]*	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x49	0x96	UART_1[7:0]	BITLEN_LSB[7:0]							
0x4A	0x80	UART_2[7:0]	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
0x4C	0x26	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4E	0x00	I2C_PT_2[7:0]	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
0x4F	0x00	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
CFGV VIDEO_X										
0x50	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x51	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x53	0x10	TX3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_Y										
0x54	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x55	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x57	0x21	TX3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
CFGA AUDIO_X										
0x60	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x61	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x63	0x10	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x64	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x65	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x66	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN

ADDRESS	RESET	NAME	MSB							LSB
0x67	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGA AUDIO_Y										
0x68	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x69	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x6B	0x21	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x6C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x6D	0x90	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x6E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x6F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGI INFOFR										
0x70	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x71	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x73	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x74	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
CFGL SPI										
0x78	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x79	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x7B	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x7D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x7E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC CC										
0x80	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x81	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x83	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x84	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x85	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x86	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO										
0x88	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x89	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x8B	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x8C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x8D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x8E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_X										
0xA0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xA4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xA5	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0xA6	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_Y										
0xA8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xAB	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xAC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xAD	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
0xAE	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xAF	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_TX X										
0x100	0x60	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	RSVD	RSVD[1:0]	
0x101	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x102	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x104	0x40	VIDEO_TX4[7:0]	DAMP_MODE	DAMP_EN	RSVD[5:0]					
0x105	0x00	VIDEO_TX5[7:0]	RSVD	HEART_TYPE	RSVD[5:0]					
0x106	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_TX Y										
0x110	0x60	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	RSVD	RSVD[1:0]	
0x111	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x112	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x114	0x40	VIDEO_TX4[7:0]	DAMP_MODE	DAMP_EN	RSVD[5:0]					
0x115	0x00	VIDEO_TX5[7:0]	RSVD	HEART_TYPE	RSVD[5:0]					
0x116	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
AUD_TX AX										
0x120	0xB0	AUDIO_TX0[7:0]*	I2S_TDM_CFG[1:0]		I2S_CFG[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x121	0x4E	AUDIO_TX1[7:0]*	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	I2S_HDR_CFG[1:0]	
0x122	0x00	AUDIO_TX2[7:0]*	AUD_HDR_L[7:0]							
0x123	0x00	AUDIO_TX3[7:0]*	AUD_HDR_M[7:0]							
0x124	0x00	AUDIO_TX4[7:0]*	AUD_HDR_H[7:0]							
0x125	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	AUD_ODIV_H[3:0]			
0x127	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x128	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_TX AY										
0x130	0xB0	AUDIO_TX0[7:0]*	I2S_TDM_CFG[1:0]		I2S_CFG[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x131	0x4E	AUDIO_TX1[7:0]*	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	I2S_HDR_CFG[1:0]	
0x132	0x00	AUDIO_TX2[7:0]*	AUD_HDR_L[7:0]							
0x133	0x00	AUDIO_TX3[7:0]*	AUD_HDR_M[7:0]							
0x134	0x00	AUDIO_TX4[7:0]*	AUD_HDR_H[7:0]							
0x135	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	AUD_ODIV_H[3:0]			
0x137	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x138	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_RX										
0x140	0x21	AUDIO_RX1[7:0]*	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
0x143	0x00	AUDIO_RX4[7:0]	APRBS_ERR[7:0]							
0x146	0x02	AUDIO_RX7[7:0]*	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
0x148	0x00	AUDIO_RX9[7:0]	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
0x14D	0x00	INFO_RX4[7:0]	–	INFO_AUD_DEPTH[6:0]						
SPI										
0x160	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x161	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
0x162	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x163	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x164	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x165	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							
0x166	0x00	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN

ADDRESS	RESET	NAME	MSB							LSB
0x167	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x168	0x00	SPI_8[7:0]	REQ_HOLD_OFF_TO[7:0]							
WM										
0x188	0x00	WM_0[7:0]*	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
0x18A	0x50	WM_2[7:0]*	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x18B	0x14	WM_3[7:0]*	–	WM_TH[6:0]						
0x18C	0x10	WM_4[7:0]*	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
0x18D	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
0x18E	0x00	WM_6[7:0]	WM_TIMER[7:0]							
DUALVIEW										
0x1A0	0x04	DV0[7:0]*	DV_LOCK	DV_SWP_AB	LINE_ALT	RSVD	RSVD	DV_CONV	DV_SPL	DV_EN
0x1A1	0x00	DV1[7:0]	DV_PPL_L[7:0]							
0x1A2	0x20	DV2[7:0]*	DV_MEM_CRC_ERR	VID_EN_Y	VID_EN_X	RSVD[4:0]				
DUALVIEW_EXT_RNG										
0x1AE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1AF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
VTX										
0x1B0	0x00	CROSS_0[7:0]*	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1B1	0x01	CROSS_1[7:0]*	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1B2	0x02	CROSS_2[7:0]*	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1B3	0x03	CROSS_3[7:0]*	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1B4	0x04	CROSS_4[7:0]*	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1B5	0x05	CROSS_5[7:0]*	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1B6	0x06	CROSS_6[7:0]*	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1B7	0x07	CROSS_7[7:0]*	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1B8	0x08	CROSS_8[7:0]*	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1B9	0x09	CROSS_9[7:0]*	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x1BA	0x0A	CROSS_10[7:0]*	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1BB	0x0B	CROSS_11[7:0]*	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1BC	0x0C	CROSS_12[7:0]*	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1BD	0x0D	CROSS_13[7:0]*	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1BE	0x0E	CROSS_14[7:0]*	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1BF	0x0F	CROSS_15[7:0]*	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1C0	0x10	CROSS_16[7:0]*	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1C1	0x11	CROSS_17[7:0]*	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1C2	0x12	CROSS_18[7:0]*	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1C3	0x13	CROSS_19[7:0]*	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1C4	0x14	CROSS_20[7:0]*	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1C5	0x15	CROSS_21[7:0]*	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1C6	0x16	CROSS_22[7:0]*	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1C7	0x17	CROSS_23[7:0]*	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1C8	0x03	VTX0[7:0]*	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x1C9	0x01	VTX1[7:0]*	HDMI_SCDT	HDMI_CKDT	PCLKDET	SEL_EXT_PCLK	CKDT_SCDT_OVR	VS_OUT_EN	HS_OUT_EN	VS_TRIG
0x1CA	0x00	VTX2[7:0]*	VS_DLY_2[7:0]							
0x1CB	0x00	VTX3[7:0]*	VS_DLY_1[7:0]							
0x1CC	0x00	VTX4[7:0]*	VS_DLY_0[7:0]							
0x1CD	0x00	VTX5[7:0]*	VS_HIGH_2[7:0]							
0x1CE	0x00	VTX6[7:0]*	VS_HIGH_1[7:0]							
0x1CF	0x00	VTX7[7:0]*	VS_HIGH_0[7:0]							
0x1D0	0x00	VTX8[7:0]*	VS_LOW_2[7:0]							
0x1D1	0x00	VTX9[7:0]*	VS_LOW_1[7:0]							
0x1D2	0x00	VTX10[7:0]*	VS_LOW_0[7:0]							
0x1D3	0x00	VTX11[7:0]*	V2H_2[7:0]							
0x1D4	0x00	VTX12[7:0]*	V2H_1[7:0]							
0x1D5	0x00	VTX13[7:0]*	V2H_0[7:0]							
0x1D6	0x00	VTX14[7:0]*	HS_HIGH_1[7:0]							
0x1D7	0x00	VTX15[7:0]*	HS_HIGH_0[7:0]							
0x1D8	0x00	VTX16[7:0]*	HS_LOW_1[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1D9	0x00	VTX17[7:0]*	HS_LOW_0[7:0]							
0x1DA	0x00	VTX18[7:0]*	HS_CNT_1[7:0]							
0x1DB	0x00	VTX19[7:0]*	HS_CNT_0[7:0]							
0x1DC	0x00	VTX20[7:0]*	V2D_2[7:0]							
0x1DD	0x00	VTX21[7:0]*	V2D_1[7:0]							
0x1DE	0x00	VTX22[7:0]*	V2D_0[7:0]							
0x1DF	0x00	VTX23[7:0]*	DE_HIGH_1[7:0]							
0x1E0	0x00	VTX24[7:0]*	DE_HIGH_0[7:0]							
0x1E1	0x00	VTX25[7:0]*	DE_LOW_1[7:0]							
0x1E2	0x00	VTX26[7:0]*	DE_LOW_0[7:0]							
0x1E3	0x00	VTX27[7:0]*	DE_CNT_1[7:0]							
0x1E4	0x00	VTX28[7:0]*	DE_CNT_0[7:0]							
0x1E5	0x00	VTX29[7:0]	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x1E6	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x1E7	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x1E8	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x1E9	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x1EA	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x1EB	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x1EC	0x00	VTX36[7:0]	CHKR_B_H[7:0]							
0x1ED	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x1EE	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							
0x1EF	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x1F0	0x18	VTX40[7:0]	–	CROSS HS_I	CROSS HS_F	CROSSHS[4:0]				
0x1F1	0x19	VTX41[7:0]	–	CROSS VS_I	CROSS VS_F	CROSSVS[4:0]				
0x1F2	0x1A	VTX42[7:0]	–	CROSS DE_I	CROSS DE_F	CROSSDE[4:0]				
GPIO0 0										
0x200	0x1C	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x201	0x40	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x202	0x40	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO1 1										
0x203	0x83	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x204	0xA1	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x205	0x41	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO2 2										
0x206	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x207	0xA2	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x208	0x42	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO3 3										
0x209	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x20A	0xA3	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20B	0x43	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x20C	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x20D	0x44	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20E	0x44	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO5 5										
0x20F	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x210	0xA5	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x211	0x45	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO6 6										
0x212	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x213	0xA6	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x214	0x46	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO7 7										
0x215	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x216	0xA7	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x217	0x47	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x218	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x219	0xA8	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x21A	0x48	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO9 9										
0x21B	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x21C	0xA9	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x21D	0x49	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO10 10										
0x21E	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x21F	0xAA	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x220	0x4A	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO11 11										
0x221	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x222	0xAB	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x223	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO12 12										
0x224	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x225	0xAC	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x226	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO13 13										
0x227	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x228	0x2D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x229	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO14 14										
0x22A	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x22B	0x2E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22C	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO15 15										
0x22D	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS

ADDRESS	RESET	NAME	MSB							LSB
0x22E	0x2F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22F	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO16 16										
0x230	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x231	0x30	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x232	0x50	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO17 17										
0x233	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x234	0x31	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x235	0x51	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO18 18										
0x236	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x237	0x52	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x238	0x52	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO19 19										
0x239	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x23A	0x53	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x23B	0x53	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
CMU										
0x245	0x00	CMU5[7:0]	RSVD[3:0]				GPIO_SPEED_B[1:0]		GPIO_SPEED_A[1:0]	
MISC										
0x24A	0xDC	UART_PT_0[7:0]	BITLEN_PT_1_L[7:0]							
0x24B	0x05	UART_PT_1[7:0]	–	–	BITLEN_PT_1_H[5:0]					
0x24C	0xDC	UART_PT_2[7:0]	BITLEN_PT_2_L[7:0]							
RLMS A										
0x403	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x404	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN

ADDRESS	RESET	NAME	MSB							LSB
0x405	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x406	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol
0x438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x43A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x43B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x43D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPh TogEn
0x43E	0xBA	RLMS3E[7:0]	ErrChPh SecTA	ErrChPhSec[6:0]						
0x43F	0x79	RLMS3F[7:0]	ErrChPh PriTA	ErrChPhPri[6:0]						
0x449	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x464	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x495	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x4A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x4A8	0x00	RLMSA8[7:0]	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
0x4A9	0x00	RLMSA9[7:0]	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	RSVD	FW_RXD_EN	RSVD	RSVD	RSVD
0x4B6	0xBB	RLMSB6[7:0]	ErrChPh SecTASRG1875	ErrChPhSecSRG1875[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x4B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
RLMS B										
0x503	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x504	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x505	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x506	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x507	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x534	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x535	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x537	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x538	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x539	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x53A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x53B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x53D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x53E	0xBA	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x53F	0x79	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x549	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x558	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x559	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x564	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x570	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x571	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x572	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x573	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x574	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x575	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x576	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x595	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x5A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x5A8	0x00	RLMSA8[7:0]	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
0x5A9	0x00	RLMSA9[7:0]	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	RSVD	FW_RXD_EN	RSVD	RSVD	RSVD
0x5B6	0xBB	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x5B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
AONREG										
0x2005	0x00	RX_AON_SRST[7:0]*	–	–	–	reg_sw_rst_auto	–	–	–	reg_sw_rst
0x2009	0xC7	RX_SYS_SWTCHC[7:0]*	reg_ddc_sda_in_del_en	reg_ddc_sda_out_del_en	ddc_filter_sel[1:0]		–	reg_ddc_scdc_en	RSVD	reg_ddc_edid_en
0x200C	0x00	RX_STATE_AON[7:0]	–	–	–	–	hdmi_tx_connected	–	ckdt	scdt
0x2040	0x00	HDMI2_MODE_CTRL[7:0]*	–	–	reg_scramble_on_ovr	reg_hdmi_on_ovr	–	–	reg_scramble_on_val	reg_hdmi2_on_val
0x2070	0x00	RX_INTR_STATE[7:0]	–	–	–	–	–	–	–	reg_intr
0x2079	0x02	RX_INT_CTRL[7:0]*	–	–	–	–	reg_soft_intr_en	–	reg_intr_polarity	–
0x2080	0x10	RX_INTR2_AON[7:0]*	–	–	reg_intr2_stat5_aon	reg_intr2_stat4_aon	reg_intr2_stat2_aon	–	–	–
0x2081	0x00	RX_INTR6_AON[7:0]*	–	–	–	–	–	–	–	reg_intr6_stat0_aon
0x2082	0x00	RX_INTR7_AON[7:0]*	reg_intr7_stat7_aon	reg_intr7_stat6_aon	–	reg_intr7_stat4_aon	reg_intr7_stat3_aon	–	–	–
0x2083	0x00	RX_INTR8_AON[7:0]*	–	–	–	–	–	RSVD	reg_intr8_stat1_aon	–
0x2084	0x00	RX_INTR9_AON[7:0]*	reg_intr9_stat7_aon	reg_intr9_stat6_aon	–	–	reg_intr9_stat3_aon	reg_intr9_stat2_aon	reg_intr9_stat1_aon	reg_intr9_stat0_aon
0x2090	0x00	RX_INTR2_MASK_AON[7:0]*	–	–	reg_intr2_mask5_aon	reg_intr2_mask4_aon	reg_intr2_mask3_aon	–	–	–
0x2091	0x00	RX_INTR6_MASK_AON[7:0]*	–	–	–	–	–	–	–	reg_intr6_mask0_aon
0x2092	0x00	RX_INTR7_MASK_AON[7:0]*	reg_intr7_mask7_aon	reg_intr7_mask6_aon	–	reg_intr7_mask4_aon	reg_intr7_mask3_aon	RSVD[2:0]		

ADDRESS	RESET	NAME	MSB							LSB
0x2093	0x00	RX_INTR8_MASK_AON[7:0]*	–	–	–	–	–	reg_intr8_mask2_aon	reg_intr8_mask1_aon	–
0x2094	0x00	RX_INTR9_MASK_AON[7:0]*	reg_intr9_mask7_aon	reg_intr9_mask6_aon	–	–	reg_intr9_mask3_aon	reg_intr9_mask2_aon	reg_intr9_mask1_aon	reg_intr9_mask0_aon
0x20A9	0x01	SCDCS_CNTL[7:0]*	RSVD[2:0]			RSVD	–	reg_sw_rd_req_set	RSVD	reg_scdcs_enabled
0x20AB	0x01	Sink_Version[7:0]*	reg_scdcs_snk_ver[7:0]							
0x20AC	0x00	Source_Version[7:0]	scdcs_src_ver[7:0]							
0x20AD	0x00	scdcs_status1[7:0]	scdcs_ch2_locked	scdcs_ch1_locked	scdcs_ch0_locked	scdcs_clk_detected	scdcs_scrbl_status	scdcs_rr_test	scdcs_ced_upd	scdcs_sts_upd
0x20AE	0x00	scdcs_Config_status[7:0]	–	–	–	–	scdcs_tmds_bclk_ratio	scdcs_scrbl_enable	–	scdcs_rr_enable
0x20B0	0x00	SCDCS_CED0_L[7:0]	scdcs_ch0_ced_cnt_7_0[7:0]							
0x20B1	0x00	SCDCS_CED0_H[7:0]	scdcs_ch0_vld	scdcs_ch0_ced_cnt_14_8[6:0]						
0x20B2	0x00	SCDCS_CED1_L[7:0]	scdcs_ch1_ced_cnt_7_0[7:0]							
0x20B3	0x00	SCDCS_CED1_H[7:0]	scdcs_ch1_vld	scdcs_ch1_ced_cnt_14_8[6:0]						
0x20B4	0x00	SCDCS_CED2_L[7:0]	scdcs_ch2_ced_cnt_7_0[7:0]							
0x20B5	0x00	SCDCS_CED2_H[7:0]	scdcs_ch2_vld	scdcs_ch2_ced_cnt_14_8[6:0]						
0x20B6	0x00	SCDCS_CED_Checksum[7:0]	scdcs_ced_chksum[7:0]							
0x20F5	0x01	RX_HPD_C_CTRL[7:0]*	–	–	–	–	–	–	–	reg_hpd_c_ctrl
0x20F6	0x01	RX_HPD_OEN_CTRL[7:0]*	–	–	–	–	–	–	–	reg_hpd_oen_ctrl
0x20F9	0x02	RX_HPD_OVRT_CTRL[7:0]*	–	–	–	–	–	–	RSVD	reg_hpd_ovrt_ctrl
AUDREG										
0x2100	0x00	RX_ACR_CTRL1[7:0]*	reg_cts_dropped_auto_en	reg_post_hw_sw_sel	reg_upll_hw_sw_sel	reg_cts_hw_sw_sel	reg_n_hw_sw_sel	reg_cts_reused_auto_en	reg_fs_hw_sw_sel	reg_acr_init
0x2101	0x93	AAC_MCLK_SEL[7:0]*	reg_vcnt_max[1:0]		reg_mclk4dac[1:0]		reg_mclk4hbra[1:0]		reg_mclk4dsd[1:0]	
0x2102	0x42	RX_FREQ_SVAL[7:0]*	reg_fm_val_sw[1:0]		reg_fs_val_sw[5:0]					
0x2103	0x00	RX_N_SVAL1[7:0]*	reg_n_val_sw_7_0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x2104	0x00	RX_N_SVAL2[7:0]*	reg_n_val_sw_15_8[7:0]							
0x2105	0x00	RX_N_SVAL3[7:0]*	–	–	–	–	reg_n_val_sw_19_16[3:0]			
0x2106	0x00	RX_N_HVAL1[7:0]	n_val_hw_7_0[7:0]							
0x2107	0x0C	RX_N_HVAL2[7:0]	n_val_hw_15_8[7:0]							
0x2108	0x00	RX_N_HVAL3[7:0]	–	–	–	–	n_val_hw_19_16[3:0]			
0x2109	0x00	RX_CTS_SVAL1[7:0]*	reg_cts_val_sw_7_0[7:0]							
0x210A	0x00	RX_CTS_SVAL2[7:0]*	reg_cts_val_sw_15_8[7:0]							
0x210B	0x00	RX_CTS_SVAL3[7:0]*	–	–	–	–	reg_cts_val_sw_19_16[3:0]			
0x210C	0x68	RX_CTS_HVAL1[7:0]	cts_val_hw_7_0[7:0]							
0x210D	0x3C	RX_CTS_HVAL2[7:0]	cts_val_hw_15_8[7:0]							
0x210E	0x01	RX_CTS_HVAL3[7:0]	–	–	–	–	cts_val_hw_19_16[3:0]			
0x210F	0x00	RX_UPLL_SVAL[7:0]*	–	reg_upll_val_sw[6:0]						
0x2110	0x00	RX_UPLL_HVAL[7:0]	–	upll_val_hw[6:0]						
0x2111	0x00	RX_POST_SVAL[7:0]*	–	–	reg_post_val_sw[5:0]					
0x2112	0x00	RX_POST_HVAL[7:0]	–	–	post_val_hw[5:0]					
0x2113	0x0F	RX_LK_WIN_SVAL[7:0]	–	–	–	reg_lk_win_sw_4_1[3:0]				reg_lk_win_sw_0
0x2114	0x00	RX_LK_THRS_SVAL1[7:0]	reg_lk_thrs_sval_7_0[7:0]							
0x2115	0x00	RX_LK_THRS_SVAL2[7:0]	reg_lk_thrs_sval_15_8[7:0]							
0x2116	0x00	RX_LK_THRS_SVAL3[7:0]	–	–	–	–	reg_lk_thrs_sval_19_16[3:0]			
0x2117	0x11	RX_TCLK_FS[7:0]*	rhdmi_aud_sample_f_extn[1:0]		–	reg_fs_filter_en	rhdmi_aud_sample_f[3:0]			
0x2118	0x0C	RX_ACR_CTRL3[7:0]*	–	reg_cts_thresh[3:0]				reg_mclk_loopback	reg_log_win_ena	reg_post_div2_ena
0x2119	0x00	RX_CHST6[7:0]	aud_sample_f_coeff[3:0]				bit43	cgms_a_validity	cgms_a[1:0]	
0x211A	0x00	RX_CHST7[7:0]	bit55_49[6:0]							info_in_pcm_signal
0x2126	0x40	RX_I2S_CTRL1[7:0]*	reg_invalid_en	reg_clk_edge	reg_size	reg_msb	reg_ws	reg_justify	reg_data_dir	reg_1st_bit

ADDRESS	RESET	NAME	MSB							LSB
0x2127	0x11	RX_I2S_CTRL2[7:0]*	reg_sd3_en	reg_sd2_en	reg_sd1_en	reg_sd0_en	reg_mclk_en	reg_mute_flat	reg_vucp	reg_pcm
0x2128	0xE4	RX_I2S_MAP[7:0]*	reg_sd3_map[1:0]		reg_sd2_map[1:0]		reg_sd1_map[1:0]		reg_sd0_map[1:0]	
0x2129	0x18	RX_AUDRX_CTRL[7:0]*	reg_i2s_length_en	reg_inv_cor_en	reg_hw_mute_en	reg_pass_spdif_err	reg_pass_aud_err	reg_i2s_mode	reg_spdif_mode	reg_spdif_en
0x212A	0x00	RX_CHST1[7:0]	bit6_7[1:0]		bit3_4_5[2:0]			bit2	bit1	bit0
0x212C	0x00	RX_CHST3a[7:0]	aud_ch_num1[3:0]				aud_source1[3:0]			
0x212D	0x02	RX_MUTE_DIV[7:0]	reg_div_incr[7:0]							
0x212E	0x00	RX_SW_OW[7:0]*	reg_swap[3:0]				–	reg_cs_bit2	–	reg_ow_en
0x212F	0x00	RX_OW_15_8[7:0]*	reg_cs_bit15_8[7:0]							
0x2130	0x01	RX_CHST4[7:0]	aud_sample_f_extn[1:0]		aud_accuracy[1:0]		aud_sample_f[3:0]			
0x2131	0x0B	RX_CHST5[7:0]	aud_org_fs[3:0]				aud_length[2:0]			aud_length_max
0x2132	0x00	RX_AUDO_MUTE[7:0]*	reg_i2s_length[3:0]				reg_ch3_mute	reg_ch2_mute	reg_ch1_mute	reg_ch0_mute
0x2137	0x00	RX_AUDP_MUTE[7:0]	–	reg_spdif4tdm_en	reg_spdif4i2s_en	aac_audio_mute	–	reg_mute_out_pol	reg_audio_mute	–
0x213D	0x00	RX_PD_SYS3[7:0]	reg_audio_toggle_mode	–	–	–	–	–	–	–
0x2140	0x0E	RX_TDM_CTRL1[7:0]*	–	–	–	reg_tdm_fs_msb[1:0]		reg_tdm_ch_num[1:0]		reg_tdm_mode
0x2141	0x10	RX_TDM_CTRL2[7:0]*	reg_tdm_fs_len[7:0]							
0x2166	0x03	VID_XPCLK_MULT[7:0]	–	–	–	–	reg_vid_pclk_cnt_mult_3_0[3:0]			
0x2167	0xFF	VID_XPCLK_Base[7:0]	reg_vid_pclk_cnt_base_7_0[7:0]							
0x2168	0x51	VID_XPCLK_EN[7:0]	reg_vres_xclk_diff[3:0]				–	–	–	reg_vid_xclkpclk_en
0x2169	0x00	VID_XPBASE0[7:0]	reg_xp_base_7_0[7:0]							
0x216A	0x00	VID_XPBASE1[7:0]	reg_xp_base_15_8[7:0]							
0x216B	0x00	VID_XPBASE2[7:0]	reg_xp_base_23_16[7:0]							
0x216C	0x00	VID_XP_THRSH[7:0]	reg_xp_thrsh[7:0]							
0x216D	0x00	RX_VID_XPCNT1[7:0]	aac_xclk_in_pclk_7_0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x216E	0x00	RX_VID_XPCNT2[7:0]	aac_xclk_in_pclk_15_8[7:0]							
0x216F	0x00	RX_VID_XPCNT3[7:0]	aac_xclk_in_pclk_23_16[7:0]							
0x218D	0x00	RX_APLL_STAT[7:0]	–	–	–	–	–	–	–	acr_dpll_lock
0x219D	0x00	RX_SM_NAPLL_STAT[7:0]	–	–	–	–	–	–	–	napll_lock
0x21A0	0x00	RX_AVG_WINDOW[7:0]	reg_avg_window[7:0]							
0x21A1	0x00	DACR_MCLK_CTRL[7:0]	–	–	–	–	–	–	–	reg_dacr_mclk_out_en
0x21A2	0x00	DACR_REF_CLK_SEL[7:0]	–	–	–	–	–	–	reg_dacr_ref_clk_sel[1:0]	
0x21B1	0x00	AEC4_CTRL[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	reg_aac_ctrl4_0
0x21B2	0x00	AEC3_CTRL[7:0]	reg_aac_ctrl3_7	reg_aac_ctrl3_6	reg_aac_ctrl3_5	reg_aac_ctrl3_4	reg_aac_ctrl3_3	reg_aac_ctrl3_2	reg_aac_ctrl3_1	reg_aac_ctrl3_0
0x21B3	0x00	AEC2_CTRL[7:0]	reg_aac_ctrl2_7	reg_aac_ctrl2_6	reg_aac_ctrl2_5	reg_aac_ctrl2_4	reg_aac_ctrl2_3	reg_aac_ctrl2_2	reg_aac_ctrl2_1	reg_aac_ctrl2_0
0x21B4	0x17	AEC1_CTRL[7:0]	reg_aac_ctrl_7	reg_aac_ctrl_6	reg_aac_ctrl_5	reg_aac_ctrl_4	reg_aac_ctrl_3	reg_aac_ctrl_2	reg_aac_ctrl_1	reg_aac_ctrl_0
0x21B5	0xE0	AEC0_CTRL[7:0]	reg_ctrl_acr_en	reg_aac_exp_sel	reg_aac_out_off_en	aud_div_min	aac_mute_stat	_	reg_aac_all	reg_aac_en
0x21B6	0x00	RX_AEC_EN1[7:0]	reg_exp_en_7_0[7:0]							
0x21B7	0x00	RX_AEC_EN2[7:0]	reg_exp_en_15_8[7:0]							
0x21B8	0x00	RX_AEC_EN3[7:0]	reg_exp_en_23_16[7:0]							
0x21BA	0x34	RX_SYS_PSTOP[7:0]	reg_pclk_max[6:0]							reg_pstop_en
0x21F3	0x00	AAC_CSC_ERR[7:0]	–	–	–	reg_aac_csc_err[4:0]				
0x21F4	0x00	AAC_VSC_ERR[7:0]	–	–	–	–	reg_aac_vsc_err[3:0]			
0x21F5	0x00	AAC_ASC_ERR[7:0]	reg_aac_asc_err[7:0]							
0x21FB	0x00	AAC_EXP_CAPT_L[7:0]	reg_aac_exp_capt_7_0[7:0]							
0x21FC	0x00	AAC_EXP_CAPT_M[7:0]	reg_aac_exp_capt_15_8[7:0]							
0x21FD	0x00	AAC_EXP_CAPT_H[7:0]	reg_aac_exp_capt_23_16[7:0]							
0x21FE	0x00	ACRGCTRL0[7:0]	reg_acr_gen_ctrl0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
PWDREG										
0x2301	0x00	RX_PWD_CTRL[7:0]	RSVD	–	RSVD	reg_tmds_mode_inv	–	–	RSVD	RSVD
0x2304	0x00	RX_PWD_SRST3[7:0]	–	–	–	reg_tdm_srst	–	–	–	–
0x2305	0x00	RX_PWD_SRST[7:0]	RSVD	reg_acr_rst_auto	reg_aac_rst	reg_dc_fifo_rst	RSVD	reg_acr_rst	reg_fifo_rst	reg_aud_fifo_rst_auto
0x2306	0x00	RX_STATE_PWD[7:0]	–	–	–	–	–	vsync_cap	–	–
0x2307	0x03	RX_SYS_CTRL1[7:0]	–	–	–	–	–	–	reg_sync_pol	RSVD
0x230E	0x24	SYS_TMDS_CH_MAP[7:0]*	–	–	reg_di_ch2_sel[1:0]		reg_di_ch1_sel[1:0]		reg_di_ch0_sel[1:0]	
0x230F	0x00	SYS_TMDS_D_IR[7:0]*	–	reg_phy_di_dff_en	reg_di_ch2_invt	reg_di_ch1_invt	reg_di_ch0_invt	reg_di_ch2_bsi	reg_di_ch1_bsi	reg_di_ch0_bsi
0x2310	0x0F	RX_RPT_RDY_CTRL[7:0]	–	–	–	–	reg_hdmi_mode_clr_en	reg_fifordy_clr_en[2:0]		
0x2311	0x00	RX_PWD_SRST2[7:0]	RSVD	–	–	reg_dacr_rst	RSVD	RSVD	RSVD	RSVD
0x2322	0x04	RX_SW_HDMI_MODE[7:0]	–	–	–	–	–	RSVD	reg_hdmi_mode_sw_value	reg_hdmi_mode_overwrite
0x2323	0x06	RX_PREAMBLE_CRIT[7:0]	–	–	–	reg_preamble_cri[4:0]				
0x2325	0x00	RX_AUDP_FILT[7:0]	–	–	–	–	–	reg_byp_dvifilt	reg_byp_sync	reg_byp_dalign
0x2326	0x00	RX_AUDP_FIFO[7:0]	–	hdmi_fifo_diff[6:0]						
0x2328	0x00	VID_BLANK_DATA0[7:0]	ri_vid_blank_data_7_0[7:0]							
0x2329	0x00	VID_BLANK_DATA1[7:0]	ri_vid_blank_data_15_8[7:0]							
0x232A	0x00	VID_BLANK_DATA2[7:0]	ri_vid_blank_data_23_16[7:0]							
0x232B	0x00	VID_BLANK_DATA3[7:0]	ri_vid_blank_data_31_24[7:0]							
0x232C	0x00	VID_BLANK_DATA4[7:0]	–	–	–	–	ri_vid_blank_data_35_32[3:0]			
0x2340	0x00	RX_INTR1[7:0]	reg_intr1_stat7	reg_intr1_stat6	reg_intr1_stat5	reg_intr1_stat4	reg_intr1_stat3	reg_intr1_stat2	RSVD	RSVD
0x2341	0x00	RX_INTR2[7:0]	reg_intr2_stat7	reg_intr2_stat6	–	–	–	–	–	reg_intr2_stat0
0x2342	0x00	RX_INTR3[7:0]	–	–	reg_intr3_stat5	–	–	–	–	–
0x2343	0x00	RX_INTR4[7:0]	–	–	–	–	reg_intr4_stat3	reg_intr4_stat2	reg_intr4_stat1	reg_intr4_stat0

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0x2344	0x00	RX_INTR5[7:0]	reg_intr5_stat7	reg_intr5_stat6	–	–	–	–	–	reg_intr5_stat0
0x2345	0x00	RX_INTR6[7:0]	–	reg_intr6_stat6	reg_intr6_stat5	–	reg_intr6_stat3	–	–	–
0x2346	0x20	RX_INTR7[7:0]	–	–	reg_intr7_stat5	–	–	reg_intr7_stat2	–	reg_intr7_stat0
0x2347	0x00	RX_INTR8[7:0]	reg_intr8_stat7	–	–	–	–	–	–	–
0x2349	0x00	RX_INTR10[7:0]	–	–	–	–	–	–	–	reg_intr10_stat0
0x234C	0x00	RX_INTR13[7:0]	–	–	RSVD	reg_intr13_stat4	reg_intr13_stat3	reg_intr13_stat2	RSVD	reg_intr13_stat0
0x234D	0x00	RX_INTR14[7:0]	–	–	–	–	reg_intr14_stat3	reg_intr14_stat2	reg_intr14_stat1	reg_intr14_stat0
0x2350	0x00	RX_INTR1_MASK[7:0]*	reg_intr1_mask7	reg_intr1_mask6	reg_intr1_mask5	reg_intr1_mask4	reg_intr1_mask3	reg_intr1_mask2	reg_intr1_mask1	reg_intr1_mask0
0x2351	0x00	RX_INTR2_MASK[7:0]*	reg_intr2_mask7	reg_intr2_mask6	–	–	–	–	–	reg_intr2_mask0
0x2352	0x00	RX_INTR3_MASK[7:0]*	–	–	reg_intr3_mask5	–	–	–	–	–
0x2353	0x00	RX_INTR4_MASK[7:0]*	–	–	–	–	reg_intr4_mask3	reg_intr4_mask2	reg_intr4_mask1	reg_intr4_mask0
0x2354	0x00	RX_INTR5_MASK[7:0]*	reg_intr5_mask7	reg_intr5_mask6	–	–	–	–	–	reg_intr5_mask0
0x2355	0x00	RX_INTR6_MASK[7:0]*	–	reg_intr6_mask6	reg_intr6_mask5	–	reg_intr6_mask3	–	–	–
0x2356	0x00	RX_INTR7_MASK[7:0]*	–	–	reg_intr7_mask5	–	–	reg_intr7_mask2	–	reg_intr7_mask0
0x2357	0x00	RX_INTR8_MASK[7:0]*	reg_intr8_mask7	–	–	–	–	–	–	–
0x2359	0x00	RX_INTR10_MASK[7:0]*	–	–	–	–	–	–	–	reg_intr10_mask0
0x235B	0x00	RX_INTR12_MASK[7:0]*	–	reg_intr12_mask6	reg_intr12_mask5	reg_intr12_mask4	reg_intr12_mask3	reg_intr12_mask2	reg_intr12_mask1	reg_intr12_mask0
0x235C	0x00	RX_INTR13_MASK[7:0]*	–	–	reg_intr13_mask5	reg_intr13_mask4	reg_intr13_mask3	reg_intr13_mask2	reg_intr13_mask1	reg_intr13_mask0
0x235D	0x00	RX_INTR14_MASK[7:0]*	–	–	–	–	reg_intr14_mask3	reg_intr14_mask2	reg_intr14_mask1	reg_intr14_mask0
0x2360	0x00	DPLL_CH0_ERR_CNT1[7:0]	reg_dpll_ch0_err_cnt_7_0[7:0]							
0x2361	0x00	DPLL_CH0_ERR_CNT2[7:0]	reg_dpll_ch0_valid	reg_dpll_ch0_err_cnt_14_8[6:0]						
0x2362	0x00	DPLL_CH1_ERR_CNT1[7:0]	reg_dpll_ch1_err_cnt_7_0[7:0]							
0x2363	0x00	DPLL_CH1_ERR_CNT2[7:0]	reg_dpll_ch1_valid	reg_dpll_ch1_err_cnt_14_8[6:0]						

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0x2364	0x00	DPLL_CH2_ERR_CNT1[7:0]	reg_dpll_ch2_err_cnt_7_0[7:0]							
0x2365	0x00	DPLL_CH2_ERR_CNT2[7:0]	reg_dpll_ch2_valid	reg_dpll_ch2_err_cnt_14_8[6:0]						
0x2366	0x00	DPLL_SCDC_CTRL[7:0]	reg_dpll_scramble_stat	reg_dpll_ch_locked[2:0]			reg_dpll_clk_detected	–	–	reg_dpll_bypass_en
VIDPATH										
0x2A0C	0x00	vp_soft_reset[7:0]	–	–	–	–	–	reset_clk_out	reset_clk_core	reset_clk_in
0x2A14	0x00	vp_input_format_1[7:0]	cbcr_order	yc_demux_polarity	yc_demux_enable	ddr_mode[2:0]			ddr_polarity	ddr_enable
0x2A15	0x00	vp_input_format_2[7:0]	–	–	–	–	RSVD	RSVD	pixel_rate[1:0]	
0x2A80	0x00	vp_fdet_config[7:0]	–	–	–	–	RSVD	vsync_polarity_3	hsync_polarity_3	sync_polarity_force
0x2A81	0x00	vp_fdet_status[7:0]	–	–	–	–	RSVD	interlaced_	vsync_polarity_2	hsync_polarity_2
0x2A84	0x10	vp_fdet_frame_rate_delta_threshold_1[7:0]	vp_fdet_frame_rate_delta_threshold_1[7:0]							
0x2A85	0x00	vp_fdet_frame_rate_delta_threshold_2[7:0]	vp_fdet_frame_rate_delta_threshold_2[7:0]							
0x2A86	0x00	vp_fdet_frame_rate_delta_threshold_3[7:0]	vp_fdet_frame_rate_delta_threshold_3[7:0]							
0x2A88	0x00	vp_fdet_frame_rate_1[7:0]	vp_fdet_frame_rate_1[7:0]							
0x2A89	0x00	vp_fdet_frame_rate_2[7:0]	vp_fdet_frame_rate_2[7:0]							
0x2A8A	0x00	vp_fdet_frame_rate_3[7:0]	vp_fdet_frame_rate_3[7:0]							
0x2A8C	0x00	vp_fdet_pixel_count_1[7:0]	vp_fdet_pixel_count_1[7:0]							
0x2A8D	0x00	vp_fdet_pixel_count_2[7:0]	vp_fdet_pixel_count_2[7:0]							
0x2A8E	0x00	vp_fdet_line_count_1[7:0]	vp_fdet_line_count_1[7:0]							
0x2A8F	0x00	vp_fdet_line_count_2[7:0]	vp_fdet_line_count_2[7:0]							
0x2A90	0x00	vp_fdet_hsync_low_count_1[7:0]	vp_fdet_hsync_low_count_1[7:0]							
0x2A91	0x00	vp_fdet_hsync_low_count_2[7:0]	vp_fdet_hsync_low_count_2[7:0]							

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0x2A92	0x00	vp_fdet_hsync_high_count_1[7:0]	vp_fdet_hsync_high_count_1[7:0]							
0x2A93	0x00	vp_fdet_hsync_high_count_2[7:0]	vp_fdet_hsync_high_count_2[7:0]							
0x2A94	0x00	vp_fdet_hfront_count_1[7:0]	vp_fdet_hfront_count_1[7:0]							
0x2A95	0x00	vp_fdet_hfront_count_2[7:0]	vp_fdet_hfront_count_2[7:0]							
0x2A96	0x00	vp_fdet_hback_count_1[7:0]	vp_fdet_hback_count_1[7:0]							
0x2A97	0x00	vp_fdet_hback_count_2[7:0]	vp_fdet_hback_count_2[7:0]							
0x2A98	0x00	vp_fdet_vsync_low_count_even_1[7:0]	vp_fdet_vsync_low_count_even_1[7:0]							
0x2A99	0x00	vp_fdet_vsync_low_count_even_2[7:0]	vp_fdet_vsync_low_count_even_2[7:0]							
0x2A9A	0x00	vp_fdet_vsync_high_count_even_1[7:0]	vp_fdet_vsync_high_count_even_1[7:0]							
0x2A9B	0x00	vp_fdet_vsync_high_count_even_2[7:0]	vp_fdet_vsync_high_count_even_2[7:0]							
0x2A9C	0x00	vp_fdet_vfront_count_even_1[7:0]	vp_fdet_vfront_count_even_1[7:0]							
0x2A9D	0x00	vp_fdet_vfront_count_even_2[7:0]	vp_fdet_vfront_count_even_2[7:0]							
0x2A9E	0x00	vp_fdet_vback_count_even_1[7:0]	vp_fdet_vback_count_even_1[7:0]							
0x2A9F	0x00	vp_fdet_vback_count_even_2[7:0]	vp_fdet_vback_count_even_2[7:0]							
0x2AA0	0x00	vp_fdet_vsync_low_count_odd_1[7:0]	vp_fdet_vsync_low_count_odd_1[7:0]							
0x2AA1	0x00	vp_fdet_vsync_low_count_odd_2[7:0]	vp_fdet_vsync_low_count_odd_2[7:0]							
0x2AA2	0x00	vp_fdet_vsync_high_count_odd_1[7:0]	vp_fdet_vsync_high_count_odd_1[7:0]							
0x2AA3	0x00	vp_fdet_vsync_high_count_odd_2[7:0]	vp_fdet_vsync_high_count_odd_2[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x2AA4	0x00	vp_fdet_vfront_count_odd_1[7:0]	vp_fdet_vfront_count_odd_1[7:0]							
0x2AA5	0x00	vp_fdet_vfront_count_odd_2[7:0]	vp_fdet_vfront_count_odd_2[7:0]							
0x2AA6	0x00	vp_fdet_vback_count_odd_1[7:0]	vp_fdet_vback_count_odd_1[7:0]							
0x2AA7	0x00	vp_fdet_vback_count_odd_2[7:0]	vp_fdet_vback_count_odd_2[7:0]							
0x2AA8	0x00	vp_fdet_frame_count_1[7:0]	vp_fdet_frame_count_1[7:0]							
0x2AA9	0x00	vp_fdet_frame_count_2[7:0]	vp_fdet_frame_count_2[7:0]							
0x2AB0	0xFF	vp_fdet_irq_mask_1[7:0]	hsync_low_count	line_count	pixel_count	frame_rate	video656	interlaced	vsync_polarity	hsync_polarity
0x2AB1	0xFF	vp_fdet_irq_mask_2[7:0]	vsync_low_count_odd	vback_count_even	vfront_count_even	vsync_high_count_even	vsync_low_count_even	hback_count	hfront_count	hsync_high_count
0x2AB2	0x07	vp_fdet_irq_mask_3[7:0]	–	–	–	–	–	vback_count_odd	vfront_count_odd	vsync_high_count_odd
0x2AB4	0x00	vp_fdet_irq_status_1[7:0]	hsync_low_count	line_count	pixel_count	frame_rate	video656	interlaced	vsync_polarity	hsync_polarity
0x2AB5	0x00	vp_fdet_irq_status_2[7:0]	vsync_low_count_odd	vback_count_even	vfront_count_even	vsync_high_count_even	vsync_low_count_even	hback_count	hfront_count	hsync_high_count
0x2AB6	0x00	vp_fdet_irq_status_3[7:0]	–	–	–	–	–	vback_count_odd	vfront_count_odd	vsync_high_count_odd
DEPAK_REG										
0x2C20	0x00	RX_INT_IF_CTRL[7:0]	reg_use_aif4vsi	reg_new_vsi_only	reg_new_acp_only	reg_new_unrec_only	reg_new_mpeg_only	reg_new_aud_only	reg_new_spd_only	reg_new_avi_only
0x2C21	0x00	RX_INT_IF_CTRL2[7:0]	–	–	–	–	reg_new_acr_only	reg_new_gcp_only	reg_new_isrc2_only	reg_new_isrc1_only
0x2C22	0x00	DEC_AV_MUTE[7:0]	–	–	reg_clear_av_mute	–	–	–	–	reg_video_mute
0x2C27	0x00	RX_AUDP_STAT[7:0]	–	hdmi_hbra_on	hdmi_aud_dsd_on	hdmi_layout[1:0]		hdmi_mute	hdmi_mode_en	hdmi_mode_det
0x2C28	0x00	RX_AUTO_CLR_PKT1[7:0]	reg_autoclr_gcp_pkt	reg_autoclr_vsi_pkt	reg_autoclr_acp_pkt	reg_autoclr_unrec_pkt	reg_autoclr_mpeg_pkt	reg_autoclr_aif_pkt	reg_autoclr_spd_pkt	reg_autoclr_avi_pkt
0x2C29	0x00	RX_AUTO_CLR_PKT2[7:0]	–	–	–	–	reg_autoclr_acr_pkt	reg_autoclr_metadata_pkt	reg_autoclr_isrc2_pkt	reg_autoclr_isrc1_pkt

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0x2C30	0x00	RX_DEPACK_INTR0[7:0]	–	–	reg_intr0_stat5	reg_intr0_stat4	reg_intr0_stat3	RSVD	reg_intr0_stat1	reg_intr0_stat0
0x2C31	0x00	RX_DEPACK_INTR0_MASK[7:0]	–	–	reg_intr0_mask5	reg_intr0_mask4	reg_intr0_mask3	reg_intr0_mask2	reg_intr0_mask1	reg_intr0_mask0
0x2C32	0x00	RX_DEPACK_INTR1[7:0]	–	reg_intr1_stat6	reg_intr1_stat5	reg_intr1_stat4	reg_intr1_stat3	reg_intr1_stat2	–	reg_intr1_stat0
0x2C33	0x00	RX_DEPACK_INTR1_MASK[7:0]	–	reg_intr1_mask6	reg_intr1_mask5	reg_intr1_mask4	reg_intr1_mask3	reg_intr1_mask2	–	reg_intr1_mask0
0x2C34	0x00	RX_DEPACK_INTR2[7:0]	reg_intr2_stat7	reg_intr2_stat6	reg_intr2_stat5	reg_intr2_stat4	reg_intr2_stat3	reg_intr2_stat2	reg_intr2_stat1	reg_intr2_stat0
0x2C35	0x00	RX_DEPACK_INTR2_MASK[7:0]	reg_intr2_mask7	reg_intr2_mask6	reg_intr2_mask5	reg_intr2_mask4	reg_intr2_mask3	reg_intr2_mask2	reg_intr2_mask1	reg_intr2_mask0
0x2C36	0x00	RX_DEPACK_INTR3[7:0]	–	–	reg_intr3_stat5	reg_intr3_stat4	reg_intr3_stat3	reg_intr3_stat2	reg_intr3_stat1	reg_intr3_stat0
0x2C37	0x00	RX_DEPACK_INTR3_MASK[7:0]	–	–	reg_intr3_mask5	reg_intr3_mask4	reg_intr3_mask3	reg_intr3_mask2	reg_intr3_mask1	reg_intr3_mask0
0x2C38	0x00	RX_DEPACK_INTR4[7:0]	–	reg_intr4_stat6	reg_intr4_stat5	reg_intr4_stat4	reg_intr4_stat3	reg_intr4_stat2	reg_intr4_stat1	reg_intr4_stat0
0x2C39	0x00	RX_DEPACK_INTR4_MASK[7:0]	–	reg_intr4_mask6	reg_intr4_mask5	reg_intr4_mask4	reg_intr4_mask3	reg_intr4_mask2	reg_intr4_mask1	reg_intr4_mask0
0x2C3A	0x00	RX_DEPACK_INTR5[7:0]	reg_intr5_stat7	reg_intr5_stat6	reg_intr5_stat5	reg_intr5_stat4	reg_intr5_stat3	reg_intr5_stat2	reg_intr5_stat1	reg_intr5_stat0
0x2C3B	0x00	RX_DEPACK_INTR5_MASK[7:0]	reg_intr5_mask7	reg_intr5_mask6	reg_intr5_mask5	reg_intr5_mask4	reg_intr5_mask3	reg_intr5_mask2	reg_intr5_mask1	reg_intr5_mask0
0x2C3C	0x00	RX_DEPACK_INTR6[7:0]	–	–	–	reg_intr6_stat4	reg_intr6_stat3	reg_intr6_stat2	reg_intr6_stat1	reg_intr6_stat0
0x2C3D	0x00	RX_DEPACK_INTR6_MASK[7:0]	–	–	–	reg_intr6_mask4	reg_intr6_mask3	reg_intr6_mask2	reg_intr6_mask1	reg_intr6_mask0
REG_TOP										
0x3C04	0x00	SW_RST_REG0[7:0]	–	–	reg_osccal_srst	reg_otp_srst	reg_core_srst	reg_osc5m_srst	reg_osc_srst	reg_srst_full
0x3C10	0x09	INTR_CTRL[7:0]	–	–	–	–	reg_intr_level	reg_intr_stat	RSVD	RSVD
0x3C11	0x00	INTR_STAT0[7:0]	reg_rxdig_intr_mask	reg_rxz_intr_mask	reg_intr0_mask1	reg_intr0_mask0	–	–	reg_intr0_stat1	reg_intr0_stat0
0x3C20	0x03	OTP_CTRL1_REG[7:0]	reg_nvmi_locked	reg_ksv_rd_done	–	–	–	reg_ksv_rd_done_clr	reg_ld_ksv	reg_nvm_en
0x3C22	0x00	KSV_BYTE0[7:0]	reg_ksv0[7:0]							
0x3C23	0x00	KSV_BYTE1[7:0]	reg_ksv1[7:0]							

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0x3C24	0x00	KSV_BYTE2[7:0]	reg_ksv2[7:0]							
0x3C25	0x00	KSV_BYTE3[7:0]	reg_ksv3[7:0]							
0x3C26	0x00	KSV_BYTE4[7:0]	reg_ksv4[7:0]							
0x3C27	0x00	RCV_ID_BYTE0[7:0]	reg_rcv_id0[7:0]							
0x3C28	0x00	RCV_ID_BYTE1[7:0]	reg_rcv_id1[7:0]							
0x3C29	0x00	RCV_ID_BYTE2[7:0]	reg_rcv_id2[7:0]							
0x3C2A	0x00	RCV_ID_BYTE3[7:0]	reg_rcv_id3[7:0]							
0x3C2B	0x00	RCV_ID_BYTE4[7:0]	reg_rcv_id4[7:0]							
0x3C30	0x00	GP_CTRL0_REG[7:0]	reg_gp_ctrl0_7_0[7:0]							
REG_ANA										
0x3D05	0x2A	CH_ENABLE_REG[7:0]*	–	–	reg_ch2_en_ovr	reg_ch2_en	reg_ch1_en_ovr	reg_ch1_en	reg_ch0_en_ovr	reg_ch0_en
0x3D0A	0x18	TMDSR_CTL_REG[7:0]	–	–	–	reg_tmdsr_bp_dff[1:0]		reg_tmdsr_pmode_2	reg_tmdsr_pmode_1	reg_tmdsr_pmode_0
0x3D0C	0x61	CP_CTL1_REG[7:0]*	–	reg_cp_ctl[4:0]					reg_cp_ctl_com[1:0]	
0x3D0E	0x02	CDR_CTL1_REG[7:0]	reg_bp_cdr	reg_cdr_en_dloop[1:0]		reg_cdr_dylsb	reg_cdr_gaink2[1:0]		reg_cdr_gaink1[1:0]	
0x3D0F	0x00	EQOS_CTL0_REG[7:0]	reg_eqos_ctl_7_0[7:0]							
0x3D10	0x00	EQOS_CTL1_REG[7:0]	–	–	–	–	–	–	–	reg_eqos_ctl_8
0x3D12	0x80	CONFIG1_REG[7:0]	reg_bias_cfg[2:0]			reg_bias_pd	–	reg_cdr_idle_2	reg_cdr_idle_1	reg_cdr_idle_0
DPLLREG										
0x3E00	0x02	DPLL_CFG1[7:0]	reg_cfg_taps[1:0]		reg_cfg_reg_edon	reg_cfg_spce_en	reg_cfg_mode[1:0]		reg_cfg_bv_sel	reg_cfg_ev_sel
0x3E01	0xC4	DPLL_CFG2[7:0]	reg_cfg_stb_rsc[1:0]		reg_cfg_chan_sel[1:0]		reg_cfg_byp	reg_cfg_bs[2:0]		
0x3E04	0x38	EV_VAL_B[7:0]	reg_cfg_ev_i2c_b[7:0]							
0x3E05	0x38	EV_VAL_G[7:0]	reg_cfg_ev_i2c_g[7:0]							
0x3E06	0x38	EV_VAL_R[7:0]	reg_cfg_ev_i2c_r[7:0]							
0x3E08	0x58	PEQ_VAL0[7:0]	reg_cfg_peq_val0[7:0]							
0x3E09	0x78	PEQ_VAL1[7:0]	reg_cfg_peq_val1[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x3E0A	0x98	PEQ_VAL2[7:0]	reg_cfg_peq_val2[7:0]							
0x3E0B	0x79	PEQ_VAL3[7:0]	reg_cfg_peq_val3[7:0]							
0x3E0C	0x5E	PEQ_VAL4[7:0]	reg_cfg_peq_val4[7:0]							
0x3E0D	0xB8	PEQ_VAL5[7:0]	reg_cfg_peq_val5[7:0]							
0x3E0E	0x7E	PEQ_VAL6[7:0]	reg_cfg_peq_val6[7:0]							
0x3E0F	0x99	PEQ_VAL7[7:0]	reg_cfg_peq_val7[7:0]							
0x3E15	0x60	DPLL_CFG6[7:0]	reg_cfg_ri_swap	reg_cfg_ri_no_zone2x	reg_cfg_ri_bp_fix	reg_cfg_ri_use_scdt	reg_cfg_ri_ebyte_sel[2:0]			reg_cfg_ri_eeval
0x3E50	0x20	DPLL_HDMI2[7:0]	–	–	ri_hdmi2_scdt_on	ri_stat_and_on	ri_scramble_on_val	ri_scramble_on_ovr	ri_hdmi2_on_val	ri_hdmi2_on_ovr
0x3E5C	0x1D	NEW_DPLL_CFG[7:0]	–	ri_mhl12_scon	ri_two_tmds_sync	ri_eq_per_ch	ri_allow_msync	ri_enh_align_fifo	ri_tdd_mode	ri_red_lat
ZONEVCO_REG										
0x3E81	0x00	ZONE_STATUS_0[7:0]	ro_pll_lk	–	–	–	ro_szone[2:0]			ro_f1g
0x3E8D	0x00	PLL_MODE0[7:0]*	ri_hdmi_mhln_sel_ow	ri_hdmi_mhln_sel_ow_en	–	RSVD[1:0]		RSVD[1:0]		RSVD
0x3E94	0x00	ZONE_INTR[7:0]	–	–	RSVD	RSVD	reg_pll_lk	reg_lkdt_timeout	reg_vcocal_done	reg_zone_done
0x3E95	0x00	ZONE_INTR_MASK[7:0]	–	–	RSVD	RSVD	ri_mask3	ri_mask2	ri_mask1	ri_mask0

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address Default value is set by the ADD[2:0] pins as follows: ADD[2:0] Device Address 000 0b1000000 001 0b1000010 010 0b1000100 011 0b1100000 100 0b1100010 101 0b1100100 110 0b0100000 111 0b0100010	0b0000000: I2C write/read address is 0x00/0x01 0b0000001: I2C write/read address is 0x02/0x03 ... ... 0b1000000: I2C write/read address is 0x80/0x81 0b1000010: I2C write/read address is 0x84/0x85 0b1000100: I2C write/read address is 0x88/0x89 0b1100000: I2C write/read address is 0xC0/0xC1 0b1100010: I2C write/read address is 0xC4/0xC5 0b1100100: I2C write/read address is 0xC8/0xC9 0b0100000: I2C write/read address is 0x40/0x41 0b0100010: I2C write/read address is 0x44/0x45 ... ... 0b1111111: I2C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

REG1 (0x1)*

BIT	7	6	5	4	3	2	1	0
Field	HDMI_AUTOS	RSVD	IIC_2_EN	IIC_1_EN	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0b0	0x1	0x0	0x0	0x2		0b0	
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HDMI_AUTOS	7	Auto-start HDMI data receive	0b0: HDMI disabled 0b1: HDMI enabled
IIC_2_EN	5	Enable pass-through I2C Channel 2 (SDA2, SCL2)	0b0: I2C Channel 2 disabled 0b1: I2C Channel 2 enabled
IIC_1_EN	4	Enable pass-through I2C Channel 1 (SDA1, SCL1)	0b0: I2C Channel 1 disabled 0b1: I2C Channel 1 enabled
TX_RATE	3:2	Transmitter (forward channel) Bit Rate When changed, this setting becomes active after next link reset. Default value is set by the CXTP pin at power-up: 6Gbps when CXTP = 1 (coax cable) and 3Gbps when CXTP = 0 (twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved
RX_RATE	1:0	Receiver (Reverse Channel) Bit Rate When changed, this setting becomes active after the next link reset.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved

REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_RX_SRC	RSVD	DIS_LOCAL_CC	DIS_REM_CC	AUD_TX_EN_Y	AUD_TX_EN_X	RSVD	RSVD
Reset	0b0	0x1	0b0	0b0	0b0	0b1	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_RX_SRC	7	Select reverse channel port to receive audio	0b0: Reverse audio received on GMSL2A 0b1: Reverse audio received on GMSL2B
DIS_LOCAL_CC	5	Disable Control-Channel Connection to RX/SDA and TX/SCL Pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disable Remote Control-Channel Link over GMSL2 Connection	0b0: Remote control channel enabled 0b1: Remote control channel disabled
AUD_TX_EN_Y	3	Audio Transmit Enable for Port Y	0b0: Audio transmit Channel Y disabled 0b1: Audio transmit Channel Y enabled
AUD_TX_EN_X	2	Audio Transmit Enable for Port X	0b0: Audio transmit Channel X disabled 0b1: Audio transmit Channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RCLKEN	I2CSEL	UART_2_EN	UART_1_EN	RCLKSEL[1:0]	
Reset	0x0	–	0b0	0b0	0x0	0x0	0x0	
Access Type		–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCLKEN	5	Enable RCLK Output Bit is set by the RCLKEN pin at power-up.	0b0: RCLK output disabled 0b1: RCLK output enabled
I2CSEL	4	I^2C/UART Selection Bit is set according to the latched I2CSEL pin value at power-up.	0b0: UART selected 0b1: I^2C selected
UART_2_EN	3	Enable pass-through UART Channel 2 (RX2, TX2)	0b0: UART Channel 2 disabled 0b1: UART Channel 2 enabled
UART_1_EN	2	Enable pass-through UART Channel 1 (RX1, TX1)	0b0: UART Channel 1 disabled 0b1: UART Channel 1 enabled
RCLKSEL	1:0	RCLKOUT Clock Selection	0b00: XTAL/1 = 25MHz 0b01: XTAL/2 = 12.5MHz 0b10: XTAL/4 = 6.25MHz 0b11: Reserved

REG4 (0x4)*

BIT	7	6	5	4	3	2	1	0
Field	LF_1_M	LF_0_M	PU_LF1	PU_LF0	LF_1[1:0]		LF_0[1:0]	
Reset	0x0	0x0	0b0	0b1	0b10		0b10	
Access Type	Read Only	Read Only	Write, Read	Write, Read	Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1_M	7	Line-fault status of wire connected to SIOA+ pin (MSb)	0b0: Line-fault status contained in bitfield LF_1 0b1: Line-fault status is line-to-line short
LF_0_M	6	Line-fault status of wire connected to SIOA- pin (MSb)	0b0: Line-fault status contained in bitfield LF_0 0b1: Line-fault status is line-to-line short
PU_LF1	5	Enable line-fault monitoring of SIOA+	0b0: Line-fault monitor for SIOA+ disabled 0b1: Line-fault monitor for SIOA+ enabled
PU_LF0	4	Enable line-fault monitoring of SIOA-	0b0: Line-fault monitor for SIOA- disabled 0b1: Line-fault monitor for SIOA- enabled
LF_1	3:2	Line-fault status of SIOA+	0b00: Short-to-Battery 0b01: Short-to-GND 0b10: Normal 0b11: Line Open
LF_0	1:0	Line-fault status of SIOA-	0b00: Short-to-Battery 0b01: Short-to-GND 0b10: Normal 0b11: Line Open

REG5 (0x5)*

BIT	7	6	5	4	3	2	1	0
Field	LF_3_M	LF_2_M	PU_LF3	PU_LF2	LF_3[1:0]		LF_2[1:0]	
Reset	0x0	0x0	0b0	0b0	0b10		0b10	
Access Type	Read Only	Read Only	Write, Read	Write, Read	Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3_M	7	Line-fault status of SIOB+	0b0: Line-fault status contained in bitfield LF_3 0b1: Line-fault status is line-to-line short
LF_2_M	6	Line-fault status of SIOB-	0b0: Line-fault status contained in bitfield LF_2 0b1: Line-fault status is line-to-line short
PU_LF3	5	Enable line-fault monitoring of SIOB+	0b0: Line-fault monitor for SIOB+ disabled 0b1: Line-fault monitor for SIOB+ enabled
PU_LF2	4	Enable line-fault monitoring of SIOB-	0b0: Line-fault monitor for SIOB- disabled 0b1: Line-fault monitor for SIOB- enabled
LF_3	3:2	Line-fault status of SIOB+	0b00: Short-to-Battery 0b01: Short-to-GND 0b10: Normal 0b11: Line Open
LF_2	1:0	Line-fault status of SIOB-	0b00: Short-to-Battery 0b01: Short-to-GND 0b10: Normal 0b11: Line Open

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x83							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0x83: MAX96751

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x0			
Access Type					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SPEED_CPBL[1:0]		DV_CPBL_N	DUAL_CPBL_N	SPLTR_CPBL_N	RSVD
Reset	0x0	0x0	0x0		0x0	0x0	0x0	0x0
Access Type			Read Only		Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
SPEED_CPBL	5:4	Video Resolution Capability	0b00: No PCLK frequency limit 0b01: Reserved 0b10: Reserved 0b11: Reserved
DV_CPBL_N	3	Dual-View Video Splitting Capability	0b0: Dual-view video splitting is available 0b1: Dual-view video splitting is not available
DUAL_CPBL_N	2	Dual-Link Capability	0b0: Dual-link mode is available 0b1: Dual-link mode is not available
SPLTR_CPBL_N	1	Splitter Mode Capability	0b0: Splitter mode is available 0b1: Splitter mode is not available

IO_CHK1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_EN_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_EN_1	7:0	Enables individual pin output buffers and drives the value selected by PIN_DRV_SEL (0x3A) to that pin so that the driven value can be read from the PIN_IN_1 (0x3C) bitfield. This allows testing of IO buffer input and output paths. When the pin is driven by using this register, it should not be driven by any other strong driver externally.	0b0: Disable HSPD output buffer 0b1: Enable HSPD output buffer

IO_CHK2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_SEL	–	PIN_DRV_EN_2[5:0]					
Reset	0b0	–	0b000000					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_SEL	7	Select polarity for driving dedicated IOs When PIN_DRV_EN = 0, this bitfield is used to enable IO buffer receivers for DEDIO pins.	0b0: Drive low level 0b1: Drive high level
PIN_DRV_EN_2	5:0	Enables individual pin output buffers and drives the value selected by PIN_DRV_SEL (0x3A) to that pin so that the driven value can be read from the PIN_IN_2 (0x3D) bitfield. This allows testing of IO buffer input and output paths. When the pin is driven by using this register, it should not be driven by any other strong driver externally.	0bXXXXX0: Disable GMSL2 output buffer 0bXXXXX1: Enable GMSL2 output buffer 0bXXXX0X: Disable LOCK output buffer 0bXXXX1X: Enable LOCK output buffer 0bXXX0XX: Disable ERRB output buffer 0bXXX1XX: Enable ERRB output buffer 0bXX0XXX: Disable HPD output buffer 0bXX1XXX: Enable HPD output buffer 0bX0XXXX: Disable DDC_SCL output buffer 0bX1XXXX: Enable DDC_SCL output buffer 0b0XXXXX: Disable DDC_SDA output buffer 0b1XXXXX: Enable DDC_SDA output buffer

IO_CHK4 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	PIN_IN_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_IN_1	7:0	Pin Level Readback Each bit contains the level at the pin, either driven externally or by the PIN_DRV_SEL (0x3A) value if the equivalent bit is enabled in the PIN_DRV_EN_1 (0x39) bitfield.	[0]: REFCLK [1]: Reserved [2]: Reserved [3]: Reserved [4]: Reserved [5]: Reserved [6]: Reserved [7]: HSPD

IO_CHK5 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PIN_IN_2[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_IN_2	5:0	Pin Level Readback Each bit contains the level at the pin, either driven externally or by the PIN_DRV_SEL (0x3A) value if the equivalent bit is enabled in the PIN_DRV_EN_2 (0x3A) bitfield.	[0]: GMSL2 [1]: LOCK [2]: ERRB [3]: HPD [4]: DDC_SCL [5]: DDC_SDA

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Power manager switched 1V supply comparator status bits	0bXX1: Latched high when V_{DD_sw} < 0.82V 0bX1X: Latched high when V_{DD_sw} < 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	Power manager comparator status bits	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when V_{DD_sw} < 0.802V 0bX0XXX: Reserved 0b0XXXX: Reserved

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	RSVD	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b1	0xA			
Access Type		Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable Wake-Up by Local µC from SDA_RX Pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_A	4	Enable Wake-Up by Remote Chip Connected to Link- A	0b0: Link-A remote wake-up disabled 0b1: Link-A remote wake-up enabled

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	–	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing 1 to this bit resets the device, including all blocks and registers. This is equivalent to toggling the PWDNB pin. This bit is cleared when written.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Reset entire data path (keep register settings) Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	Reset entire data path (keep register settings) in one shot Write 1 to activate reset. Bit automatically clears and releases reset.	0b0: No action 0b1: Reset data path
AUTO_LINK	4	Automatically selects which link to enable (A or B) Dual-link and Splitter modes are not automatic. For Dual-link mode, set LINK_CFG = 00. For Splitter mode, set LINK_CFG = 11.	0b0: Disable automatic link configuration 0b1: Enable automatic link configuration
SLEEP	3	Enable Sleep mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
LINK_CFG	1:0	AUTO_LINK and this bitfield select the link configuration per the decode table	0b00: If AUTO_LINK = 0, Dual-link is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b01: If AUTO_LINK = 0, Link-A is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b10: If AUTO_LINK = 0, Link-B is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b11: Splitter mode

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	CXTP_B	RSVD	RSVD	RSVD	CXTP_A
Reset	–	–	0b1	0b0	0x0	0x0	0b1	0b0
Access Type	–	–		Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	4	Coax/Twisted-Pair Cable Select for Link-B Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link-A Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	0b0	0b01		0b0	0b0	0b0	–
Access Type			Read Only		Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_MODE	5:4	Active Link mode	0b00: Dual link 0b01: Link-A 0b10: Link-B 0b11: Splitter mode
LOCKED	3	GMSL2 Link Locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) Locked	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0x1	0x0	0x1	–	0b0	0b000		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22), DEC_ERR_B (0x23), and IDLE_ERR (0x24) registers after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and Idle-Error Reporting Threshold DEC_ERR_FLAG_A (0x1B) is asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR. DEC_ERR_FLAG_B (0x1B) is asserted when DEC_ERR_B (0x23) ≥ DEC_ERR_THR. IDLE_ERR_FLAG (0x1B) is asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128

INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT bitfield (0x25).	0xX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically reset PKT_CNT bitfield (0x25) after ERRB pin is asserted for 1µs	0b0: Automatic reset disabled 0b1: Automatic enabled
PKT_CNT_THR	2:0	Packet Count Reporting Threshold (see PKT_CNT description) PKT_CNT_FLAG is asserted when PKT_CNT ≥ PKT_CNT_THR	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128

INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	HDMI_INT_OEN	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b1
Access Type			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enable reporting of remote-error status (REM_ERR - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
HDMI_INT_OEN	4	Enable reporting of HDMI interrupt (HDMI_INT - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_OEN	3	Enable reporting of line-fault interrupt (LFLT_INT - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enable reporting of idle-word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enable reporting of decoding errors (DEC_ERR_FLAG_B - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enable reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	HDMI_INT	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type			Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote side error status (inverse of remote side ERRB pin level)	0b0: No remote side error 0b1: Remote side error
HDMI_INT	4	HDMI Receiver Interrupt	0b0: No HDMI receiver interrupt 0b1: HDMI receiver interrupt
LFLT_INT	3	Line-Fault Interrupt Asserted when either line-fault monitor indicates a fault status. See LF_0 (0x04) and LF_1 (0x04) bitfields for more information.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle-Word Error Flag Asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link-B Asserted when DEC_ERR_B (0x23) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error Flag for Link-A Asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	MEM_INT_ERR_OEN	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b1
Access Type			Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_INT_ERR_OEN	5	Enable reporting of memory error status (MEM_INT_ERR_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Reserved	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
WM_ERR_OEN	0	Enable reporting of watermark errors (WM_ERR_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	MEM_INT_ERR_FLAG	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type			Read Only		Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_INT_ERR_FLAG	5	Memory Error Status	0b0: No memory CRC error 0b1: Memory CRC error
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag, asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ Retransmission Event Flag Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag Asserted when PKT_CNT (0x25) ≥ PKT_CNT_THR (0x19).	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark Error Flag Asserted when a watermark error is detected.	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VDDCMP_INT_OEN	RSVD	APRBS_ERR_OEN	VDDBAD_INT_OEN
Reset	–	–	–	–	0x1	0x1	0b1	0x1
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	3	Enable reporting of V_{DDBAD} interrupt (VDDCMP_INT_FLAG) at ERRB pin	0x0: Disable reporting 0x1: Enable reporting
APRBS_ERR_OEN	1	Enable reporting of audio PRBS errors (APRBS_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_INT_OEN	0	Enable reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG - 0x1F) at ERRB pin	0x0: Disable reporting 0x1: Enable reporting

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD	VDDCMP_INT_FLAG	RSVD	APRBS_ERR_FLAG	VDDBAD_INT_FLAG
Reset	0x3		0x0	0x0	0b0	0b0	0b0	0b0
Access Type					Read Clears All		Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	3	V_{DDCMP} Interrupt Flag	0b0: Flag not asserted 0b1: Flag asserted
APRBS_ERR_FLAG	1	Audio PRBS Error Flag Asserted when APRBS_ERR (0x143) > 0.	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	0	Combined V_{DDBAD} Indicator	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b0	–	–	0b11111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b0	0b1	–	0b11111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receive remote error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected at Link-A Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link-A decoding errors detected

CNT1 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	Number of decoding (disparity) errors detected at Link-B Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link-B decoding errors detected

CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle-word errors detected Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type Packet type is selected with PKT_CNT_SEL (0x2C). Reported packet count is a scaled value, such that actual packet count is greater than or equal to PKT_CNT x ($2^{PKT\_CNT\_EXP}$) and less than (PKT_CNT + 1) x ($2^{PKT\_CNT\_EXP}$). When the maximum value is reported, packet count is greater than or equal to the reported value.	0xXX: Scaled number of received packets

TX1 (0x29)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
Reset	0x0	–	0b0	0b0	–	–	0x0	0x0
Access Type	Write, Read	–	Write, Read	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enable Link PRBS-7 Generator	0b0: Link PRBS generator disabled 0b1: Link PRBS generator enabled
ERRG_EN_B	5	Error Generator Enable for Link-B	0b0: Link-B error generator disabled 0b1: Link-B error generator enabled
ERRG_EN_A	4	Error Generator Enable for Link-A	0b0: Link A error generator disabled 0b1: Link A error generator enabled

TX2 (0x2A)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error-Generator Average Bit-Error Rate	0b00: One error in 5120 bits 0b01: One error in 81920 bits 0b10: One error in 1310720 bits 0b11: One error in 20971520 bits

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_BURST	3:1	Error-Generator Burst-Error Length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error-Generator Error-Distribution Selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x2B)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0b100		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. The timeout base is set by the reverse channel link rate (RX_RATE) as follows: When 12Gbps link is used, values 6 and 7 are reserved. RX_RATE Timeout Base 187.5Mbps 8µs	0b000: 0.5 x timeout base 0b001: 1.0 x timeout base 0b010: 1.5 x timeout base 0b011: 2.0 x timeout base 0b100: 2.5 x timeout base 0b101: 3.0 x timeout base 0b110: 3.5 x timeout base 0b111: 4.0 x timeout base

RX0 (0x2C)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0x0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the subtype of low-bandwidth (LBW) packets to count at PKT_CNT (0x5) bitfields	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT (0x25) bitfield	0x0: None 0x1: VIDEO 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

GPIOA (0x30)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0x0	0b1	0b000001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO Fast-Direction Switch for Bidirectional IO	0b0: Fast-direction switch disabled 0b1: Fast-direction switch enabled
GPIO_FWD_CDLY	5:0	Compensation Delay Multiplier for the Forward Direction This must be the same value as GPIO_FWD_CDLY (0x31) of the chip on the other side of the link. Total delay is (value + 1) x 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x8					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet This allows grouping transitions of different GPIO inputs in a single packet, which increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation Delay Multiplier for the Reverse Direction This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C Subordinate-Setup and Hold-Time Setting Configures the interval between SDA and SCL transitions when driven by the internal I^2C subordinate. Set this according to the I^2C Speed mode.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C Standard-mode speed 0b11: Reserved
SLV_TO	2:0	I^2C-to-I^2C Subordinate Timeout setting Internal GMSL2 I^2C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0x0	0x5			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C Main Bit-Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). Set this according to the I²C Speed mode.	0b000: 9.92Kbps: Set for I²C Standard-mode speed 0b001: 33.2Kbps: Set for I²C Standard-mode speed 0b010: 99.2Kbps: Set for I²C Standard- or Fast-mode speed 0b011: 123Kbps: Set for I²C Fast-mode speed 0b100: 203Kbps: Set for I²C Fast-mode speed 0b101: 397Kbps: Set for I²C Fast- or Fast-mode Plus speed 0b110: 625Kbps: Set for I²C Fast-mode Plus speed 0b111: 980Kbps: Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0b0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I²C Address Translator Source A When I²C device address matches I²C SRC_A, internal I²C main (on remote side) replaces the device address by I²C DST_A (0x43).	0bXXXXXXX: Value of I²C SRC_A

I2C_3 (0x43)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I²C Address Translator Destination A See the description of I²C SRC_A (0x42).	0bXXXXXXX: Value of I²C DST_A

I2C_4 (0x44)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I²C Address Translator Source B When I²C device address matches I²C SRC_B, internal I²C main (on remote side) replaces the device address by I²C DST_B (0x45).	0bXXXXXXX: Value of I²C SRC_B

I2C_5 (0x45)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I²C Address Translator Destination B See the description of I²C SRC_B (0x44).	0bXXXXXXX: Value of I²C DST_B

I2C_6 (0x46)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_AUTO_CFG	I2C_SRC_CNT[2:0]		
Reset	–	–	–	–	0x1	0b0		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_AUTO_CFG	3	When this bit is set to 1, I²C-to-I²C number of links is automatically determined based on splitter mode. In Splitter mode, response from two I²C channels are expected; otherwise, response from one I²C channel is expected.	0b0: Number of I²C-to-I²C links set by I²C SRC_CNT[2:0] bits 0b1: Splitter mode automatically determines the number of I²C-to-I²C links
I2C_SRC_CNT	2:0	I²C-to-I²C number of links (valid when I2C_AUTO_SRC = 0). Set this field to N - 1 when expecting I²C response from N remote I²C transmitters (usually the same as the number of remote devices connected to this device).	0b000: One deserializer connected 0b001: Two deserializers connected 0b010: Reserved 0b011: Reserved 0b100: Reserved 0b101: Reserved 0b110: Reserved 0b111: Reserved

I2C_7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
Reset	0x0	0x0	–	–	–	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_RX_OVERFLOW	7	UART Rx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW	6	UART Tx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
I2C_TIMED_OUT	2	Internal I^2C-to-I^2C subordinate or main has timed out while receiving packet from remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED	1	Inverse of the I^2C acknowledge bit received from remote side	0x0: I^2C acknowledge bit received as 1 0x1: I^2C acknowledge bit received as 0
REM_ACK_RECVED	0	I^2C acknowledge bit for any I^2C byte has been received from the remote side for the previous I^2C packet.	0b0: I^2C acknowledge bit not received 0b1: I^2C acknowledge bit received

UART_0 (0x48)*

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0x1		0x0	0x0	0x0	0x1		0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN	7:6	UART Rx Source Arbitration Timeout Duration UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it selects the next UART source according to the source ID of the next following received packet.	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
REM_MS_EN	5	Enable UART Bypass Mode Control by Remote GPIO Pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, the chip is in Bypass mode; otherwise, the chip is in Base mode.	0b0: UART Bypass mode not controlled by remote MS pin 0b1: UART Bypass mode controlled by remote MS pin

BITFIELD	BITS	DESCRIPTION	DECODE
LOC_MS_EN	4	Enable UART Bypass Mode Control by Local GPIO Pin Set to use GPIO2 pin as MS pin (UART mode select). When MS is high, the chip is in Bypass mode; otherwise, the chip is in Base mode.	0b0: UART Bypass mode not controlled by local MS pin 0b1: UART Bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in Bypass mode	0b0: Receive and send parity bit in Bypass mode 0b1: Do not receive and send parity bit in Bypass mode
BYPASS_TO	2:1	UART Soft Bypass Timeout Duration When set to 11, BYPASS_EN is never cleared, so the device stays in Bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN	0	Enable UART Soft-Bypass Mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO register), device exits Bypass mode, and the bit is automatically cleared.	0b0: UART soft Bypass mode disabled 0b1: UART soft Bypass mode enabled

UART_1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length in terms of internal 150MHz clock (lower 8 bits)	0xXX: UART detected bit length (lower 8 bits)

UART_2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY	7:6	UART Initial Output Delay In Base mode, the first received UART byte of a packet (sync or acknowledge frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back to back on remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB	5:0	UART detected bit length in terms of internal 150MHz clock (upper 6 bits)	0bXXXXXX: UART detected bit length (upper 6 bits)

I2C_PT_0 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-through I²C-to-I²C subordinate setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C Speed mode: Fast-mode Plus = 00 Fast-mode = 01 Standard-mode = 10	0x0: Setup = 45, Hold = 1 0x1: Setup = 60, Hold = 8 0x2: Setup = 120, Hold = 16 0x3: Setup = 180, Hold = 32
SLV_TO_PT	2:0	Pass-through I²C-to-I²C subordinate timeout setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0x0: 16µs 0x1: 1024µs 0x2: 2048µs 0x3: 4096µs 0x4: 8192µs 0x5: 16384µs 0x6: 32768µs 0x7: 0 (no timeout)

I2C_PT_2 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Write, Read	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
XOVER_EN_2	7	Connect pass-through I²C/UART Channel 2 to primary control channel on the remote side	0x0: Do not connect 0x1: Connect
I2C_TIMED_OUT_2	6	In pass-through I²C Channel 2, internal I²C-to-I²C subordinate or main has timed out while receiving a packet from the remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_2	5	In pass-through I²C Channel 2, inverse of the I²C acknowledge bit received from the remote side	0x0: I²C acknowledge bit received as 1 0x1: Inverse I²C acknowledge bit received as 0
REM_ACK_RECVED_2	4	In pass-through I²C Channel 2, I²C acknowledge bit for any I²C byte is received from the remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received
XOVER_EN_1	3	Connect pass-through I²C/UART Channel 1 to primary control channel on the remote side	0x0: Do not connect 0x1: Connect

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT_1	2	In pass-through I²C Channel 1, internal I²C-to-I²C subordinate or main has timed out while receiving a packet from the remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_1	1	In pass-through I²C Channel 1, inverse of the I²C acknowledge bit received from the remote side	0x0: I²C acknowledge bit received as 1 0x1: I²C acknowledge bit received as 0
REM_ACK_RECVED_1	0	In pass-through I²C Channel 1, I²C acknowledge bit for any I²C byte is received from the remote side for the previous I²C packet	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_PT_0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Read Clears All	Read Clears All	Write, Read	Write, Read	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Selects whether or not to use custom UART bit rate (BITLEN_PT_1 bitfield) in pass-through UART Channel 2	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disable or enable parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_2	5	Pass-through UART Rx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW_2	4	Pass-through UART Tx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
BITLEN_MAN_CFG_1	3	Selects whether or not to use custom UART bit rate (BITLEN_PT_1 bitfield) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disable or enable parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_1	1	Pass-through UART Rx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW_1	0	Pass-through UART Tx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred

TX0 (0x50)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x0	–	0x3		0x0		0x0	
Access Type	Write, Read	–			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmit CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TX1 (0x51)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TX3 (0x53)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
Reset	–	–	0x0	0x1	–	–	0x0	
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

TX0 (0x54)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x0	–	0x3		0x0		0x0	
Access Type	Write, Read	–			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmit CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TX1 (0x55)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TX3 (0x57)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
Reset	–	–	0x1	0x0	–	–	0x1	
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

TR0 (0x60)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x61)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x63)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x0	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSBs are set by ADD2 and ADD1. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x64)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received … … 0xFF: Packets from all source IDs received

ARQ0 (0x65)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on Splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for 1 acknowledge packet 0b1: Wait for 2 acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Select what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x66)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit. ARQ will stop retransmitting after this many retransmission attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmit limit not reached 0b1: Maximum retransmit limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x68)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, this bit indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x69)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x6B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x0	–	0x1		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSBs are set by ADD2 and ADD1. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x6C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x6D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x0	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on Splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Select what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x6E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit. ARQ will stop retransmitting after this many retransmission attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x70)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, this bit indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x71)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x73)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSBs are set by ADD2 and ADD1. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x74)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x78, 0x88, 0xA0, 0xA8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, this bit indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x79, 0x89, 0xA1, 0xA9)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x7B, 0x8B, 0xA3, 0xAB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSBs are set by ADD2 and ADD1. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x7C, 0x8C, 0xA4, 0xAC)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x7D, 0x8D, 0xA5, 0xAD)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on Splitter mode	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets

BITFIELD	BITS	DESCRIPTION	DECODE
MATCH_SRC_ID	5	Acknowledge packet source ID checking method The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID bitfield
ACK_SRC_ID	4	Select what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID bitfield
ARQ_EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x7E, 0x8E, 0xA6, 0xAE)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit. ARQ will stop retransmitting after this many retransmission attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x7F, 0x8F, 0xA7, 0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x80)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, this bit indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x81)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x83)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In Splitter mode: When 0, packets from this port are NOT transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in Splitter mode 0b1: Packets are transmitted over GMSLB in Splitter mode
TX_SPLT_MASK_A	4	In Splitter mode: When 0, packets from this port are NOT transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in Splitter mode 0b1: Packets are transmitted over GMSLA in Splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSBs are set by ADD2 and ADD1. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x84)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x85)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on Splitter mode	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for 1 ACK 0b1: Wait for 2 ACK's

BITFIELD	BITS	DESCRIPTION	DECODE
MATCH_SRC_ID	5	Acknowledge packet source ID checking method The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID bitfield
ACK_SRC_ID	4	Select what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID bitfield
ARQ_EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x86)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit. ARQ will stop retransmitting after this many retransmission attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

VIDEO_TX0 (0x100, 0x110)*

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	RSVD	RSVD[1:0]	
Reset	0x0	0x1	0x2		–	0x0	0x0	
Access Type	Write, Read	Write, Read	Write, Read		–			

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_SEL	7	Line CRC checksum generation with DE or HS	0b0: Use DE for line CRC 0b1: Use HS for line CRC
LINE_CRC_EN	6	Line CRC Enable Generate a CRC code for the video line and send it to the receiver side for comparison.	0b0: Line CRC disabled 0b1: Line CRC enabled
ENC_MODE	5:4	HS, VS, DE Encoding mode	0b00: HS, VS, DE encoding off 0b01: HS, VS, DE encoding on, color bits always sent 0b10: HS, VS, DE encoding on, color bits sent only when DE is high 0b11: HS, VS, DE encoding on, color bits sent only when HS is high

VIDEO_TX1 (0x101, 0x111)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		BPP[5:0]					
Reset	0x1		0x18					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BPP	5:0	Color bits per pixel (RGB888 = 24)	0bXXXXXX: Number of bits per pixel

VIDEO_TX2 (0x102, 0x112)*

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
Reset	0x0	0x0	0x0	0x0	0x1	0x0	0x1	0x0
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET	7	PCLK detected	0b0: Video transmit PCLK not detected 0b1: Video transmit PCLK detected
DRIFT_ERR	6	VID_TX PCLK drift error detected. After the video pipeline starts, PCLK drift cannot exceed the given threshold without restarting the sub-system.	0b0: Video transmit PCLK drift error not detected 0b1: Video transmit PCLK drift error detected

BITFIELD	BITS	DESCRIPTION	DECODE
OVERFLOW	5	VID_TX FIFO has overflowed. Video input throughput may be too high, or bandwidth allocation on GMSL2 link for video may be insufficient.	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN	4	VID_TX FIFO is more than half full. Video data coming from the HDMI receiver is read by the scheduler.	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full
LIM_HEART	2	Disable heartbeat during blanking. Use this bit in conjunction with SEQ_MISS_EN and DIS_PKT_DET registers in the deserializer.	0x0: Enable heartbeat 0x1: Disable heartbeat

VIDEO_TX4 (0x104, 0x114)

BIT	7	6	5	4	3	2	1	0
Field	DAMP_MODE	DAMP_EN	RSVD[5:0]					
Reset	0x0	0x1	0x0					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
DAMP_MODE	7	Select damping count for heartbeat packets
DAMP_EN	6	Enable damping for heartbeat packets

VIDEO_TX5 (0x105, 0x115)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HEART_TYPE	RSVD[5:0]					
Reset	0x0	0x0	0x0					
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
HEART_TYPE	6	Enable use of higher efficiency heartbeat packet

VIDEO_TX6 (0x106, 0x116)

BIT	7	6	5	4	3	2	1	0
Field	–	MASK_VIDEO_DE	RSVD[5:0]					
Reset	–	0x0	0x00					
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_VIDEO_DE	6	Mask video with DE	0x0: Do not mask video with DE 0x1: Mask video with DE

AUDIO_TX0 (0x120, 0x130)*

BIT	7	6	5	4	3	2	1	0
Field	I2S_TDM_CFG[1:0]		I2S_CFG[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
Reset	0x2		0x3		0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2S_TDM_CFG	7:6	Audio format configuration (HDMI audio only)	0b00: Force stereo 0b01: Force TDM 0b10: Auto select stereo or TDM 0b11: Reserved
I2S_CFG	5:4	Audio channel configuration	0b00: Use HDMI as audio source 0b01: Reserved 0b10: Reserved 0b11: Use local I^2S input pins as audio source
INV_SCK	3	Invert SCK (when using local I^2S interface)	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Invert WS (when using local I^2S interface)	0b0: Do not invert WS 0b1: Invert WS
FORCE_AUD	1	Force audio data to zero	0b0: Normal audio data 0b1: Audio data forced to zero
AUD_SINK_SRC	0	Sink-sourced mode enable for audio Tx (for use on the deserializer side when forward audio clock is the main)	0b0: Transmit audio in Normal mode 0b1: Transmit audio in Sink-sourced mode

AUDIO_TX1 (0x121, 0x131)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	I2S_HDR_CFG[1:0]	
Reset	0x1		0x0		0x1	0x1	0x2	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_PRIO	7:6	Scheduler audio priority	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3
AUD_STR_TX	5:4	Audio stream ID	0b00: Use Stream ID 0 0b01: Use Stream ID 1 0b10: Use Stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Audio clock drift detection enable. Resets sub-system on SCK frequency drift and reports event.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Audio periodic info frame transmission enable	0b0: Audio periodic info frame transmission disabled 0b1: Audio periodic info frame transmission enabled

BITFIELD	BITS	DESCRIPTION	DECODE
I2S_HDR_CFG	1:0	Audio header configuration (only applicable for TDM audio) (HDMI audio only)	0b00: Use audio info received on HDMI link 0b01: Use header programmed to register 0b10: No header 0b11: Reserved

AUDIO_TX2 (0x122, 0x132)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_HDR_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_HDR_L	7:0	First byte of audio header data (HDMI audio only)	0xX: Lower byte of audio header data

AUDIO_TX3 (0x123, 0x133)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_HDR_M[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_HDR_M	7:0	Second byte of audio header data (HDMI audio only)	0xX: Middle byte of audio header data

AUDIO_TX4 (0x124, 0x134)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_HDR_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_HDR_H	7:0	Third byte of audio header data (HDMI audio only)	0xX: Upper byte of audio header data

AUDIO_TX5 (0x125, 0x135)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	AUD_ODIV_H[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Audio clock frequency drift detected	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Audio FIFO is more than half full	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Audio buffer overflow detected	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio clock detected	0b0: Audio clock not detected 0b1: Audio clock detected
AUD_ODIV_H	3:0	Audio PLL estimated output divider value	0bXXXX: Audio PLL estimated output divider value

AUDIO_TX7 (0x127, 0x137)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Reset	0x0	0x0	0x0					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection (program to 0 in Sink-sourced mode)	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Audio PRBS enable	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x128, 0x138)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Reset	0x0	0x1	0x0					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Audio PRBS WS generation enable	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

AUDIO_RX1 (0x140)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
Reset	0x0	0x0	0x1	0x0	0x0	0x0	–	0x1
Access Type	Write, Read				Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_RX_SINK_SRC	7	Sink-sourced mode enable for audio Rx (for use on the serializer side)	0b0: Received audio in Normal mode 0b1: Received audio in Sink-sourced mode
INV_SCK_RX	3	Invert SCK at I^2S output	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS_RX	2	Invert WS at I^2S output	0b0: Do not invert WS 0b1: Invert WS
AUD_EN_RX	0	Audio receiver adapter enable	0b0: Audio receiver disabled 0b1: Audio receiver enabled

AUDIO_RX4 (0x143)

BIT	7	6	5	4	3	2	1	0
Field	APRBS_ERR[7:0]							
Reset	0x0							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_ERR	7:0	Audio PRBS error counter, clears on read	0xXX: Number of audio PRBS errors

AUDIO_RX7 (0x146)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
Reset	0x0			0x0	0x0		0x1	0x0
Access Type				Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_CHK_EN	4	Enable audio PRBS checker	0b0: Audio PRBS checker disabled 0b1: Audio PRBS checker enabled
AUD_STRM	3:2	Selected audio stream for reception	0b00: Receive Stream ID 0 0b01: Receive Stream ID 1 0b10: Receive Stream ID 2 0b11: Receive Stream ID 3

AUDIO_RX9 (0x148)

BIT	7	6	5	4	3	2	1	0
Field	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Read Clears All	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_BLK_LEN_ERR	7	Audio Rx block length error detected	0b0: Received audio block length error not detected 0b1: Received audio block length error detected

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_LOCK	6	Audio pipeline frequency locked	0b0: Audio pipeline frequency is not locked 0b1: Audio pipeline frequency is locked
AUD_PKT_DET	5	Audio Rx: Sufficient packet throughput detected	0b0: Valid audio stream not detected 0b1: Valid audio stream detected
APRBS_VALID	4	Audio PRBS is running	0b0: Audio PRBS is not running 0b1: Audio PRBS is running

INFO_RX4 (0x14D)

BIT	7	6	5	4	3	2	1	0
Field	–	INFO_AUD_DEPTH[6:0]						
Reset	–	0x0						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
INFO_AUD_DEPTH	6:0	Received audio depth value from info frames

SPI_0 (0x160)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Program to local ID if filtering packets based on header ID.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNR_ID	3	Selects whether SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enable control channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects whether SPI is main or subordinate	0b0: SPI subordinate 0b1: SPI main
SPI_EN	0	Enable SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x161)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0x7						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value greater than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... ... 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 request priority advances by one (capacity permitting) if Tx buffer is over half full.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3

SPI_2 (0x162)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Hold off GMSL2 request until this number of extra bytes is received on SPI port	0b00: No extra bytes 0b01: One extra byte 0b10: Two extra bytes 0b11: Three extra bytes
FULL_SCK_SETUP	4	Sample MISO after half or full SCK period.	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a main.	0b0: Subordinate select 2 is active low 0b1: Subordinate select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a main.	0b0: Subordinate select 1 is active low 0b1: Subordinate select 1 is active high

SPI_3 (0x163)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between each of the following: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

SPI_4 (0x164)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x165)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x166)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available	0b0: Buffer empty 0b1: Buffer not empty

BITFIELD	BITS	DESCRIPTION	DECODE
SPIS_RWN	4	Alternate GPU control register to use for Rd/ WrN control if GPIO is not available	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enable GPIO for use as subordinate select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enable GPIO for use as subordinate select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enable GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enable GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x167)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0x0	0x0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx Buffer Overflow Flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx Buffer Overflow Flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI_8 (0x168)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100ns increments) for GMSL2 request hold off (0 is disable)	0xXX: Number of 100ns delay increments for GMSL2 request hold off

WM_0 (0x188)*

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0x0	0x0			0x0		–	0x0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: 32-bit 0b1: 64-bit
WM_MODE	6:4	Watermark Mode	0b000: Default Generator mode - cycle through all four watermarks in video stream (default) 0b001: Error Generator mode - cycle through only two watermarks to replicate a frozen frame error condition 0b010: Reserved 0b011: Reserved 0b100: Reserved 0b101: Reserved 0b110: Reserved 0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

WM_2 (0x18A)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0x5			0x0	0x0	0x0	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS polarity (only effective for watermark block)	0b0: Noninverting 0x1: Invert
VsyncPol	2	VS polarity (only effective for watermark block)	0b0: Noninverting 0x1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count	0bXX: Phase accumulator terminal count

WM_3 (0x18B)*

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x14						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched filter threshold	0bXXXXXXX: Matched Filter Threshold

WM_4 (0x18C)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
Reset	–	–	0x1		0x0	–	0x0	
Access Type	–	–				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_MASKMODE	1:0	Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x18D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DETOUT	1	Live frame-based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM_6 (0x18E)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time (in 2ms steps) the frozen frame condition must be observed before an error is generated. 0 = No filter	0xXX: Number of milliseconds

DV0 (0x1A0)*

BIT	7	6	5	4	3	2	1	0
Field	DV_LOCK	DV_SWP_AB	LINE_ALT	RSVD	RSVD	DV_CONV	DV_SPL	DV_EN
Reset	0x0	0x0	0x0	0x0	0x0	0x1	0x0	0x0
Access Type	Read Only	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DV_LOCK	7	Dual-view pixel per line count stable, processor can start	0b0: Not locked 0b1: Locked
DV_SWP_AB	6	Swap video data going to video transmit pipelines	0b0: Normal video split between SIOA and SIOB 0b1: Swaps video split between SIOA and SIOB
LINE_ALT	5	Enable Line Alternating mode	0b0: Line Alternating mode disabled 0b1: Line Alternating mode enabled
DV_CONV	2	Dual-view conversion. When enabled, side-by-side input is converted to pixel interleaved.	0b0: Bypass 0b1: Convert
DV_SPL	1	Enables Dual-view Split mode	0b0: Dual-view split disabled 0b1: Dual-view split enabled
DV_EN	0	Dual-view processor enable	0b0: Dual-view processing disabled 0b1: Dual-view processing enabled

DV1 (0x1A1)

BIT	7	6	5	4	3	2	1	0
Field	DV_PPL_L[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DV_PPL_L	7:0	Dual-view detected pixels per line

DV2 (0x1A2)*

BIT	7	6	5	4	3	2	1	0
Field	DV_MEM_CRC_ERR	VID_EN_Y	VID_EN_X	RSVD[4:0]				
Reset	0x0	0x0	0x1	0x0				
Access Type	Read Only	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
DV_MEM_CRC_ERR	7	Dual-view memory CRC error	0x0: No CRC error 0x1: CRC error
VID_EN_Y	6	Enables split video on SIOB	0b0: Split video on SIOB disabled 0b1: Split video on SIOB enabled
VID_EN_X	5	Enables split video on SIOA	0b0: Split video on SIOA disabled 0b1: Split video on SIOA enabled

WM_WREN_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H (0x1AE) bitfields to enable writing to watermark registers; otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

WM_WREN_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Write 0xBA to WM_WREN_L (0x1AE) and 0xDC to WM_WREN_H registers to enable writing to watermark registers; otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

CROSS_0 (0x1B0)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0x0	0x0	0x0				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

CROSS_1 (0x1B1)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0x0	0x0	0x1				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x1B2)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0x0	0x0	0x2				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x1B3)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0x0	0x0	0x3				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

CROSS_4 (0x1B4)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0x0	0x0	0x4				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x1B5)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0x0	0x0	0x5				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x1B6)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0x0	0x0	0x6				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

CROSS_7 (0x1B7)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0x0	0x0	0x7				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x1B8)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0x0	0x0	0x8				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x1B9)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0x0	0x0	0x9				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

CROSS_10 (0x1BA)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0x0	0x0	0xA				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10	0bXXXXX: Incoming bit position

CROSS_11 (0x1BB)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0x0	0x0	0xB				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x1BC)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0x0	0x0	0xC				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

CROSS_13 (0x1BD)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0x0	0x0	0xD				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x1BE)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0x0	0x0	0xE				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x1BF)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0x0	0x0	0xF				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

CROSS_16 (0x1C0)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0x0	0x0	0x10				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x1C1)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0x0	0x0	0x11				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x1C2)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0x0	0x0	0x12				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

CROSS_19 (0x1C3)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0x0	0x0	0x13				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x1C4)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0x0	0x0	0x14				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x1C5)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0x0	0x0	0x15				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

CROSS_22 (0x1C6)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0x0	0x0	0x16				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x1C7)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0x0	0x0	0x17				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

VTX0 (0x1C8)*

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable VS output generation according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable HS output generation according to the timing definition	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable DE output generation according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Invert VSYNC output of video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Invert HSYNC output of video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Invert DE output of video timing generator	0b0: Do not invert DE 0b1: Invert DE
VTG_MODE	1:0	Video Timing Generation mode	0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto repeat mode 0b11: Free running mode

VTX1 (0x1C9)*

BIT	7	6	5	4	3	2	1	0
Field	HDMI_SCDT	HDMI_CKDT	PCLKDET	SEL_EXT_PCLK	CKDT_SCDT_OVR	VS_OUT_EN	HS_OUT_EN	VS_TRIG
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDMI_SCDT	7	HDMI sync detected	0b0: HDMI sync not detected 0b1: HDMI sync detected
HDMI_CKDT	6	HDMI clock detected	0b0: HDMI clock not detected 0b1: HDMI clock detected
PCLKDET	5	PCLK detected	0b0: PCLK not detected 0b1: PCLK detected
SEL_EXT_PCLK	4	Selects whether to use GPIO4 as PCLK input instead of the clock received from HDMI input	0b0: Use clock received from HDMI input 0b1: Use GPIO4 as PCLK
CKDT_SCDT_OVR	3	Selects whether to reset video pipeline with HDMI IP's SCDT, CKDT signals	0b0: Reset video pipeline 0b1: Do not reset video pipeline
VS_OUT_EN	2	Selects whether to output VSYNC from GPIO	0x0: Do not output VSYNC from GPIO 0x1: Output VSYNC from GPIO
HS_OUT_EN	1	Selects whether to output HSYNC from GPIO	0x0: Do not output HSYNC from GPIO 0x1: Output HSYNC from GPIO
VS_TRIG	0	Select VS trigger edge	0b0: Falling edge 0b1: Rising edge

VTX2 (0x1CA)*

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS [23:16].	0xXX: Most significant byte of VS delay

VTX3 (0x1CB)*

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS [15:8].	0xXX: Middle significant byte of VS delay

VTX4 (0x1CC)*

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS [7:0].	0xXX: Least significant byte of VS delay

VTX5 (0x1CD)*

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles [23:16]	0xXX: Most significant byte of VS high period

VTX6 (0x1CE)*

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles [15:8]	0xXX: Middle significant byte of VS high period

VTX7 (0x1CF)*

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of VS high period

VTX8 (0x1D0)*

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles [23:16]	0xXX: Most significant byte of VS low period

VTX9 (0x1D1)*

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles [15:8]	0xXX: Middle significant byte of VS low period

VTX10 (0x1D2)*

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of VS low period

VTX11 (0x1D3)*

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to rising edge of the first HS in terms of PCLK cycles [23:16]	0xXX: Most significant byte of VS edge to first HS rising edge

VTX12 (0x1D4)*

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to rising edge of the first HS in terms of PCLK cycles [15:8]	0xXX: Middle significant byte of VS edge to first HS rising edge

VTX13 (0x1D5)*

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to rising edge of the first HS in terms of PCLK cycles [7:0]	0xXX: Least significant byte of VS edge to first HS rising edge

VTX14 (0x1D6)*

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles [15:8]	0xXX: Most significant byte of HS high period

VTX15 (0x1D7)*

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of HS high period

VTX16 (0x1D8)*

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles [15:8]	0xXX: Most significant byte of HS low period

VTX17 (0x1D9)*

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of HS low period

VTX18 (0x1DA)*

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame [15:8]	0xXX: Most significant byte of HS pulses per frame

VTX19 (0x1DB)*

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame [7:0]	0xXX: Least significant byte of HS pulses per frame

VTX20 (0x1DC)*

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to rising edge of the first DE in terms of PCLK cycles [23:16]	0xXX: Most significant byte of VS edge to first DE

VTX21 (0x1DD)*

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to rising edge of the first DE in terms of PCLK cycles [15:8]	0xXX: Middle significant byte of VS edge to first DE

VTX22 (0x1DE)*

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to rising edge of the first DE in terms of PCLK cycles [7:0]	0xXX: Least significant byte of VS edge to first DE

VTX23 (0x1DF)*

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles [15:8]	0xXX: Most significant byte of DE high period

VTX24 (0x1E0)*

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of DE high period

VTX25 (0x1E1)*

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles [15:8]	0xXX: Most significant byte of DE low period

VTX26 (0x1E2)*

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles [7:0]	0xXX: Least significant byte of DE low period

VTX27 (0x1E3)*

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame [15:8]	0xXX: Most significant byte of DE pulses per frame

VTX28 (0x1E4)*

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame [7:0]	0xXX: Least significant byte of DE pulses per frame

VTX29 (0x1E5)

BIT	7	6	5	4	3	2	1	0
Field	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
Reset	0x0	–	–	–	–	0x0	0x0	
Access Type	Write, Read	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PRBS_EN	7	Enable video PRBS generator	0b0: Video PRBS generator disabled 0b1: Video PRBS generator enabled
GRAD_MODE	2	Gradient Pattern Generator mode	0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00
PATGEN_MODE	1:0	Pattern Generator mode	0b00: Pattern generator disabled - use video from the serializer input 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved

VTX30 (0x1E6)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INC[7:0]							
Reset	0x4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INC	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)	0xXX: Gradient increment base

VTX31 (0x1E7)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_L	7:0	Checkerboard mode color A lower byte	0xXX: Least significant byte of Checkerboard mode color A

VTX32 (0x1E8)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_M[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_M	7:0	Checkerboard mode color A middle byte	0xXX: Middle significant byte of Checkerboard mode color A

VTX33 (0x1E9)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_H	7:0	Checkerboard mode color A upper byte	0xXX: Most significant byte of Checkerboard mode color A

VTX34 (0x1EA)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_L	7:0	Checkerboard mode color B lower byte	0xXX: Least significant byte of Checkerboard mode color B

VTX35 (0x1EB)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_M[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_M	7:0	Checkerboard mode color B middle byte	0xXX: Middle significant byte of Checkerboard mode color B

VTX36 (0x1EC)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_H	7:0	Checkerboard mode color B upper byte	0xXX: Most significant byte of Checkerboard mode color B

VTX37 (0x1ED)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode color A repeat count	0xXX: Repeat count of Checkerboard mode color A

VTX38 (0x1EE)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode color B repeat count	0xXX: Repeat count of Checkerboard mode color B

VTX39 (0x1EF)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

VTX40 (0x1F0)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSSHS_I	CROSSHS_F	CROSSHS[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSHS_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSSHS_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSSHS	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

VTX41 (0x1F1)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSSVS_I	CROSSVS_F	CROSSVS[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSVS_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSSVS_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSSVS	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

VTX42 (0x1F2)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSSDE_I	CROSSDE_F	CROSSDE[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSDE_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSSDE_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSSDE	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

GPIO_A (0x200)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x0	0x0	0x0	0x1	0x1	0x1	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x201)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x1		0x0	0x0				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x202)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x0				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x203)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x204)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x1				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x205)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x1				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x206)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x207)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x2				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x208)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x2				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x209)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x20A)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x3				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x20B)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x3				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x20C)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x0	0x0	0x0	0x1	0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x20D)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x1		0x0	0x4				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x20E)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x4				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x20F)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x210)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x5				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x211)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x5				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x212)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x213)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x6				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x214)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x6				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x215)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x216)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x7				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x217)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x7				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x218)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x219)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x8				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x21A)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x8				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x21B)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x21C)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0x9				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x21D)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x9				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x21E)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x21F)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0xA				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x220)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xA				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x221)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x222)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0xB				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x223)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xB				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x224)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x225)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0x1	0xC				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x226)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xC				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x227)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x228)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0x1	0xD				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x229)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xD				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x22A)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x22B)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0x1	0xE				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x22C)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xE				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x22D)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x22E)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0x1	0xF				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x22F)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0xF				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x230)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x231)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0x1	0x10				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x232)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x10				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x233)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x234)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0x1	0x11				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x235)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x11				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x236)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x0	0x0	0x0	0x1	0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x237)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0x1		0x0	0x12				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
RSVD	5	I^2C IO is open-drain only	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x238)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x12				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x239)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0x0	0x0	0x0	0x1	0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x23A)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0x1		0x0	0x13				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull-up/pull-down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
RSVD	5	Driver type selection (I^2C IO is only open-drain)	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x23B)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0x1	–	0x13				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

CMU5 (0x245)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				GPIO_SPEED_B[1:0]		GPIO_SPEED_A[1:0]	
Reset	0x00				0x00		0x00	
Access Type					Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_SPEED_B	3:2	Controls GPIO Speed Group B (GPIO 0-13, HPD) transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns
GPIO_SPEED_A	1:0	Controls GPIO Speed Group A (GPIO 14-17, LOCK, ERRB, HSPD) transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns

UART_PT_0 (0x24A)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Low-byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (8 LSb). Set BITLEN_MAN_CFG_1 to 1 to use this value.	0xXX: Lower byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x24B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0x05					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	Custom UART bit length for pass-through UART Channel 1. Set BITLEN_MAN_CFG_1 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (6 MSb)	0xXX: Upper byte of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x24C)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Custom UART bit length for pass-through UART Channel 2 Set BITLEN_MAN_CFG_2 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (8 LSb)	0xXX: Lower byte of custom UART bit length for pass-through UART Channel 2

RLMS3 (0x403, 0x503)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
Reset	0x0	0x0	0x0	0x0	0x1	–	0x2	
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt Process Enable	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x404, 0x504)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0x2		0x1	0x1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye-opening monitor window, as follows: Observations = $6.29 \times 10^{(N + 2)}$	0bX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow 1 error 0b10: Allow 2 errors 0b11: Allow 3 errors
EOM_PER_MODE	1	Eye-Opening Monitor Periodic Mode Enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-Opening Monitor Enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x405, 0x505)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0x0	0x10						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger for use when periodic mode is disabled	0b0: No action 0b1: Eye-opening monitor manual trigger request
EOM_MIN_THR	6:0	The eye-opening monitor minimum threshold as defined by the following equation: Eye-opening percentage = EOM_MIN_THR/64. If the value is zero, the eye-opening monitor is disabled.	0bXXXXXXX: Eye-opening monitor minimum threshold factor

RLMS6 (0x406, 0x506)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0x1	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally	0b0: Vertical Opening mode 0b1: Horizontal Opening mode
EOM_RST_THR	6:0	The eye-opening monitor refresh threshold as defined by the following equation: Eye-opening percentage = EOM_MIN_THR/64. If the value is zero, the eye-opening monitor is disabled.	0bXXXXXXX: Eye-opening monitor refresh threshold factor

RLMS7 (0x407, 0x507)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0x0	0x0						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-Opening Monitor Measurement Done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed eye-opening monitor observation	0bXXXXXXX: EOM measurement result

RLMS34 (0x434, 0x534)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-Monitor Period Count (RxClk20) LSb	0xXX: Eye-monitor period count (LSb)

RLMS35 (0x435, 0x535)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-Monitor Period Count (RxClk20) MSb	0xXX: Eye-monitor period count (MSb)

RLMS37 (0x437, 0x537)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-Monitor Period Done (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot) readback is EyeMonClrPL from long-pulse generation	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-Monitor Start (one-shot) Readback is EyeMonStClrPL from long pulse generation for both start and clear.	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-Monitor Phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-Monitor Data Polarity	0b0: Eye monitor search for 1s 0b1: Eye monitor search for 0s

RLMS38 (0x438, 0x538)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-Monitor Error Count (read-only)	0xXX: Eye-monitor error count (LSB)

RLMS39 (0x439, 0x539)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-Monitor Error Count (read-only)	0xXX: Eye-monitor error count (MSB)

RLMS3A (0x43A, 0x53A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-Monitor Valid (Hit) Count (Read-Only)	0xXX: Eye-monitor valid count (LSB)

RLMS3B (0x43B, 0x53B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-Monitor Valid (Hit) Count (Read-Only)	0xXX: Eye-monitor valid count (MSB)

RLMS3D (0x43D, 0x53D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0x0							0x1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Active Error Channel Phase Command (Read-Only)	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Error Channel Phase Toggle Enable	0: Use primary phase only 1: Auto toggle phase between primary and secondary

RLMS3E (0x43E, 0x53E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0x1	0x3A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	Error Channel Phase Secondary Timing Adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value: 7'h3A	0bxxxxxxx: Error channel phase secondary (odd)

RLMS3F (0x43F, 0x53F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0x0	0x79						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	Error Channel Phase Primary Timing Adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPri	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value 7'h79	0bxxxxxxx: Error channel phase primary (even)

RLMS49 (0x449, 0x549)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	–	0x1	0x1	0x1	0x0	0x0	–	0x1
Access Type	–					Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error Channel Power-Up	0b0: Error channel power disabled 0b1: Error channel power enabled

RLMS58 (0x458, 0x558)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error Channel Target Amplitude for 1s	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude: binary amplitude 4.7mV per count

RLMS59 (0x459, 0x559)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0x68						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error Channel Target Amplitude for 0s	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude: binary amplitude 4.7mV per count

RLMS64 (0x464, 0x564)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0x0	0x0	
Access Type	–	–	–	–	–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx Spread Spectrum Mode	0b00: Spread spectrum disabled 0b01: Reserved 0b10: Reserved 0b11: Spread spectrum enabled (center spread)

RLMS70 (0x470, 0x570)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0x1						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx Spread Spectrum Frequency Control	0bXXXXXXX: Tx spread spectrum center frequency control

RLMS71 (0x471, 0x571)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0x1						0x0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx Spread Spectrum Center Spread Startup Control	0bXXXXXX: Tx spread spectrum center spread startup control
TxSSCEn	0	Tx Spread Spectrum Enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x472, 0x572)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx Spread Spectrum Frequency Prescaler Lower Byte	0xXX: Tx spread spectrum frequency prescaler lower byte

RLMS73 (0x473, 0x573)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreScIH	2:0	Tx Spread Spectrum Frequency Prescaler Upper Bits	0bXXX: Tx spread spectrum frequency prescaler upper bits

RLMS74 (0x474, 0x574)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx Spread Spectrum Interpolator phase Lower Byte	0xXX: Tx spread spectrum frequency interpolator phase lower byte

RLMS75 (0x475, 0x575)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx Spread Spectrum Interpolator Phase	0bXXXXXXX: Tx spread spectrum frequency interpolator phase upper bits

RLMS76 (0x476, 0x576)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx Spread Spectrum Interpolator Phase Quadrant	0bXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x495, 0x595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0x0	0x1	0x29					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx Amplitude Manual Override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx Amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x4A4, 0x5A4)*

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0x2		0x3D					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ Period Multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ Period Periodic adaptation is disabled when value is 0. Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT).	0bXXXXXX: Only 0s have a special meaning. See description

RLMSA8 (0x4A8, 0x5A8)

BIT	7	6	5	4	3	2	1	0
Field	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
FW_PHY_CTRL	7	PHY controller firmware mode enable
FW_PHY_PU_TX	6	Override PHY controller output
FW_PHY_RSTB	5	Override PHY controller output

RLMSA9 (0x4A9, 0x5A9)

BIT	7	6	5	4	3	2	1	0
Field	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	RSVD	FW_RXD_EN	RSVD	RSVD	RSVD
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION
FW_REPCAL_RSTB	7	Override PHY controller output
FW_TXD_SQUELCH	5	Override PHY controller output
FW_RXD_EN	3	Override PHY controller output

RLMSB6 (0x4B6, 0x5B6)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
Reset	0x1	0x3B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG1875	7	Error Channel Phase Secondary Timing Adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG1875	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel (slow receive, secondary phase, 187.5Mbps)	0bXXXXXXX: 7'h3B

RLMSB7 (0x4B7, 0x5B7)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
Reset	0x0	0x7A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG1875	7	Error Channel Phase Primary Timing Adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG1875	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel (slow receive, primary phase, 187.5Mbps)	0bXXXXXXX: 7'h7A

RX_AON_SRST (0x2005)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_sw_rst_auto	–	–	–	reg_sw_rst
Reset	–	–	–	0b0	–	–	–	0b0
Access Type	–	–	–	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_sw_rst_auto	4	Auto software reset - will not reset AAC.	0x0: Manual software reset (default) 0x1: Auto software reset whenever SCDT = 0
reg_sw_rst	0	Software reset. Reset all internal logic; except register interface; ACR; AAC and EEPROM interface. Note: Asserting software reset will not reset writable register contents.	0x0: Normal operation (default) 0x1: Reset

RX_SYS_SWTCHC (0x2009)*

BIT	7	6	5	4	3	2	1	0
Field	reg_ddc_sda_in_del_en	reg_ddc_sda_out_del_en	ddc_filter_sel[1:0]		–	reg_ddc_scdc_en	RSVD	reg_ddc_edid_en
Reset	0b1	0b1	0b00		–	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read		–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
reg_ddc_sda_in_del_en	7	Enable the DDC del: "1" - default is enable. DDC delay is inserted into the SDA line to create 300ns delay for the falling edge of the DDC SDA signal in order to avoid erroneous I2C START condition. The real START condition must have setup time of the 600ns. This delay of 300ns does not remove the real START condition.
reg_ddc_sda_out_del_en	6	Enable the I2C SDA del: "1" - default is enable. I2C delay is inserted into the SDA line to create 300ns delay for the falling edge of the DDC SDA signal in order to avoid erroneous I2C START condition. The real START condition must have a set-up time of the 600ns. This delay of 300ns does not remove the real START condition.
ddc_filter_sel	5:4	Enable DDC Filter: 2'b10 - 3 taps 2'b11 - 5 taps Rest are No Filter
reg_ddc_scdc_en	2	SCDC DDC Select: 0 - Disables SCDC accesses on DDC 1 - Enables SCDC accesses on DDC
reg_ddc_edid_en	0	EDID DDC Select

RX_STATE_AON (0x200C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	hdmi_tx_connected	–	ckdt	scdt
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Read Only	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
hdmi_tx_connected	3	State of the selected port's 5V power detect pin.	0b0: HDMI cable is not connected 0b1: HDMI cable is connected
ckdt	1	State of the Clock Detect. '1' if a clock is detected on the TMDS signals.	0b0: Clock is not detected 0b1: Clock is detected
scdt	0	State of the Sync Detect. A HIGH level is outputted when DE is actively toggling, indicating that the link is alive. A low level is outputted when DE is inactive, indicating the link is down.	0b0: Sync not detected 0b1: Sync detected

HDMI2_MODE_CTRL (0x2040)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_scramble_on_ovr	reg_hdmi_on_ovr	–	–	reg_scramble_on_val	reg_hdmi2_on_val
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_scramble_on_ovr	5	Scramble on FW overwrite enable	0: Disable overwrite on scramble_on 1: Enable overwrite on scramble_on
reg_hdmi_on_ovr	4	HDMI2 mode FW overwrite enable	0: Disable overwrite on HDMI2 mode 1: Enable overwrite on HDMI2 mode
reg_scramble_on_val	1	Scramble on FW overwrite value	0: Clear scramble_on during overwrite 1: Set scramble_on during overwrite
reg_hdmi2_on_val	0	HDMI2 mode FW overwrite value	0: Clear HDMI2 mode during overwrite 1: Set HDMI2 mode during overwrite

RX_INTR_STATE (0x2070)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_intr
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
reg_intr	0	Interrupt state bit value that indicates whether the interrupt is active or not. It is one gate before the polarity is applied to the interrupt. Whenever the interrupt is asserted, this bit is high.	0b0: Interrupt is not asserted 0b1: Interrupt is asserted

RX_INT_CTRL (0x2079)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_soft_intr_en	–	reg_intr_polarity	–
Reset	–	–	–	–	0b0	–	0b1	–
Access Type	–	–	–	–	Write, Read	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION
reg_soft_intr_en	3	Set software interrupt: 0 - Disable software interrupt (default) 1 - Set software interrupt (triggers interrupt until this bit is cleared)
reg_intr_polarity	1	INT pin asserts polarity level: 1 - INT output is asserted when set to '0' (default) 0 - INT output is asserted when set to '1'

RX_INTR2_AON (0x2080)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr2_stat5_aon	reg_intr2_stat4_aon	reg_intr2_stat2_aon	–	–	–
Reset	–	–	0b0	0b1	0b0	–	–	–
Access Type	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr2_stat5_aon	5	Software induced interrupt. Asserted if set to 1. This is a dynamic interrupt and clears on programming the reg_soft_intr_en bit of RX_INT_CTRL register LOW.
reg_intr2_stat4_aon	4	CKDT - Clock Detect. '1' if a clock is detected on the TMDS signals. Asserted if change in CKDT is detected. Asserted if set to 1. Write '1' to clear.
reg_intr2_stat2_aon	3	Sync Detect. During normal operation: A HIGH level is outputted when DE is actively toggling, indicating that the link is alive. A low level is outputted when DE is inactive, indicating the link is down. It is asserted if change in SCDT is detected. During power down: A HIGH level is outputted when DE is changed from 0 to 1. Asserted if set to 1. Write 1 to clear.

RX_INTR6_AON (0x2081)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_intr6_stat0_aon
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION
reg_intr6_stat0_aon	0	Cable Unplug Interrupt: When asserted, this interrupt indicates the cable is unplugged. Asserted HIGH when a falling edge is detected on PWR5V. Write 1 to clear.

RX_INTR7_AON (0x2082)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr7_stat7_aon	reg_intr7_stat6_aon	–	reg_intr7_stat4_aon	reg_intr7_stat3_aon	–	–	–
Reset	0b0	0b0	–	0b0	0b0	–	–	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	–	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr7_stat7_aon	7	tmds_clk_ratio change from 0→1 and 1→0
reg_intr7_stat6_aon	6	scramble_en change from 0→1 and 1→0
reg_intr7_stat4_aon	4	CEC Interrupt Status

BITFIELD	BITS	DESCRIPTION
reg_intr7_stat3_aon	3	CBUS Interrupt Status

RX_INTR8_AON (0x2083)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	reg_intr8_stat1_aon	–
Reset	–	–	–	–	–	0b0	0b0	–
Access Type	–	–	–	–	–		Write 1 to Clear, Read	–

BITFIELD	BITS	DESCRIPTION
reg_intr8_stat1_aon	1	Cable Plugin Interrupt: When asserted, this interrupt indicates the cable is plugged in. Asserted HIGH when a rising edge is detected on PWR5V. Write 1 to clear.

RX_INTR9_AON (0x2084)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr9_stat7_aon	reg_intr9_stat6_aon	–	–	reg_intr9_stat3_aon	reg_intr9_stat2_aon	reg_intr9_stat1_aon	reg_intr9_stat0_aon
Reset	0b0	0b0	–	–	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION
reg_intr9_stat7_aon	7	test_rd_req change
reg_intr9_stat6_aon	6	char_errdet_cnt change
reg_intr9_stat3_aon	3	rr_test change from 0→1 or 1→0
reg_intr9_stat2_aon	2	ced_update change from 0→1 or 1→ 0
reg_intr9_stat1_aon	1	status_update change from 0→1 or 1→0
reg_intr9_stat0_aon	0	src_ver value or rr_enable value change

RX_INTR2_MASK_AON (0x2090)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr2_mask5_aon	reg_intr2_mask4_aon	reg_intr2_mask3_aon	–	–	–
Reset	–	–	0b0	0b0	0b0	–	–	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr2_mask5_aon	5	Enable INT2[5]: 1 - Enable 0 - Disable (default)
reg_intr2_mask4_aon	4	Enable INT2[4]: 1 - Enable 0 - Disable (default)

BITFIELD	BITS	DESCRIPTION
reg_intr2_mask3_aon	3	Enable INT2[3]: 1 - Enable 0 - Disable (default)

RX_INTR6_MASK_AON (0x2091)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_intr6_mask0_aon
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr6_mask0_aon	0	Enable INT6[0]: 1 - Enable 0 - Disable (defualt)

RX_INTR7_MASK_AON (0x2092)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr7_mask7_aon	reg_intr7_mask6_aon	–	reg_intr7_mask4_aon	reg_intr7_mask3_aon	RSVD[2:0]		
Reset	0b0	0b0	–	0b0	0b0	0b000		
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
reg_intr7_mask7_aon	7	Enable INT7[7]: 1 - Enable 0 - Disable (default)
reg_intr7_mask6_aon	6	Enable INT7[6]: 1 - Enable 0 - Disable (default)
reg_intr7_mask4_aon	4	Enable INT7[4]: 1 - Enable 0 - Disable (default)
reg_intr7_mask3_aon	3	Enable INT7[3]: 1 - Enable 0 - Disable (default)

RX_INTR8_MASK_AON (0x2093)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	reg_intr8_mask2_aon	reg_intr8_mask1_aon	–
Reset	–	–	–	–	–	0b0	0b0	–
Access Type	–	–	–	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION
reg_intr8_mask2_aon	2	Enable INT8[2]: 1 - Enable 0 - Disable (default)
reg_intr8_mask1_aon	1	Enable INT8[1]: 1 - Enable 0 - Disable (default)

RX_INTR9_MASK_AON (0x2094)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr9_mask7_aon	reg_intr9_mask6_aon	–	–	reg_intr9_mask3_aon	reg_intr9_mask2_aon	reg_intr9_mask1_aon	reg_intr9_mask0_aon
Reset	0b0	0b0	–	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr9_mask7_aon	7	Enable INT7[7]: 1 - Enable 0 - Disable (default)
reg_intr9_mask6_aon	6	Enable INT7[6]: 1 - Enable 0 - Disable (default)
reg_intr9_mask3_aon	3	Enable INT7[3]: 1 - Enable 0 - Disable (default)
reg_intr9_mask2_aon	2	Enable INT7[2]: 1 - Enable 0 - Disable (default)
reg_intr9_mask1_aon	1	Enable INT7[1]: 1 - Enable 0 - Disable (default)
reg_intr9_mask0_aon	0	Enable INT7[0]: 1 - Enable 0 - Disable (default)

SCDCS_CNTL (0x20A9)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			RSVD	–	reg_sw_rd_req_set	RSVD	reg_scdcs_enabled
Reset	0b000			0b0	–	0b0	0b0	0b1
Access Type					–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_sw_rd_req_set	2	SCDCS Firmware Read Request Set FW can assert the read request by setting this bit. This bit automatically clears by HW once the corresponding read request is set by RX SCDC DDC.	

BITFIELD	BITS	DESCRIPTION	DECODE
reg_scdcs_enabled	0	SCDCS enabled. FW should set this bit if SCDCS of Sink is set in E-EDID. FW should program it initially after boot up. Whenever FW changes this bit in E-EDID, the same should be programmed into this bit by FW. When this bit is changed from 0 to 1 (disabled → enabled), RX/Sink resets the RE_Enable bit in DDC-SCDC registers. If the programming clock is much faster and ss implemented hardware operates with 2MHz oscillator clock, Sink should see this transition. Frequent switching (0 → 1) of this bit may not affect until the first transition is sampled on the destination domain.	0b0: Disabled 0b1: Enabled

Sink_Version (0x20AB)*

BIT	7	6	5	4	3	2	1	0
Field	reg_scdcs_snk_ver[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_scdcs_snk_ver	7:0	Sink Version: This field configures the sink version for the source to read through DDC.

Source_Version (0x20AC)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_src_ver[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
scdcs_src_ver	7:0	Source Version: This field contains the source version as programmed through DDC into the SCDCS.

scdcs_status1 (0x20AD)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch2_locked	scdcs_ch1_locked	scdcs_ch0_locked	scdcs_clk_detected	scdcs_scrbl_status	scdcs_rr_test	scdcs_ced_upd	scdcs_sts_upd
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
scdcs_ch2_locked	7	The Sink sets this bit to 1 when the Sink device is successfully decoding data on HDMI Channel 2 and resets it to 0 if this condition no longer exists.
scdcs_ch1_locked	6	The Sink sets this bit to 1 when the Sink device is successfully decoding data on HDMI Channel 1 and resets it to 0 if this condition no longer exists.
scdcs_ch0_locked	5	The Sink sets this bit to 1 when the Sink device is successfully decoding data on HDMI Channel 0 and resets it to 0 if this condition no longer exists.
scdcs_clk_detected	4	The Sink sets this bit to 1 when the Sink device detects a valid clock signal and resets it to 0 if this condition no longer exists.
scdcs_scrbl_status	3	Scramble Status. The Sink sets this bit to 1 when the Sink device detects scrambled control code sequences and resets it to 0 when the sink does not detect scrambled control code sequences.
scdcs_rr_test	2	The Sink sets this bit to 1 when a test Read Request is generated in response to the setting 1 of the TestReadRequest bit in the Test Configuration register.
scdcs_ced_upd	1	This sets this bit to 1 when a value is changed in the Character Error Detection registers. The Source may write this bit to 1 to clear it. The Sink resets the bit to 0 when the Source writes a 1 value to this bit. The Sink does not change this bit when the Source reads a Character Error Detection Register.
scdcs_sts_upd	0	This is set to 1 when a value is changed in the Status Flags register. The Sink does not change this bit when the Source reads a Character Error Detection Register. The Source may write this bit to 1 to clear it. The Sink resets the bit to 0 when the Source writes a 1 value to this bit.

scdcs_Config_status (0x20AE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	scdcs_tmds_bclk_ratio	scdcs_scrbl_enable	–	scdcs_rr_enable
Reset	–	–	–	–	0b0	0b0	–	0b0
Access Type	–	–	–	–	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION
scdcs_tmds_bclk_ratio	3	TMDS Bit Clock Ratio 0 = (TMDS Bit Period)/(TMDS Clock Period) ratio is 1/10 1 = (TMDS Bit Period)/(TMDS Clock Period) ratio is 1/40
scdcs_scrbl_enable	2	Scramble Enable The Source sets (=1) this bit to enable scrambling in the Sink The Source resets (=0) this bit to disable scrambling in the Sink
scdcs_rr_enable	0	Read Request Enable The Source sets this bit (=1) when the Source supports Read Request. The Source resets this bit (=0) when the Source supports only polling of the update flags. The Sink resets (=0) this bit when one of the following occurs: 1. +5V Power Signal is not provided by the Source. 2. The Hot-Plug Detect pin has voltage = low for 100ms or more. 3. The SCDC of the Sink goes from disabled to enabled state.

SCDCS_CED0_L (0x20B0)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch0_ced_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
scdcs_ch0_ced_cnt_7_0	7:0	Channel 0 character error count byte 0. Bits: [7:0] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED0_H (0x20B1)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch0_vld	scdcs_ch0_ced_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION
scdcs_ch0_vld	7	Channel 0 valid. Cleared on read by the Source.
scdcs_ch0_ced_cnt_14_8	6:0	Channel 0 character error count byte 0. Bits: [14:8] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED1_L (0x20B2)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch1_ced_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
scdcs_ch1_ced_cnt_7_0	7:0	Channel 1 character error count byte 0. Bits: [7:0] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED1_H (0x20B3)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch1_vld	scdcs_ch1_ced_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION
scdcs_ch1_vld	7	Channel 1 valid. Cleared on read by the Source.

BITFIELD	BITS	DESCRIPTION
scdcs_ch1_ced_cnt_14_8	6:0	Channel 1 character error count byte 0. Bits: [14:8] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED2_L (0x20B4)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch2_ced_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
scdcs_ch2_ced_cnt_7_0	7:0	Channel 2 character error count byte 0. Bits: [7:0] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED2_H (0x20B5)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ch2_vld	scdcs_ch2_ced_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION
scdcs_ch2_vld	7	Channel 2 valid. Cleared on read by the Source.
scdcs_ch2_ced_cnt_14_8	6:0	Channel 2 character error count byte 0. Bits: [14:8] The Character Error Detection counters are not writable by the Source and cleared on read by the Source.

SCDCS_CED_Checksum (0x20B6)

BIT	7	6	5	4	3	2	1	0
Field	scdcs_ced_chksum[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
scdcs_ced_chksum	7:0	The Checksum is implemented such that a 1-byte sum of the 7 registers of Character Error Detection, including the Checksum itself (reg_chX_chr_errdet_cnt and reg_chr_errcnt_chksum), is equal to zero.

RX_HPD_C_CTRL (0x20F5)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_hpd_c_ctrl
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_hpd_c_ctrl	0	This register bit carries the value to be driven on hpd_c output. Value in this register bit is driven onto hpd_c output when any of the following conditions are true. 1. reg_hpd_ovrt_ctrl field of RX_HPD_OVRT_CTRL register is HIGH. 2. When the link established is not an MHL connection, and a HDMI connection is established.

RX_HPD_OEN_CTRL (0x20F6)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_hpd_oen_ctrl
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_hpd_oen_ctrl	0	This register bit carries the value to be driven on hpd_oen output. Value in this register bit is driven onto hpd_oen output when any of the following conditions are true. 1. reg_hpd_ovrt_ctrl field of RX_HPD_OVRT_CTRL register is HIGH 2. When the link established is not an MHL connection

RX_HPD_OVRT_CTRL (0x20F9)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	reg_hpd_ovrt_ctrl
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–		Write, Read

BITFIELD	BITS	DESCRIPTION
reg_hpd_ovrt_ctrl	0	HPD Overwrite control: This register bit controls the HPD PAD signal overriding. 0: No Override. Values from hardware drive the HPD PAD signals 1: Override. Values from respective registers above drive the HPD PAD signals

RX_ACR_CTRL1 (0x2100)*

BIT	7	6	5	4	3	2	1	0
Field	reg_cts_dropped_auto_en	reg_post_hw_sw_sel	reg_upll_hw_sw_sel	reg_cts_hw_sw_sel	reg_n_hw_sw_sel	reg_cts_reused_auto_en	reg_fs_hw_sw_sel	reg_acr_init
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_cts_dropped_auto_en	7	0: No ACR reinitialization is triggered if a CTS value is dropped (default) 1: If the CTS value is dropped because a new packet value overwrote a CTS value before it was used to generate an NCLK period, an ACR reinitialization is automatically triggered to realign the NCLK edge to the timing of the incoming ACR packets
reg_post_hw_sw_sel	6	Audio PLL Post Divider Value Select: 0: ACR uses hardware-determined post divider value (POST_HVAL) (default) 1: ACR uses software-determined post divider value (POST_SVAL)
reg_upll_hw_sw_sel	5	Audio PLL Feedback Divider UPLL Value Select: 0: ACR uses hardware-determined UPLL value (UPLL_HVAL (default) 1: ACR uses software-determined UPLL value (UPLL_SVAL)
reg_cts_hw_sw_sel	4	ACR CTS Value Select: 0: ACR uses hardware-determined CTS value (CTS_HVAL) (default) 1: ACR uses software-determined CTS value (CTS_SVAL)
reg_n_hw_sw_sel	3	ACR N Value Select: 0: ACR uses hardware-determined N value (N_HVAL) (default) 1: ACR uses software-determined N value (N_SVAL)
reg_cts_reused_auto_en	2	0: No ACR reinitialization is triggered if a CTS value is reused (default) 1: If the CTS value is reused because a new packet value was not available when the previous NCLK period was finished, an ACR reinitialization is automatically triggered to realign the NCLK edge to the timing of the incoming ACR packets
reg_fs_hw_sw_sel	1	Audio Sample Frequency Select: 0: ACR uses hardware-determined Fs value (CHST4) (default) 1: ACR uses software-determined Fs value (FREQ_SVAL)
reg_acr_init	0	Generates a 1-TCLK strobe that starts an ACR reinitialization to realign the NCLK edge to the timing of the incoming ACR packets. The NCLK is held low while realignment occurs.

AAC_MCLK_SEL (0x2101)*

BIT	7	6	5	4	3	2	1	0
Field	reg_vcnt_max[1:0]		reg_mclk4dac[1:0]		reg_mclk4hbra[1:0]		reg_mclk4dsd[1:0]	
Reset	0b10		0b01		0b00		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
reg_vcnt_max	7:6	VSYNC count to wait for Video Stability check. This register field contains the number of VSYNCs the hardware waits/monitors for the Video/Audio Stability checks to be through. The hardware waits for the number of VSYNCs programmed into this field and confirms the Video/Audio Stability check pass/fail status to the AAC FSM and unmutes the audio if no errors.	0b00: 0 0b01: 1 0b10: 2 0b11: 3
reg_mclk4dac	5:4	Audio main clock frequency mode software select	0b00: Fm = 128*Fs 0b01: Fm = 256*Fs (default) 0b10: Fm = 384*Fs 0b11: Fm = 512*Fs
reg_mclk4hbra	3:2	Audio main clock frequency mode software select	0b00: Fm = 128*Fs (default) 0b01: Fm = 256*Fs 0b10: Fm = 384*Fs 0b11: Fm = 512*Fs
reg_mclk4dsd	1:0	Audio main clock frequency mode software select	0b00: Fm = 128*Fs 0b01: Fm = 256*Fs 0b10: Fm = 384*Fs 0b11: Fm = 512*Fs (default)

RX_FREQ_SVAL (0x2102)*

BIT	7	6	5	4	3	2	1	0
Field	reg_fm_val_sw[1:0]		reg_fs_val_sw[5:0]					
Reset	0b01		0b000010					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
reg_fm_val_sw	7:6	Audio main clock output frequency mode software select. Used for determining UPLL and POST divider hardware values.	0b00: Fm = 128*Fs 0b01: Fm = 256*Fs (default) 0b10: Fm = 384*Fs 0b11: Fm = 512*Fs
reg_fs_val_sw	5:0	Audio sampling frequency mode software select (in kHz). These bits correspond to the Channel Status bits 24, 25, 26, 27, 30, 31 where bit 24 = LSB and 31 = MSB: "31 30 27 26 25 24" Fs	0bxx0011: 32 kHz 0b001011: 64 kHz 0b101011: 128 kHz 0b011011: 256 kHz 0b111011: 512 kHz 0b110101: 1024 kHz 0bxx0000: 44.1 kHz 0bxx1000: 88.2 kHz 0bxx1100: 176.4 kHz 0b001101: 352.8 kHz 0b101101: 705.6 kHz 0b011101: 1411.2 kHz 0bxx0010: 48 kHz 0bxx1010: 96 kHz 0bxx1110: 192 kHz 0b000101: 384 kHz 0bxx1001: 768 kHz 0b010101: 1536 kHz Others: Reserved

RX_N_SVAL1 (0x2103)*

BIT	7	6	5	4	3	2	1	0
Field	reg_n_val_sw_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_n_val_sw_7_0	7:0	Bits [7:0] of [19:0] of the audio clock regeneration N value that is set by software. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_N_SVAL2 (0x2104)*

BIT	7	6	5	4	3	2	1	0
Field	reg_n_val_sw_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_n_val_sw_15_8	7:0	Bits [15:8] of [19:0] of the audio clock regeneration N value that is set by software. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_N_SVAL3 (0x2105)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_n_val_sw_19_16[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
reg_n_val_sw_19_16	3:0	Bits [19:16] of [19:0] of the audio clock regeneration N value that is set by software. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_N_HVAL1 (0x2106)

BIT	7	6	5	4	3	2	1	0
Field	n_val_hw_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
n_val_hw_7_0	7:0	Bits [7:0] of [19:0] of the audio clock regeneration N packet value that is received by the Rx from the Tx. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_N_HVAL2 (0x2107)

BIT	7	6	5	4	3	2	1	0
Field	n_val_hw_15_8[7:0]							
Reset	0x0C							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
n_val_hw_15_8	7:0	Bits [15:8] of [19:0] of the audio clock regeneration N packet value that is received by the Rx from the Tx. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_N_HVAL3 (0x2108)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	n_val_hw_19_16[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
n_val_hw_19_16	3:0	Bits [19:16] of [19:0] of the audio clock regeneration N packet value that is received by the Rx from the Tx. ACR_CTRL1[3] controls whether this value is used for the audio clock regeneration.

RX_CTS_SVAL1 (0x2109)*

BIT	7	6	5	4	3	2	1	0
Field	reg_cts_val_sw_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cts_val_sw_7_0	7:0	Bits [7:0] of [19:0] of the audio clock regeneration CTS value that is set by software. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_CTS_SVAL2 (0x210A)*

BIT	7	6	5	4	3	2	1	0
Field	reg_cts_val_sw_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cts_val_sw_15_8	7:0	Bits [15:8] of [19:0] of the audio clock regeneration CTS value that is set by software. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_CTS_SVAL3 (0x210B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_cts_val_sw_19_16[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
reg_cts_val_sw_19_16	3:0	Bits [19:16] of [19:0] of the audio clock regeneration CTS value that is set by software. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_CTS_HVAL1 (0x210C)

BIT	7	6	5	4	3	2	1	0
Field	cts_val_hw_7_0[7:0]							
Reset	0x68							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
cts_val_hw_7_0	7:0	Bits [7:0] of [19:0] of the audio clock regeneration CTS packet value that is received by the Rx from the Tx. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_CTS_HVAL2 (0x210D)

BIT	7	6	5	4	3	2	1	0
Field	cts_val_hw_15_8[7:0]							
Reset	0x3C							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
cts_val_hw_15_8	7:0	Bits [15:8] of [19:0] of the audio clock regeneration CTS packet value that is received by the Rx from the Tx. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_CTS_HVAL3 (0x210E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	cts_val_hw_19_16[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
cts_val_hw_19_16	3:0	Bits [19:16] of [19:0] of the audio clock regeneration CTS packet value that is received by the Rx from the Tx. ACR_CTRL1[4] controls whether this value is used for the audio clock regeneration.

RX_UPLL_SVAL (0x210F)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_upll_val_sw[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
reg_upll_val_sw	6:0	The audio clock regeneration PLL feedback divider determines, along with N, the frequency of the PLL VCO. This value is set by software. ACR_CTRL1[5] controls whether this value is used for the audio clock regeneration.

RX_UPLL_HVAL (0x2110)

BIT	7	6	5	4	3	2	1	0
Field	–	upll_val_hw[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
upll_val_hw	6:0	The audio clock regeneration PLL feedback divider determines, along with N, the frequency of the PLL VCO. This value is decoded from the audio sample and main clock frequency data in FREQ_SVAL. ACR_CTRL1[5] controls whether this value is used for the audio clock regeneration.

RX_POST_SVAL (0x2111)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_post_val_sw[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
reg_post_val_sw	5:0	The audio clock regeneration PLL post divider that determines the frequency of MCLKOUT. This value is set by software. ACR_CTRL1[6] controls whether this value is used for the audio clock regeneration.

RX_POST_HVAL (0x2112)

BIT	7	6	5	4	3	2	1	0
Field	–	–	post_val_hw[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
post_val_hw	5:0	The audio clock regeneration PLL post divider that determines the frequency of MCLKOUT. This value is decoded from the audio sample and main clock frequency data in FREQ_SVAL. ACR_CTRL1[6] controls whether this value is used for the audio clock regeneration.

RX_LK_WIN_SVAL (0x2113)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_lk_win_sw_4_1[3:0]				reg_lk_win_sw_0
Reset	–	–	–	0x7				0b1
Access Type	–	–	–	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION
reg_lk_win_sw_4_1	4:1	Most recent count must be within ±(previous count) / $2^{(lk\_win\_sw)}$ to enable the stability duration counter to increment: b0000 = d0: window is ±(previous count) / 2^0 = ±(previous count) b0001 = d1: window is ±(previous count) / 2^1 = ±(previous count) / 2 b0010 = d2: window is ±(previous count) / 2^2 = ±(previous count) / 4 b0011 = d3: window is ±(previous count) / 2^3 = ±(previous count) / 8 ... b0111 = d7: window is ±(previous count) / 2^3 = ±(previous count) / 128 (default) etc.
reg_lk_win_sw_0	0	LK_WIN_SVAL determines the ±window within; the latest and previous number of pixel clocks in a sampling period must agree. 1 - Most recent count and previous count must match exactly to enable the stability duration counter to increment (default). 0 - Stability window deternined by LK_WIN_SW[4:1].

RX_LK_THRS_SVAL1 (0x2114)

BIT	7	6	5	4	3	2	1	0
Field	reg_lk_thrs_sval_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_lk_thrs_sval_7_0	7:0	Bits [7:0] of 20-bit value used as a PLL lock stability threshold. If the number of pixel clocks in a sampling period stays within the stability window determined by LK_WIN_SVAL for LK_THRS_SVAL number of sampling cycles, the PLL is locked, and the pll_unlocked interrupt INTR1[4] is deasserted.

RX_LK_THRS_SVAL2 (0x2115)

BIT	7	6	5	4	3	2	1	0
Field	reg_lk_thrs_sval_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_lk_thrs_sval_15_8	7:0	Bits [15:8] of 20-bit value used as a PLL lock stability threshold. If the number of pixel clocks in a sampling period stays within the stability window determined by LK_WIN_SVAL for LK_THRS_SVAL number of sampling cycles, the PLL is locked, and the pll_unlocked interrupt INTR1[4] is deasserted.

RX_LK_THRS_SVAL3 (0x2116)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_lk_thrs_sval_19_16[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
reg_lk_thrs_sval_19_16	3:0	Bits [19:16] of 20-bit value used as a PLL lock stability threshold. If the number of pixel clocks in a sampling period stays within the stability window determined by LK_WIN_SVAL for LK_THRS_SVAL number of sampling cycles, the PLL is locked, and the pll_unlocked interrupt INTR1[4] is deasserted.

RX_TCLK_FS (0x2117)*

BIT	7	6	5	4	3	2	1	0
Field	rhdmi_aud_sample_f_extn[1:0]		–	reg_fs_filter_en	rhdmi_aud_sample_f[3:0]			
Reset	0b00		–	0b1	0x1			
Access Type	Read Only		–	Write, Read	Read Only			

BITFIELD	BITS	DESCRIPTION
rhdmi_aud_sample_f_extn	7:6	Sampling frequency extended bits
reg_fs_filter_en	4	Enable update of the Fs number only if new Fs are acquired 3 times in the row

BITFIELD	BITS	DESCRIPTION
rhdmi_aud_sample_f	3:0	Sampling frequency. These bits correspond to the Channel Status bits 24, 25, 26, 27, where bit 24 = LSB and 27 = MSB. This Fs is extracted on the TCLK domain: 27 26 25 24 "0 1 0 0" - Fs = 22.05kHz "0 0 0 0" - Fs = 44.1kHz "1 0 0 0" - Fs = 88.2kHz "1 1 0 0" - Fs = 176.4kHz "0 1 1 0" - Fs = 24kHz "0 0 1 0" - Fs = 48kHz "1 0 1 0" - Fs = 96kHz "1 1 1 0" - Fs = 192kHz "0 0 1 1" - Fs = 32kHz "1 0 0 1" - Fs = 768kHz (192 x 4) for High Bit Rate Audio "0 0 0 1" - Sampling frequency not indicated

RX_ACR_CTRL3 (0x2118)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_cts_thresh[3:0]				reg_mclk_loopback	reg_log_win_ena	reg_post_div2_ena
Reset	–	0x1				0b1	0b0	0b0
Access Type	–	Write, Read				Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_cts_thresh	6:3	4-bit threshold value for the CTS change. Default is 1.
reg_mclk_loopback	2	This is for MCLK internal loopback: "1" internal loopback is enabled
reg_log_win_ena	1	Enable for simplified window (linear) for pll_unlocked
reg_post_div2_ena	0	Control for Post Divide value of PLL used for generating Audio Main Clock (MCLK). 0: Uses HW selected divide value. 1: Uses Divide by 2 of HW selected divide value.

RX_CHST6 (0x2119)

BIT	7	6	5	4	3	2	1	0
Field	aud_sample_f_coeff[3:0]				bit43	cgms_a_validity	cgms_a[1:0]	
Reset	0x0				0b0	0b0	0b00	
Access Type	Read Only				Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION
aud_sample_f_coeff	7:4	Audio sampling frequency coefficient. These bits correspond to the Channel Status bits 44, 45, 46, 47, where bit 44 = LSB and 47 = MSB: 47 46 45 44 "0 0 0 0" - Fs_coeff = No indication "1 0 0 0" - Fs_coeff = Equal to transmission sampling frequency "0 1 0 0" - Fs_coeff = 1/2 "1 1 0 0" - Fs_coeff = 1/4 "0 0 1 0" - Fs_coeff = 1/8 "1 0 1 0" - Fs_coeff = 1/16 "0 1 1 0" - Fs_coeff = 1/32 "1 1 1 0" - Fs_coeff = Reserved "0 0 0 1" - Fs_coeff = Reserved "1 0 0 1" - Fs_coeff = Reserved "0 1 0 1" - Fs_coeff = Reserved "1 1 0 1" - Fs_coeff = x32 "0 0 1 1" - Fs_coeff = x16 "1 0 1 1" - Fs_coeff = x8 "0 1 1 1" - Fs_coeff = x4 "1 1 1 1" - Fs_coeff = x2
bit43	3	Not indicated.
cgms_a_validity	2	CGMS-A validity 0 - No indication 1 - CGMS-A valid
cgms_a	1:0	CGMS-A

RX_CHST7 (0x211A)

BIT	7	6	5	4	3	2	1	0
Field	bit55_49[6:0]							info_in_pcm_signal
Reset	0b0000000							0b0
Access Type	Read Only							Read Only

BITFIELD	BITS	DESCRIPTION
bit55_49	7:1	Reserved (0000000).
info_in_pcm_signal	0	Information hidden in PCM signal; 0 - No indication 1 - Additional information in LSB

RX_I2S_CTRL1 (0x2126)*

BIT	7	6	5	4	3	2	1	0
Field	reg_invalid_en	reg_clk_edge	reg_size	reg_msb	reg_ws	reg_justify	reg_data_dir	reg_1st_bit
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_invalid_en	7	Enable sending off all data; even invalid one according to the aud_length_max and aud_length fields extracted from the SPDIF stream: 0 - Send only valid data (default). 1 - Send all data.
reg_clk_edge	6	SCK: Sample edge positive/negative 0 - SD0 and WS change on the positive edge of the SCK 1 - SDO and WS change on the negative edge of the SCK
reg_size	5	Size of word: 0 - 32 bits (default). 1 - 16 bits.
reg_msb	4	SD: MSb sign-extended 0 - MSb sign-extended (default) 1 - Not extended
reg_ws	3	WS: Left/Right polarity 0 - Left polarity when Word Select is low (default) 1 - Left polarity when Word Select is high
reg_justify	2	SD: Left-/Right-justified 0 - Data is left-justified (default) 1 - Data is right-justified
reg_data_dir	1	SD: MSb/LSb first 0 - MSb first (default) 1 - LSb first
reg_1st_bit	0	WS to SD: First bit shift 0 - First bit shift; Philips spec.(default) 1 - No shift

RX_I2S_CTRL2 (0x2127)*

BIT	7	6	5	4	3	2	1	0
Field	reg_sd3_en	reg_sd2_en	reg_sd1_en	reg_sd0_en	reg_mclk_en	reg_mute_flat	reg_vucp	reg_pcm
Reset	0b0	0b0	0b0	0b1	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_sd3_en	7	SD3 output control 0 - SD3 is disabled (default) 1 - SD3 is enabled.
reg_sd2_en	6	SD2 output control 0 - SD2 is disabled (default) 1 - SD2 is enabled.
reg_sd1_en	5	SD1 output control 0 - SD1 is disabled (default) 1 - SD1 is enabled.
reg_sd0_en	4	SD0 output control 0 - SD0 is disabled (default) 1 - SD0 is enabled.
reg_mclk_en	3	MCLK output enable control 0 - 3-state MCLKOUT (default) 1 - MCLKOUT enabled

BITFIELD	BITS	DESCRIPTION
reg_mute_flat	2	1 - Enable mute of the channel if "flat/invalid" bit is acquired from the audio packet 0 - Do not enable mute
reg_vucp	1	0 - 24 bits of read-only data sent via I2S (default) 1 - 28 bits of data sent via I2S. The VUCP bits are sent as well.
reg_pcm	0	I2S data pass select: 0 - Pass whatever data is in SPDIF packet. 1 - Only pass data from SPDIF packet if it is recognized as PCM data. If non-PCM data detected, send 0 as the data. (default)

RX_I2S_MAP (0x2128)*

BIT	7	6	5	4	3	2	1	0
Field	reg_sd3_map[1:0]		reg_sd2_map[1:0]		reg_sd1_map[1:0]		reg_sd0_map[1:0]	
Reset	0b11		0b10		0b01		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
reg_sd3_map	7:6	Map Data 1 of the four FIFO audio streams into the SD3: 00 - Map audio stream from FIFO 0 into the SD3 01 - Map audio stream from FIFO 1 into the SD3 10 - Map audio stream from FIFO 2 into the SD3 11 - Map audio stream from FIFO 3 into the SD3 (default)
reg_sd2_map	5:4	Map Data 1 of the four FIFO audio streams into the SD2: 00 - Map audio stream from FIFO 0 into the SD2 01 - Map audio stream from FIFO 1 into the SD2 10 - Map audio stream from FIFO 2 into the SD2 (default) 11 - Map audio stream from FIFO 3 into the SD2
reg_sd1_map	3:2	Map Data 1 of the four FIFO audio streams into the SD1: 00 - Map audio stream from FIFO 0 into the SD1 01 - Map audio stream from FIFO 1 into the SD1 (default) 10 - Map audio stream from FIFO 2 into the SD1 11 - Map audio stream from FIFO 3 into the SD1
reg_sd0_map	1:0	Map Data 1 of the four FIFO audio streams into the SD0: 00 - Map audio stream from FIFO 0 into the SD0 (default) 01 - Map audio stream from FIFO 1 into the SD0 10 - Map audio stream from FIFO 2 into the SD0 11 - Map audio stream from FIFO 3 into the SD0

RX_AUDRX_CTRL (0x2129)*

BIT	7	6	5	4	3	2	1	0
Field	reg_i2s_length_en	reg_inv_cor_en	reg_hw_mute_en	reg_pass_spdif_err	reg_pass_aud_err	reg_i2s_mode	reg_spdif_mode	reg_spdif_en
Reset	0b0	0b0	0b0	0b1	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_i2s_length_en	7	Enable overwrite of the length related Channel Status bits for the I2S data: 0 - Take from the HDMI packet (default); 1 - Take from the CHST[7:4].

BITFIELD	BITS	DESCRIPTION
reg_inv_cor_en	6	Enable Sine Wave Reconstruction: 0 - Pass-through (default). 1 - Will start to reconstruct sine wave based on the last amplitude and frequency.
reg_hw_mute_en	5	Enable hardware smooth mute: 0 - During the mute, the hardware only repeats the previous good sample (default); 1 - During the mute, the hardware gradually decrements to 0db
reg_pass_spdif_err	4	0 - Do not pass SPDIF type of errors (Parity or VUC left/right sub-frame mismatch) (i.e., conceal audio errors by repeating last good sample). 1 - Pass all audio data, regardless of errors (default).
reg_pass_aud_err	3	0 - Do not pass ECC audio errors (i.e., conceal audio errors by repeating last good sample): Audio data is repeated unless valid B preamble is acquired, and Channel Status is set based on the following logic: • If reg_pcm (0x2127) is 0, then Channel Status bit is set to the same bit from the last good SPDIF block. • If reg_pcm (0x2127) is 1, then Channel Status is set to Channel Status bit from the last good sample. 1 - Pass all audio data, regardless of ECC audio errors (default).
reg_i2s_mode	2	I^2S Output mode. 0 - All I^2S outputs are grounded - SD, SCK, WS (default). 1 - SCK and WS toggle; SD is "on" or "off" depending on the value of the reg_sd0_en (I2S_CTRL2[4]).
reg_spdif_mode	1	SPDIF flat line enable. 0 - SPDIF output always produces valid biphase mark encoded data even during flat line (default). 1 - SPDIF output is grounded if flat line is detected
reg_spdif_en	0	0 - SPDIF output disabled (defaut); 1 - SPDIF output stream is enabled

RX_CHST1 (0x212A)

BIT	7	6	5	4	3	2	1	0
Field	bit6_7[1:0]		bit3_4_5[2:0]			bit2	bit1	bit0
Reset	0b00		0b000			0b0	0b0	0b0
Access Type	Read Only		Read Only			Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
bit6_7	7:6	"00" - Mode 0
bit3_4_5	5:3	"000" - Two audio channels without pre-emphasis "100" - Two audio channels with 50/15 us pre-emphasis.
bit2	2	0 - Software for which copyright is asserted 1 - Software for which no copyright is asserted
bit1	1	0 - Audio sample word represents linear PCM samples 1 - Audio sample word used for other purposes
bit0	0	Primary application: 0 - Consumer 1 - Professional

RX_CHST3a (0x212C)

BIT	7	6	5	4	3	2	1	0
Field	aud_ch_num1[3:0]				aud_source1[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
aud_ch_num 1	7:4	Channel number; bit 20 - LSB; bit 23 MSB. The Channel number is specific to the channel.	0b0000: Do not take into account 0b1000: A (Left channel for stereo channel format) 0b0100: B (Right channel for stereo channel format) 0b1100: C ... 0b1111: O
aud_source1	3:0	Source number; bit 16 - LSB; bit 19 MSB: The source number is specific to the channel	0b0000: Do not take into account 0b1000: 1 0b0100: 2 0b1100: 3 ... 0b1111: 15

RX_MUTE_DIV (0x212D)

BIT	7	6	5	4	3	2	1	0
Field	reg_div_incr[7:0]							
Reset	0x02							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_div_incr	7:0	Part of the Hardware Soft Mute logic. The value programmed in this register sets the step of hardware soft mute. The higher the value, the faster the soft mute is done, and the steeper the decreasing curve is.

RX_SW_OW (0x212E)*

BIT	7	6	5	4	3	2	1	0
Field	reg_swap[3:0]				–	reg_cs_bit2	–	reg_ow_en
Reset	0x0				–	0b0	–	0b0
Access Type	Write, Read				–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_swap	7:4	Left/Right Channel Swap control: Bit 4: Swap enable for Channel 0 ("0" - no swap) Bit 5: Swap enable for Channel 1 ("0" - no swap) Bit 6: Swap enable for Channel 2 ("0" - no swap) Bit 7: Swap enable for Channel 3 ("0" - no swap)
reg_cs_bit2	2	Overwrite data for Channel Status bit 2, if overwrite is enabled.
reg_ow_en	0	Overwrite enable for Channel Status bits 2 and 8-15

RX_OW_15_8 (0x212F)*

BIT	7	6	5	4	3	2	1	0
Field	reg_cs_bit15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cs_bit15_8	7:0	Overwrite data for Channel Status bits 8-15, if overwrite is enabled.

RX_CHST4 (0x2130)

BIT	7	6	5	4	3	2	1	0
Field	aud_sample_f_extn[1:0]		aud_accuracy[1:0]		aud_sample_f[3:0]			
Reset	0b00		0b00		0x1			
Access Type	Read Only		Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
aud_sample_f_extn	7:6	Sampling frequency extension. These bits correspond to the Channel Status bits 30, 31, where bit 30 = LSB and 31 = MSB. Sampling frequency extension with sampling frequency bits 24 to 31: 31 30 27 26 25 24 "0 0 0 1 0 1" - Fs = 384kHz "0 1 0 1 0 1" - Fs = 1536kHz "1 1 0 1 0 1" - Fs = 1024kHz "0 0 1 1 0 1" - Fs = 3528kHz "1 0 1 1 0 1" - Fs = 7056kHz "0 1 1 1 0 1" - Fs = 14112kHz "0 0 1 0 1 1" - Fs = 64kHz "1 0 1 0 1 1" - Fs = 128kHz "0 1 1 0 1 1" - Fs = 256kHz "1 1 1 0 1 1" - Fs = 512kHz
aud_accuracy	5:4	Clock accuracy: "00" Level II "10" Level I "01" Level III
aud_sample_f	3:0	Sampling frequency. These bits correspond to the Channel Status bits 24 to 27, where bit 24 = LSB and 27 = MSB: 27 26 25 24 "0 1 0 0" - Fs = 22.05 kHz "0 0 0 0" - Fs = 44.1 kHz "1 0 0 0" - Fs = 88.2 kHz "1 1 0 0" - Fs = 176.4 kHz "0 1 1 0" - Fs = 24 kHz "0 0 1 0" - Fs = 48 kHz "1 0 1 0" - Fs = 96 kHz "1 1 1 0" - Fs = 192 kHz "0 0 1 1" - Fs = 32 kHz "1 0 0 1" - Fs = 768 kHz (192 x 4) for High Bit Rate Audio "0 0 0 1" - Sampling frequency not indicated

RX_CHST5 (0x2131)

BIT	7	6	5	4	3	2	1	0
Field	aud_org_fs[3:0]				aud_length[2:0]			aud_length_max
Reset	0x0				0b101			0b1
Access Type	Read Only				Read Only			Read Only

BITFIELD	BITS	DESCRIPTION
aud_org_fs	7:4	Original Fs
aud_length	3:1	Channel Status bits 33 to 35, where bit 33 = LSB and 35 = MSB max 24 max 20 "000" not indicated (default) not indicated (default) "001" 20 bits 16 bits "010" 22 bits 18 bits "100" 23 bits 19 bits "101" 24 bits 20 bits "110" 21 bits 17 bits
aud_length_max	0	Channel Status bits 32: "0" - Max audio sample word length is 20 bits "1" - Max audio sample word length is 24 bits

RX_AUDO_MUTE (0x2132)*

BIT	7	6	5	4	3	2	1	0
Field	reg_i2s_length[3:0]				reg_ch3_mute	reg_ch2_mute	reg_ch1_mute	reg_ch0_mute
Reset	0x0				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_i2s_length	7:4	Overwrite number for bits 35-32 of the Channel Status (CHST5[3:0])
reg_ch3_mute	3	Channel 3 mute control: "1" mute
reg_ch2_mute	2	Channel 2 mute control: "1" mute
reg_ch1_mute	1	Channel 1 mute control: "1" mute
reg_ch0_mute	0	Channel 0 mute control: "1" mute

RX_AUDP_MUTE (0x2137)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_spdif4tdm_en	reg_spdif4i2s_en	aac_audio_mute	–	reg_mute_out_pol	reg_audio_mute	–
Reset	–	0b0	0b0	0b0	–	0b0	0b0	–
Access Type	–	Write, Read	Write, Read	Read Only	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION
reg_spdif4tdm_en	6	Enable SPDIF over TDM
reg_spdif4i2s_en	5	Enable SPDIF over I^2S

BITFIELD	BITS	DESCRIPTION
aac_audio_mute	4	Audio Mute Status 1 - Muted; (by either AAC or reg_audio_mute) 0 - Active
reg_mute_out_pol	2	Polarity of the MUTE_OUT: 1 - Negative; 0 - Positive (default).
reg_audio_mute	1	Audio Mute (repeat last good data sample): 1 - Mute; 0 - Not mute (default).

RX_PD_SYS3 (0x213D)

BIT	7	6	5	4	3	2	1	0
Field	reg_audio_toggle_mode	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_audio_toggle_mode	7	Audio Output Toggle mode enable 0 - Normal audio operations. 1 - Audio output toggle by MCLK.

RX_TDM_CTRL1 (0x2140)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_tdm_fs_msb[1:0]		reg_tdm_ch_num[1:0]		reg_tdm_mode
Reset	–	–	–	0b01		0b11		0b0
Access Type	–	–	–	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_tdm_fs_msb	4:3	Delay between the valid edge of FS and MSB of data.	0b00: No delay 0b01: 1-cycle delay 0b10: 2-cycle delay 0b11: 3-cycle delay
reg_tdm_ch_num	2:1	This field specifies the number of channels on TDM.	0b00: 2-channel 0b01: 4-channel 0b10: 6-channel 0b11: 8-channel
reg_tdm_mode	0	0 - TDM output disabled (defaut); 1 - TDM output stream is enabled	

RX_TDM_CTRL2 (0x2141)*

BIT	7	6	5	4	3	2	1	0
Field	reg_tdm_fs_len[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_tdm_fs_len	7:0	The length of FS signal. 8'b0: 256 clock cycles; 8'd1: 1 clock cycle; 8'd2: 2 clock cycles …

VID_XPCLK_MULT (0x2166)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_vid_pclk_cnt_mult_3_0[3:0]			
Reset	–	–	–	–	0x3			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
reg_vid_pclk_cnt_mult_3_0	3:0	PCLK Count Multiply mode. 4-bit value with adding [4:3] of this register. 4'b0000: Multiply by 1 4'b0001: Multiply by 2 4'b0010: Multiply by 4 4'b0011: Multiply by 8 4'b0100: Multiply by 16 4'b0101: Multiply by 32 4'b0110: Multiply by 64 4'b0111: Multiply by 128 4'b1000: Multiply by 256 4'b1001: Multiply by 512 4'b1010: Multiply by 1024 4'b1011: Multiply by 2048 4'b1100: Multiply by 4096 4'b1101: Multiply by 8192 4'b1110: Multiply by 16384 4'b1111: Multiply by 32768

VID_XPCLK_Base (0x2167)

BIT	7	6	5	4	3	2	1	0
Field	reg_vid_pclk_cnt_base_7_0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_vid_pclk_cnt_base_7_0	7:0	The base of PCLK count is 255 (decimal). This register must come with 0x68 for multiplying 255 with a number to be the value of XPCNT.

VID_XPCLK_EN (0x2168)

BIT	7	6	5	4	3	2	1	0
Field	reg_vres_xclk_diff[3:0]				–	–	–	reg_vid_xclkpclk_en
Reset	0x5				–	–	–	0b1
Access Type	Write, Read				–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_vres_xclk_diff	7:4	Video Resolution Change Difference XCLK Count: This field contains the Video Resolution Change minimum difference in XCLK cycles. The value programmed into this field indicates the minimum number of XCLK cycles of difference to be observed in the current video frame with the previous to identify a Video Resolution change on the HDMI/MHL link.
reg_vid_xclkpclk_en	0	Enable for updating XCLK to PCLK counter (Note: SW gets the correct XPCNT need to set and clear this bit before reading the XPCNT) 0x0: Disable the real time update for SW to read the static values 0x1: Enable updating on the fly values (default)

VID_XPBASE0 (0x2169)

BIT	7	6	5	4	3	2	1	0
Field	reg_xp_base_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_xp_base_7_0	7:0	Base number for the VIDA_XPCNT register

VID_XPBASE1 (0x216A)

BIT	7	6	5	4	3	2	1	0
Field	reg_xp_base_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_xp_base_15_8	7:0	Base number for the VIDA_XPCNT register

VID_XPBASE2 (0x216B)

BIT	7	6	5	4	3	2	1	0
Field	reg_xp_base_23_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_xp_base_23_16	7:0	Base number for the VIDA_XPCNT register. 24-bit value with 0x06B and 0x06C.

VID_XP_THRSH (0x216C)

BIT	7	6	5	4	3	2	1	0
Field	reg_xp_thrsh[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_xp_thrsh	7:0	Threshold for the VID_XPCNT register

RX_VID_XPCNT1 (0x216D)

BIT	7	6	5	4	3	2	1	0
Field	aac_xclk_in_pclk_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
aac_xclk_in_pclk_7_0	7:0	Number of XCLK per 2048 Video CLK

RX_VID_XPCNT2 (0x216E)

BIT	7	6	5	4	3	2	1	0
Field	aac_xclk_in_pclk_15_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
aac_xclk_in_pclk_15_8	7:0	Number of XCLK per 2048 Video CLK

RX_VID_XPCNT3 (0x216F)

BIT	7	6	5	4	3	2	1	0
Field	aac_xclk_in_pclk_23_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
aac_xclk_in_pclk_23_16	7:0	Number of XCLK per 2048 Video CLK. 24-bit value with 0x06Fand 0x06E.

RX_APLL_STAT (0x218D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	acr_dpll_lock
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
acr_dpll_lock	0	Indicates phase error is within lock range when asserted.

RX_SM_NAPLL_STAT (0x219D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	napll_lock
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
napll_lock	0	PLL Lock Indicator (LOCK indicates no cycle slips in 256 consecutive FREF/REFDIV cycles). To be used to integrate SMIC40LL audio PLL.

RX_AVG_WINDOW (0x21A0)

BIT	7	6	5	4	3	2	1	0
Field	reg_avg_window[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
reg_avg_window	7:0	Size of average window for fine_mclk_out	0x00: No average Others: Number of ACR packet duration

DACR_MCLK_CTRL (0x21A1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_dacr_mclk_out_en
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_dacr_mclk_out_en	0	Selection between DACR mclk_out and fine_mclk_out as source of MCLK. 0: fine_mclk_out is source of MCLK 1: mclk_out is source of MCLK

DACR_REF_CLK_SEL (0x21A2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	reg_dacr_ref_clk_sel[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
reg_dacr_ref_clk_sel	1:0	Select signal to PHY for selecting the required reference clock for Digital ACR. Selection logic below should be present in PHY logic. 0b11: mint8_div3[1] 0b10: mint8_div2 0b01: 1'b0 0b00: div5out

AEC4_CTRL (0x21B1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	reg_aac_ctrl 4_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved
RSVD	6	Reserved
RSVD	5	Reserved
RSVD	4	Reserved
RSVD	3	Reserved
RSVD	2	Reserved
RSVD	1	Reserved
reg_aac_ctrl4_0	0	1: Enable clear of interrupts after every stability check 0: Do not enable

AEC3_CTRL (0x21B2)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_ctrl 3_7	reg_aac_ctrl 3_6	reg_aac_ctrl 3_5	reg_aac_ctrl 3_4	reg_aac_ctrl 3_3	reg_aac_ctrl 3_2	reg_aac_ctrl 3_1	reg_aac_ctrl 3_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_aac_ctrl3_7	7	If "1", set MUTE_OUT only if AAC is done with soft mute
reg_aac_ctrl3_6	6	Bit [6] - When "1", enable AAC to check PCLK stable before unmuting.
reg_aac_ctrl3_5	5	Bit [5] - When "1", enable AAC to check if cable is unplugged before unmuting.

BITFIELD	BITS	DESCRIPTION
reg_aac_ctrl3_4	4	Bit [4] - When "1", enable AAC to check power down before unplugging.
reg_aac_ctrl3_3	3	Bit [3] - When "1", enable AAC to check for clock detect before unmuting.
reg_aac_ctrl3_2	2	Bit [2] - When "1", enable AAC to check for SCDT before unmuting.
reg_aac_ctrl3_1	1	Bit [1] - When "1", enable AAC to unmute only if "new audio packet" interrupt is present.
reg_aac_ctrl3_0	0	Bit [0] - When "1", enable AAC to unmute only if "got CTS" interrupt.

AEC2_CTRL (0x21B3)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_ctrl2_7	reg_aac_ctrl2_6	reg_aac_ctrl2_5	reg_aac_ctrl2_4	reg_aac_ctrl2_3	reg_aac_ctrl2_2	reg_aac_ctrl2_1	reg_aac_ctrl2_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_aac_ctrl2_7	7	Bit [7] - When "1", enable AAC will not unmute if "CTS dropped" exception is present.
reg_aac_ctrl2_6	6	Bit [6] - When "1", enable AAC will not unmute if "CTS reused" exception is present.
reg_aac_ctrl2_5	5	Bit [5] - When "1", enable AAC will not unmute if "N changed" exception is present.
reg_aac_ctrl2_4	4	Bit [4] - When "1", enable AAC will not unmute if "CTS changed" exception is present.
reg_aac_ctrl2_3	3	Bit [3] - When "1", enable AAC will not unmute if "FIFO under-run" exception is present.
reg_aac_ctrl2_2	2	Bit [2] - When "1", enable AAC will not unmute if "FIFO over-run" exception is present.
reg_aac_ctrl2_1	1	Bit [1] - When "1", enable AAC will not unmute if "PLL unlock" exception is present.
reg_aac_ctrl2_0	0	Bit [0] - When "1", enable AAC unmute only if "hdmi_mode" indication is present.

AEC1_CTRL (0x21B4)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_ctrl_7	reg_aac_ctrl_6	reg_aac_ctrl_5	reg_aac_ctrl_4	reg_aac_ctrl_3	reg_aac_ctrl_2	reg_aac_ctrl_1	reg_aac_ctrl_0
Reset	0b0	0b0	0b0	0b1	0b0	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_aac_ctrl_7	7	aac_ctrl[7] - Enable for the ACR init during ASC: "1" - enable
reg_aac_ctrl_6	6	aac_ctrl[6] - Enable for the ACR reset during ASC: "1" - enable

BITFIELD	BITS	DESCRIPTION
reg_aac_ctrl_5	5	aac_ctrl[5] - Select between method 1 and 2 of checking for audio stability check. During unmute, AAC performs first cable stability check (CSC). If it passes, CSC performs video stability check (VSC). If it passes, VSC performs audio stability check (ASC). If it passes ASC, then it unmutes: "1" - Enable more sophisticated method "0" - Enable simpler method (recommended)
reg_aac_ctrl_4	4	aac_ctrl[4] - Enable for the mute time out "1" - Brake mute function if it is longer than 20'hF_FFFF XCLK clocks (recommended) "0" - Disable time out
reg_aac_ctrl_3	3	aac_ctrl[3] - Enable brake of unmute algorithm on lost of sync; CLKDT or cable unplug. "1" - Enable "0" - Disable (recommended)
reg_aac_ctrl_2	2	aac_ctrl[2] - Enable for new unmute main algorithm "1" - Enable (recommended) "0" - Disable
reg_aac_ctrl_1	1	aac ctrl [1] - Enabled for ignoring AAC stop function, works only with aac_ctrl[0] = 1: "1" - Ignore AAC stop function and disable audio I/Os as soon as audio is muted (recommended) "0" - Wait for the stop function to finish
reg_aac_ctrl_0	0	aac_ctrl[0] - Enable simple method to control audio output enables "1" - Enable (recommended) "0" - Disable (more sophisticated method is used)

AEC0_CTRL (0x21B5)

BIT	7	6	5	4	3	2	1	0
Field	reg_ctrl_acr_en	reg_aac_exp_sel	reg_aac_out_off_en	aud_div_min	aac_mute_stat	–	reg_aac_all	reg_aac_en
Reset	0b1	0b1	0b1	0b0	0b0	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Read Only	Read Only	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_ctrl_acr_en	7	Enable AAC to Control ACR functions: MCLK and Fs setup. "1" - Enabled (default)
reg_aac_exp_sel	6	Force ASC to look only at enabled exceptions: "1" - Enabled (default)
reg_aac_out_off_en	5	Enable AAC to turn off SD0, SD1, SD2, SD3, SCK, and SPDIF. Default AAC does it.
aud_div_min	4	Status of the hardware soft mute: "1" - Output of mute is "0"
aac_mute_stat	3	OR of all unmasked exceptions
reg_aac_all	1	Enable hardware auto unmute: "0" - Disabled (default)
reg_aac_en	0	Enabled hardware auto mute: "0" - Disabled (default)

RX_AEC_EN1 (0x21B6)

BIT	7	6	5	4	3	2	1	0
Field	reg_exp_en_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_exp_en_7_0	7:0	Enable for Exception: Bit [0] - Cable unplug; Bit [1] - PLL unlocked; Bit [2] - ACR N changed Bit [3] - ACR CTS changed; Bit [4] - Video clock changed; Bit [5] - InfoFrame CP Mute set; Bit [6] - Sync detect; Bit [7] - Clock detect

RX_AEC_EN2 (0x21B7)

BIT	7	6	5	4	3	2	1	0
Field	reg_exp_en_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_exp_en_15_8	7:0	Enable for Exception: Bit [8] - HDMI mode; Bit [9] - Audio FIFO underun; Bit [10] - Audio FIFO overun Bit [11] - CTS reused Bit [12] - Change of the Fs; Bit [13] - Change of interlaced; Bit [14] - Polarity change; Bit [15] - H resolution change

RX_AEC_EN3 (0x21B8)

BIT	7	6	5	4	3	2	1	0
Field	reg_exp_en_23_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_exp_en_23_16	7:0	Enable for Exception: Bit [16] - V resolution changed; Bit [17] - Link error Bit [18] - Fn CLK changed; Bit [19] - DSD invalid; Bit [20] - HBRA on is detected; Bit [21] - Got audio flat bit; Bit [22] - DSD on is detected Bit [23] - CTS dropped exception is detected

RX_SYS_PSTOP (0x21BA)

BIT	7	6	5	4	3	2	1	0
Field	reg_pclk_max[6:0]							reg_pstop_en
Reset	0b0011010							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
reg_pclk_max	7:1	Bits 7:1 of the PCLK max count. Default is 0x34 and upper 11:8 bits are set to 4'b0001
reg_pstop_en	0	Enable for the auto stop of the PCLK if it is above 165MHz. This is done by counting the number of XCLK (28Mhz) in 2024 PCLK. If number of XCLK in 2024 PCLK is less than 330 (PCLK is more than 170MHz), then PCLK is stopped if this bit is set to "1". Afterwards, firmware needs to set analog core registers, then disable this bit.

AAC_CSC_ERR (0x21F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_aac_csc_err[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
reg_aac_csc_err	4:0	AAC CSC Error

AAC_VSC_ERR (0x21F4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_aac_vsc_err[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
reg_aac_vsc_err	3:0	AAC VSC Error

AAC_ASC_ERR (0x21F5)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_asc_err[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_aac_asc_err	7:0	AAC ASC Error

AAC_EXP_CAPT_L (0x21FB)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_exp_capt_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_aac_exp_capt_7_0	7:0	AAC Exception Capture Status

AAC_EXP_CAPT_M (0x21FC)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_exp_capt_15_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_aac_exp_capt_15_8	7:0	AAC Exception Capture Status

AAC_EXP_CAPT_H (0x21FD)

BIT	7	6	5	4	3	2	1	0
Field	reg_aac_exp_capt_23_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_aac_exp_capt_23_16	7:0	AAC Exception Capture Status

ACRGCTRL0 (0x21FE)

BIT	7	6	5	4	3	2	1	0
Field	reg_acr_gen_ctrl0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_acr_gen_ctrl0	7:0	Enable logic for the video stability checkpoints. If all of them are disabled, then VSC will pass: Bit [2] - If "1", then will check for intr_vid_polChange (reg. 0x07B[2]) Bit [3] - If "1", then will check for intr_vid_hResChange (reg. 0x07B[3]) Bit [4] - If "1", then will check for intr_vid_vResChange (reg. Bx07B[4]) Bit [5] - If "1", then will check for intr_vid_clk_change (reg. 0x072[0]) Other bits - Unused

RX_PWD_CTRL (0x2301)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	reg_tmds_mode_inv	–	–	RSVD	RSVD
Reset	0b0	–	0b0	0b0	–	–	0b0	0b0
Access Type		–		Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
reg_tmds_mode_inv	4	Default = 0; This bit is XORed with mode signal coming from TMDS core and then used to send the data out in dvi_rx_dig Bypass mode	0b0: Do not invert mode signal 0b1: Invert mode signal

RX_PWD_SRST3 (0x2304)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_tdm_srst	–	–	–	–
Reset	–	–	–	0b0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_tdm_srst	4	Active high reset soft signal for TDM. Power on reset and should be controlled by software. (External synchronizer is required)

RX_PWD_SRST (0x2305)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	reg_acr_rst_auto	reg_aac_rst	reg_dc_fifo_rst	RSVD	reg_acr_rst	reg_fifo_rst	reg_aud_fifo_rst_auto
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_acr_rst_auto	6	Auto-ACR Reset: 0 - Manual ACR reset (default) 1 - Auto ACR reset whenever SCDT = 0 If SRST (reg. 0x005[0]) is applied, then PCLK stop interrupt may continue to be stuck in asserted condition. Need to assert this reset to clear receiving side of the handshaking logic.
reg_aac_rst	5	Auto-Audio Config Reset: 1 - Reset AAC logic; 0 - Normal operation (default).
reg_dc_fifo_rst	4	Deep-Color FIFO Reset. Note: Asserting Software Reset also resets (flush) the FIFO: 1 - Reset (flush) FIFO. 0 - Normal operation (default).
reg_acr_rst	2	Audio Clock Regeneration Reset: 1 - Reset ACR clock divider circuits; 0 - Normal operation (default).
reg_fifo_rst	1	Audio FIFO Reset. Note: Asserting Software Reset also resets (flush) the FIFO: 1 - Reset (flush) FIFO. 0 - Normal operation (default).
reg_aud_fifo_rst_auto	0	Auto-Audio FIFO Reset: 0 - Manual audio FIFO reset (default) 1 - Auto audio FIFO reset whenever audio FIFO overflows or under runs

RX_STATE_PWD (0x2306)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	vsync_cap	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION
vsync_cap	2	State of VSYNC: This signal indicates the state/level of VSYNC in the hardware. It is more or less useful for hardware debug in case of any basic check needed. No software action is required on this status register.

RX_SYS_CTRL1 (0x2307)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	reg_sync_pol	RSVD
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
reg_sync_pol	1	1 - Sync polarity is positive (default). 0 - Sync polarity is negative.

SYS_TMDS_CH_MAP (0x230E)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_di_ch2_sel[1:0]		reg_di_ch1_sel[1:0]		reg_di_ch0_sel[1:0]	
Reset	–	–	0b10		0b01		0b00	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
reg_di_ch2_sel	5:4	TMDS data select for Channel 1	00: Will take TMDS PHY data[23:16] 01: Will take TMDS PHY data[15:8] 10: Will take TMDS PHY data[7:0] (default) 11: Will assign zero
reg_di_ch1_sel	3:2	TMDS data select for Channel 1	00: Will take TMDS PHY data[23:16] 01: Will take TMDS PHY data[15:8] (default) 10: Will take TMDS PHY data[7:0] 11: Will assign zero
reg_di_ch0_sel	1:0	TMDS data select for Channel 0	00: Will take TMDS PHY data[23:16] (default) 01: Will take TMDS PHY data[15:8] 10: Will take TMDS PHY data[7:0] 11: Will assign zero

SYS_TMDS_D_IR (0x230F)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_phy_di_dff_en	reg_di_ch2_invt	reg_di_ch1_invt	reg_di_ch0_invt	reg_di_ch2_bsi	reg_di_ch1_bsi	reg_di_ch0_bsi
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_phy_di_dff_en	6	Enable for DFF latching data coming from TMDS PHY	0: Enable latch (always leave as 0) 1: Disable latch
reg_di_ch2_invt	5	Select for Channel 2 to invert data	0: No inversion 1: Invert
reg_di_ch1_invt	4	Select for Channel 1 to invert data	0: No inversion 1: Invert

BITFIELD	BITS	DESCRIPTION	DECODE
reg_di_ch0_invt	3	Select for Channel 0 to invert data:	0: No inversion 1: Invert
reg_di_ch2_bsi	2	Select for Channel 2 between [7:0] and [0:7] format	0: Select [7:0] 1: Select [0:7]
reg_di_ch1_bsi	1	Select for Channel 1 between [7:0] and [0:7] format	0: Select [7:0] 1: Select [0:7]
reg_di_ch0_bsi	0	Select for Channel 0 between [7:0] and [0:7] format	0: Select [7:0] 1: Select [0:7]

RX_RPT_RDY_CTRL (0x2310)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_hdmi_mode_clr_en	reg_fifordy_clr_en[2:0]		
Reset	–	–	–	–	0b1	0b111		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
reg_hdmi_mode_clr_en	3	Enable clear of BSTATUS HDMI mode if no PWR5V
reg_fifordy_clr_en	2:0	Bit [0]: Enable clear of FIFO_RDY if CKDT interrupt is set Bit [1]: Enable clear of FIFO_RDY if SKDT interrupt is set Bit [2]: Enable clear of FIFO_RDY if no PWR5V interrupt is set This is also used to clear the HDMI mode enable when reg_hdmi_mode_clr_en is set

RX_PWD_SRST2 (0x2311)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	reg_dacr_rst	RSVD	RSVD	RSVD	RSVD
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type		–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
reg_dacr_rst	4	Digital Audio Clock Regeneration Soft Reset: 1 - Resets (DACR) Digital clock recovery circuits 0 - Normal operation (default).

RX_SW_HDMI_MODE (0x2322)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	reg_hdmi_mode_sw_value	reg_hdmi_mode_overwrite
Reset	–	–	–	–	–	0b1	0b0	0b0
Access Type	–	–	–	–	–		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_hdmi_mode_sw_value	1	HDMI Mode Software Overwrite Value
reg_hdmi_mode_overwrite	0	If "1", overwrite HDMI mode hardware value with software value

RX_PREAMBLE_CRIT (0x2323)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_preamble_cri[4:0]				
Reset	–	–	–	0b00110				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
reg_preamble_cri	4:0	Preamble criteria: Selects the required number of repetition for valid preamble

RX_AUDP_FILT (0x2325)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	reg_byp_dvifilt	reg_byp_sync	reg_byp_dalign
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_byp_dvifilt	2	1 - Disable DVI filtering (default 0)
reg_byp_sync	1	1 - Set disables HSYNC/VSYNC glitch filtering (default 0 - clear)
reg_byp_dalign	0	1 - Set disables data alignment to DE (default 0 - clear)

RX_AUDP_FIFO (0x2326)

BIT	7	6	5	4	3	2	1	0
Field	–	hdmi_fifo_diff[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
hdmi_fifo_diff	6:0	FIFO read/write PTR difference

VID_BLANK_DATA0 (0x2328)

BIT	7	6	5	4	3	2	1	0
Field	ri_vid_blank_data_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ri_vid_blank_data_7_0	7:0	Video Blank Data: This register controls bits [7:0] of the Video Blank Data muxed with the output from tclk2pclk converter on an AV Mute through a GCP. When an AV Mute is received through a GCP, the value in this register contains the blank data to be routed to the Video Processing block according to the input video format and color depth. [11:0] - lane0 [23:12] - lane1 [35:24] - lane2

VID_BLANK_DATA1 (0x2329)

BIT	7	6	5	4	3	2	1	0
Field	ri_vid_blank_data_15_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ri_vid_blank_data_15_8	7:0	Video Blank Data: This register controls bits [15:8] of the Video Blank Data muxed with the output from tclk2pclk converter on an AV Mute through a GCP. When an AV Mute is received through a GCP, the value in this register contains the blank data to be routed to the Video Processing block according to the input video format and color depth. [11:0] - lane0 [23:12] - lane1 [35:24] - lane2

VID_BLANK_DATA2 (0x232A)

BIT	7	6	5	4	3	2	1	0
Field	ri_vid_blank_data_23_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ri_vid_blank_data_23_16	7:0	Video Blank Data: This register controls bits [23:16] of the Video Blank Data muxed with the output from tclk2pclk converter on an AV Mute through a GCP. When an AV Mute is received through a GCP, the value in this register contains the blank data to be routed to the Video Processing block according to the input video format and color depth. [11:0] - lane0 [23:12] - lane1 [35:24] - lane2

VID_BLANK_DATA3 (0x232B)

BIT	7	6	5	4	3	2	1	0
Field	ri_vid_blank_data_31_24[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ri_vid_blank_data_31_24	7:0	Video Blank Data: This register controls bits [31:24] of the Video Blank Data muxed with the output from tclk2pclk converter on an AV Mute through a GCP. When an AV Mute is received through a GCP, the value in this register contains the blank data to be routed to the Video Processing block according to the input video format and color depth. [11:0] - lane0 [23:12] - lane1 [35:24] - lane2

VID_BLANK_DATA4 (0x232C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ri_vid_blank_data_35_32[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
ri_vid_blank_data_35_32	3:0	Video Blank Data: This register controls bits [35:32] of the Video Blank Data muxed with the output from tclk2pclk converter on an AV Mute through a GCP. When an AV Mute is received through a GCP, the value in this register contains the blank data to be routed to the Video Processing block according to the input video format and color depth. [11:0] - lane0 [23:12] - lane1 [35:24] - lane2

RX_INTR1 (0x2340)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr1_stat7	reg_intr1_stat6	reg_intr1_stat5	reg_intr1_stat4	reg_intr1_stat3	reg_intr1_stat2	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
reg_intr1_stat7	7	Most recent ACR hardware CTS value is different from previous. Write 1 to clear

BITFIELD	BITS	DESCRIPTION
reg_intr1_stat6	6	Most recent ACR hardware N value is different from previous. Write 1 to clear
reg_intr1_stat5	5	Audio N/CTS packet decode error. Asserted if set to 1. Write 1 to clear
reg_intr1_stat4	4	Audio PLL Unlocked. Asserted if set to 1. Write 1 to clear
reg_intr1_stat3	3	Audio FIFO Error. Asserted if set to 1. Write 1 to clear
reg_intr1_stat2	2	This bit indicates the Depacketizer block Interrupt status. 0 - No Depacketizer Interrupt is Set 1 - One or more Depacketizer Interrupts are Set Write 1 to clear

RX_INTR2 (0x2341)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr2_stat7	reg_intr2_stat6	–	–	–	–	–	reg_intr2_stat0
Reset	0b0	0b0	–	–	–	–	–	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr2_stat7	7	This Interrupt indicates a change in the HDMI mode of the link. This Interrupt is asserted HIGH if the link changes from HDMI to DVI or vice-versa. Software override changes due to change in programming of the reg_hdmi_mode_sw_value bitfield in register RX_SW_HDMI_MODE (0x2322), when register bit reg_hdmi_mode_overwrite in register RX_SW_HDMI_MODE is HIGH also asserts this Interrupt bit. Write 1 to clear the Interrupt.
reg_intr2_stat6	6	VSYNC active edge is recognized. Asserted if set to 1. Write 1 to clear
reg_intr2_stat0	0	Video Clock change. Asserted if set to 1. Write 1 to clear

RX_INTR3 (0x2342)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr3_stat5	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr3_stat5	5	SPDIF parity error. Asserted if set to 1. Write 1 to clear

RX_INTR4 (0x2343)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_intr4_stat3	reg_intr4_stat2	reg_intr4_stat1	reg_intr4_stat0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr4_stat3	3	Interrupt indicating the CTS value was dropped because a new packet value overwrote a CTS value before it was used to generate an NCLK period; Write 1 to clear
reg_intr4_stat2	2	Interrupt indicating the CTS value was reused because a new CTS packet value was not available when the previous NCLK period was finished. Write 1 to clear.
reg_intr4_stat1	1	FIFO overun. Write 1 to clear
reg_intr4_stat0	0	FIFO underun. Write 1 to clear

RX_INTR5 (0x2344)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr5_stat7	reg_intr5_stat6	–	–	–	–	–	reg_intr5_stat0
Reset	0b0	0b0	–	–	–	–	–	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr5_stat7	7	This Interrupt is asserted when an N value change is noticed by the Auto Audio Control block in the hardware. Value change in N is initiated from receiving an ACR packet from the source. Software can write 1 to clear. Apart from that, this bit gets auto-cleared by the Auto Audio Control block if any of the following conditions are true. 1. When enabling CSC. 2. When CSC is done and bit [0] of reg_aac_ctrl4 register is set HIGH. 3. If ASC is done successfully.
reg_intr5_stat6	6	Audio Auto Config muted the audio as result of the interrupt. Write 1 to clear.
reg_intr5_stat0	0	Audio Fs changed. Asserted if set to 1. Write 1 to clear

RX_INTR6 (0x2345)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr6_stat6	reg_intr6_stat5	–	reg_intr6_stat3	–	–	–
Reset	–	0b0	0b0	–	0b0	–	–	–
Access Type	–	Write, Read	Write, Read	–	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr6_stat6	6	1 or all audio stream got flat bit: Asserted if set to 1. Write 1 to clear
reg_intr6_stat5	5	Finished loading the Channel Status bits: Asserted if set to 1. Write 1 to clear

BITFIELD	BITS	DESCRIPTION
reg_intr6_stat3	3	DSD invalid. Write 1 to clear.

RX_INTR7 (0x2346)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr7_stat5	–	–	reg_intr7_stat2	–	reg_intr7_stat0
Reset	–	–	0b1	–	–	0b0	–	0b0
Access Type	–	–	Write, Read	–	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr7_stat5	5	Left and Right data mismatch flag This Interrupt indicates a Left-Right channel mismatch in transmission of data on the I^2S SD lines. This Interrupt goes HIGH if a new word transfer has started, and the channel data for transmission is Right while I^2S protocol starts with Left. 0 - No Left-Right channel mismatch occurred 1 - Left-Right channel mismatch occurred. Write 1 to clear.
reg_intr7_stat2	2	PCLK is stopped. Write 1 to clear.
reg_intr7_stat0	0	The state of the pclk_stable has changed. Write 1 to clear.

RX_INTR8 (0x2347)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr8_stat7	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr8_stat7	7	Interrupt indicating the audio Channel status is changed; Write 1 to clear

RX_INTR10 (0x2349)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_intr10_stat0
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr10_stat0	0	AAC has completed unmute. Write 1 to clear.

RX_INTR13 (0x234C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	reg_intr13_stat4	reg_intr13_stat3	reg_intr13_stat2	RSVD	reg_intr13_stat0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–		Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION
reg_intr13_stat4	4	This bit indicates the USB Tunnel Core block Interrupt status. 0 - No USB Tunnel Core interrupt is set 1 - One or more USB Tunnel Core interrupts are set This Interrupt status is valid only for MHL3 devices supporting USB Tunneling feature.
reg_intr13_stat3	3	This bit indicates the EMSC block Interrupt status. 0 - No EMSC interrupt is set 1 - One or more EMSC interrupts are set This Interrupt status is valid only for MHL3 devices supporting EMSC feature.
reg_intr13_stat2	2	This bit indicates the TDM Core block Interrupt status. 0 - No TDM core interrupt is set 1 - One or more TDM core interrupts are set This Interrupt status is valid only for MHL3 compliant devices.
reg_intr13_stat0	0	This bit indicates the Video Path Core block Interrupt status. 0 - No Video Path Core interrupt is set 1 - One or more Video Path Core interrupts are set

RX_INTR14 (0x234D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_intr14_stat3	reg_intr14_stat2	reg_intr14_stat1	reg_intr14_stat0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr14_stat3	3	This bit indicates the p1_clk_lost interrupt. Write 1 to Clear.
reg_intr14_stat2	2	This bit indicates the p1_clk_rdy interrupt. Write 1 to Clear.
reg_intr14_stat1	1	This bit indicates the p1_invalid interrupt. Write 1 to Clear.
reg_intr14_stat0	0	This bit indicates the p1_valid interrupt. Write 1 to Clear.

RX_INTR1_MASK (0x2350)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr1_mask7	reg_intr1_mask6	reg_intr1_mask5	reg_intr1_mask4	reg_intr1_mask3	reg_intr1_mask2	reg_intr1_mask1	reg_intr1_mask0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr1_mask7	7	Enable INT1[7]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask6	6	Enable INT1[6]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask5	5	Enable INT1[5]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask4	4	Enable INT1[4]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask3	3	Enable INT1[3]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask2	2	Enable INT1[2]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask1	1	Enable INT1[1]: 1 - Enable; 0 - Disable (default)
reg_intr1_mask0	0	Enable INT1[0]: 1 - Enable; 0 - Disable (default)

RX_INTR2_MASK (0x2351)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr2_mask7	reg_intr2_mask6	–	–	–	–	–	reg_intr2_mask0
Reset	0b0	0b0	–	–	–	–	–	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr2_mask7	7	Enable INT2[7]: 1 - Enable; 0 - Disable (default)
reg_intr2_mask6	6	Enable INT2[6]: 1 - Enable; 0 - Disable (default)

BITFIELD	BITS	DESCRIPTION
reg_intr2_mask0	0	Enable INT2[0]: 1 - Enable; 0 - Disable (default)

RX_INTR3_MASK (0x2352)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr3_mask5	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr3_mask5	5	Enable INT3[5]: 1 - Enable; 0 - Disable (default)

RX_INTR4_MASK (0x2353)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_intr4_mask3	reg_intr4_mask2	reg_intr4_mask1	reg_intr4_mask0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr4_mask3	3	Enable INT4[3]: 1 - Enable; 0 - Disable (default)
reg_intr4_mask2	2	Enable INT4[2]: 1 - Enable; 0 - Disable (default)
reg_intr4_mask1	1	Enable INT4[1]: 1 - Enable; 0 - Disable (default)
reg_intr4_mask0	0	Enable INT4[0]: 1 - Enable; 0 - Disable (default)

RX_INTR5_MASK (0x2354)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr5_mask7	reg_intr5_mask6	–	–	–	–	–	reg_intr5_mask0
Reset	0b0	0b0	–	–	–	–	–	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr5_mask7	7	Enable INT5[7]: 1 - Enable; 0 - Disable (default)
reg_intr5_mask6	6	Enable INT5[6]: 1 - Enable; 0 - Disable (default)
reg_intr5_mask0	0	Enable INT5[0]: 1 - Enable; 0 - Disable (default)

RX_INTR6_MASK (0x2355)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr6_mask6	reg_intr6_mask5	–	reg_intr6_mask3	–	–	–
Reset	–	0b0	0b0	–	0b0	–	–	–
Access Type	–	Write, Read	Write, Read	–	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr6_mask6	6	Enable INT6[6]: 1 - Enable; 0 - Disable (default)
reg_intr6_mask5	5	Enable INT6[5]: 1 - Enable; 0 - Disable (default)
reg_intr6_mask3	3	Enable INT6[3]: 1 - Enable; 0 - Disable (default)

RX_INTR7_MASK (0x2356)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr7_mask5	–	–	reg_intr7_mask2	–	reg_intr7_mask0
Reset	–	–	0b0	–	–	0b0	–	0b0
Access Type	–	–	Write, Read	–	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr7_mask5	5	Enable INT7[5]: 1 - Enable; 0 - Disable (default)
reg_intr7_mask2	2	Enable INT7[2]: 1 - Enable; 0 - Disable (default)
reg_intr7_mask0	0	Enable INT7[0]: 1 - Enable; 0 - Disable (default)

RX_INTR8_MASK (0x2357)*

BIT	7	6	5	4	3	2	1	0
Field	reg_intr8_mask7	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
reg_intr8_mask7	7	Enable INT8[7]: 1 - Enable; 0 - Disable (default)

RX_INTR10_MASK (0x2359)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_intr10_mask0
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr10_mask0	0	Enable INT10[0]: 1 - Enable; 0 - Disable (default)

RX_INTR12_MASK (0x235B)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr12_mask6	reg_intr12_mask5	reg_intr12_mask4	reg_intr12_mask3	reg_intr12_mask2	reg_intr12_mask1	reg_intr12_mask0
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr12_mask6	6	Enable INT12[6]: 1 - Enable; 0 - Disable (default)
reg_intr12_mask5	5	Enable INT12[5]: 1 - Enable; 0 - Disable (default)
reg_intr12_mask4	4	Enable INT12[4]: 1 - Enable; 0 - Disable (default)
reg_intr12_mask3	3	Enable INT12[3]: 1 - Enable; 0 - Disable (default)
reg_intr12_mask2	2	Enable INT12[2]: 1 - Enable; 0 - Disable (default)

BITFIELD	BITS	DESCRIPTION
reg_intr12_mask1	1	Enable INT12[1]: 1 - Enable; 0 - Disable (default)
reg_intr12_mask0	0	Enable INT12[0]: 1 - Enable; 0 - Disable (default)

RX_INTR13_MASK (0x235C)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr13_mask5	reg_intr13_mask4	reg_intr13_mask3	reg_intr13_mask2	reg_intr13_mask1	reg_intr13_mask0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr13_mask5	5	Enable INT13[5]: 1 - Enable 0 - Disable (default)
reg_intr13_mask4	4	Enable INT13[4]: 1 - Enable 0 - Disable (default)
reg_intr13_mask3	3	Enable INT13[3]: 1 - Enable 0 - Disable (default)
reg_intr13_mask2	2	Enable INT13[2]: 1 - Enable 0 - Disable (default)
reg_intr13_mask1	1	Enable INT13[1]: 1 - Enable 0 - Disable (default)
reg_intr13_mask0	0	Enable INT13[0]: 1 - Enable 0 - Disable (default)

RX_INTR14_MASK (0x235D)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_intr14_mask3	reg_intr14_mask2	reg_intr14_mask1	reg_intr14_mask0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr14_mask3	3	Enable INT14[3]: 1 - Enable; 0 - Disable (default)
reg_intr14_mask2	2	Enable INT14[2]: 1 - Enable; 0 - Disable (default)

BITFIELD	BITS	DESCRIPTION
reg_intr14_mask1	1	Enable INT14[1]: 1 - Enable; 0 - Disable (default)
reg_intr14_mask0	0	Enable INT14[0]: 1 - Enable; 0 - Disable (default)

DPLL_CH0_ERR_CNT1 (0x2360)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch0_err_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch0_err_cnt_7_0	7:0	Channel 0 Error Count Lower Byte. Write sets register value

DPLL_CH0_ERR_CNT2 (0x2361)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch0_valid	reg_dpll_ch0_err_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch0_valid	7	Channel 0 Valid. Write sets register value.
reg_dpll_ch0_err_cnt_14_8	6:0	Channel 0 Error Count Upper Byte. Write sets register value.

DPLL_CH1_ERR_CNT1 (0x2362)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch1_err_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch1_err_cnt_7_0	7:0	Channel 1 Error Count Lower Byte. Write sets register value.

DPLL_CH1_ERR_CNT2 (0x2363)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch1_valid	reg_dpll_ch1_err_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch1_valid	7	Channel 1 Valid. Write sets register value.
reg_dpll_ch1_err_cnt_14_8	6:0	Channel 1 Error Count Upper Byte. Write sets register value.

DPLL_CH2_ERR_CNT1 (0x2364)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch2_err_cnt_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch2_err_cnt_7_0	7:0	Channel 2 Error Count Lower Byte. Write sets register value.

DPLL_CH2_ERR_CNT2 (0x2365)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_ch2_valid	reg_dpll_ch2_err_cnt_14_8[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
reg_dpll_ch2_valid	7	Channel 2 Valid. Write sets register value.
reg_dpll_ch2_err_cnt_14_8	6:0	Channel 2 Error Count Upper Byte. Write sets register value.

DPLL_SCDC_CTRL (0x2366)

BIT	7	6	5	4	3	2	1	0
Field	reg_dpll_scramble_stat	reg_dpll_ch_locked[2:0]			reg_dpll_clk_detected	–	–	reg_dpll_bypass_en
Reset	0b0	0b000			0b0	–	–	0b0
Access Type	Write, Read	Write, Read			Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_dpll_scramble_stat	7	DPLL Scramble Status. Write sets register value.
reg_dpll_ch_locked	6:4	DPLL Channel Locked. Write sets register value.
reg_dpll_clk_detected	3	DPLL Clock Detected. Write sets register value.
reg_dpll_bypass_en	0	DPLL Bypass Enable: This bit controls the DPLL → SCDC signal bypass. 0 - No Bypass 1 - Bypass This bit when set HIGH; bypasses the signals from DPLL to SCDC logic and provides the values from registers. This is useful in case of isolating DPLL from SCDC logic and eases debug of SCDC logic as a stand-alone.

vp_soft_reset (0x2A0C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	reset_clk_out	reset_clk_core	reset_clk_in
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reset_clk_out	2	Video Input software reset for back end only (clk_out domain)
reset_clk_core	1	Video Input software reset for core only (clk_core domain)
reset_clk_in	0	Video Input software reset for front end only (clk_in domain)

vp_input_format_1 (0x2A14)

BIT	7	6	5	4	3	2	1	0
Field	cbcr_order	yc_demux_polarity	yc_demux_enable	ddr_mode[2:0]			ddr_polarity	ddr_enable
Reset	0b0	0b0	0b0	0b000			0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
cbcr_order	7	Select Cb/Cr order for muxed signals 0b0 - Cb before Cr 0b1 - Cr before Cb
yc_demux_polarity	6	Select polarity of Y/C demux logic 0b0 - C before Y 0b1 - Y before C
yc_demux_enable	5	Enable Y/C demux logic 0b0 - Separate Y/C data 0b1 - Muxed Y/C data

BITFIELD	BITS	DESCRIPTION
ddr_mode	4:2	Select DDR mode 0b000 - C data on posedge of mapped Y bus, Y data on negedge of mapped Y bus 0b001 - 8-bit BG/CbY data on posedge of mapped Cb/Y bus, GR/YCr data on negedge of mapped Cb/Y bus 0b010 - 10-bit BG/CbY data on posedge of mapped Cb/Y bus, GR/YCr data on negedge of mapped Cb/Y bus 0b011 - 12-bit BG/CbY data on posedge of mapped Cb/Y bus, GR/YCr data on negedge of mapped Cb/Y bus 0b100 - Reserved 0b101 - Reserved 0b101 - Reserved 0b111 - Reserved
ddr_polarity	1	Select polarity of DDR decoder 0b0 - CLK rising edge captures chroma 0b1 - CLK rising edge captures luma
ddr_enable	0	Strobe data on both posedge and negedge of input clock 0b0 - DDR mode disabled (single-edge mode) 0b1 - DDR mode enabled (dual-edge mode)

vp_input_format_2 (0x2A15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RSVD	pixel_rate[1:0]	
Reset	–	–	–	–	0b0	0b0	0b00	
Access Type	–	–	–	–			Write, Read	

BITFIELD	BITS	DESCRIPTION
pixel_rate	1:0	Remove replicated pixels 0x0 Pixel replication 1x 0x1 Pixel replication 2x 0x2 Pixel replication 4x 0x3 Pixel replication 8x

vp_fdet_config (0x2A80)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	vsync_polarity_3	hsync_polarity_3	sync_polarity_force
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
vsync_polarity_3	2	Select forced VSYNC polarity	0b0: Negative sync polarity 0b1: Positive sync polarity
hsync_polarity_3	1	Select forced HSYNC polarity	0b0: Negative sync polarity 0b1: Positive sync polarity
sync_polarity_force	0	Select which sync polarity to use	0b0: Use internally detected sync polarity 0b1: Use programmed sync polarity

vp_fdet_status (0x2A81)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	interlaced_	vsync_polarity_2	hsync_polarity_2
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–		Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
interlaced_	2	Interlaced signal detected
vsync_polarity_2	1	Detected VSYNC polarity (requires VSYNC/DE input active)
hsync_polarity_2	0	Detected HSYNC polarity (requires HSYNC/DE input active)

vp_fdet_frame_rate_delta_threshold_1 (0x2A84)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_delta_threshold_1[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_delta_threshold_1	7:0	Delta threshold. If frame rate counter differs by more than this amount between frames, an IRQ is issued.

vp_fdet_frame_rate_delta_threshold_2 (0x2A85)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_delta_threshold_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_delta_threshold_2	7:0	Delta threshold. If frame rate counter differs by more than this amount between frames, an IRQ is issued.

vp_fdet_frame_rate_delta_threshold_3 (0x2A86)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_delta_threshold_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_delta_threshold_3	7:0	Delta threshold. If frame rate counter differs by more than this amount between frames, an IRQ is issued.

vp_fdet_frame_rate_1 (0x2A88)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_1	7:0	Frame rate = (1/fdet_frame_rate) x f_clk_reg. Write any value to clear the counter.

vp_fdet_frame_rate_2 (0x2A89)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_2	7:0	Frame rate = (1/fdet_frame_rate) x f_clk_reg. Write any value to clear the counter.

vp_fdet_frame_rate_3 (0x2A8A)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_rate_3[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_rate_3	7:0	Frame rate = (1/fdet_frame_rate) x f_clk_reg. Write any value to clear the counter.

vp_fdet_pixel_count_1 (0x2A8C)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_pixel_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_pixel_count_1	7:0	Pixels per line (requires DE input active). Write any value to clear the counter.

vp_fdet_pixel_count_2 (0x2A8D)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_pixel_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_pixel_count_2	7:0	Pixels per line (requires DE input active). Write any value to clear the counter.

vp_fdet_line_count_1 (0x2A8E)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_line_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_line_count_1	7:0	Active video lines per frame (requires DE input active). Write any value to clear the counter.

vp_fdet_line_count_2 (0x2A8F)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_line_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_line_count_2	7:0	Active video lines per frame (requires DE input active). Write any value to clear the counter.

vp_fdet_hsync_low_count_1 (0x2A90)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hsync_low_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hsync_low_count_1	7:0	Number of HSYNC low cycles (requires HSYNC input active). Write any value to clear the counter.

vp_fdet_hsync_low_count_2 (0x2A91)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hsync_low_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hsync_low_count_2	7:0	Number of HSYNC low cycles (requires HSYNC input active). Write any value to clear the counter.

vp_fdet_hsync_high_count_1 (0x2A92)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hsync_high_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hsync_high_count_1	7:0	Number of HSYNC high cycles (requires HSYNC input active). Write any value to clear the counter.

vp_fdet_hsync_high_count_2 (0x2A93)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hsync_high_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hsync_high_count_2	7:0	Number of HSYNC high cycles (requires HSYNC input active). Write any value to clear the counter.

vp_fdet_hfront_count_1 (0x2A94)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hfront_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hfront_count_1	7:0	Number of HFRONT cycles (requires HSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_hfront_count_2 (0x2A95)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hfront_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hfront_count_2	7:0	Number of HFRONT cycles (requires HSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_hback_count_1 (0x2A96)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hback_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hback_count_1	7:0	Number of HBACK cycles (requires HSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_hback_count_2 (0x2A97)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_hback_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_hback_count_2	7:0	Number of HBACK cycles (requires HSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_vsync_low_count_even_1 (0x2A98)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_low_count_even_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_low_count_even_1	7:0	Number of VSYNC low cycles in the EVEN field (or progressive frame) (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_low_count_even_2 (0x2A99)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_low_count_even_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_low_count_even_2	7:0	Number of VSYNC low cycles in the EVEN field (or progressive frame) (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_high_count_even_1 (0x2A9A)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_high_count_even_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_high_count_even_1	7:0	Number of VSYNC high cycles in the EVEN field (or progressive frame) (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_high_count_even_2 (0x2A9B)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_high_count_even_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_high_count_even_2	7:0	Number of VSYNC high cycles in the EVEN field (or progressive frame) (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vfront_count_even_1 (0x2A9C)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vfront_count_even_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vfront_count_even_1	7:0	Number of VFRONT cycles in the EVEN field (or progressive frame) (requires VSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_vfront_count_even_2 (0x2A9D)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vfront_count_even_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vfront_count_even_2	7:0	Number of VFRONT cycles in the EVEN field (or progressive frame) (requires VSYNC/DE inputs active). Write any value to clear the counter.

vp_fdet_vback_count_even_1 (0x2A9E)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vback_count_even_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vback_count_even_1	7:0	Number of VBACK cycles in the EVEN field (or progressive frame) (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_vback_count_even_2 (0x2A9F)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vback_count_even_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vback_count_even_2	7:0	Number of VBACK cycles in the EVEN field (or progressive frame) (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_vsync_low_count_odd_1 (0x2AA0)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_low_count_odd_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_low_count_odd_1	7:0	Number of VSYNC low cycles in the ODD field (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_low_count_odd_2 (0x2AA1)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_low_count_odd_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_low_count_odd_2	7:0	Number of VSYNC low cycles in the ODD field (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_high_count_odd_1 (0x2AA2)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_high_count_odd_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_high_count_odd_1	7:0	Number of VSYNC high cycles in the ODD field (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vsync_high_count_odd_2 (0x2AA3)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vsync_high_count_odd_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vsync_high_count_odd_2	7:0	Number of VSYNC high cycles in the ODD field (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_vfront_count_odd_1 (0x2AA4)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vfront_count_odd_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vfront_count_odd_1	7:0	Number of VFRONT cycles in the ODD field (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_vfront_count_odd_2 (0x2AA5)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vfront_count_odd_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vfront_count_odd_2	7:0	Number of VFRONT cycles in the ODD field (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_vback_count_odd_1 (0x2AA6)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vback_count_odd_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vback_count_odd_1	7:0	Number of VBACK cycles in the ODD field (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_vback_count_odd_2 (0x2AA7)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_vback_count_odd_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_vback_count_odd_2	7:0	Number of VBACK cycles in the ODD field (requires VSYNC/DE input active). Write any value to clear the counter.

vp_fdet_frame_count_1 (0x2AA8)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_count_1[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_count_1	7:0	Running frame count (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_frame_count_2 (0x2AA9)

BIT	7	6	5	4	3	2	1	0
Field	vp_fdet_frame_count_2[7:0]							
Reset	0x00							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
vp_fdet_frame_count_2	7:0	Running frame count (requires VSYNC input active). Write any value to clear the counter.

vp_fdet_irq_mask_1 (0x2AB0)

Configure which format changes cause IRQ. Each bit enables the corresponding bit in the IRQ status register to cause an interrupt.

BIT	7	6	5	4	3	2	1	0
Field	hsync_low_count	line_count	pixel_count	frame_rate	video656	interlaced	vsync_polarity	hsync_polarity
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
hsync_low_count	7	HSYNC low count changes
line_count	6	Line count changes
pixel_count	5	Pixel count changes
frame_rate	4	Frame rate changes above threshold
video656	3	BT.656 status changes
interlaced	2	Interlaced status changes
vsync_polarity	1	VSYNC polarity changes
hsync_polarity	0	HSYNC polarity changes

vp_fdet_irq_mask_2 (0x2AB1)

Configure which format changes cause IRQ. Each bit enables the corresponding bit in the IRQ status register to cause an interrupt.

BIT	7	6	5	4	3	2	1	0
Field	vsync_low_count_odd	vback_count_even	vfront_count_even	vsync_high_count_even	vsync_low_count_even	hback_count	hfront_count	hsync_high_count
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
vsync_low_count_odd	7	VSYNC low count changes (odd fields)
vback_count_even	6	VBACK count changes (even fields/progressive)
vfront_count_even	5	VFRONT count changes (even fields/progressive)
vsync_high_count_even	4	VSYNC hight count changes (even fields/progressive)

BITFIELD	BITS	DESCRIPTION
vsync_low_count_even	3	VSYNC low count changes (even fields/progressive)
hback_count	2	HBACK count changes
hfront_count	1	HFRONT count changes
hsync_high_count	0	HSYNC high count changes

vp_fdet_irq_mask_3 (0x2AB2)

Configure which format changes cause IRQ. Each bit enables the corresponding bit in the IRQ status register to cause an interrupt.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	vback_count_odd	vfront_count_odd	vsync_high_count_odd
Reset	–	–	–	–	–	0b1	0b1	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
vback_count_odd	2	VBACK count changes (odd fields)
vfront_count_odd	1	VFRONT count changes (odd fields)
vsync_high_count_odd	0	VSYNC hight count changes (odd fields)

vp_fdet_irq_status_1 (0x2AB4)

IRQ status register

BIT	7	6	5	4	3	2	1	0
Field	hsync_low_count	line_count	pixel_count	frame_rate	video656	interlaced	vsync_polarity	hsync_polarity
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
hsync_low_count	7	HSYNC low count changes
line_count	6	Line count changes
pixel_count	5	Pixel count changes
frame_rate	4	Frame rate changes above threshold
video656	3	BT.656 status changes
interlaced	2	Interlaced status changes
vsync_polarity	1	VSYNC polarity changes
hsync_polarity	0	HSYNC polarity changes

vp_fdet_irq_status_2 (0x2AB5)

IRQ status register

BIT	7	6	5	4	3	2	1	0
Field	vsync_low_count_odd	vback_count_even	vfront_count_even	vsync_high_count_even	vsync_low_count_even	hback_count	hfront_count	hsync_high_count
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
vsync_low_count_odd	7	VSYNC low count changes (odd fields)
vback_count_even	6	VBACK count changes (even fields/progressive)
vfront_count_even	5	VFRONT count changes (even fields/progressive)
vsync_high_count_even	4	VSYNC hight count changes (even fields/progressive)
vsync_low_count_even	3	VSYNC low count changes (even fields/progressive)
hback_count	2	HBACK count changes
hfront_count	1	HFRONT count changes
hsync_high_count	0	HSYNC high count changes

vp_fdet_irq_status_3 (0x2AB6)

IRQ status register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	vback_count_odd	vfront_count_odd	vsync_high_count_odd
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
vback_count_odd	2	VBACK count changes (odd fields)
vfront_count_odd	1	VFRONT count changes (odd fields)
vsync_high_count_odd	0	VSYNC hight count changes (odd fields)

RX_INT_IF_CTRL (0x2C20)

BIT	7	6	5	4	3	2	1	0
Field	reg_use_aif4vsi	reg_new_vsi_only	reg_new_acp_only	reg_new_unrec_only	reg_new_mpeg_only	reg_new_aud_only	reg_new_spd_only	reg_new_avi_only
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_use_aif4vsi	7	Enable to use AIF for VSI storage. If it is set, then VSIF ID should not match ID 24'h030C00, instead it should match ID programmed in registers 0xD01-0xD04. To update VSI info frames in AIF registers, program the following register bits: (1) RX_INT_IF_CTRL[7] = 1 (i.e reg_use_aif4vsi = 1) (2) VSI_CTRL2[0] = 1 (i.e reg_vsi_ieee_id_chk_en = 1)

BITFIELD	BITS	DESCRIPTION
reg_new_vsi_only	6	Select when to set interrupts for the VSIF InfoFrames: 0 - Interrupt is set only if new VSIF InfoFrame is received (default); 1 - Interrupt is set if any VSIF InfoFrame arrives
reg_new_acp_only	5	Select when to set interrupts for the ACP InfoFrames: 0 - Interrupt is set only if new ACP InfoFrame is received (default); 1 - Interrupt is set if any ACP InfoFrame arrives
reg_new_unrec_only	4	Select when to set interrupts for the Unrecognized InfoFrames: 0 - Interrupt is set only if new Unrecognized InfoFrame is received (default); 1 - Interrupt is set if any Unrecognized InfoFrame arrives
reg_new_mpeg_only	3	Select when to set interrupts for the MPEG InfoFrames: 0 - Interrupt is set only if new MPEG InfoFrame is received (default); 1 - Interrupt is set if any MPEG InfoFrame arrives
reg_new_aud_only	2	Select when to set interrupts for the AUD InfoFrames: 0 - Interrupt is set only if new AUD InfoFrame is received (default); 1 - Interrupt is set if any AUD InfoFrame arrives.
reg_new_spd_only	1	Select when to set interrupts for the SPD InfoFrames: 0 - Interrupt is set only if new SPD InfoFrame is received (default); 1 - Interrupt is set if any SPD InfoFrame arrives.
reg_new_avi_only	0	Select when to set interrupts for the AVI InfoFrames: 0 - Interrupt is set only if new AVI InfoFrame is received (default); 1 - Interrupt is set if any AVI InfoFrame received .

RX_INT_IF_CTRL2 (0x2C21)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_new_acr_only	reg_new_gcp_only	reg_new_isrc2_only	reg_new_isrc1_only
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_new_acr_only	3	Select when to set interrupts for the ACR packet: 0 - Interrupt is set only if new ACR packet is received (default); 1 - Interrupt is set if any ACR packet arrives.
reg_new_gcp_only	2	Select when to set interrupts for the GCP InfoFrames: 0 - Interrupt is set only if new GCP InfoFrame is received (default); 1 - Interrupt is set if any GCP InfoFrame arrives.
reg_new_isrc2_only	1	Select when to set interrupts for the ISRC2 InfoFrames: 0 - Interrupt is set only if new ISRC2 InfoFrame is received (default); 1 - Interrupt is set if any ISRC2 InfoFrame arrives.
reg_new_isrc1_only	0	Select when to set interrupts for the ISRC1 InfoFrames: 0 - Interrupt is set only if new ISRC1 InfoFrame is received (default); 1 - Interrupt is set if any ISRC1 InfoFrame received.

DEC_AV_MUTE (0x2C22)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_clear_av_mute	–	–	–	–	reg_video_mute
Reset	–	–	0b0	–	–	–	–	0b0
Access Type	–	–	Write, Read	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_clear_av_mute	5	Writing 1 to this field clears the GCP Write and the respective AV Mute related fields.
reg_video_mute	0	Video mute (ground output): 1 - Mute; 0 - Do not mute (default)

RX_AUDP_STAT (0x2C27)

BIT	7	6	5	4	3	2	1	0
Field	–	hdmi_hbra_on	hdmi_aud_dsd_on	hdmi_layout[1:0]		hdmi_mute	hdmi_mode_en	hdmi_mode_det
Reset	–	0b0	0b0	0b00		0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only		Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
hdmi_hbra_on	6	High Bit Rate audio flag: when "1" means that Rx decoded that audio stream is High Bit Rate audio; when "0" means that Rx decoded that audio stream is not High Bit Rate audio.
hdmi_aud_dsd_on	5	DSD status: when "1" means that Rx decoded that input stream is DSD; when "0" means that RX decoded that input stream is not DSD.
hdmi_layout	4:3	HDMI Audio packet layout indicator: 0 - Layout 0 (2-channel) (default) 1 - Layout 1 (Up to 8-channel)
hdmi_mute	2	State of AV Mute; the state of the internal AV Mute state machine.
hdmi_mode_en	1	HDMI Mode detected with software override: This signal indicates the mode of the connection as detected by the hardware with software override. 0 - DVI 1 - HDMI This status detected for hardware can be overridden by the software through programming appropriate values into reg_hdmi_mode_overwrite and reg_hdmi_mode_sw_value bits of RX_SW_HDMI_MODE register.
hdmi_mode_det	0	HDMI Mode Detected by hardware: This signal indicates the mode of the connection as detected by the hardware. 0 - DVI 1 - HDMI

RX_AUTO_CLR_PKT1 (0x2C28)

BIT	7	6	5	4	3	2	1	0
Field	reg_autoclr_gcp_pkt	reg_autoclr_vsi_pkt	reg_autoclr_acp_pkt	reg_autoclr_unrec_pkt	reg_autoclr_mpeg_pkt	reg_autoclr_aif_pkt	reg_autoclr_spd_pkt	reg_autoclr_avi_pkt
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_autoclr_gcp_pkt	7	Auto Clear Stored GCP Packet: This bit controls the automated clearing of stored GCP packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored GCP packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_vsi_pkt	6	Auto Clear Stored VSI Packet: This bit controls the automated clearing of stored VSI packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored VSI packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_acp_pkt	5	Auto Clear Stored ACP Packet: This bit controls the automated clearing of stored ACP packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored ACP packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_unrec_pkt	4	Auto Clear Stored Unrecognized Packet: This bit controls the automated clearing of stored Unrecognized packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored Unrecognized packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost

BITFIELD	BITS	DESCRIPTION
reg_autoclr_mpeg_pkt	3	Auto Clear Stored MPEG Packet: This bit controls the automated clearing of stored MPEG packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored MPEG packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_aif_pkt	2	Auto Clear Stored AIF Packet: This bit controls the automated clearing of stored AIF packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored AIF packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_spd_pkt	1	Auto Clear Stored SPD Packet: This bit controls the automated clearing of stored SPD packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored SPD packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_avi_pkt	0	Auto Clear Stored AVI Packet: This bit controls the automated clearing of stored AVI packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored AVI packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost

RX_AUTO_CLR_PKT2 (0x2C29)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_autoclr_acr_pkt	reg_autoclr_metadata_pkt	reg_autoclr_isrc2_pkt	reg_autoclr_isrc1_pkt
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_autoclr_acr_pkt	3	Auto Clear Stored ACR Packet: This bit controls the automated clearing of stored ACR packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored ACR packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_metadata_pkt	2	Auto Clear Stored Metadata Packet: This bit controls the automated clearing of stored Metadata packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored Metadata packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_isrc2_pkt	1	Auto Clear Stored ISRC2 Packet: This bit controls the automated clearing of stored ISRC2 packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored ISRC2 packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost
reg_autoclr_isrc1_pkt	0	Auto Clear Stored ISRC1 Packet: This bit controls the automated clearing of stored ISRC1 packet by the hardware. 0 - Disabled 1 - Enabled If this bit is set HIGH, stored ISRC1 packet is cleared by the hardware if any of the following conditions are true: 1. Cable unplugged 2. Sync detection lost

RX_DEPACK_INTR0 (0x2C30)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr0_stat5	reg_intr0_stat4	reg_intr0_stat3	RSVD	reg_intr0_stat1	reg_intr0_stat0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr0_stat5	5	This Interrupt indicates a change in Deep Color mode. This Interrupt is asserted HIGH when a change is noticed on the Color Depth of the video as indicated through the GCP packet. Note: When CD field of GCP is changed to all zeros, this interrupt is asserted only if the GCP is consecutively transmitted for more than four times. This is per HDMI specification. Write 1 to clear.
reg_intr0_stat4	4	Deep color packet error interrupt. Write 1 to clear.
reg_intr0_stat3	3	Packet received interrupt; set if number of the received HDMI packets exceeds threshold; Write 1 to clear.
reg_intr0_stat1	1	T4 interrupt; set if number of the T4 errors exceeds threshold. Write 1 to clear.
reg_intr0_stat0	0	Audio ECC error. Asserted if set to 1. Write 1 to clear.

RX_DEPACK_INTR0_MASK (0x2C31)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr0_mask5	reg_intr0_mask4	reg_intr0_mask3	reg_intr0_mask2	reg_intr0_mask1	reg_intr0_mask0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr0_mask5	5	Enable INTR0[5]: 0 - Disable (default) 1 - Enable
reg_intr0_mask4	4	Enable INTR0[4]: 0 - Disable (default) 1 - Enable
reg_intr0_mask3	3	Enable INTR0[3]: 0 - Disable (default) 1 - Enable
reg_intr0_mask2	2	Enable INTR0[2]: 0 - Disable (default) 1 - Enable
reg_intr0_mask1	1	Enable INTR0[1]: 0 - Disable (default) 1 - Enable
reg_intr0_mask0	0	Enable INTR0[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR1 (0x2C32)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr1_stat6	reg_intr1_stat5	reg_intr1_stat4	reg_intr1_stat3	reg_intr1_stat2	_	reg_intr1_stat0
Reset	–	0b0	0b0	0b0	0b0	0b0	–	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr1_stat6	6	HBRA on status is changed: Asserted if HBRA on status is changed. Write 1 to clear.
reg_intr1_stat5	5	DSD on status is changed: Asserted if DSD on status is changed. Write 1 to clear.
reg_intr1_stat4	4	This Interrupt indicates a change in the Audio layout. This Interrupt is asserted HIGH when a change is noticed in the Audio layout, indicated by the source. Write 1 to clear.
reg_intr1_stat3	3	Audio link error. Occurs only when there are ECC errors and no TERC4 errors. Write 1 to clear.
reg_intr1_stat2	2	CP info frame is set to Mute. Write 1 to clear.
reg_intr1_stat0	0	No Audio packet. Asserted if set to 1. Write 1 to clear.

RX_DEPACK_INTR1_MASK (0x2C33)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr1_mask6	reg_intr1_mask5	reg_intr1_mask4	reg_intr1_mask3	reg_intr1_mask2	_	reg_intr1_mask0
Reset	–	0b0	0b0	0b0	0b0	0b0	–	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr1_mask6	6	Enable INTR1[6]: 0 - Disable (default) 1 - Enable
reg_intr1_mask5	5	Enable INTR1[5]: 0 - Disable (default) 1 - Enable
reg_intr1_mask4	4	Enable INTR1[4]: 0 - Disable (default) 1 - Enable
reg_intr1_mask3	3	Enable INTR1[3]: 0 - Disable (default) 1 - Enable
reg_intr1_mask2	2	Enable INTR1[2]: 0 - Disable (default) 1 - Enable
reg_intr1_mask0	0	Enable INTR1[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR2 (0x2C34)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr2_stat7	reg_intr2_stat6	reg_intr2_stat5	reg_intr2_stat4	reg_intr2_stat3	reg_intr2_stat2	reg_intr2_stat1	reg_intr2_stat0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr2_stat7	7	New GCP packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat6	6	New ACP packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat5	5	New CP packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat4	4	New Unrecognized packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat3	3	New MPEG Info packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat2	2	New AUD Info packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat1	1	New SP Info packet. Asserted if set to 1. Write 1 to clear.
reg_intr2_stat0	0	New AVI Info packet. Asserted if set to 1. Write 1 to clear.

RX_DEPACK_INTR2_MASK (0x2C35)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr2_mask7	reg_intr2_mask6	reg_intr2_mask5	reg_intr2_mask4	reg_intr2_mask3	reg_intr2_mask2	reg_intr2_mask1	reg_intr2_mask0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr2_mask7	7	Enable INTR2[7]: 0 - Disable (default) 1 - Enable
reg_intr2_mask6	6	Enable INTR2[6]: 0 - Disable (default) 1 - Enable
reg_intr2_mask5	5	Enable INTR2[5]: 0 - Disable (default) 1 - Enable
reg_intr2_mask4	4	Enable INTR2[4]: 0 - Disable (default) 1 - Enable
reg_intr2_mask3	3	Enable INTR2[3]: 0 - Disable (default) 1 - Enable
reg_intr2_mask2	2	Enable INTR2[2]: 0 - Disable (default) 1 - Enable
reg_intr2_mask1	1	Enable INTR2[1]: 0 - Disable (default) 1 - Enable
reg_intr2_mask0	0	Enable INTR2[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR3 (0x2C36)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr3_stat5	reg_intr3_stat4	reg_intr3_stat3	reg_intr3_stat2	reg_intr3_stat1	reg_intr3_stat0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr3_stat5	5	New ACR packet. Asserted if set to 1. Write 1 to clear.
reg_intr3_stat4	4	Same HF_VSI info frame is repeated. Write 1 to clear.
reg_intr3_stat3	3	New HF_VSI info frame is received. Write 1 to clear.
reg_intr3_stat2	2	New VSI packet. Asserted if set to 1. Write 1 to clear.
reg_intr3_stat1	1	New ISRC2 packet. Asserted if set to 1. Write 1 to clear.
reg_intr3_stat0	0	New ISRC1 packet. Asserted if set to 1. Write 1 to clear.

RX_DEPACK_INTR3_MASK (0x2C37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_intr3_mask5	reg_intr3_mask4	reg_intr3_mask3	reg_intr3_mask2	reg_intr3_mask1	reg_intr3_mask0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr3_mask5	5	Enable INTR3[5]: 0 - Disable (default) 1 - Enable
reg_intr3_mask4	4	Enable INTR3[4]: 0 - Disable (default) 1 - Enable
reg_intr3_mask3	3	Enable INTR3[3]: 0 - Disable (default) 1 - Enable
reg_intr3_mask2	2	Enable INTR3[2]: 0 - Disable (default) 1 - Enable
reg_intr3_mask1	1	Enable INTR3[1]: 0 - Disable (default) 1 - Enable
reg_intr3_mask0	0	Enable INTR3[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR4 (0x2C38)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr4_stat6	reg_intr4_stat5	reg_intr4_stat4	reg_intr4_stat3	reg_intr4_stat2	reg_intr4_stat1	reg_intr4_stat0
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr4_stat6	6	3d22d or 2d23d change of transmission. Write 1 to clear.
reg_intr4_stat5	5	New Metadata packet is received. Write 1 to clear.
reg_intr4_stat4	4	New 1-bit Multi-stream Audio packet is received. Write 1 to clear.
reg_intr4_stat3	3	New Multi-stream Audio packet is received. Write 1 to clear.
reg_intr4_stat2	2	Metadata Audio packet is received. Write 1 to clear.
reg_intr4_stat1	1	New 1-bit 3D-Audio packet is received. Write 1 to clear.
reg_intr4_stat0	0	New 3D-Audio packet is received. Write 1 to clear.

RX_DEPACK_INTR4_MASK (0x2C39)

BIT	7	6	5	4	3	2	1	0
Field	–	reg_intr4_mask6	reg_intr4_mask5	reg_intr4_mask4	reg_intr4_mask3	reg_intr4_mask2	reg_intr4_mask1	reg_intr4_mask0
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr4_mask6	6	Enable INTR4[6]: 0 - Disable (default) 1 - Enable
reg_intr4_mask5	5	Enable INTR4[5]: 0 - Disable (default) 1 - Enable
reg_intr4_mask4	4	Enable INTR4[4]: 0 - Disable (default) 1 - Enable
reg_intr4_mask3	3	Enable INTR4[3]: 0 - Disable (default) 1 - Enable
reg_intr4_mask2	2	Enable INTR4[2]: 0 - Disable (default) 1 - Enable
reg_intr4_mask1	1	Enable INTR4[1]: 0 - Disable (default) 1 - Enable
reg_intr4_mask0	0	Enable INTR4[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR5 (0x2C3A)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr5_stat7	reg_intr5_stat6	reg_intr5_stat5	reg_intr5_stat4	reg_intr5_stat3	reg_intr5_stat2	reg_intr5_stat1	reg_intr5_stat0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr5_stat7	7	Interrupt indicating the ACP info frame did not arrive for more then 4 frames. Write 1 to clear.
reg_intr5_stat6	6	Interrupt indicating the UNREC InfoFrame did not arrive for more then 4 frames. Write 1 to clear.
reg_intr5_stat5	5	Interrupt indicating the MPEG InfoFrame did not arrive for more then 4 frames. Write 1 to clear.
reg_intr5_stat4	4	Interrupt indicating the SPD InfoFrame did not arrive for more then 4 frames. Write 1 to clear.
reg_intr5_stat3	3	Interrupt indicating the AIF InfoFrame did not arrive for more then 4 frames. Write 1 to clear. Depends on the setting in VSI_CTRL1[4:2]
reg_intr5_stat2	2	Interrupt indicating the VSI InfoFrame did not arrive for more then 4 frames. Write 1 to clear. Depends on the setting in VSI_CTRL1[4:2]
reg_intr5_stat1	1	No Deep-color packet has been received for 4 frames. Write 1 to clear.
reg_intr5_stat0	0	Interrupt indicating the AVI InfoFrame did not arrive for more then 4 frames. Write 1 to clear.

RX_DEPACK_INTR5_MASK (0x2C3B)

BIT	7	6	5	4	3	2	1	0
Field	reg_intr5_mask7	reg_intr5_mask6	reg_intr5_mask5	reg_intr5_mask4	reg_intr5_mask3	reg_intr5_mask2	reg_intr5_mask1	reg_intr5_mask0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr5_mask7	7	Enable INTR5[7]: 0 - Disable (default) 1 - Enable
reg_intr5_mask6	6	Enable INTR5[6]: 0 - Disable (default) 1 - Enable
reg_intr5_mask5	5	Enable INTR5[5]: 0 - Disable (default) 1 - Enable
reg_intr5_mask4	4	Enable INTR5[4]: 0 - Disable (default) 1 - Enable

BITFIELD	BITS	DESCRIPTION
reg_intr5_mask3	3	Enable INTR5[3]: 0 - Disable (default) 1 - Enable
reg_intr5_mask2	2	Enable INTR5[2]: 0 - Disable (default) 1 - Enable
reg_intr5_mask1	1	Enable INTR5[1]: 0 - Disable (default) 1 - Enable
reg_intr5_mask0	0	Enable INTR5[0]: 0 - Disable (default) 1 - Enable

RX_DEPACK_INTR6 (0x2C3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_intr6_stat4	reg_intr6_stat3	reg_intr6_stat2	reg_intr6_stat1	reg_intr6_stat0
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr6_stat4	4	No metadata packet is received. Write 1 to clear.
reg_intr6_stat3	3	No HF_VSI InfoFrame is received. Write 1 to clear.
reg_intr6_stat2	2	Interrupt indicating the GCP InfoFrame has not arrived for more than 4 frames. Write 1 to clear.
reg_intr6_stat1	1	Interrupt indicating the ISRC2 InfoFrame has not arrived for more than 4 frames. Write 1 to clear.
reg_intr6_stat0	0	Interrupt indicating the ISRC1 InfoFrame has not arrived for more than 4 frames. Write 1 to clear.

RX_DEPACK_INTR6_MASK (0x2C3D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_intr6_mask4	reg_intr6_mask3	reg_intr6_mask2	reg_intr6_mask1	reg_intr6_mask0
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_intr6_mask4	4	Enable INTR6[4]: 0 - Disable (default) 1 - Enable
reg_intr6_mask3	3	Enable INTR6[3]: 0 - Disable (default) 1 - Enable

BITFIELD	BITS	DESCRIPTION
reg_intr6_mask2	2	Enable INTR6[2]: 0 - Disable (default) 1 - Enable
reg_intr6_mask1	1	Enable INTR6[1]: 0 - Disable (default) 1 - Enable
reg_intr6_mask0	0	Enable INTR6[0]: 0 - Disable (default) 1 - Enable

SW_RST_REG0 (0x3C04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_osccal_srst	reg_otp_srst	reg_core_srst	reg_osc5m_srst	reg_osc_srst	reg_srst_full
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_osccal_srst	5	Soft-reset control to oscillator calibration logic.	0: Normal operation (default) 1: Reset
reg_otp_srst	4	Soft-reset control to top OTP logic.	0: Normal operation (default) 1: Reset
reg_core_srst	3	Soft-reset control for core clock domain.	0: Normal operation (default) 1: Reset
reg_osc5m_srst	2	Soft-reset control for 5MHz OSC clock domain used in zone control.	0: Normal operation (default) 1: Reset
reg_osc_srst	1	Soft-reset control for 2MHz OSC clock domain.	0: Normal operation (default) 1: Reset
reg_srst_full	0	Soft-reset control to complete logic of IP. This resets all internal logic except register interface.	0: Normal operation (default) 1: Reset

INTR_CTRL (0x3C10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	reg_intr_level	reg_intr_stat	RSVD	RSVD
Reset	–	–	–	–	0b1	0b0	0b0	0b1
Access Type	–	–	–	–	Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION
reg_intr_level	3	Interrupt level
reg_intr_stat	2	Interrupt status

INTR_STAT0 (0x3C11)

BIT	7	6	5	4	3	2	1	0
Field	reg_rxdig_intr_mask	reg_rxz_intr_mask	reg_intr0_mask1	reg_intr0_mask0	–	–	reg_intr0_stat1	reg_intr0_stat0
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
reg_rxdig_intr_mask	7	Rx digital interrupt mask	0: Disable (default) 1: Enable
reg_rxz_intr_mask	6	Rx zone control logic interrupt mask	0: Disable (default) 1: Enable
reg_intr0_mask1	5	OTP KSV read done interrupt mask	0: Disable (default) 1: Enable
reg_intr0_mask0	4	Rx zone PLL locked change interrupt mask	0: Disable (default) 1: Enable
reg_intr0_stat1	1	OTP KSV read done interrupt status	0: Disable (default) 1: Enable
reg_intr0_stat0	0	Rx zone PLL locked change interrupt status	0: Disable (default) 1: Enable

OTP_CTRL1_REG (0x3C20)

BIT	7	6	5	4	3	2	1	0
Field	reg_nvmi_locked	reg_ksv_rd_done	–	–	–	reg_ksv_rd_done_clr	reg_ld_ksv	reg_nvm_en
Reset	0b0	0b0	–	–	–	0b0	0b1	0b1
Access Type	Read Only	Read Only	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_nvmi_locked	7	Locked status of Top OTP content
reg_ksv_rd_done	6	KSV read done status.
reg_ksv_rd_done_clr	2	KSV read done clear. Software clear to the KSV read done flag assrted after the KSV sequence read is completed.
reg_ld_ksv	1	KSV read enable. Enables the reading RX KSVs and Receiver ID bytes.
reg_nvm_en	0	NVMI enable. Enables the control logic to access NVMI/OTP data

KSV_BYTE0 (0x3C22)

BIT	7	6	5	4	3	2	1	0
Field	reg_ksv0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_ksv0	7:0	OTP KSV Byte 0. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

KSV_BYTE1 (0x3C23)

BIT	7	6	5	4	3	2	1	0
Field	reg_ksv1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_ksv1	7:0	OTP KSV Byte 1. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

KSV_BYTE2 (0x3C24)

BIT	7	6	5	4	3	2	1	0
Field	reg_ksv2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_ksv2	7:0	OTP KSV Byte 2. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

KSV_BYTE3 (0x3C25)

BIT	7	6	5	4	3	2	1	0
Field	reg_ksv3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_ksv3	7:0	OTP KSV Byte 3. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

KSV_BYTE4 (0x3C26)

BIT	7	6	5	4	3	2	1	0
Field	reg_ksv4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_ksv4	7:0	OTP KSV Byte 4. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

RCV_ID_BYTE0 (0x3C27)

BIT	7	6	5	4	3	2	1	0
Field	reg_rcv_id0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_rcv_id0	7:0	OTP Receive ID Byte 0. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

RCV_ID_BYTE1 (0x3C28)

BIT	7	6	5	4	3	2	1	0
Field	reg_rcv_id1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_rcv_id1	7:0	OTP Receive ID Byte 1. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

RCV_ID_BYTE2 (0x3C29)

BIT	7	6	5	4	3	2	1	0
Field	reg_rcv_id2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_rcv_id2	7:0	OTP Receive ID Byte 2. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

RCV_ID_BYTE3 (0x3C2A)

BIT	7	6	5	4	3	2	1	0
Field	reg_rcv_id3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_rcv_id3	7:0	OTP Receive ID Byte 3. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

RCV_ID_BYTE4 (0x3C2B)

BIT	7	6	5	4	3	2	1	0
Field	reg_rcv_id4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
reg_rcv_id4	7:0	OTP Receive ID Byte 4. Read for valid KSV once OTP_CTRL1_REG[6] is asserted.

GP_CTRL0_REG (0x3C30)

BIT	7	6	5	4	3	2	1	0
Field	reg_gp_ctrl0_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_gp_ctrl0_7_0	7:0	General Purpose Control Register

CH_ENABLE_REG (0x3D05)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	reg_ch2_en_ovr	reg_ch2_en	reg_ch1_en_ovr	reg_ch1_en	reg_ch0_en_ovr	reg_ch0_en
Reset	–	–	0b1	0b0	0b1	0b0	0b1	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_ch2_en_ovr	5	TMDS Channel 2 enable SW overwrite	0: Disable overwrite 1: Enable overwrite (default)
reg_ch2_en	4	TMDS Channel 2 enable	0: Disable channel 1: Enable channel
reg_ch1_en_ovr	3	TMDS Channel 1 enable SW overwrite	0: Disable overwrite 1: Enable overwrite (default)
reg_ch1_en	2	TMDS Channel 1 enable	0: Disable channel 1: Enable channel
reg_ch0_en_ovr	1	TMDS Channel 0 enable SW overwrite	0: Disable overwrite 1: Enable overwrite (default)
reg_ch0_en	0	TMDS Channel 0 enable	0: Disable channel 1: Enable channel

TMDSR_CTL_REG (0x3D0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	reg_tmdsr_bp_dff[1:0]		reg_tmdsr_pmode_2	reg_tmdsr_pmode_1	reg_tmdsr_pmode_0
Reset	–	–	–	0b11		0b0	0b0	0b0
Access Type	–	–	–	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_tmdsr_bp_dff	4:3	Delay bypass enable for CDR loop	0b00: Add one DFF delay for CDR loop 0b01: Bypass DFF in CDR loop 0b10: Reserved 0b11: Reserved
reg_tmdsr_pmode_2	2	Power mode control for Channel 2.	0b0: Normal mode for 6.8Gbps 0b1: Power Saving mode for low data rate on equalizer
reg_tmdsr_pmode_1	1	Power mode control for Channel 1.	0b0: Normal mode for 6.8Gbps 0b1: Power Saving mode for low data rate on equalizer
reg_tmdsr_pmode_0	0	Power mode control for Channel 0.	0b0: Normal mode for 6.8Gbps 0b1: Power Saving mode for low data rate on equalizer

CP_CTL1_REG (0x3D0C)*

BIT	7	6	5	4	3	2	1	0
Field	–	reg_cp_ctl[4:0]					reg_cp_ctl_com[1:0]	
Reset	–	0b11000					0b01	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
reg_cp_ctl	6:2	Clock threshold selection	reg_cp_ctl[3:0] decode as manual offset bits when reg_cp_ctl[4.0] = 0 0: Disable auto calibration of offset bits reg_cp_ctl[3.0] 1: Enable auto calibration of offset bits reg_cp_ctl[3.0]
reg_cp_ctl_com	1:0	CPATH common mode voltage control.	Do not modify value.

CDR_CTL1_REG (0x3D0E)

BIT	7	6	5	4	3	2	1	0
Field	reg_bp_cdr	reg_cdr_en_dloop[1:0]		reg_cdr_dlysb	reg_cdr_gaink2[1:0]		reg_cdr_gaink1[1:0]	
Reset	0b0	0b00		0b0	0b00		0b10	
Access Type	Write, Read	Write, Read		Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
reg_bp_cdr	7	CDR function bypass. 0: Enable CDR loop (HDMI2.0 default) 1: Bypass CDR function (HDMI1.4)
reg_cdr_en_dloop	6:5	Enable Data Loop mode for low-speed clock application 00: Disable Data Loop mode 01: Enable Data Loop mode with adjust phase-point value only 11: Enable Data Loop and PI control together 10: Unused
reg_cdr_dylsb	4	Dynamic step control. 0: Fixed the dynamic step in Second mode 1: Dynamic increase step in Second mode
reg_cdr_gaink2	3:2	CDR loop integral path gain control 00: 1/32 01: 1/16 10: 1/8 11: 1/4
reg_cdr_gaink1	1:0	CDR loop proportional path gain control (bandwidth control) 00: 1/8 01: 1/4 10: 1/2 11: 1/1

EQOS_CTL0_REG (0x3D0F)

BIT	7	6	5	4	3	2	1	0
Field	reg_eqos_ctl_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_eqos_ctl_7_0	7:0	reg_eqos_ctl[0]: Input common control reg_eqos_ctl[1]: eq ctrl bit<8> which is combined with eq_ctl_0/1/2<7:0> reg_eqos_ctl[4:2]: noise coupling cap size ctrl reg_eqos_ctl[7:5]: eq offset ctrl[2:0]

EQOS_CTL1_REG (0x3D10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	reg_eqos_ctl_8
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_eqos_ctl_8	0	reg_eqos_ctl_8: Eq offset ctrl[3]

CONFIG1_REG (0x3D12)

BIT	7	6	5	4	3	2	1	0
Field	reg_bias_cfg[2:0]			reg_bias_pd	–	reg_cdr_idle_2	reg_cdr_idle_1	reg_cdr_idle_0
Reset	0b100			0b0	–	0b0	0b0	0b0
Access Type	Write, Read			Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_bias_cfg	7:5	Current fine-tune bits	
reg_bias_pd	4	Current power-down bit	
reg_cdr_idle_2	2	CDR idle state enables signal in TDD for Channel 2.	0b0: CDR tracks input data (CDR normal state) 0b1: CDR does not track input data (CDR idle state)
reg_cdr_idle_1	1	CDR idle state enables signal in TDD for Channel 1.	0b0: CDR tracks input data (CDR normal state) 0b1: CDR does not track input data (CDR idle state)
reg_cdr_idle_0	0	CDR idle state enables signal in TDD for Channel 0.	0b0: CDR tracks input data (CDR normal state) 0b1: CDR does not track input data (CDR idle state)

DPLL_CFG1 (0x3E00)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_taps[1:0]		reg_cfg_reg_edon	reg_cfg_spce_en	reg_cfg_mode[1:0]		reg_cfg_bv_sel	reg_cfg_ev_sel
Reset	0b00		0b0	0b0	0b00		0b1	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
reg_cfg_taps	7:6	LPF tap control (default = 2'b00)
reg_cfg_reg_edon	5	Auto-decision engine enable 0: Disables DPLL auto-decision engine (HDMI2.0 default) 1: Enables DPLL auto-decision engine (HDMI1.4)
reg_cfg_spce_en	4	Enable "external sync" for the ease of testing (default = 1'b0)
reg_cfg_mode	3:2	EQ Scanning mode (default = 2'b00)
reg_cfg_bv_sel	1	Selection of BWV between DEQ when 0 and I^2C when '1'
reg_cfg_ev_sel	0	Selection of EQV between DEQ when 0 or I^2C when '1'

DPLL_CFG2 (0x3E01)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_stb_rsc[1:0]		reg_cfg_chan_sel[1:0]		reg_cfg_byp	reg_cfg_bs[2:0]		
Reset	0b11		0b00		0b0	0b100		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
reg_cfg_stb_rsc	7:6	Stable Rescan mode (default = 2'b11)

BITFIELD	BITS	DESCRIPTION
reg_cfg_chan_sel	5:4	Bypass channel selection (default = 2'b00)
reg_cfg_byp	3	Enable Bypass mode (default = 1'b0)
reg_cfg_bs	2:0	Bit count limit control (default = 3'b010)

EV_VAL_B (0x3E04)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_ev_i2c_b[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
reg_cfg_ev_i2c_b	7:0	User specified EQV through I2C of Channel B. Equalizer control used by DPLL auto EQ control. Bitfield is broken up into several controls.	eq_ctl<1:0> DC gain (in dB) 00: 2.6 01: 2.57 10: -1.93 11: -2.52 eq_ctl<4:2> AC gain (in dB) 000: -2.72 001: -1.77 010: -0.88 011: -0.15 100: 0.39 101: 0.82 110: 1.25 111: 1.41 eq_ctl<5> Input Common mode level 0: 868mV 1: 789mV eq_ctl<7:6> Output Common mode level 00: 753mV 01: 793.6mV 10: 814.5mV 11: 856.7mV reg_cfg_ev_sel, (0[0]) should be 1'b1. If this is zero, eq val comes from DPLL.

EV_VAL_G (0x3E05)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_ev_i2c_g[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_ev_i2c_g	7:0	User specified EQV via I2C of Channel G. See reg_cfg_ev_i2c_b register for bit decode values.

EV_VAL_R (0x3E06)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_ev_i2c_r[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_ev_i2c_r	7:0	User specified EQV via I^2C of Channel R. See reg_cfg_ev_i2c_b register for bit decode values.

PEQ_VAL0 (0x3E08)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val0[7:0]							
Reset	0x58							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val0	7:0	One of EQVs used in DEQ

PEQ_VAL1 (0x3E09)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val1[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val1	7:0	One of EQVs used in DEQ

PEQ_VAL2 (0x3E0A)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val2[7:0]							
Reset	0x98							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val2	7:0	One of EQVs used in DEQ

PEQ_VAL3 (0x3E0B)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val3[7:0]							
Reset	0x79							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val3	7:0	One of EQVs used in DEQ

PEQ_VAL4 (0x3E0C)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val4[7:0]							
Reset	0x5E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val4	7:0	One of EQVs used in DEQ

PEQ_VAL5 (0x3E0D)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val5[7:0]							
Reset	0xB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val5	7:0	One of EQVs used in DEQ

PEQ_VAL6 (0x3E0E)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val6[7:0]							
Reset	0x7E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val6	7:0	One of EQVs used in DEQ

PEQ_VAL7 (0x3E0F)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_peq_val7[7:0]							
Reset	0x99							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
reg_cfg_peq_val7	7:0	One of EQVs used in DEQ

DPLL_CFG6 (0x3E15)

BIT	7	6	5	4	3	2	1	0
Field	reg_cfg_ri_swap	reg_cfg_ri_no_zone2x	reg_cfg_ri_bp_fix	reg_cfg_ri_use_scdt	reg_cfg_ri_ebyte_sel[2:0]			reg_cfg_ri_eeval
Reset	0b0	0b1	0b1	0b0	0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION
reg_cfg_ri_swap	7	TMDS (q0; q1; q2) bit order swap (default = 1'b0)
reg_cfg_ri_no_zone2x	6	1 - Zone 2x is not used in zone decision; Only 1x and 4x are used; 0 - Zone 2x is used as well (default = 1'b1)
reg_cfg_ri_bp_fix	5	Controls DPLL tracking. 0: Enables DPLL tracking (HDMI1.4) 1: DPLL stops tracking (HDMI2.0 default)
reg_cfg_ri_use_scdt	4	1 - Reset zone control logic when SCDT is 0; 0 - No, use SCDT (default = 1'b0)
reg_cfg_ri_ebyte_sel	3:1	Eye-monitor byte selection (default = 3'd0)
reg_cfg_ri_eeval	0	Eye-monitor enable (default = 1'b0)

DPLL_HDMI2 (0x3E50)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ri_hdmi2_scdt_on	ri_stat_and_on	ri_scramble_on_val	ri_scramble_on_ovr	ri_hdmi2_on_val	ri_hdmi2_on_ovr
Reset	–	–	0b1	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ri_hdmi2_scdt_on	5	HDMI2 SCDT on	Write 1
ri_stat_and_on	4	Scrambler on only after detecting scrambled stat.	Write 0
ri_scramble_on_val	3	Scramble on value. Considered only when ri_scramble_on_ovr is high.	Write 0
ri_scramble_on_ovr	2	1: Scramble on overwrite with ri_scramble_on_val 0: Scramble on value from CBUS/Top	Write 0

BITFIELD	BITS	DESCRIPTION	DECODE
ri_hdmi2_on_val	1	HDMI2 on value. Considered only when ri_hdmi2_on_ovr is high.	0: Clear HDMI2 on 1: Set HDMI2 on
ri_hdmi2_on_ovr	0	1: HDMI2 on overwrite with ri_hdmi2_on_val 0: HDMI2 on value from CBUS/Top	0: Disable overwrite of HDMI2 on 1: Enable overwrite of HDMI2 on

NEW_DPLL_CFG (0x3E5C)

BIT	7	6	5	4	3	2	1	0
Field	–	ri_mhl12_scon	ri_two_tmds_sync	ri_eq_per_ch	ri_allow_msync	ri_enh_algn_fifo	ri_tdd_mode	ri_red_lat
Reset	–	0b0	0b0	0b1	0b1	0b1	0b0	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ri_mhl12_scon	6	MHL1/2 descrambler enable control	0b0: Disable 0b1: Enable
ri_two_tmds_sync	5	For TMDS SYNC; enable to look for two SYNCs instead of one SYNC in TDD mode	0b0: Disable 0b1: Enable
ri_eq_per_ch	4	Enable auto EQ per channel for 600MHz+ operation	0b0: Disable 0b1: Enable
ri_allow_msync	3	Enable using multi-SYNCs in sync period in MHL+ TDD mode	0b0: Disable 0b1: Enable
ri_enh_algn_fifo	2	Enable limited past up to 16 cycles	0b0: Disable 0b1: Enable
ri_tdd_mode	1	Enable MHL3+ TDD mode sync detection	0b0: Disable 0b1: Enable
ri_red_lat	0	Enable reduced latency option	0b0: Disable 0b1: Enable

ZONE_STATUS_0 (0x3E81)

BIT	7	6	5	4	3	2	1	0
Field	ro_pll_lk	–	–	–	ro_szone[2:0]			ro_f1g
Reset	0b0	–	–	–	0b000			0b0
Access Type	Read Only	–	–	–	Read Only			Read Only

BITFIELD	BITS	DESCRIPTION
ro_pll_lk	7	PLL lock status. 1 indicates PLL locked. Enabled if ri_lkdt_en.
ro_szone	3:1	3-bit zone control value.
ro_f1g	0	High when zone input clock is higher than 1G.

PLL_MODE0 (0x3E8D)*

BIT	7	6	5	4	3	2	1	0
Field	ri_hdmi_mhln_sel_ow	ri_hdmi_mhln_sel_ow_en	–	RSVD[1:0]		RSVD[1:0]		RSVD
Reset	0b0	0b0	–	0b00		0b00		0b0
Access Type	Write, Read	Write, Read	–					

BITFIELD	BITS	DESCRIPTION	DECODE
ri_hdmi_mhln_sel_ow	7	HDMI/MHL select for overwrite	0: HDMI mode 1: MHL mode
ri_hdmi_mhln_sel_ow_en	6	HDMI/MHL select overwrite enable	0: Disable overwrite 1: Enable overwrite

ZONE_INTR (0x3E94)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	reg_pll_lk	reg_lkdt_timeout	reg_vcocal_done	reg_zone_done
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
reg_pll_lk	3	PLL lock interrupt	0b0: No PLL lock interrupt 0b1: PLL lock interrupt
reg_lkdt_timeout	2	Lock detect timeout	0b0: No lock detect timeout interrupt 0b1: Lock detect timeout interrupt
reg_vcocal_done	1	VCO calibration done interrupt	0b0: No VCO calibration done interrupt 0b1: VCO calibration done interrupt
reg_zone_done	0	Zone done interrupt	0b0: No zone done interrupt 0b1: Zone done interrupt

ZONE_INTR_MASK (0x3E95)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	ri_mask3	ri_mask2	ri_mask1	ri_mask0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ri_mask3	3	Interrupt mask for reg_pll_lk	0b0: Disable 0b1: Enable
ri_mask2	2	Interrupt mask for reg_lkdt_timeout	0b0: Disable 0b1: Enable
ri_mask1	1	Interrupt mask for reg_vcocal_done	0b0: Disable 0b1: Enable
ri_mask0	0	Interrupt mask for reg_zone_done	0b0: Disable 0b1: Enable

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/24	Initial release	—

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