19-5760; Rev 0; 7/11

EVALUATION KIT AVAILABLE

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

MAX9679A

General Description

The MAX9679A provides multiple programmable reference voltages for gamma correction in TFT LCDs and a programmable reference voltage for VCOM adjustment. All gamma and VCOM reference voltages have a 10-bit digital-to-analog converter (DAC) and high- current buffer, which reduces the recovery time of the output voltages when critical levels and patterns are displayed. A programmable internal reference sets the full-scale voltage of the DACs.

Two independent sets of gamma curves and VCOM codes can be stored in the IC's volatile memory; BKSEL signal selects between the two sets.

Features

- ♦ **12 Channels of Programmable Gamma Voltages with 10-Bit Resolution**
- ♦ **Programmable VCOM Voltage with 10-Bit Resolution**
- ♦ **Programmable Reference for DACs**
- ♦ **Switching Between Two Gamma Curves and VCOM Voltages**
- ♦ **AVDD1, AVDD2, and AVDD_AMP Supplies to Reduce Heat**
- ♦ **I²C Interface (1MHz Fast-Mode Plus)**

Applications

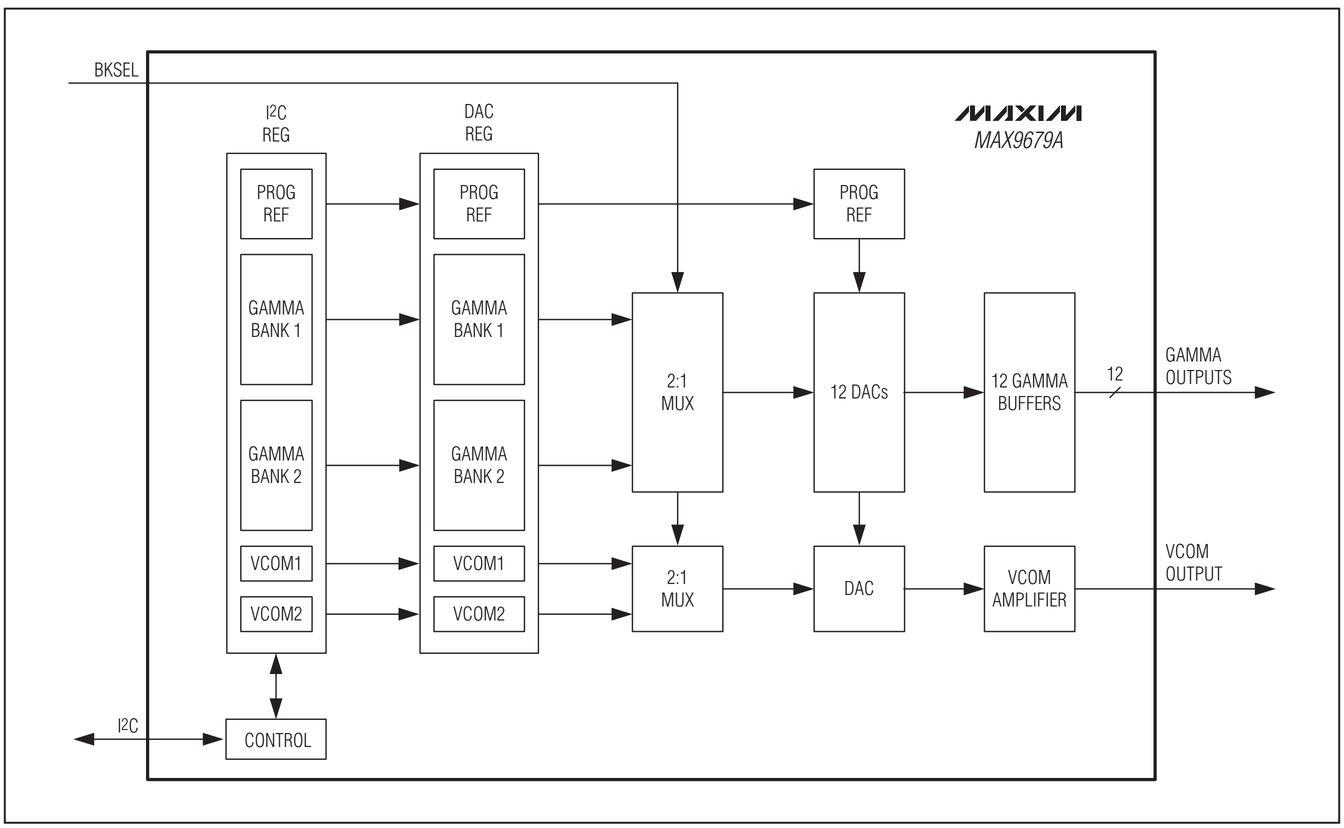
TFT LCDs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9679AETG+	-40°C to +85°C	24 TQFP-EP*

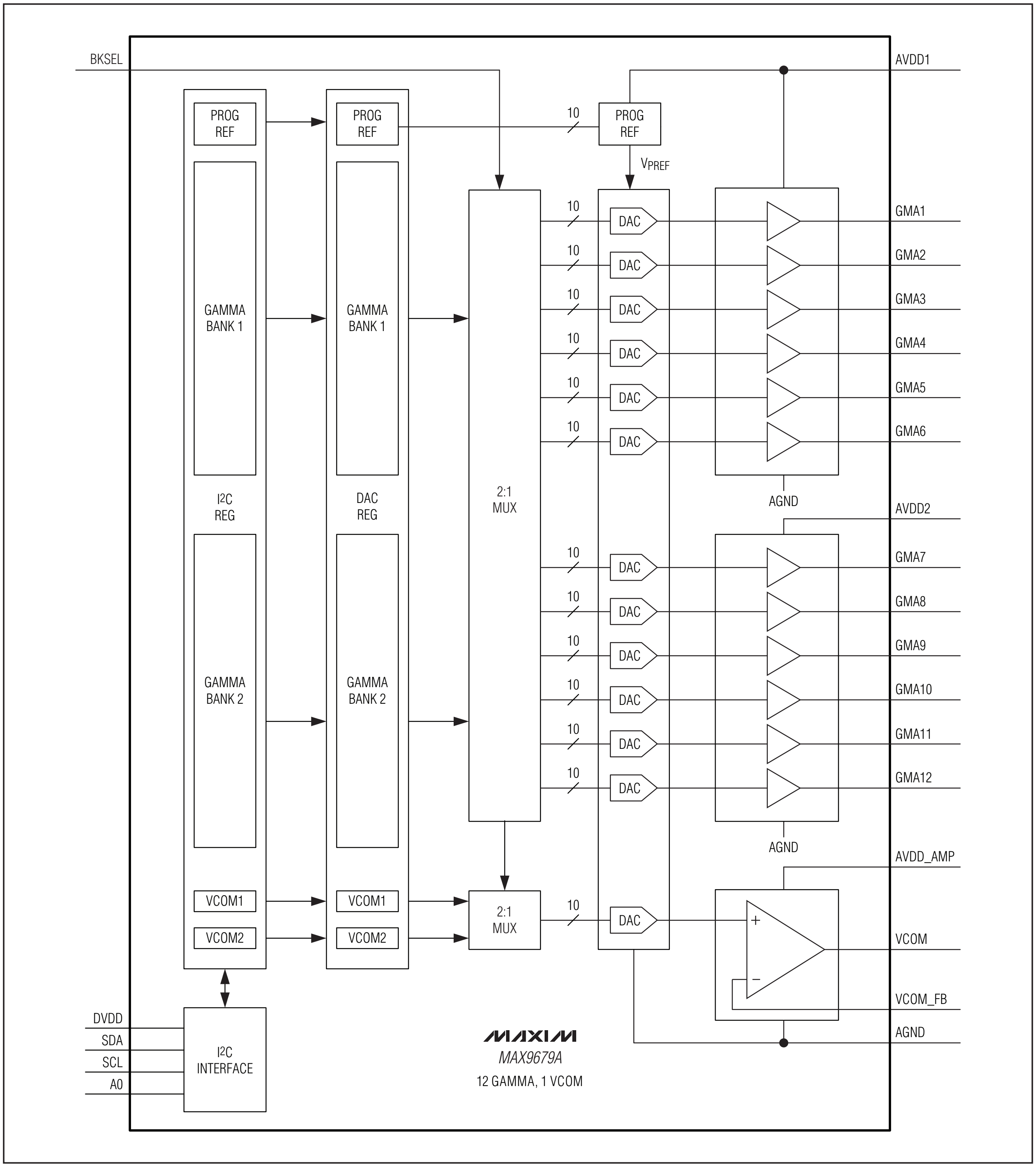
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Block Diagram

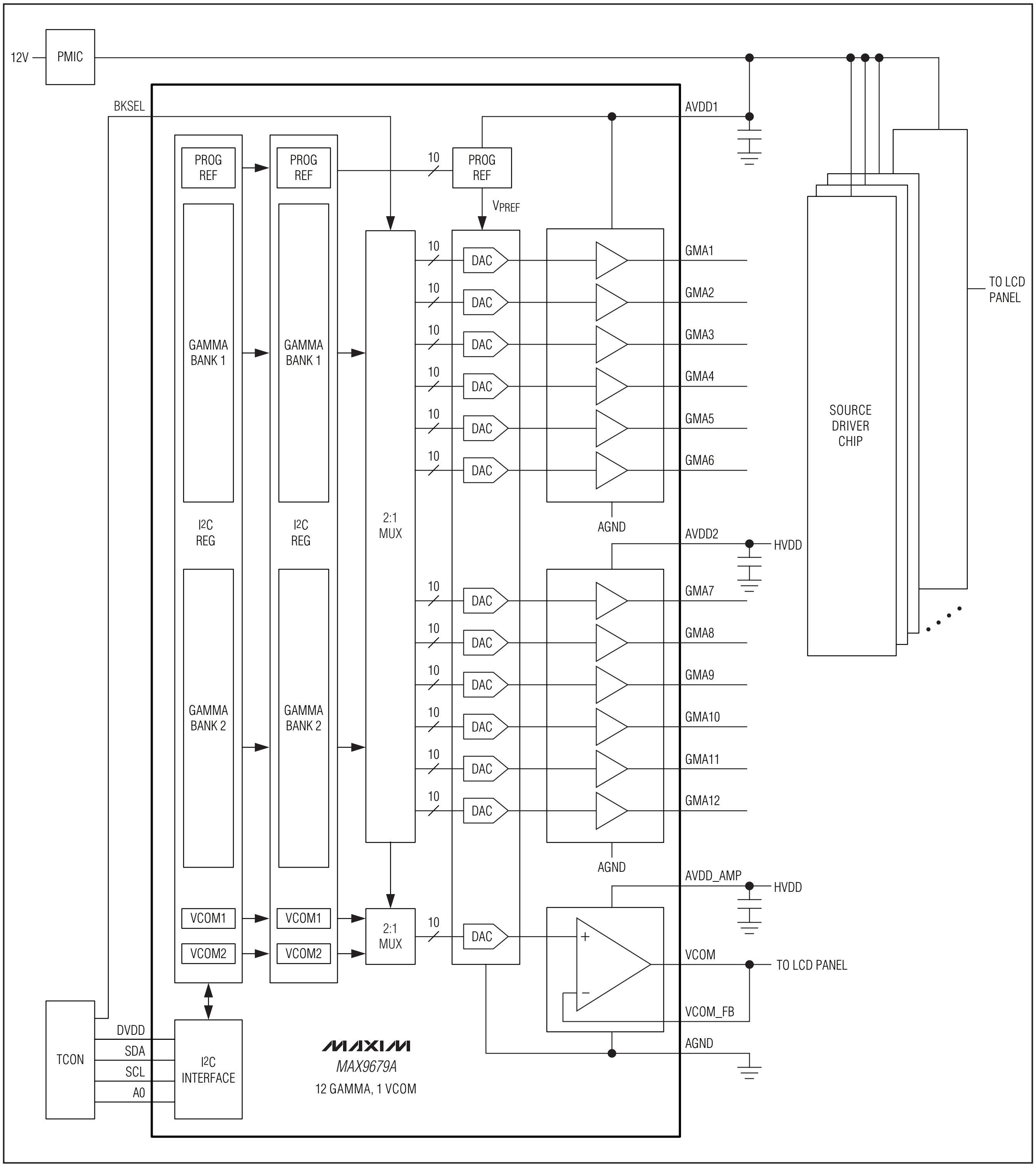


12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

Functional Diagram



Typical Application Circuit



12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

ABSOLUTE MAXIMUM RATINGS

(All voltages are with respect to AGND.)
Supply Voltages
AVDD1, AVDD2, AVDD_AMP .... -0.3V to +22V
DVDD .... -0.3V to +4V
Outputs
GMA1–GMA6 .... -0.3V to (V_{AVDD1} + 0.3V)
GMA7–GMA12 .... -0.3V to (V_{AVDD2} + 0.3V)
VCOM .... -0.3V to (V_{AVDD_AMP} + 0.3V)
Inputs
SDA, SCL, A0, BKSEL .... -0.3V to +6V
VCOM_FB .... -0.3V to (V_{AVDD_AMP} + 0.3V)
Continuous Current
SDA, SCL .... ±20mA
GMA1–GMA8 .... ±200mA
VCOM .... ±600mA
Continuous Power Dissipation (T_A = +70°C)
TQFN Multilayer Board
(derate 25.6mW/°C above +70°C) 2051.3mW
Junction Temperature .... +125°C
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
AVDD1 Analog Supply Voltage Range	V_{AVDD1}	Guaranteed by PSRR	9		20	V
AVDD2 Analog Supply Voltage Range	V_{AVDD2}	Guaranteed by PSRR	6		20	V
AVDD_AMP Analog Supply Voltage Range	V_{AVDD_AMP}	Guaranteed by PSRR	9		20	V
Digital Supply Voltage	V_{DVDD}		2.7		3.6	V
AVDD1 Analog Quiescent Current	I_{AVDD1}			7	11	mA
AVDD2 Quiescent Current	I_{AVDD2}			6	9	mA
AVDD_AMP Quiescent Current	I_{AVDD_AMP}			5	8	mA
Digital Quiescent Current	I_{DVDD}	No SCL or SDA transitions		4.4	6.3	mA
Thermal Shutdown				+160		°C
Thermal-Shutdown Hysteresis				15		°C
Undervoltage-Lockout Threshold	UVLO	DVDD undervoltage-lockout threshold	2.1	2.3	2.6	V
PROGRAMMABLE REFERENCE (V_{PREF})						
Full-Scale Voltage		Referred to output, T_A = +25°C	19.96	19.98	20	V
Resolution			10			Bits

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Nonlinearity Error		T_A = +25°C, 336 ≤ reference code ≤ 1007		0.5	1	LSB
Differential Nonlinearity Error		T_A = +25°C, 336 ≤ reference code ≤ 1007		0.5	1	LSB
DAC						
Resolution			10			Bits
Integral Nonlinearity Error		T_A = +25°C, 16 ≤ code ≤ 1008 for gamma, 256 ≤ code ≤ 1008 for VCOM		0.5	1	LSB
Differential Nonlinearity Error		T_A = +25°C, 16 ≤ code ≤ 1008 for gamma, 256 ≤ code ≤ 1008 for VCOM		0.5	1	LSB
GAMMA						
Short-Circuit Current		Output connected to either supply rail		200		mA
Total Output Error		T_A = +25°C, code = 768 for GMA1–GMA6 and code = 256 for GMA7–GMA12		40		mV
Load Regulation		-5mA ≤ I_{LOAD} ≤ +5mA, code = 768 for GMA1–GMA6 and code = 256 for GMA7–GMA12		0.5		mV/mA
Low Output Voltage		Sinking 4mA, referred to lower supply rail		0.15	0.2	V
High Output Voltage		Sourcing 4mA, referred to upper supply rail	-0.2	-0.15		V
Power Supply Rejection Ratio		GMA1–GMA6, code = 768, V_{AVDD1} = 9V to 20V; GMA7–GMA12, code = 256, V_{AVDD2} = 5V to 20V	60	90		dB
		GMA1–GMA6, code = 768, frequency = 120kHz; GMA7–GMA12, code = 256, frequency = 120kHz		40		
Output Resistance		Buffer is disabled		78		kΩ
Maximum Capacitive Load		Placed directly at output		150		pF
Noise		RMS noise (10MHz bandwidth)		375		µV
VCOM OUTPUT (VCOM)						
Short-Circuit Current		Output connected to either VCOM amplifier supplies		600		mA
Total Output Error		T_A = +25°C, code = 256, V_{AVDD_AMP} = 9V and 20V		40		mV
Load Regulation		-80mA ≤ I_{LOAD} ≤ +80mA, code = 256		0.5		mV/mA
Low Output Voltage		Sinking 10mA, referred to lower supply rail		0.15	0.2	V
High Output Voltage		Sourcing 10mA, referred to upper supply rail	-0.2	-0.15		V

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio		9V ≤ V_{AVDD_AMP} ≤ 20V, code = 256	60	90		dB
		Frequency = 120kHz, code = 256		40		
Maximum Capacitive Load		Placed directly at output		50		pF
Slew Rate		Swing 4V_{P-P} at VCOM, 10% to 90%, R_L = 10kΩ, C_L = 50pF		100		V/µs
Bandwidth		R_L = 10kΩ, C_L = 50pF		60		MHz
Noise		RMS noise (10MHz bandwidth)		375		µV

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

DIGITAL I/O CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 x DVDD			V
Low-Level Output Voltage	V_{OL}	Open drain, I_{SINK} = 3mA	0		0.4	V
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V	20			mA
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0 or DVDD	-10	+0.01	+10	µA
Input Capacitance				5		pF
Power-Down Input Current	I_{IN}	DVDD = 0, V_{IN} = 1.98V	-10		+10	µA

I²C TIMING CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD,STA}$	After this period, the first clock pulse is generated	0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a REPEATED START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$	I²C-bus devices	0			ns
Data Setup Time	$t_{SU,DAT}$		50			ns

I2C TIMING CHARACTERISTICS (continued)

(V_{DVDD} = 3.3V, V_{AGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA and SCL Receiving Rise Time	t_R				120	ns
SDA and SCL Receiving Fall Time	t_F				120	ns
SDA Transmitting Fall Time	t_F				120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Bus Capacitance	C_B				550	pF
Data Valid Time	$t_{VD;DAT}$				0.45	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$				0.45	µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

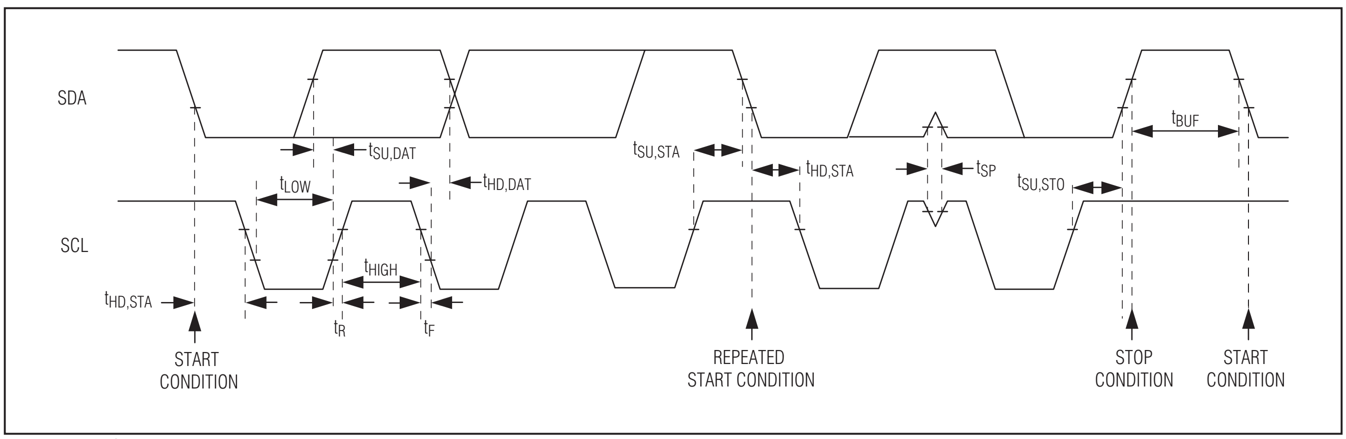


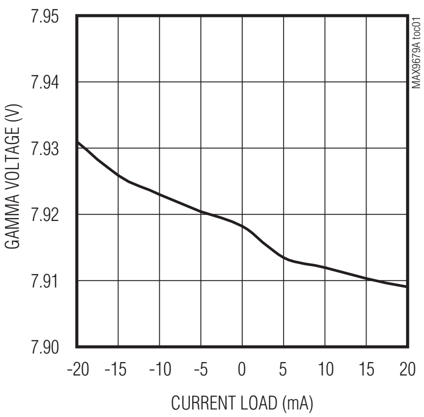
Figure 1. I2C Interface Timing Diagram

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

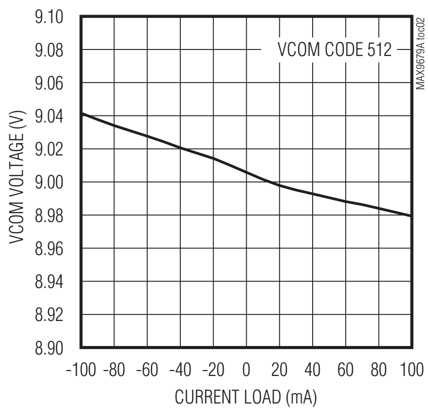
Typical Operating Characteristics

(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

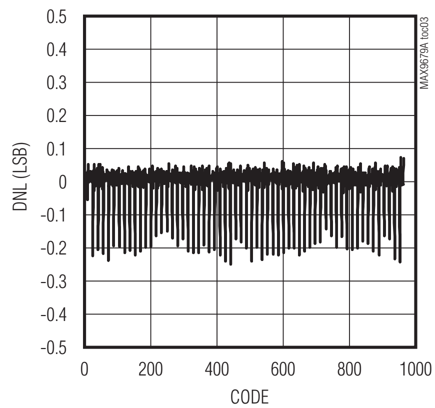
GAMMA LOAD REGULATION



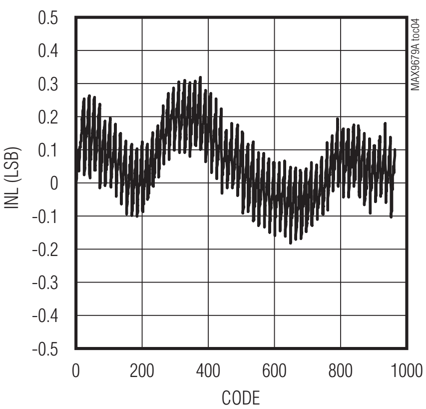
VCOM LOAD REGULATION



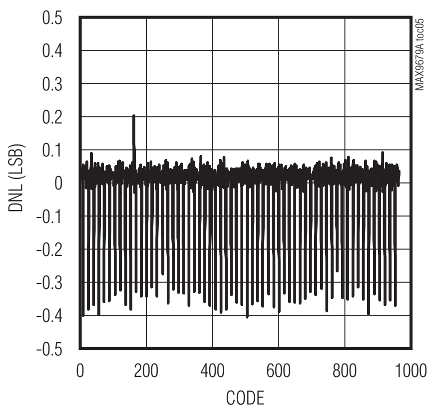
GAMMA DNL



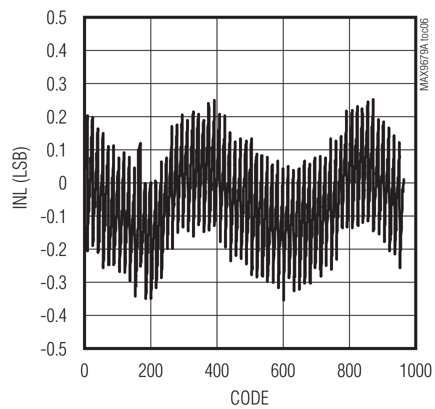
GAMMA INL



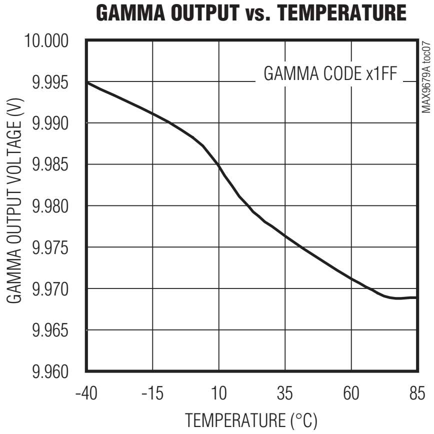
VCOM DNL



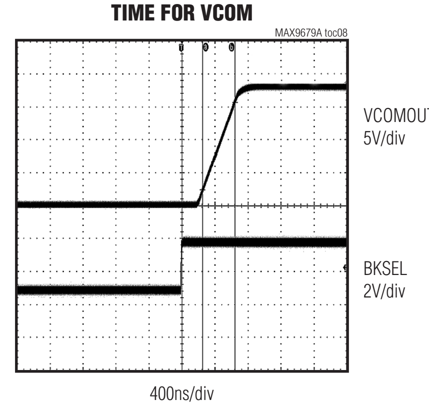
VCOM INL



GAMMA OUTPUT vs. TEMPERATURE



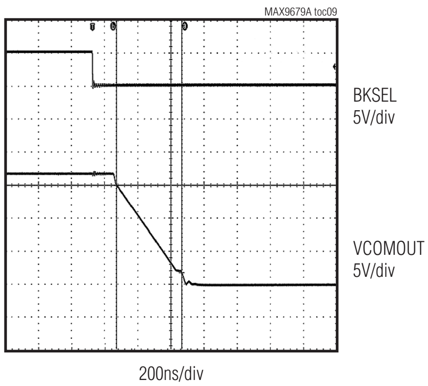
BANK SWITCHING SETTLING TIME FOR VCOM



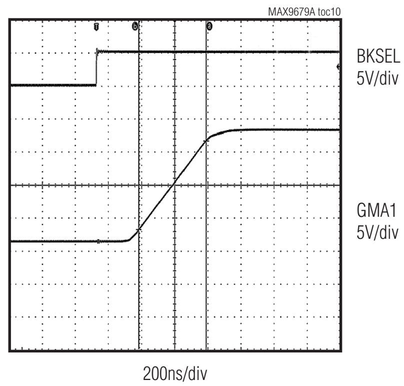
Typical Operating Characteristics (continued)

(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

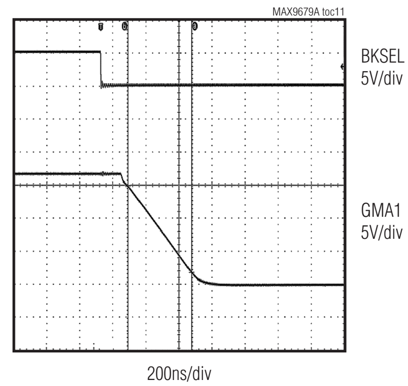
BANK SWITCHING SETTLING TIME FOR VCOM



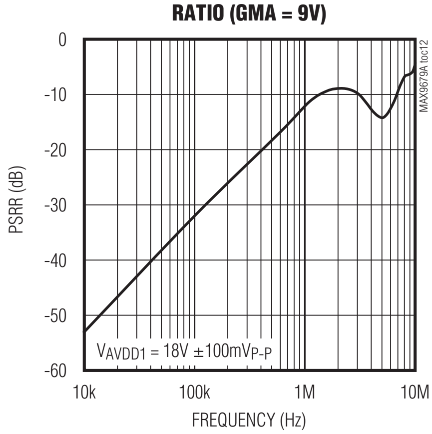
BANK SWITCHING SETTLING TIME FOR GAMMA



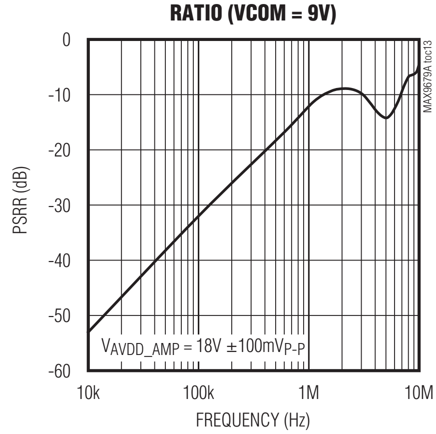
BANK SWITCHING SETTLING TIME FOR GAMMA



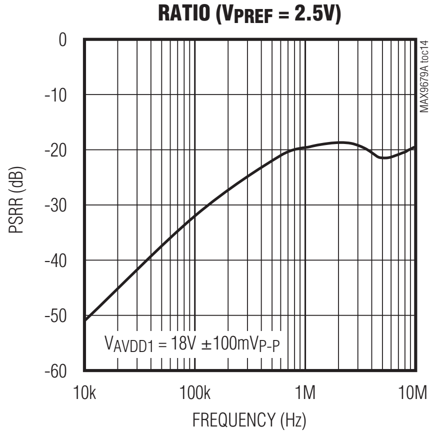
POWER-SUPPLY REJECTION RATIO (GMA = 9V)



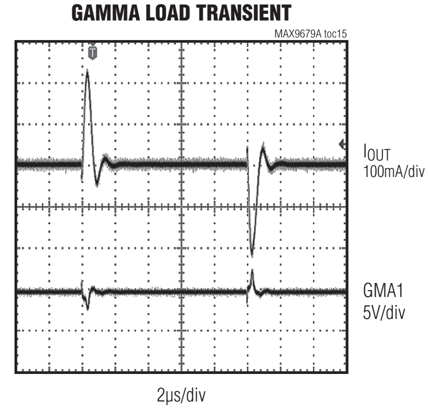
POWER-SUPPLY REJECTION RATIO (VCOM = 9V)



POWER-SUPPLY REJECTION RATIO (V_{PREF} = 2.5V)



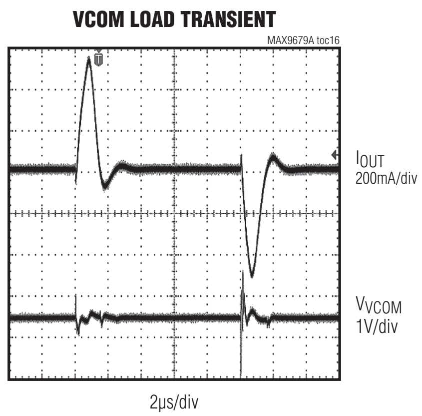
GAMMA LOAD TRANSIENT

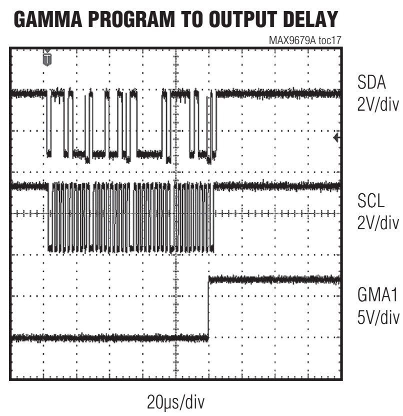


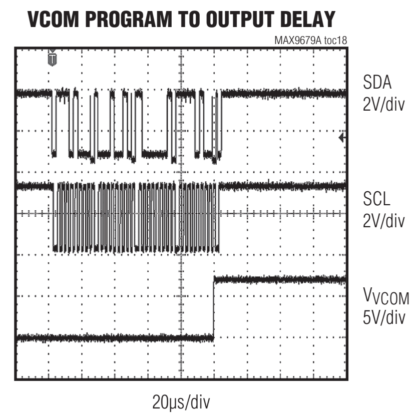
12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

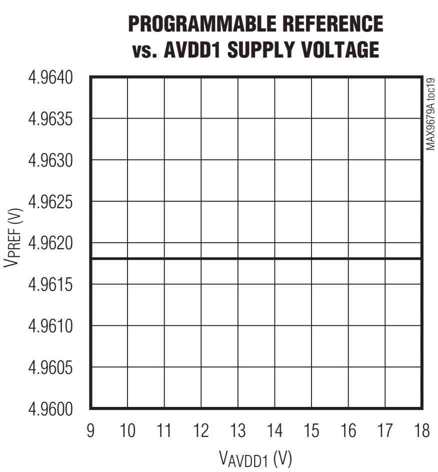
Typical Operating Characteristics (continued)

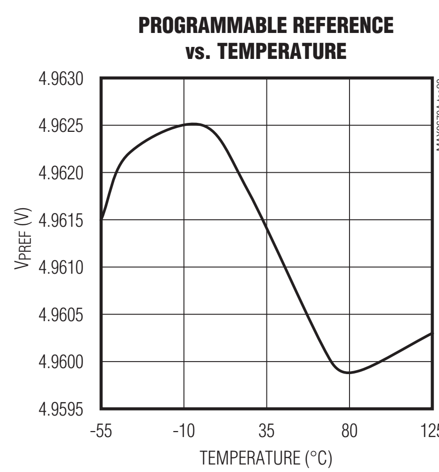
(V_{AVDD1} = 18V, V_{AVDD2} = V_{AVDD_AMP} = 9V, V_{DVDD} = 3.3V, V_{AGND} = 0V, VCOM = VCOM_FB, programmable reference code = 905, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)



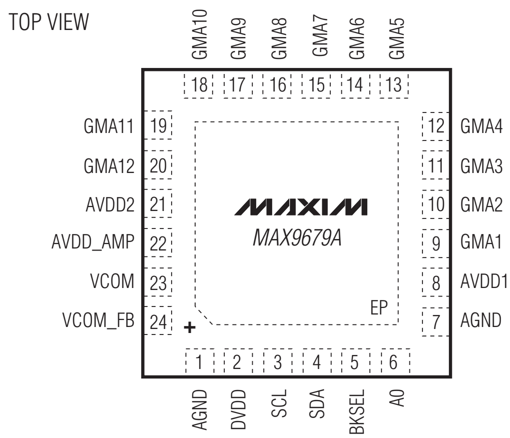








Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 7	AGND	Analog Ground
2	DVDD	Digital Power Supply. Bypass DVDD with a 0.1µF capacitor to AGND.
3	SCL	I^2C-Compatible Serial-Clock Input
4	SDA	I^2C-Compatible Serial-Data Input/Output
5	BKSEL	Bank Select Logic Input. Selects which bank of volatile registers are switched through to the DACs.
6	A0	I^2C-Compatible Device Address Bit 0 (Input)
8	AVDD1	Analog Power Supply 1. The buffers for GMA1 through GMA6 operate from AVDD1. Bypass AVDD1 with a 0.1µF capacitor to AGND.
9	GMA1	Gamma DAC Analog Output 1
10	GMA2	Gamma DAC Analog Output 2
11	GMA3	Gamma DAC Analog Output 3
12	GMA4	Gamma DAC Analog Output 4
13	GMA5	Gamma DAC Analog Output 5
14	GMA6	Gamma DAC Analog Output 6
15	GMA7	Gamma DAC Analog Output 7
16	GMA8	Gamma DAC Analog Output 8
17	GMA9	Gamma DAC Analog Output 9
18	GMA10	Gamma DAC Analog Output 10
19	GMA11	Gamma DAC Analog Output 11
20	GMA12	Gamma DAC Analog Output 12
21	AVDD2	Analog Power Supply 2. The buffers for GMA7 through GMA12 operate from AVDD2. Bypass AVDD2 with a 0.1µF capacitor to AGND.
22	AVDD_AMP	Power Supply for VCOM Amplifier. Bypass AVDD_AMP with a 0.1µF capacitor to AGND.
23	VCOM	VCOM Output
24	VCOM_FB	Feedback for VCOM Amplifier. VCOM_FB is the negative input terminal of the VCOM operational amplifier.
—	EP	Exposed Pad. EP is internally connected to AGND. EP must be connected to AGND.

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

Detailed Description

The MAX9679A combines gamma, VCOM, and the DAC reference voltage into a single chip. All the output voltages are programmable. Power sequencing is well behaved since a single chip generates all the various reference voltages needed for the LCD panel.

Previous generations of programmable gamma chips required an external reference voltage for the digital-to-analog converters (DACs). This IC integrates a programmable reference voltage (V_{PREF}) for the DACs, eliminating the need for an external reference voltage. Accuracy of the full-scale programmable reference voltage is ±0.1%, and resolution is 10 bits. Both the DC and AC power-supply rejection of the programmable reference voltage is extremely high since it is powered from an internal linear regulator.

The gamma outputs are divided into an upper bank (GMA1–GMA6) that is powered from AVDD1 and a lower bank (GMA7–GMA12) that is powered from AVDD2. AVDD1 is the analog supply voltage for the LCD panel. AVDD2 can be connected to the same supply as AVDD1. If the IC's heat generation needs to be reduced, AVDD2 can be connected to a lower voltage such as 12V (input voltage to the LCD panel) or HVDD (half of the AVDD1 supply).

The VCOM operational amplifier operates from AVDD_AMP. Similar to AVDD2, AVDD_AMP can be connected to AVDD1, 12V, or HVDD. Peak VCOM output current is 600mA. The negative input terminal of the VCOM operational amplifier is available for applications that require external push-pull transistors.

The interface and control of the IC are completely digital. Functions that are not real-time such as gamma and VCOM are set through the I^2C interface. Real-time functions, such as the switching of the gamma and VCOM, are done through the dedicated logic input signal BKSEL.

Programmable Reference

The IC has an internal programmable reference, which when referred to the output, has a full-scale voltage of 20V (±0.1%). The reference voltage is calculated using the following equation:

$$V_{PREF} = (20V \times CODE)/2^N$$

where CODE is the numeric value stored in register address and N is the bits of resolution. For the IC, N = 10 and CODE ranges from 0 to 1023.

Note that V_{PREF} cannot be 20V because the maximum value of CODE is always one LSB less than the full-scale voltage. When the programmable reference code is 1023, then V_{PREF} is:

$$V_{PREF} = (20V \times 1023)/2^{10} = 19.98V$$

10-Bit Digital-to-Analog Converters

V_{PREF} sets the full-scale output of the DACs. Determine the output voltages using the following equations:

$$V_{GMA\_} = (V_{PREF} \times CODE)/2^N$$

$$V_{VCOM} = (V_{PREF} \times CODE)/2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the IC, N = 10 and CODE ranges from 0 to 1023.

Note that the DAC can never output V_{PREF} because the maximum value of CODE is always one LSB less than the reference. For example, if V_{PREF} = 16V and the DAC CODE is 1023, then the gamma output voltage is:

$$V_{GMA\_} = (16V \times 1023)/2^{10} = 15.98438V$$

Gamma Buffers

The gamma buffers can typically source or sink 4mA of DC current within 200mV of the supplies.

The source drivers can kick back a great deal of current to the buffer outputs during a horizontal line change or a polarity switch. The DAC output buffers can source/sink 200mA of peak transient current to reduce the recovery time of the output voltages when critical levels and patterns are displayed.

VCOM Amplifier

The operational amplifier attached to the VCOM DAC holds the VCOM voltage stable while providing the ability to source and sink 600mA into the backplane of a TFT-LCD panel. The operational amplifier can directly drive the capacitive load of the TFT-LCD backplane without the need for a series resistor in most cases. The VCOM amplifier has current limiting on its output to protect its bond wires.

If the application requires more than 600mA, buffer the output of the VCOM amplifier with a MAX9650, a VCOM power amplifier. The MAX9650 can source or sink 1.3A of current.

Switching Gamma and VCOM

The IC can keep two independent sets of gamma and VCOM codes in volatile memory (Table 1).

The BKSEL signal determines which set of gamma and VCOM codes is driven out (Table 2).

Power-On Reset (POR)

The IC contains an integrated POR circuit that ensures all registers are reset to a known state on power-up. Once DVDD rises above 2.4V (typ), the POR circuit releases the registers for normal operation. Should the internal supply input drop to less than 2.4V (typ), the contents of the IC registers can no longer be guaranteed.

Thermal Shutdown

The IC features thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +165°C, all of the gamma outputs and the VCOM output are disabled. When the die cools down by 15°C, the outputs are enabled again.

Register and Bit Descriptions

The IC has volatile memory. The volatile memory structure has I^2C registers and DAC registers (see the *Functional Diagram*). The I^2C master must first write data into the I^2C registers of the IC before the data can be moved into the DAC registers. The advantage of having the I^2C registers serve as a data buffer for the IC is that data can be transferred in a parallel operation from the I^2C registers to the DAC registers, and so the entire gamma curve is essentially updated instantaneously rather than serially on a point-by-point basis.

The volatile memory stores two independent sets of gamma curves and VCOM codes. The first set consists of gamma codes from bank 1, VCOM1 code, VCOM1MIN code, and VCOM1MAX code. The second set consists of gamma codes from bank 2, VCOM2 code, VCOM2MIN code, and VCOM2MAX code. In addition, volatile memory stores the programmable reference code.

Each memory location in volatile memory holds a 10-bit word. Two bytes must be read or written through the I^2C interface for every register. Table 3 shows the register map.

Table 1. Registers in Each of the Two Independent Sets

REGISTERS IN SET 1	REGISTERS IN SET 2
GMA1BK1	GMA1BK2
GMA2BK1	GMA2BK2
GMA3BK1	GMA3BK2
GMA4BK1	GMA4BK2
GMA5BK1	GMA5BK2
GMA6BK1	GMA6BK2
GMA7BK1	GMA7BK2
GMA8BK1	GMA8BK2
GMA9BK1	GMA9BK2
GMA10BK1	GMA10BK2
GMA11BK1	GMA11BK2
GMA12BK1	GMA12BK2
VCOM1	VCOM2
VCOM1MIN	VCOM2MIN
VCOM1MAX	VCOM2MAX

Table 2. BKSEL Logic Table

OUTPUT	BKSEL = LOW	BKSEL = HIGH
GMA1	GMA1BK1	GMA1BK2
GMA2	GMA2BK1	GMA2BK2
GMA3	GMA3BK1	GMA3BK2
GMA4	GMA4BK1	GMA4BK2
GMA5	GMA5BK1	GMA5BK2
GMA6	GMA6BK1	GMA6BK2
GMA7	GMA7BK1	GMA7BK2
GMA8	GMA8BK1	GMA8BK2
GMA9	GMA9BK1	GMA9BK2
GMA10	GMA10BK1	GMA10BK2
GMA11	GMA11BK1	GMA11BK2
GMA12	GMA12BK1	GMA12BK2
VCOM	VCOM1	VCOM2

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

Register Description

Only the 10 least significant bits (LSBs) are written to the registers (Table 4). During a write operation, the write control bits (the two MSBs) are stripped from the incoming data stream and are used to determine whether the DAC registers are updated (Table 5). Note the I²C registers are only 10 bits.

Table 3. Register Map

REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	POWER-ON RESET VALUE
0x00	GMA1BK1	Gamma 1 of Bank 1	0x200
0x01	GMA2BK1	Gamma 2 of Bank 1	0x200
0x02	GMA3BK1	Gamma 3 of Bank 1	0x200
0x03	GMA4BK1	Gamma 4 of Bank 1	0x200
0x04	GMA5BK1	Gamma 5 of Bank 1	0x200
0x05	GMA6BK1	Gamma 6 of Bank 1	0x200
0x06	GMA7BK1	Gamma 7 of Bank 1	0x200
0x07	GMA8BK1	Gamma 8 of Bank 1	0x200
0x08	GMA9BK1	Gamma 9 of Bank 1	0x200
0x09	GMA10BK1	Gamma 10 of Bank 1	0x200
0x0A	GMA11BK1	Gamma 11 of Bank 1	0x200
0x0B	GMA12BK1	Gamma 12 of Bank 1	0x200
0x0C	Reserved	—	0x000
0x0D	Reserved	—	0x000
0x0E	Reserved	—	0x000
0x0F	Reserved	—	0x000
0x10	Reserved	—	0x000
0x11	Reserved	—	0x000
0x12	VCOM1	Common voltage 1	0x200
0x13	Reserved	—	0x000
0x14	Reserved	—	0x000
0x15	Reserved	—	0x000
0x16	Reserved	—	0x000
0x17	Reserved	—	0x000
0x18	VCOM1MIN	Minimum VCOM1 value	0x000
0x19	VCOM1MAX	Maximum VCOM1 value	0x3FF
0x1A	Reserved	—	0x000
0x1B	Reserved	—	0x000
0x1C	Reserved	—	0x000
0x1D	Reserved	—	0x000
0x1E	Reserved	—	0x000

Table 3. Register Map (continued)

REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	POWER-ON RESET VALUE
0x1F	VPREF	Programmable reference voltage	0x200
0x20	GMA1BK2	Gamma 1 of Bank 2	0x200
0x21	GMA2BK2	Gamma 2 of Bank 2	0x200
0x22	GMA3BK2	Gamma 3 of Bank 2	0x200
0x23	GMA4BK2	Gamma 4 of Bank 2	0x200
0x24	GMA5BK2	Gamma 5 of Bank 2	0x200
0x25	GMA6BK2	Gamma 6 of Bank 2	0x200
0x26	GMA7BK2	Gamma 7 of Bank 2	0x200
0x27	GMA8BK2	Gamma 8 of Bank 2	0x200
0x28	GMA9BK2	Gamma 9 of Bank 2	0x200
0x29	GMA10BK2	Gamma 10 of Bank 2	0x200
0x2A	GMA11BK2	Gamma 11 of Bank 2	0x200
0x2B	GMA12BK2	Gamma 12 of Bank 2	0x200
0x2C	VCOM2	Common voltage 2	0x200
0x2D	VCOM2MIN	Minimum VCOM2 value	0x000
0x2E	VCOM2MAX	Maximum VCOM2 value	0x3FF

Table 4. Register Description

REG	REG ADDR	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
GMA1BK1	0x00	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA2BK1	0x01	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA3BK1	0x02	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA4BK1	0x03	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA5BK1	0x04	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA6BK1	0x05	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA7BK1	0x06	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA8BK1	0x07	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA9BK1	0x08	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA10BK1	0x09	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA11BK1	0x0A	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA12BK1	0x0B	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Reserved	0x0C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x0D	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x0E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x0F	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x10	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x11	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VCOM1	0x12	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

Table 4. Register Description (continued)

REG	REG ADDR	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved	0x13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x15	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VCOM1MIN	0x18	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VCOM1MAX	0x19	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Reserved	0x1A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x1B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x1C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x1D	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reserved	0x1E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VPREF	0x1F	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA1BK2	0x20	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA2BK2	0x21	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA3BK2	0x22	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA4BK2	0x23	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA5BK2	0x24	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA6BK2	0x25	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA7BK2	0x26	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA8BK2	0x27	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA9BK2	0x28	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA10BK2	0x29	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA11BK2	0x2A	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA12BK2	0x2B	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VCOM2	0x2C	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VCOM2MIN	0x2D	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VCOM2MAX	0x2E	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 5. Write Control Bits

W1	W0	ACTION
0	0	No update.
0	1	Do not use.
1	0	All DAC registers get updated when the current I^2C register has finished updating (end of B0).
1	1	No update.

VCOM Programmable Range (VCOMMIN and VCOMMAX)

The IC features a programmable range for VCOM1 and VCOM2. VCOM1MIN and VCOM1MAX registers provide low and high limits for the VCOM1 register. At the factory, VCOM1MIN is set to 0 and VCOM1MAX is set to 1023 (default values) to provide the full rail-to-rail programmable range for VCOM1. Later, the user can define their own limits by programming VCOM1MIN and VCOM1MAX registers.

VCOM1 register values are limited to the defined range. If the VCOM1 register accidentally gets programmed with a value higher than VCOM1MAX, it automatically gets locked to the VCOM1MAX value. The I²C bus does acknowledge and receive the data sent on the bus; however, internally the part recognizes that the value is outside of the range and adjusts it accordingly. The same scenario is true if the value programming VCOM1 is below VCOM1MIN.

VCOM2MIN and VCOM2MAX have a similar relationship with VCOM2.

Volatile Memory

The IC features a double-buffered register structure with the I²C registers as the first buffer and the DAC registers as the second buffer. The benefit is that the I²C registers can be updated without updating the DAC registers. After the I²C registers have been updated, the value or values in the I²C registers can be transferred all at the same time to the DAC registers.

Figure 2 shows how to program a single DAC register. The output voltage is updated after sending LSB (D0). It is possible to write to multiple I²C registers first, then update the output voltage of all channels simultaneously, as shown in Figure 3. In this mode, it is possible for the I²C master to write to all registers of the IC (gamma, VCOM, and programmable reference) in one communication. In that case, the value programmed on addresses 0x0C–0x11, 0x13–0x17, 0x1A–0x1E, and 0x20–0x2E are meaningless. However, the IC does send an acknowledge bit for each of the two bytes on any of these addresses. The control bits (W1, W0) shown in Figure 3 are set in a way that all DACs are programmed to their desired value with no changes to the output voltages until the LSB of the last DAC is received and then all the channels update simultaneously.

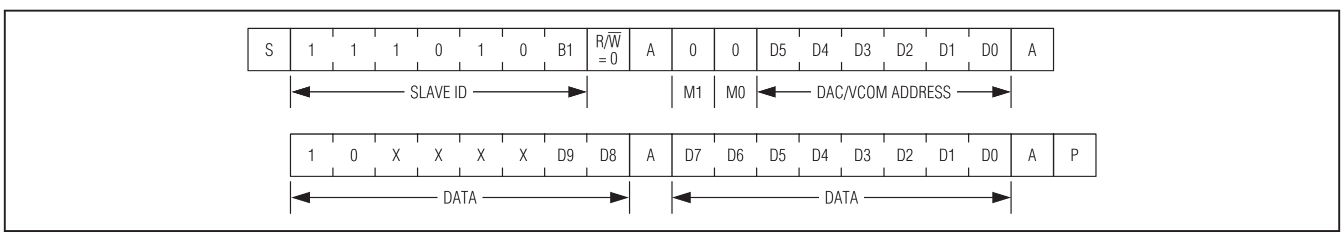


Figure 2. Single DAC Programming

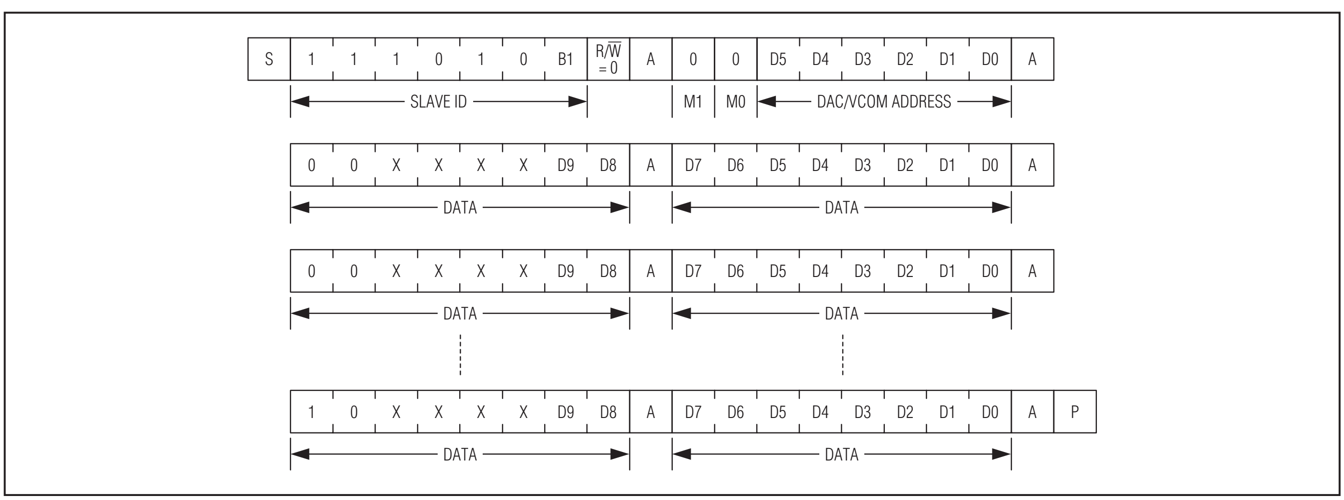


Figure 3. Multiple (or All) DACs Programming

I2C Serial Interface

The IC features an I2C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the devices and the master at clock rates up to 1MHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the devices by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9679A is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the devices transmits the proper slave address followed by a series of nine SCL pulses. The devices transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section. SDA and SCL idle high when the I2C bus is not busy.

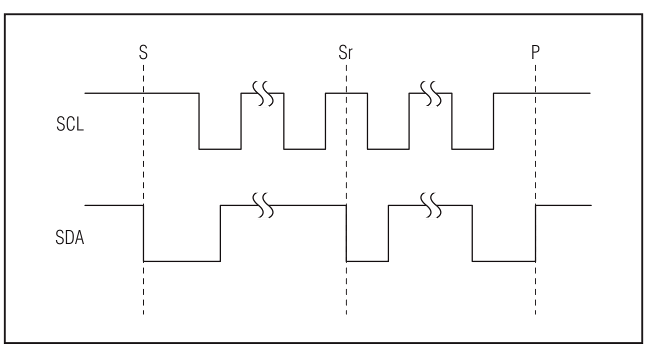


Figure 4. START, STOP, and REPEATED START Conditions

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4).

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the IC to read mode. Set the R/W bit to 0 to configure the IC to write mode. The address is the first byte of information sent to the IC after the START condition. The IC's slave address is configured with A0. Table 6 shows the possible addresses for the IC.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt of each byte of data when in write mode (Figure 5).

Table 6. Slave Address

A0	READ ADDRESS	WRITE ADDRESS
AGND	E9h (11101001)	E8h (11101000)
DVDD	EBh (11101011)	EAh (11101010)

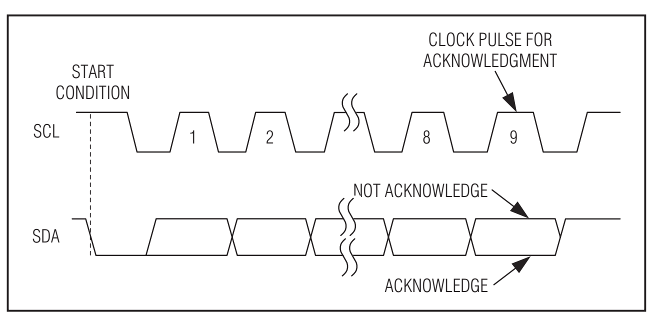


Figure 5. Acknowledge

SMBus is a trademark of Intel Corp.

The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Write Data Format

A write to the IC consists of transmitting a START condition, the slave address with the R/W bit set to 0, 1 data byte of data to configure the internal register address pointer, one word (2 bytes) of data or more, and a STOP condition.

Figure 6 illustrates the proper frame format for writing one word of data to the IC. Figure 7 illustrates the frame format for writing n-bytes of data to the IC.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The IC's internal address pointer consists of the six least significant bits (LSB) of the second byte. The 2 MSBs of the second byte (M1 and M0) are set to 00b when writing to the internal registers. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data when writing to the DAC registers.

The third and fourth bytes sent to the IC contain the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of each data byte.

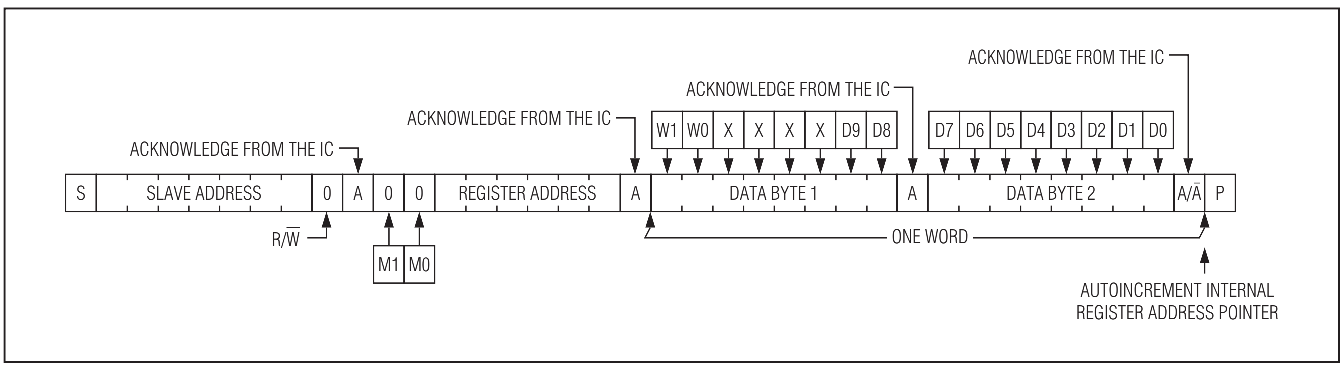


Figure 6. Writing a Word of Data to the IC

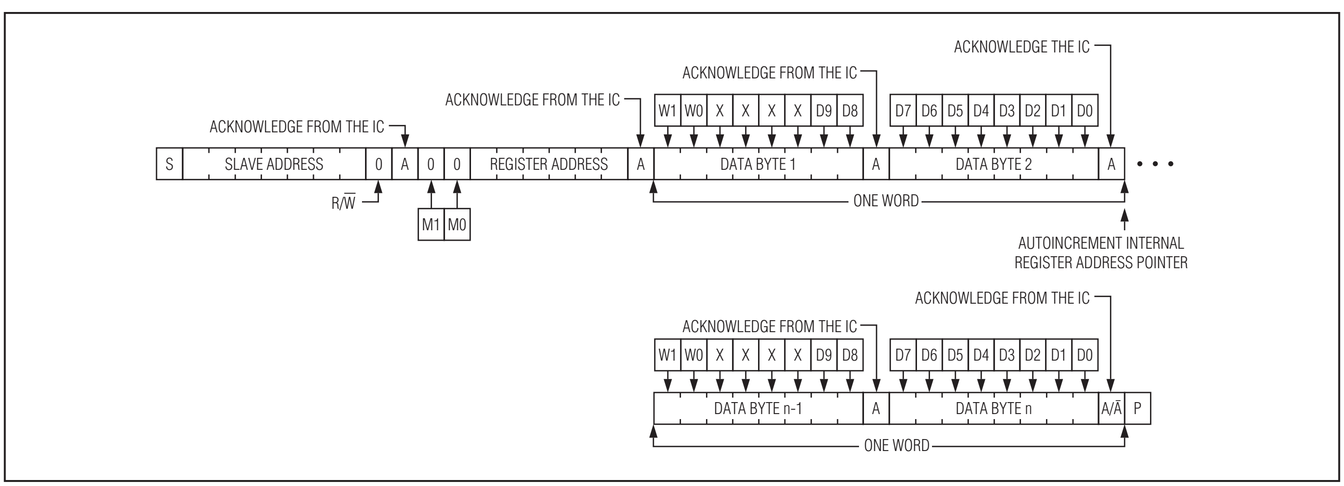


Figure 7. Writing n-Bytes of Data to the IC

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

The address pointer autoincrements to the next register address after receiving every other data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition. If data is written into register address 0x2E, the address pointer autoincrements to 0xFF and stays at 0xFF until the master writes a new value into the register address pointer.

Read Data Format

The master presets the address pointer by first sending the IC's slave address with the R/W bit set to 0 followed by the register address with M1 and M0 set to 00 after a START condition. The IC acknowledges receipt of its slave address and the register address by pulling SDA low during the 9th SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The IC transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after every other read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from the register address location set by the previous transaction and not 0x00, and subsequent reads autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than 0x2E results in repeated reads from a dummy register containing all one data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 8 and 9 illustrate the frame format for reading data from the IC.

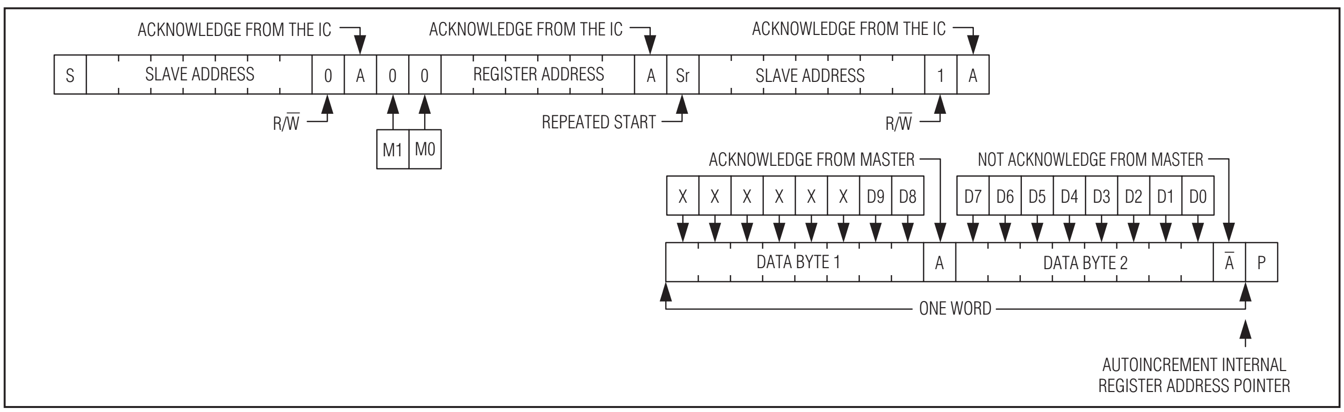


Figure 8. Reading One Indexed Word of Data from the IC

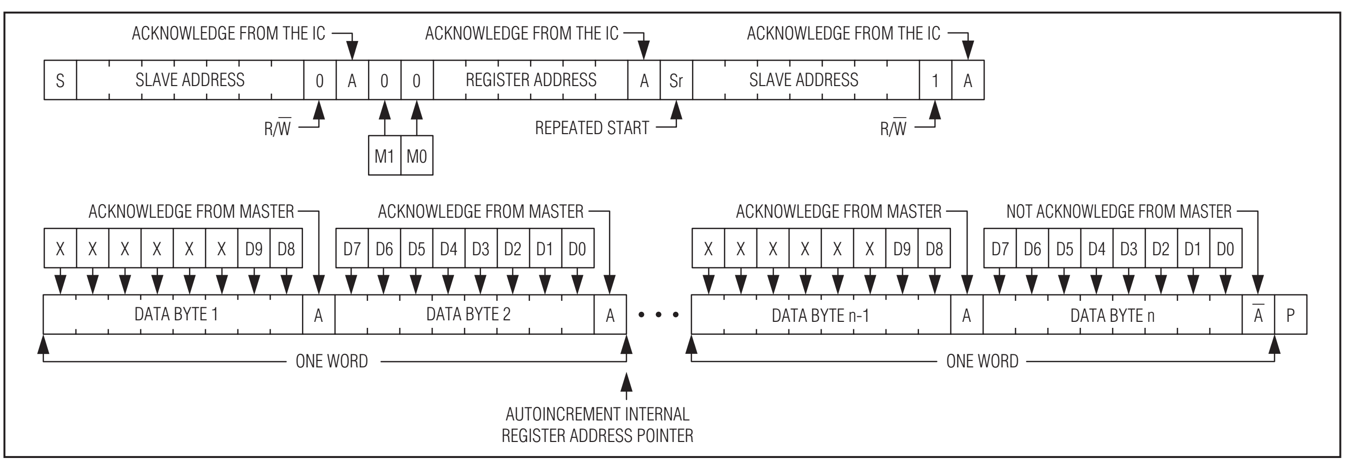


Figure 9. Reading n Bytes of Indexed Data from the IC

Applications Information

Power Sequencing

AVDD1, AVDD2, AVDD_AMP, and DVDD are independent of each other and can be powered up and powered down in any sequence. However, output voltages are only guaranteed to power up in a well-behaved manner when DVDD is powered up first and powered down last (Figures 10 and 11). Connecting AVDD2 and AVDD_AMP to half AVDD supply reduces the temperature of the IC. I^2C commnication is available 150ms after DVDD power-up.

If AVDD2 and AVDD_AMP are connected to the 12V supply to the LCD module because a half AVDD supply is not available, then Figure 12 shows the power-up and power-down sequence. The gamma and VCOM outputs are close to ground until AVDD1 is greater than its power-on reset voltage because AVDD1 is used to power the internal voltage reference.

PCB Layout and Grounding

If the IC is mounted using reflow soldering or waver soldering, the ground vias for the exposed pad should have a finished hole size of at least 14 mils to ensure adequate wicking of soldering onto the exposed pad. If the IC is mounted using solder mask technique, the vias requirement does not apply. In either case, the exposed pad on the TQFN package is electrically connected to both digital and analog grounds through a low thermal resistance path to ensure adequate heat dissipation. Do not route traces under these packages. The layout of the exposed pad should have multiple small vias over a single large via as shown in Figure 13.

Thermal resistance between top and ground layers can be optimized with multiple small vias, and it is recommended to have a plated via with 15 mils diameter. The via should be flooded with solder for good thermal performance.

Power-Supply Bypassing

The IC operates from a single 9V to 20V analog supply (AVDD) and a 2.7V to 3.6V digital supply (DVDD). Bypass AVDD to AGND with 0.1µF and 10µF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to AGND with a 0.1µF capacitor. The 0.1µF bypass capacitors should be as close as possible to the device. Refer to the MAX9679A Evaluation Kit for a proven PCB layout.

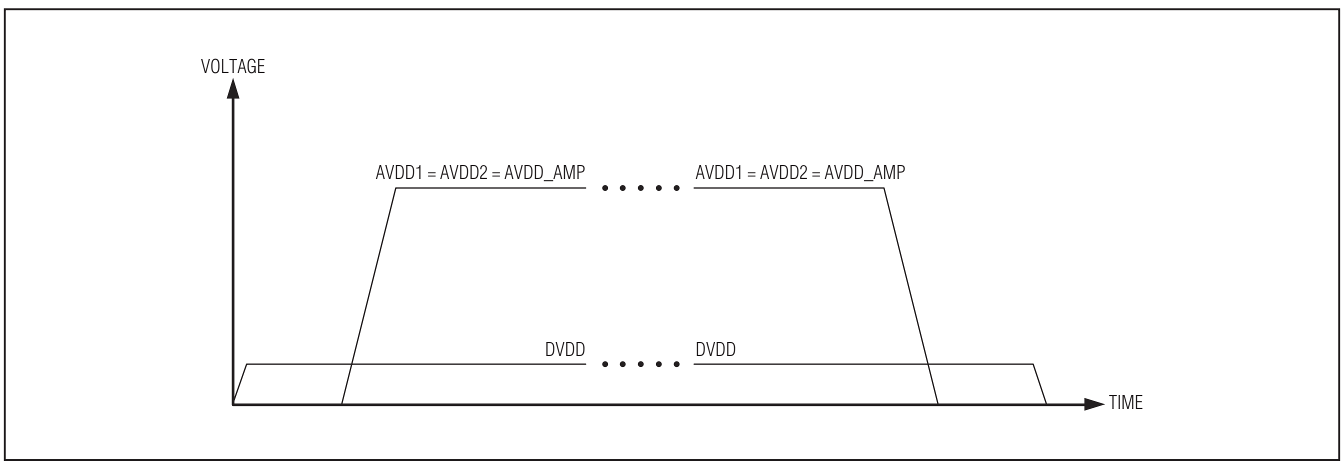


Figure 10. Conventional Power-Up and Power-Down Sequence

12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

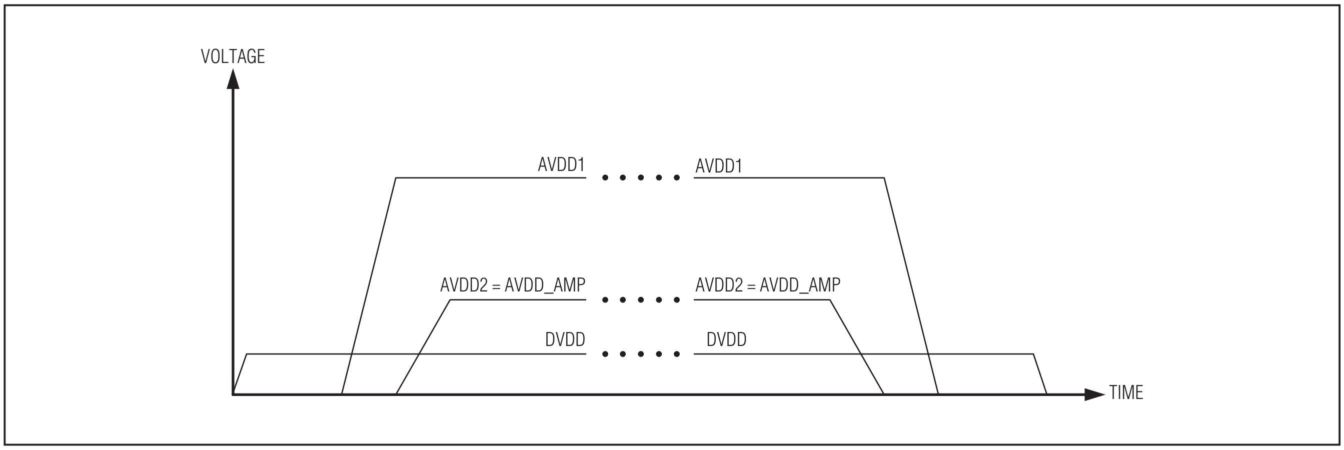


Figure 11. Power-Up and Power-Down Sequence with AVDD2 and AVDD_AMP Connected to Half AVDD

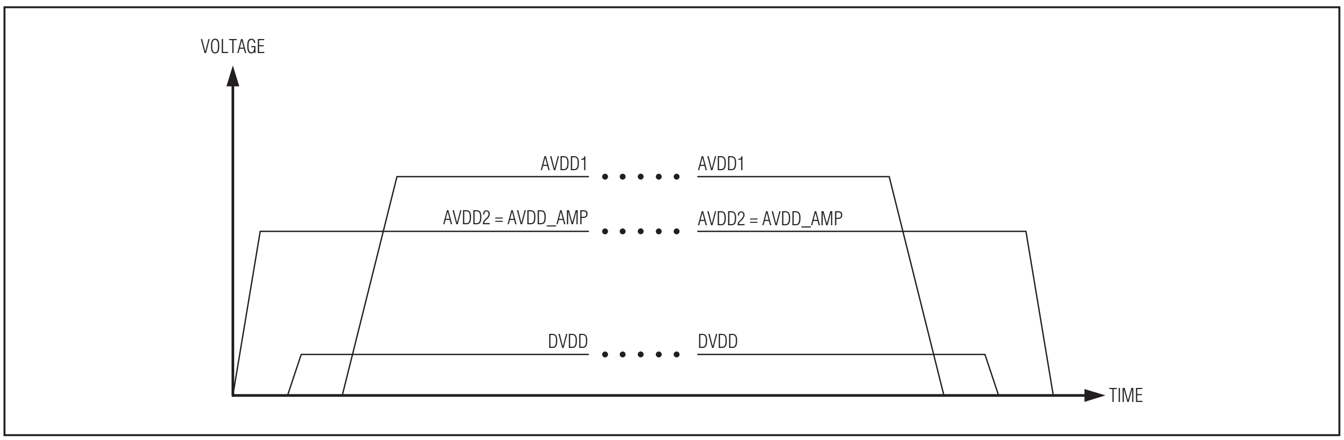


Figure 12. Power-Up and Power-Down Sequence with AVDD2 and AVDD_AMP Connected to 12V

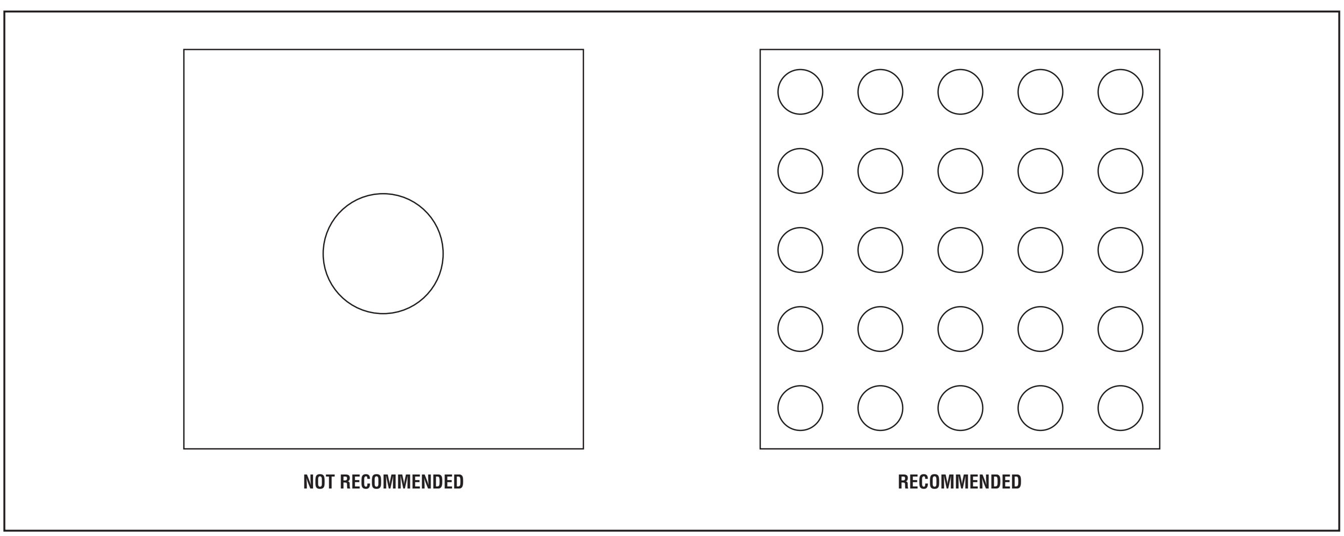
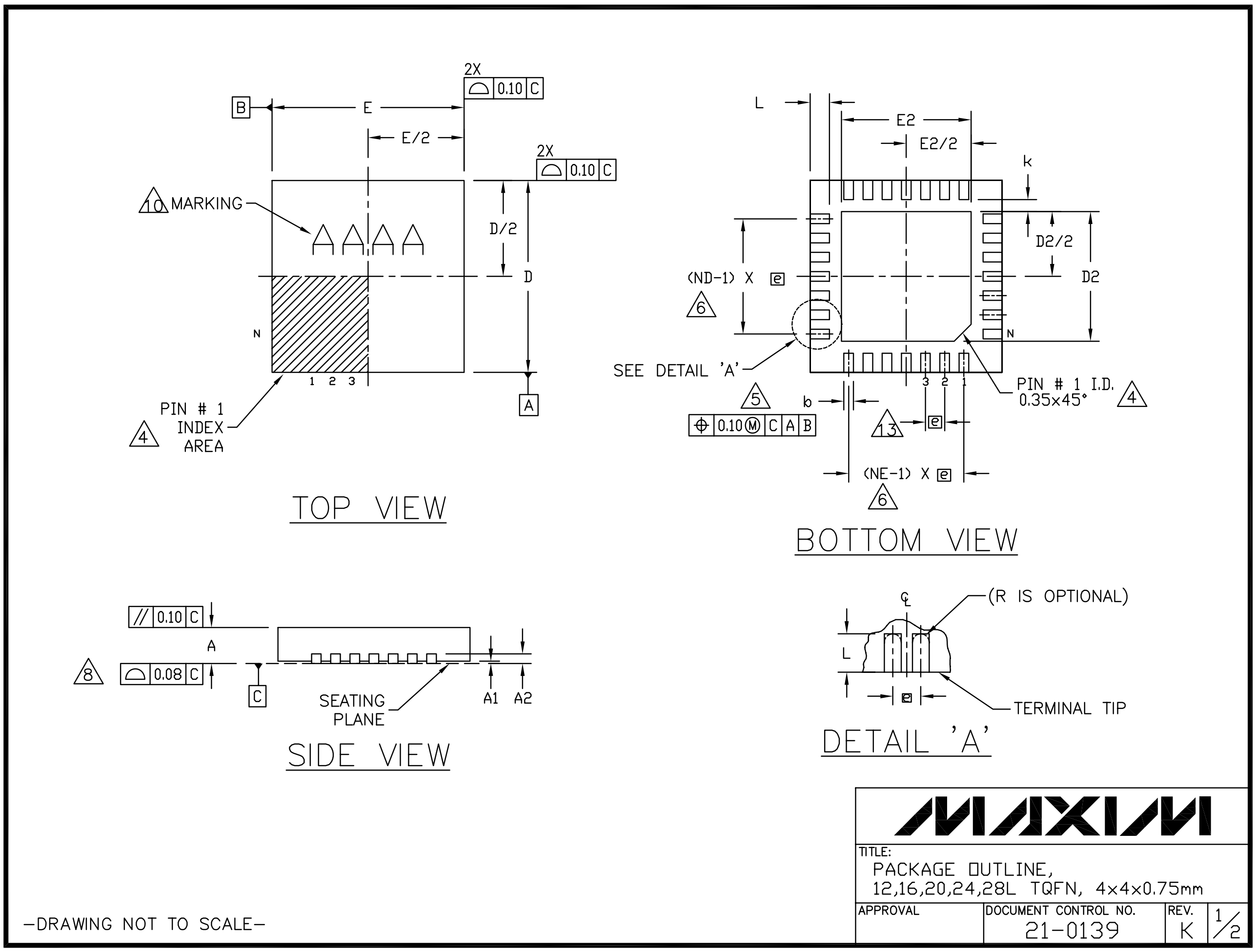


Figure 13. Multiple Small Vias are Recommended over a Single Large Via in the PCB Layout

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN	T2444M+1	21-0139	90-0068



12-Channel, 10-Bit Programmable Gamma and VCOM Reference Voltages

Package Information (continued)

For the latest package outline information and land patterns (footprings), go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75

DIMENSION VARIATIONS

PKG. CODE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 12,16,20,24,28L TQFN, 4x4x0.75mm

APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. K | 2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/11	Initial release	—