FUJITSU

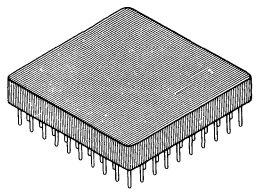
LS-TTL ERROR CHECKING AND CORRECTION CIRCUIT

MB 1412A

May 1981

FUJITSU MB 1412A EIGHT-BIT SLICE ECC LSI

The MB 1412A is an 8-bit slice Error Checking and Correction (ECC) monolithic integrated circuit fabricated in a low-power Schottky TTL process. The device is utilized in memory system designs, and is suitable for constructing 2-byte, 4-byte, or 8-byte ECC circuitry. The MB 1412A will detect and correct single-bit errors, and detect double-bit errors utilizing a built-in modified Hamming single-error-correction, double-error-detection (SEC-DED) code. A 64-pin square package with 100 mil pin spacing is utilized for the MB 1412A to provide high board packing density.



CERAMIC PACKAGE
PGA-64C-M01

- 8-bit slice ECC function in one LSI.
- 100% single-bit error detection/correction and double-bit error detection.
- Simplified circuit design for 2, 4, or 8-byte memory systems. 4/8-byte system requires only 4/8 ECC circuits and 4/8 TTL SSI devices.
- Uses built-in modified Hamming SEC-DED Code.
- 4/8-byte data word requires only 7/8 check bits for full SEC-DED operation.
- High speed: 31/47 nsec. typical for 4/8-byte detect system, 40/56 nsec, for 4/8-byte correct.
- Low-power dissipation: 1.6 watts maximum. For 8-byte system, 8.7 watts typical system power including peripheral circuitry.
- Low-power Schottky TTL process; single +5 volt supply.
- Space-saving 64-pin square-pack with 100 mil pin spacing.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltates to this device.

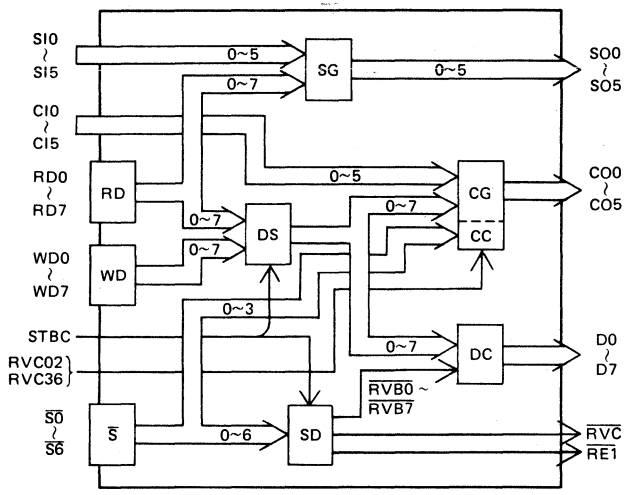
ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	-0.5~+5.5	V
Temperature Under Operation	T_{op}	-25~+85	°C
Temperature Under Storage	T_{stg}	-65~+150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 MB 1412A BLOCK DIAGRAM



RD: Read Data Buffer
SG: Syndrome Generator
WD: Write Data Buffer
DS: Data Selector
CG: Check-bit Generator
CC: Check-bit Corrector
$\overline{S}$: Syndrome Input Buffer
DC: Data Corrector
SD: Syndrome Decoder/Locator

FUNCTIONS OF BLOCK ELEMENTS

RD (Read Data Buffer)
Input buffer gate for memory read data.

SG (Syndrome Generator)
Generates syndrome for the data to be checked in the read data buffer.

WD (Write Data Buffer)
Input buffer gate for memory write data.

DS (Data Selector)
Selects RD or WD depending on the mode ("0" or "1") of the STBC input.

CG (Check-Bit Generator)
Generates check-bits for memory data being checked.

$\overline{S}$ (Syndrome Input Buffer)
Input buffer gate for synthesized syndrome input data.

SD (Syndrome Decoder/Locater)
Locates a data bit for correction and indicates when a one-bit error is detected.

DC (Data Corrector)
Corrects the data bit indicated as an error by the syndrome decoder.

CC (Check-bit Corrector)
Corrects one check-bit by reversing depending on the mode of RVC and $\overline{S}$.

INPUT/OUTPUT PINS

Input Pins:

RD0–RD7 (Read Data)
Memory data inputs. READ data operation is dictated when STBC is "0" (low).

WD0–WD7 (Write Data)
WRITE data inputs. WRITE data operation is dictated when STBC is "1" (high).

SI0–SI5 (Syndrome Input)
Syndrome code inputs to read the synthesized syndrome from the previous ECC LSI (SO output) in a cascaded multi-byte ECC system configuration. The syndrome inputs for the first ECC LSI in the system read memory check-bit data previously generated.

CI0–CI5 (Check-Bit Input)
Reads check-bits into the internal Check-Bit generator in a cascaded ECC system.

STBC (Store Byte Control)
Set "0" (low) to read RD inputs; set "1" (high) to read WD inputs.

$\overline{S0}$–$\overline{S5}$ (Synthesized Syndrome Input)
Reads the synthesized syndrome code output from the last ECC LSI (SO outputs) in a cascaded multi-byte ECC system configuration. $\overline{S0}$–$\overline{S5}$ must correspond to the order of the SO0–SO5 outputs on the same ECC LSI to accomplish syndrome decoding (see ECC system examples). In the event of a single data bit error (during memory READ), the syndrome decoder (SD) decodes $\overline{S0}$–$\overline{S5}$ to locate the error bit to be corrected. The binary location of the error bit is read from $\overline{S0}$–$\overline{S2}$ (e.g., $\overline{S0}$ = 0, $\overline{S1}$ = 1, $\overline{S2}$ = 0 is binary 010 or decimal "2" which corresponds to input data bit "2").

$\overline{S6}$ (Synthesized Syndrome Input #6)
Reads a synthesized syndrome bit output from a cascaded multi-byte ECC system configuration. A "0" input indicates that no bit error is detected within the read memory byte for the ECC IC, and forces the $\overline{RE1}$ and $\overline{RVC}$ outputs high (1). A "1" input indicates that a 1-bit error is detected within the read memory byte.

RVC02 (Reverse Check-Bit #02)
A "0" (low) input indicates no error detected. A "1" (high) indicates an error is detected within the input memory data byte, and corrects the first three check bits (see Fig. 13, C0–C2). A "0" on syndrome data $\overline{S0}$, $\overline{S1}$, or $\overline{S2}$ dictates correction of C0, C1, or C2 respectively.

RVC36 (Reverse Check-Bit #36)
A "0" (low) input indicates no correction to check-bit C3. A "1" (high) input performs correction of check-bit C3.

Output Pins:

SO0–SO5 (Syndrome Output)
Synthesized syndrome output code, normally connected to Syndrome Input (SI) in the next sequential ECC IC in a cascaded multi-byte ECC configuration. Syndromes are effective for the system at the output of the last ECC LSI in sequence.

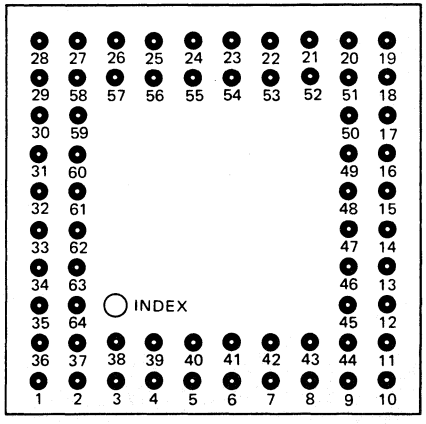
CO0–CO5 (Check-Bit Output)
Check-bit output code, normally connected to Check-Bit Input (CI) in the next sequential ECC LSI in a cascaded multi-byte ECC configuration. Check-bits are effective for the system at the output of the last ECC LSI in sequence.

$\overline{RE1}$ (Read Error One)
A "0" (low) indicates that a one-bit error has occurred in fetched data or check bits.

$\overline{RVC}$ (Reverse Check-Bit)
A "0" (low) indicates that an error in check-bit must be corrected.

D0–D7 (Data Output)
Corrected data output.

Fig. 2 PIN ASSIGNMENT OF PACKAGE



TOP VIEW

Fig. 3 PIN ASSIGNMENT TABLE

PIN NO.	I/O	NAME	PIN NO.	I/O	NAME
1	I	RVC02	33	O	D7
2	O	CO0	34	O	D5
3	I	CI1	35	O	D3
4	I	CI2	36	O	D1
5	O	CO2	37	O	D0
6	I	RVC36	38	I	CI0
7	I	CI3	39	O	CO1
8	I	CI4	40	–	GND
9	I	CI5	41	O	CO3
10	I	WD1	42	O	CO4
11	I	WD3	43	O	CO5
12	I	WD4	44	I	WD0
13	I	WD6	45	I	WD2
14	I	WD7	46	I	WD5
15	I	STBC	47	–	VCC
16	I	RD1	48	I	RD0
17	I	RD3	49	I	RD2
18	I	RD5	50	I	RD4
19	I	RD7	51	I	RD6
20	O	SO0	52	I	SI0
21	I	SI1	53	O	SO1
22	I	SI2	54	–	GND
23	O	SO2	55	I	SI3
24	O	SO3	56	I	SI4
25	O	SO4	57	I	SI5
26	O	SO5	58	I	$\overline{S1}$
27	I	$\overline{S0}$	59	I	$\overline{S3}$
28	I	$\overline{S2}$	60	I	$\overline{S6}$
29	I	$\overline{S4}$	61	–	VCC
30	I	$\overline{S5}$	62	O	D6
31	O	$\overline{RE1}$	63	O	D4
32	O	$\overline{RVC}$	64	O	D2

3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	T_{OP}
Power Supply Voltage	V_{CC}	5.0V ±5%	0°C – 70°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
Output Low Level		V_{OL}			0.5	V	V_{CC}=4.75V, V_{IL}=0.8V V_{IH}=2.0V, I_{OL}=20mA
Output High Level		V_{OH}	2.7			V	V_{CC}=4.75V, V_{IL}=0.8V V_{IH}=2.0V, I_{OH}=1mA
Input Low Current	RDn, WDn, $\overline{Sn}$, RVC02, RVC36	I_{IL1}			1.6	mA	V_{CC}=5.25V, V_{IL}=0.5V
	STBC	I_{IL2}			3.2	mA	
	SIn, CIn	I_{IL3}			4.8	mA	
Input High Current	RDn, WDn, $\overline{Sn}$, RVC02, RVC36	I_{IH1}			20	μA	V_{CC}=5.25V, V_{IH}=2.7V
	STBC	I_{IH2}			40	μA	
	SIn, CIn	I_{IH3}			60	μA	
Input High Current		I_{IH}			1	mA	V_{CC}=5.25V, V_{IH}=5.5V
Output Short Current		I_{OS}	30		120	mA	V_{CC}=5.25V, V_O=0.5V
Power Supply Current		I_{CC}		190	300	mA	V_{CC}=5.25V
Input Clamp Voltage		V_{IC}			1.2	V	V_{CC}=4.75V, I_{IL}=18mA

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
(RD1 ~ RD7) to (SO0 ~ SO2) *	t_{pd1}		14	19	ns
(RD0 ~ RD7) to SO3, SO4	t_{pd2}			25	ns
RD0 to SO5	t_{pd4}			17	ns
(RD0 ~ RD7) to (CO0 ~ CO5)	t_{pd3}			36	ns
(RD0 ~ RD7) to (D0 ~ D7)	t_{pd4}			18	ns
(SI0 ~ SI5) to (SO0 ~ SO5) *	t_{pd5}		4	9	ns
(CI0 ~CI5) to (CO0 ~ CO5) *	t_{pd6}		4	9	ns
(WD0 ~ WD7) to (CO0 ~ CO5) *	t_{pd7}		25	36	ns
(WD0 ~ WD7) to (D0 ~ D7)	t_{pd8}			18	ns
($\overline{S0}$ ~ $\overline{S6}$) to (CO0 ~ CO5)	t_{pd9}			22	ns
($\overline{S0}$ ~ $\overline{S6}$) to (D0 ~ D7) *	t_{pd10}		14	19	ns
($\overline{S0}$ ~ $\overline{S6}$) to $\overline{RE1}$	t_{pd11}			22	ns
($\overline{S0}$ ~ $\overline{S6}$) to $\overline{RVC}$	t_{pd12}			21	ns
RVC02 to (CO0 ~ CO3)	t_{pd13}			18	ns
RVC36 to (CO0 ~ CO3)	t_{pd14}			17	ns
STBC to (CO0 ~ CO5)	t_{pd15}			36	ns
STBC to (D0 ~ D7)	t_{pd16}			22	ns
STBC to $\overline{RVC}$	t_{pd17}			18	ns

* Note: Critical path on a chip

Fig. 4 DELAY TIME MEASUREMENT CIRCUIT

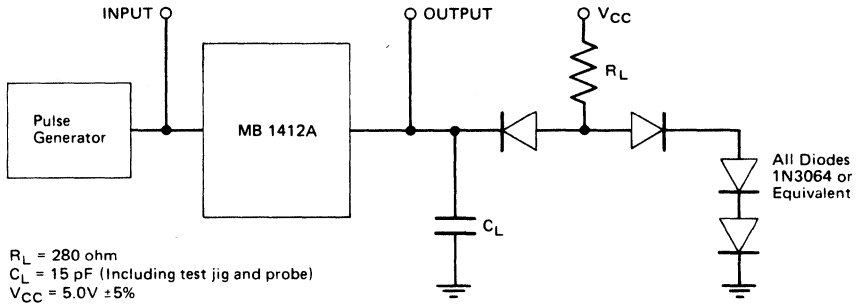
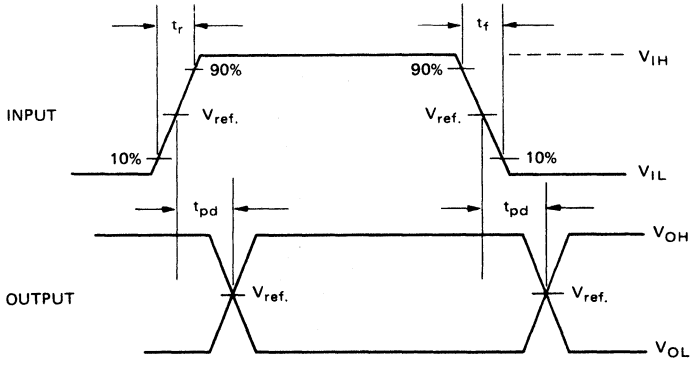


Fig. 5 INPUT SIGNAL/OUTPUT SIGNAL TIMING



CRITICAL PATH TIMING

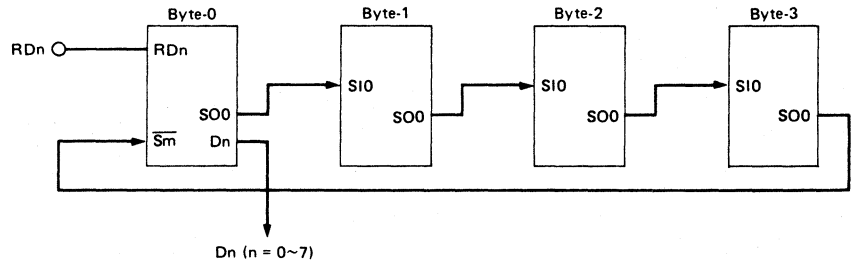
Critical timing paths for the MB 1412A are shown under AC Characteristics as indicated by the notation "Critical Path on Chip". In a typical, multi-chip ECC system application, system delay time would be measured from the RD input to the D output for processing of the complete data input. The equation is as follows, where ℓ is the number of bytes in the data input:

$$t_{pd}\,(RDn - Dn) = t_{pd}\,(RDn - SO0) + (\ell - 1) \times t_{pd}\,(SI0 - SO0) + t_{pd}\,(\overline{Sm} - Dn)$$

For a 4-byte system (see Figure 6), delay time from READ data (RD) to corrected data (D) is 40 nsec typical:

$t_{pd}\,(RD - D)_4$ = 14ns + (3 x 4 ns) + 14 ns = 40 nsec.

Fig. 6 CRITICAL PATH TIMING (Data Correction)



THEORY AND APPLICATION OF ECC

In most any data processing system, binary bit errors are going to occur when blocks of data are moved from one location to another. As such errors are not uncommon and can lead to entirely bogus or meaningless results in routine programs, it has become requisite design discipline to include ECC (Error Checking and Correction) Circuitry in main memory control logic. The MB 1412A accomplishes this in a highly integrated form which allows ECC implementation with a minimal package count.

The MB 1412A will correct one-bit errors in every input data word, and flag the occurence of two-bit errors. One-bit error correction is considered adequate, as the probability of more than a one-bit error is quite low. As an example, consider a data word of 5-bits with the error possibility of .0001 (one in ten-thousand) per bit. The chances of an error occuring in a data word are:

no error $P_0 = (1 - P)^5 = 0.9995$

one error $P_1 = {}_5C_1 \cdot P\,(1 - P)^4 = 0.0005$

two errors $P_2 = {}_5C_2 \cdot P^2\,(1 - P)^3 = 0.00000025$

Thus, one-bit detection and correction and two-bit detection only should provide adequate insurance, and satisfactory system performance. When a two-bit error occurs, of course, the program must be interrupted to prevent miscalculation.

In order to detect data bit errors, memory check-bits must be stored with the data words. For 1-bit error detection of a word of n-bits, assume the number of check-bits required is C_n. The number of possible bit combinations for no error is therefore 1 (all bits, both data bits and check-bits correct); and the number of possible bit combinations for a 1-bit error is: $n + C_n$.

The number of combinations made by check-bits is 2^{C_n}. To detect 1-bit errors a hundred percent, the following must be satisfied:

$1 + (n + C_n) \leqslant 2^{C_n}$.

This means, for example, that a 1-bit error in 16-bits of data can be detected by five additional check-bits. Following the same calculation, 1-bit errors in 32-bit data words require 6 check-bits, and 64-bit data words require 7 check bits. To detect 2-bit errors, one additional bit is required; e.g., 6 check-bits for a 16-bit word.

The MB 1412A is designed for use in a memory system configuration of either 2-bytes (16 data bits), 4-bytes (32 data bits), or 8-bytes (64 data bits). Simple external gating, as shown in Figures 7 and 8, is required in the error indication and reverse check-bit circuitry.

When data is first written into memory, the ECC system does not correct or detect errors. But it does generate the necessary check-bits (as a function of the number of bytes of data in the memory system configuration) which are stored in memory along with the data bits. The check-bit code conforms to the ECC system output of the modified Hamming code check-bit generator as shown in Figure 9. The check-bit generator takes the parity of all the data bits marked by an X in the rows of the input data bits.

When memory is read, both data bits and check-bits form inputs into the ECC system. Data bits are entered in parallel, one byte per ECC IC in the ECC system. The check-bits are entered into the first ECC IC in the chain, and additional ECC IC's as shown in the example in Figure 15.

These fetched check-bits are exclusive-ORed with newly generated check-bits created from the data input in order to generate a syndrome code for the fetched data as shown in Figure 9. From the syndrome code, the ECC system can determine if there is an error in the input data bits, as follows:

- If the syndrome code is all "0", there is no error.
- If one syndrome bit is "1", the corresponding check-bit is in error. As a result, $\overline{RE1}$ will go to "0" and $\overline{RVC}$ will go to "1" so that no correction will be made in the data bits.
- If more than one syndrome bit is "1", and the parity of all syndrome bits is even, a multiple error has occurred. No correction is made, and the program should be interrupted.
- If more than one syndrome bit is "1", and the parity of all syndrome bits is odd, a single error has occurred in the data bits. The binary location of the error in the input data bits can be determined by decoding of the syndrome code as shown in Figure 10.

In the event of multiple errors, no data correction is made; rather the event is flagged and system software should be interrupted. As a two-bit error without ECC would normally result in program execution errors, program interruption is presumed to be the only satisfactory outcome of the multiple error detection event.

When one error is detected in the fetched check-bits, the ECC system, in effect, generates a new set of check-bits (and "ignores" the fetched check-bits) with respect to processing the input data bits.

WRITE Mode:

A "1" input on STBC initiates the WRITE mode operation and tells the Data Selector (DS) to read data from the Write Data (WD) buffer (WD0—WD7 inputs). The $\overline{RVC}$ (Reverse Check Bit) and $\overline{RE1}$ (Read Error One) outputs of the Syndrome Decoder/Locator (SD) go high so that no error indication for the data is possible. Further, the function of the Check-bit Corrector (CC) is inhibited by feedback of the $\overline{RVC}$ signal (high state) to the RVC02 and RVC36 inputs. Data correction can not occur because the $\overline{RVC}$ output is high.

The Check-bit Generator (CG) will generate check-bit data from the WRITE data transferred from the Data Selector (DS) and output it on CO0—CO5 in accordance with the logic table shown in Figure 9. At the same time, the Data Corrector (DC) will transfer the WRITE data onto outputs D0—D7. Thus the WRITE data on D0—D7 can be stored in main memory along with the appropriate output check-bits corresponding to the data bits input into the ECC system.

READ Mode:
A "0" input on STBC indicates the READ mode operation and tells the Data Selector (DS) to transfer read data from inputs RD0–RD7 through the Read Data (RD) buffer to the Data Corrector (DC) and Check-bit Generator (CG). The Syndrome Generator (SG) will generate check-bits from the same data inputs and XOR (exclusive-OR) them with the data on SI0–SI5 (Syndrome Inputs). XORed data becomes the output on SO0–SO5 (Syndrome Output) according to the logic table shown in Figure 9. At the same time, the Check-bit Generator (CG) will generate check-bits from the input read data and will accept check-bit correction if the data from memory contains an error. Note that by performing syndrome generation and check-bit correction simultaneously, high speed operation is maintained.
A "0" on STBC also gates the Syndrome Decoder/Locator (SD) to decode syndrome inputs on $\overline{S0}$–$\overline{S6}$. When syndrome data is not all "0", both $\overline{RVC}$ (Reverse Check-Bit) and $\overline{RE1}$ (Read Error-One) go "0" (low) to indicate error detection. Logic tables are shown in Figure 10. The error bit position is indicated to the Data Corrector (DC), and the data output at D0–D7 is corrected.
$\overline{RVC}$ is fedback to the RVC02 and RVC36 inputs. So when an error is detected ($\overline{RVC}$ = low), the input syndrome data from the Syndrome Buffer ($\overline{S}$) is gated into the Check-bit Corrector (CC). The check-bits are corrected in accordance with the logic table shown in Figure 9.

Fig. 7 ERROR INDICATION CIRCUIT

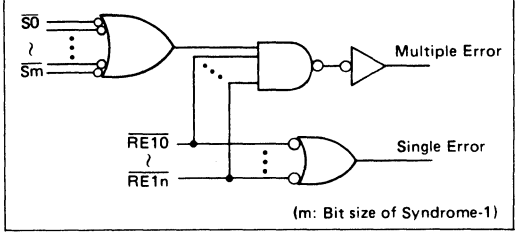


Fig. 8 REVERSE CHECK-BIT CIRCUIT

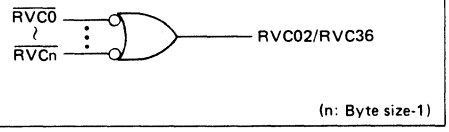


Fig. 9 LOGICAL DESCRIPTION OF SYNDROME GENERATION/DECODING AND CHECK-BIT GENERATION

Table 1 Syndrome Generation (See Note *)

SI						RD								XOR TREE	OUTPUT
0	1	2	3	4	5	0	1	2	3	4	5	6	7		
X							X		X		X		X	EVEN	SO0
	X							X	X			X	X	EVEN	SO1
		X								X	X	X	X	EVEN	SO2
			X			X	X	X	X	X	X	X	X	ODD	SO3
				X		X	X	X		X			X	ODD	SO4
					X	X								ODD	SO5

Table 2 Check-Bit Generation (See Note *)

CI						RD (STBC=0)/WD (STBC=1)								XOR TREE	MODIFICATION **	OUT-PUT
0	1	2	3	4	5	0	1	2	3	4	5	6	7			
X							X		X		X		X	ODD	⊕ RVC02·S0	CO0
	X							X	X			X	X	ODD	⊕ RVC02·S1	CO1
		X								X	X	X	X	ODD	⊕ RVC02·S2	CO2
			X			X	X	X	X	X	X	X	X	EVEN	⊕ RVC36·S3	CO3
				X		X	X	X		X			X	EVEN		CO4
					X	X								EVEN		CO5

Note:
* Inputs marked "X" are gated to the XOR-TREE.
** ⊕ indicates XOR.

Fig. 10 SYNDROME DECODING

For data

S							Error Indication / Error Location
0	1	2	3	4	5	6	
0	0	0	1	1	1	0	Data Bit 0
1	0	0	1	1	0	0	Data Bit 1
0	1	0	1	1	0	0	Data Bit 2
1	1	0	1	0	0	0	Data Bit 3
0	0	1	1	1	0	0	Data Bit 4
1	0	1	1	0	0	0	Data Bit 5
0	1	1	1	0	0	0	Data Bit 6
1	1	1	1	1	0	0	Data Bit 7

For check-bit

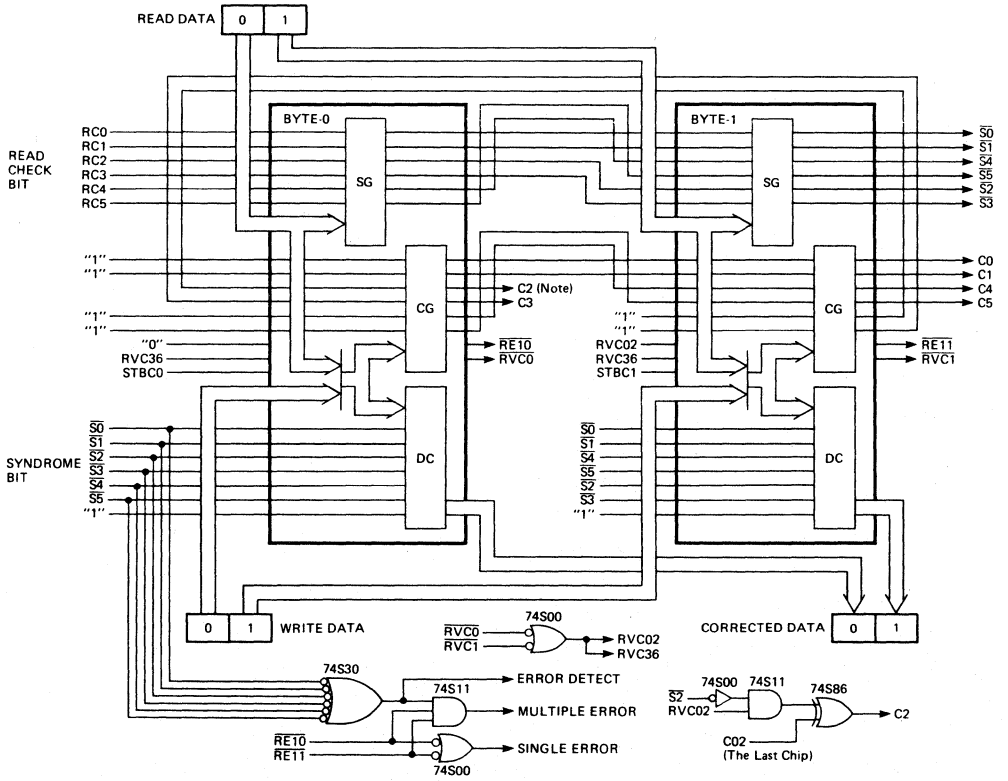
S							Error Indication / Error Location
0	1	2	3	4	5	6	
1	0	0	0	0	0	0	Check-Bit 0
0	1	0	0	0	0	0	Check-Bit 1
0	0	1	0	0	0	0	Check-Bit 2
0	0	0	1	0	0	0	Check Bit 3

EXAMPLE OF A 2-BYTE SYSTEM

Figure 11 is a block diagram of a 2-byte ECC system configuration, including the external gate requirements. Two MB 1412As are connected so that the bits indicated by an X in the Hamming code shown in Figure 12 are exclusive-ORed in the Check-Bit Generator. In the example, the 16-bit input data word is 00011100 01011101, and the check-bits generated in WRITE mode are 101000.

In the READ mode shown in Figure 13, we assume that bit 10 has been inverted (error). The data bits are gated to the exclusive-OR tree to regenerate check-bits (now 110001) which are exclusive-ORed with the original check-bits (101000). The syndrome bits (011001) are then decoded as shown which indicates an error on bit 10 of the input data. This is corrected by inverting (change "1" to "0").

Fig. 11 TWO-BYTE ERROR CHECKING AND CORRECTION SYSTEM



Note: When ECC system is used in "Partial Write Mode", C2 must be connected to the C02 input of the external reverse check bit circuit.

Fig. 12 WRITE OPERATION IN 2-BYTE ECC SYSTEM

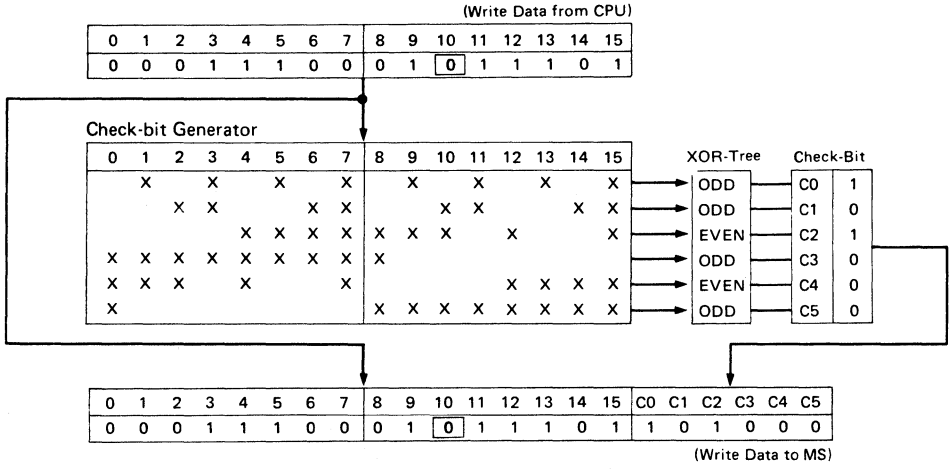
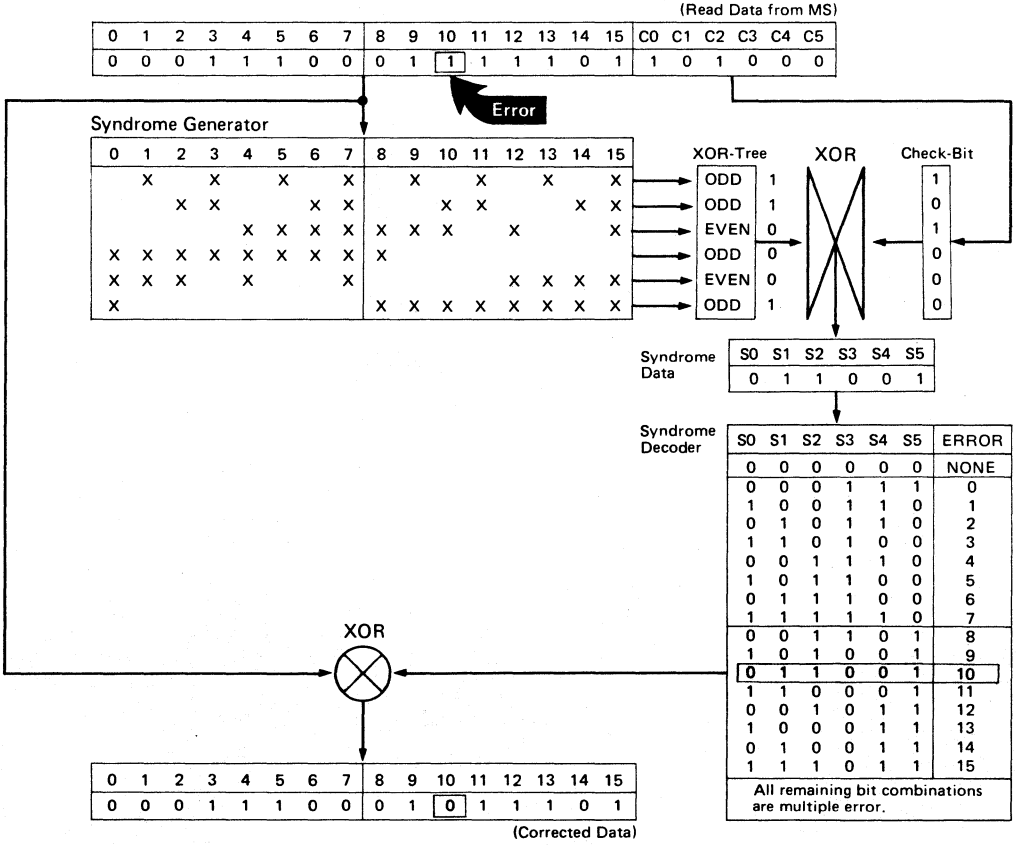


Fig. 13 READ OPERATION IN 2-BYTE ECC SYSTEM



3

EXAMPLE OF A 4-BYTE SYSTEM

In a 4-Byte ECC system, four MB 1412A LSIs are connected in a cascaded manner as shown in Figure 14. The Hamming code depicted in Figure 15 is realized from the interconnection of the LSIs as shown. Data bits marked with an X in Figure 15 are gated to an exclusive-OR tree to generate check-bits. The WRITE mode is diagrammed in Figure 16, and READ mode is shown in Figure 17. Figure 18 diagrams a Partial WRITE operation on the 1st and 2nd bytes, with READ mode on the 3rd and 4th.

Fig. 14 FOUR-BYTE ERROR CHECKING AND CORRECTION SYSTEM

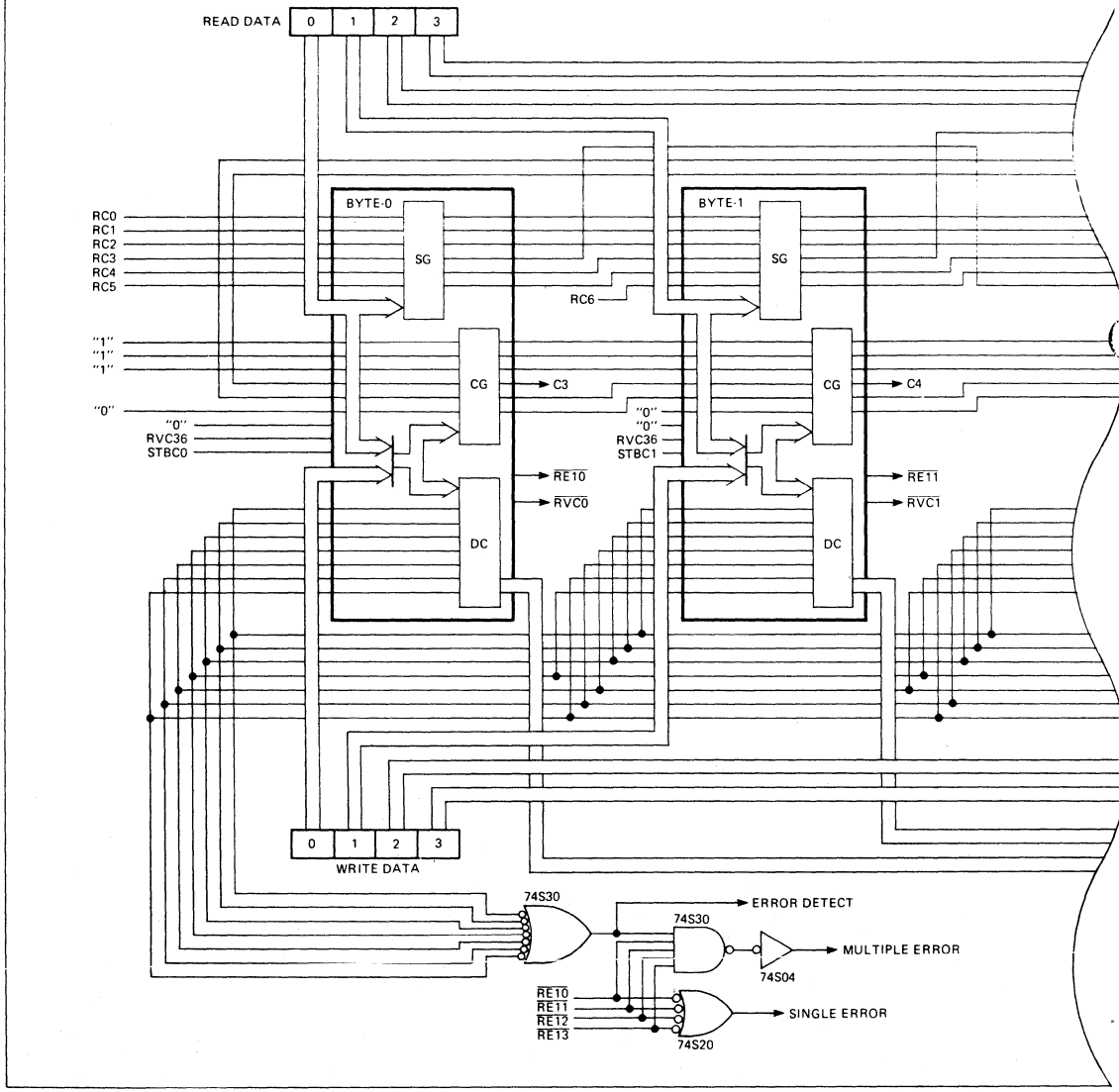
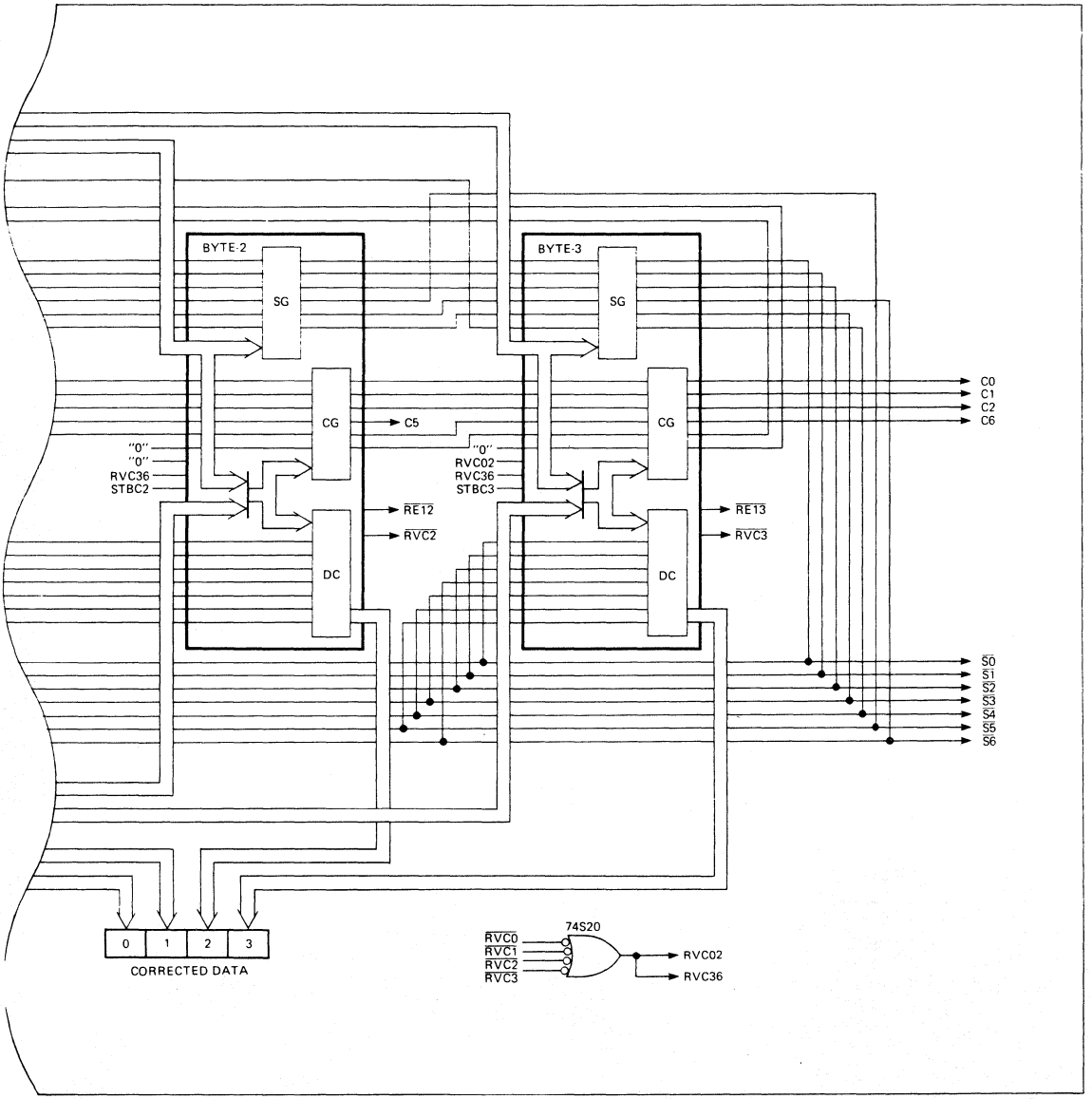


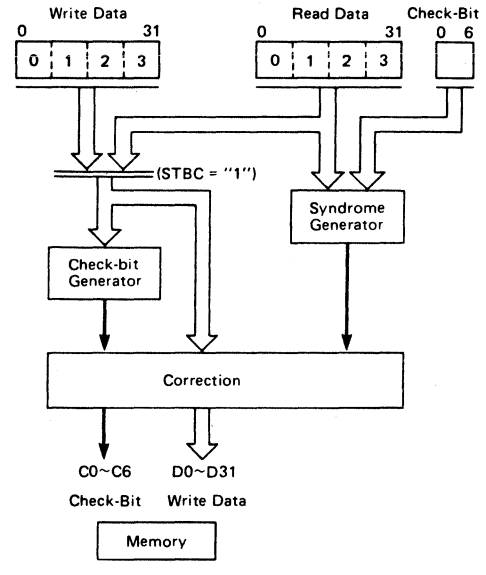
Fig. 15 FOUR-BYTE ECC CODE TABLE

Data Bits																												XOR-Tree	Check-Bit
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X	ODD	C0
		X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X	ODD	C1
				X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X	ODD	C2
X	X	X	X	X	X	X	X									X								X	X	X		X			X	EVEN	C3
X	X	X		X			X	X	X	X	X	X	X	X	X									X								EVEN	C4
X								X	X	X		X			X	X	X	X	X	X	X	X	X									EVEN	C5
								X								X	X	X		X			X	X	X	X	X	X	X	X	X	EVEN	C6



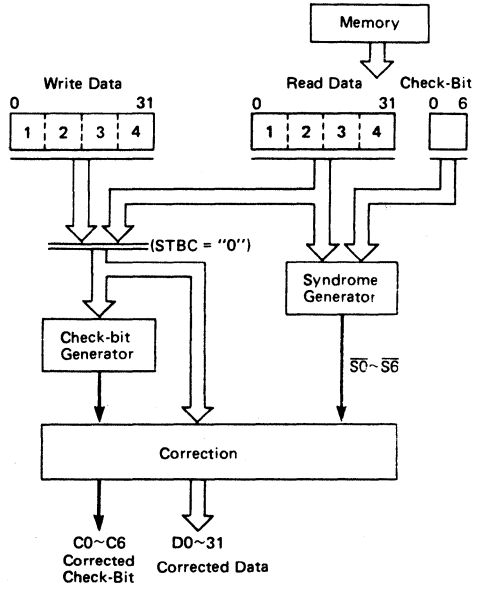
3

Fig. 16 WRITE OPERATION (4-BYTE)



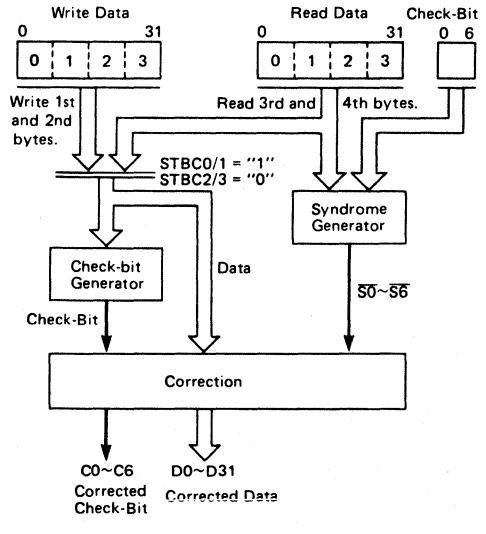
No correction is done on any byte data.

Fig. 17 READ OPERATION (4-BYTE)



One bit error in Read Data can be corrected.

Fig. 18 PARTIAL WRITE OPERATION (4-BYTE)



1. When one bit error is detected on 3rd and 4th byte data, Data and Check-bit can be corrected. (READ Data)
2. No correction is done on 1st and 2nd byte Data. (WRITE Data)
3. One bit error on check-bit need not be corrected.

EXAMPLE OF AN 8-BYTE SYSTEM

In a 8-Byte ECC system, eight MB 1412A LSIs are connected in a cascaded manner as shown in Figure 20. The Hamming code depicted in Figure 19 is realized from the interconnection of the LSIs as shown. Data bits marked with an X in Figure 19 are gated to an exclusive-OR tree to generate check-bits.

Fig. 19 EIGHT-BYTE ECC CODE TABLE

Byte-0								Byte-1								Byte-2							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	X		X		X		X		X		X		X		X		X		X		X		X
		X	X			X	X			X	X			X	X			X	X			X	X
				X	X	X	X					X	X	X	X					X	X	X	X
X	X	X	X	X	X	X	X									X							
X	X	X		X			X	X	X	X	X	X	X	X	X								
X								X	X	X		X			X	X	X	X	X	X	X	X	X
								X								X	X	X		X			X

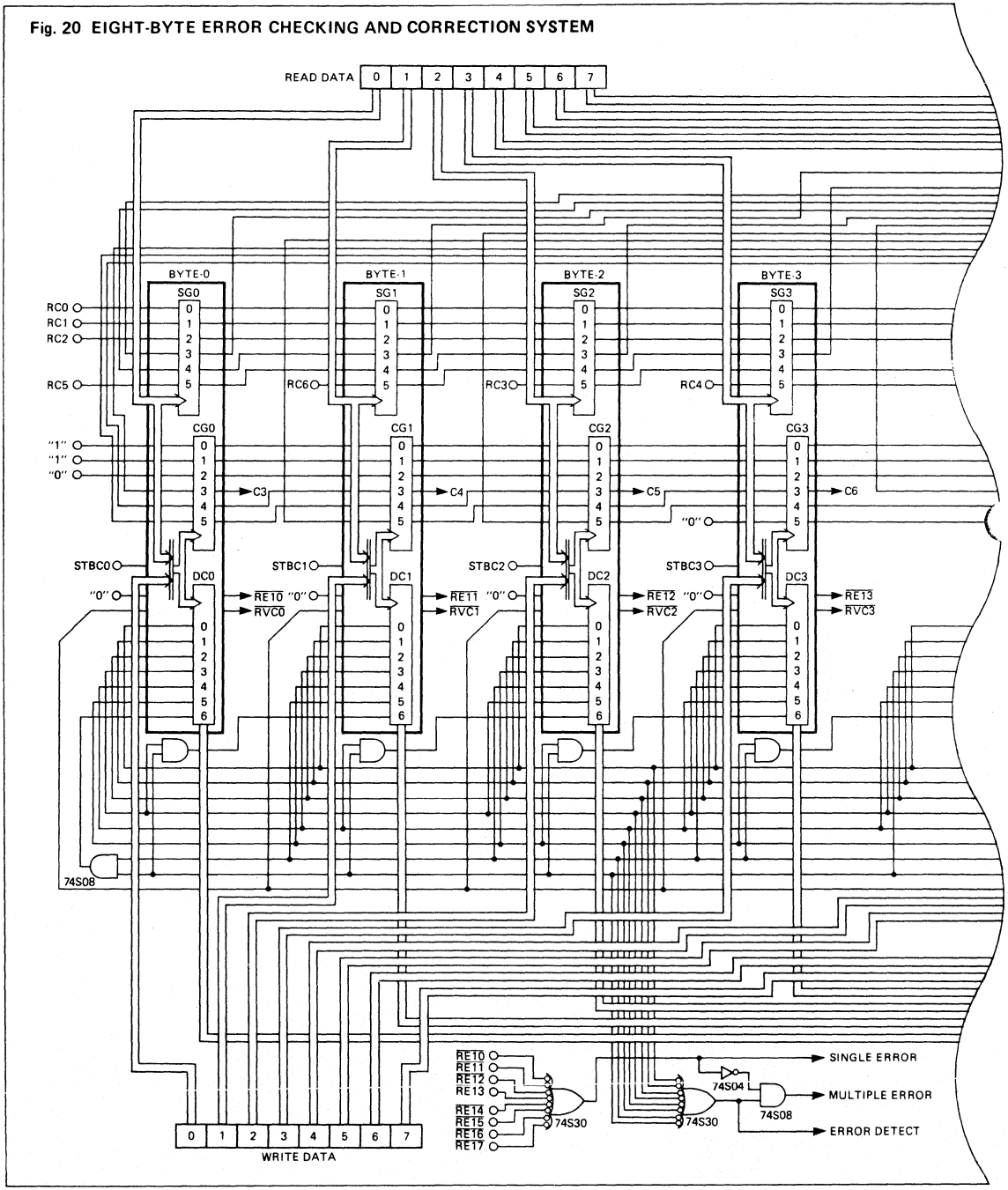
Byte-3								Byte-4								Byte-5							
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
	X		X		X		X		X		X		X		X		X		X		X		X
		X	X			X	X			X	X			X	X	X							
				X	X	X	X					X	X	X	X								
X	X	X		X			X	X	X	X		X			X								
X								X										X	X			X	X
																X	X	X		X			X
X	X	X	X	X	X	X	X													X	X	X	X
								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

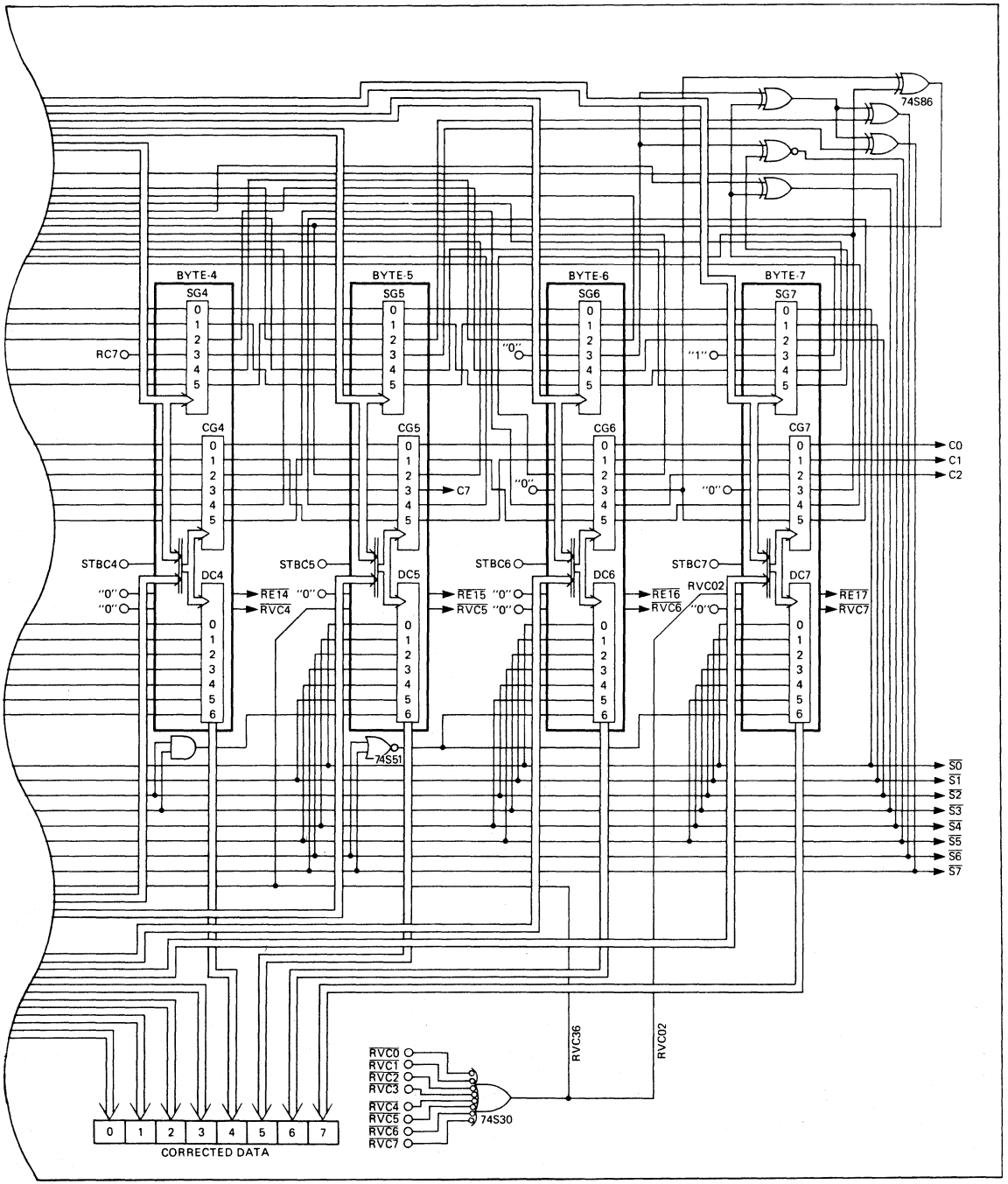
Byte-6								Byte-7							
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
	X		X		X		X		X		X		X		X
		X	X			X	X			X	X			X	X
X	X	X		X			X					X	X	X	X
				X	X	X	X	X	X	X	X	X	X	X	X
X								X	X	X		X			X
X	X	X	X	X	X	X	X	X							
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

XOR-Tree	Check-Bit
ODD	C0
EVEN	C1
EVEN	C2
ODD	C3
ODD	C4
EVEN	C5
ODD	C6
EVEN	C7

3

Fig. 20 EIGHT-BYTE ERROR CHECKING AND CORRECTION SYSTEM

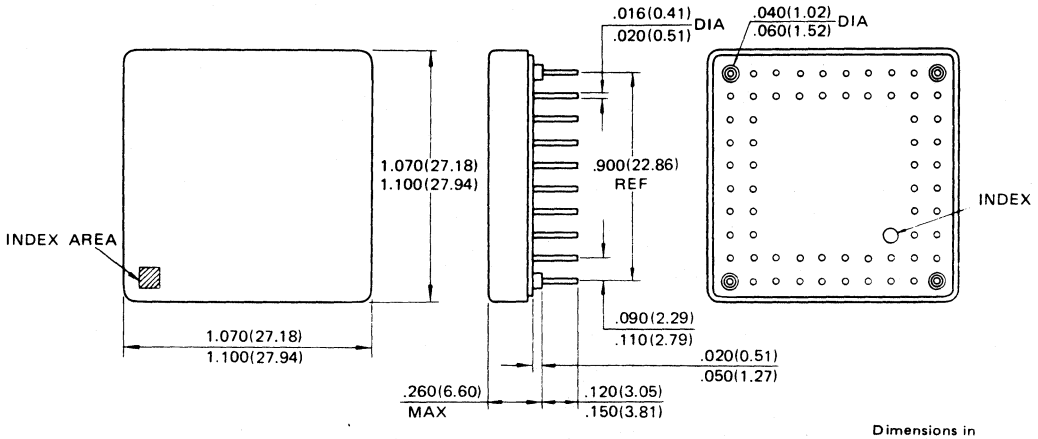



74S86
BYTE-4
BYTE-5
BYTE-6
BYTE-7
SG4
SG5
SG6
SG7
RC7
"0"
"1"
CG4
CG5
CG6
CG7
C0
C1
C2
C7
STBC4
STBC5
STBC6
STBC7
DC4
DC5
DC6
DC7
RE14
RVC4
RE15
RVC5
RE16
RVC6
RVC02
RE17
RVC7
74S51
S0
S1
S2
S3
S4
S5
S6
S7
RVC0
RVC1
RVC2
RVC3
RVC4
RVC5
RVC6
RVC7
74S30
RVC36
RVC02
0 1 2 3 4 5 6 7
CORRECTED DATA

3

PACKAGE DIMENSIONS

64-LEAD CERAMIC (RESIN SEAL WITH METAL CAP) REPEATED QUAD IN-LINE PACKAGE
(CASE No.: PGA-64C-M01)



Dimensions in inches (millimeters)