FUJITSU

DYNAMIC RAM CONTROLLER LSI

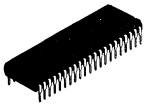
MB 1422A

June 1986
Edition 1.0

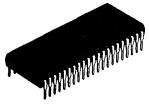
DYNAMIC RAM CONTROLLER

The Fujitsu MB 1422A is a high performance DRAM controller LSI.
The MB 1422A controls address multiplexing, refresh timing and their arbitration, and realizes one chip DRAM peripheral controller.
The MB 1422A is designed to easily interface 64K and 256K DRAM to the system based on the 8086 or 68000.
The MB 1422A is fabricated in an advanced low-power Schottky TTL process.
The device is housed in a plastic 42-pin Dual In-line-Package, 42 pin shrink DIP, and 44-pin PLCC.

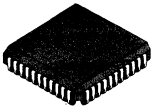
- 256k and 64k Dynamic-RAM control capability
- Directly addresses and drives up to 44 DRAMs without external drivers
- Internal/external refresh capability
- Supports 8086 (5MHz or 8MHz) or 68000 (8MHz or 12.5MHz) type microprocessor
- +5V only schottky TTL technology for high performance
- Low power dissipation: 440mW Typ.
- TTL compatible I/O
- Standard 42 pin Plastic DIP (Suffix: -P)
- Standard 42 pin Plastic Shrink DIP (Suffix: -P)
- Standard 44 pin Plastic LCC (Suffix: -PD)



PLASTIC PACKAGE
DIP-42P-M01

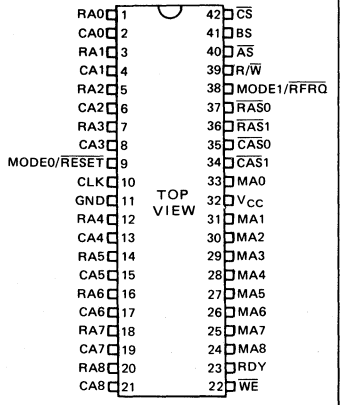


PLASTIC PACKAGE
DIP-42P-M02



PLASTIC PACKAGE
LCC-44P-M01

PIN ASSIGNMENT



PLCC PIN ASSIGNMENT: See Page 21

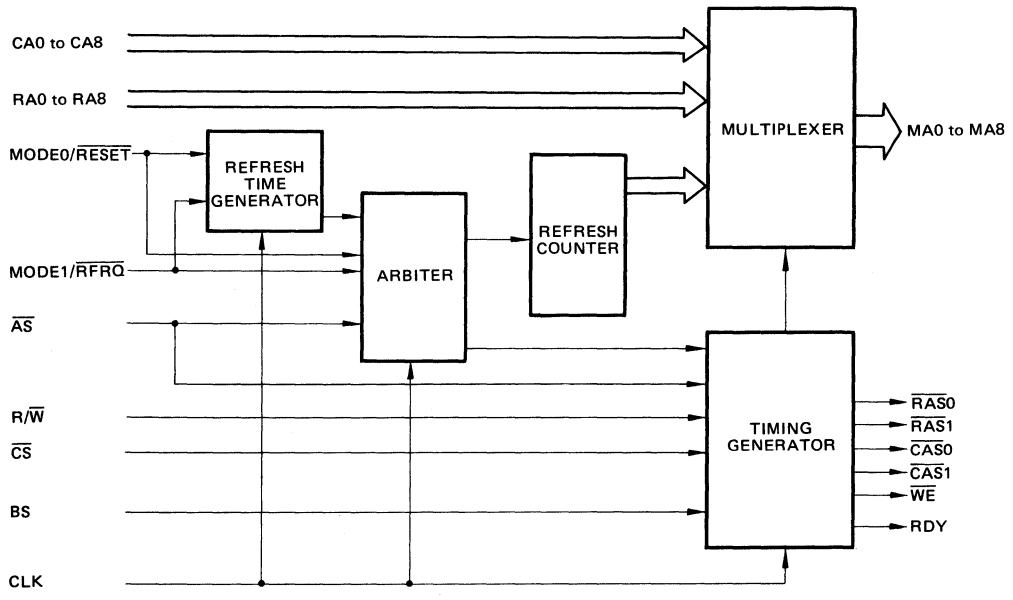
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Powery Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Operating Temperature	T_{OP}	−25 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 1422A BLOCK DIAGRAM



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BLOCK FUNCTIONS

Multiplexer: Multiplexes the CPU addresses (CA and RA) and refresh address to nine row and nine column address.
Timing Generator: Generates $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals by address strobe (AS) and R/$\overline{W}$ signals from CPU and refresh request signal from the arbiter. Sends select signals for row, column or refresh address to multiplexer.
Refresh Counter: Generates the refresh address and counts up at each cycle.
Refresh Time Generator: Generates an internal refresh request signal.
Arbiter: Resolves the conflict of read/write and refresh cycle.

Table 1 – PIN DESCRIPTION

Symbol	Pin		Type	Pin Name and Function
	DIP	PLCC		
MODE0/ $\overline{\text{RESET}}$	9	10	I	**Internal/External Refresh Select;** This pin is used to select refresh mode, internal refresh or external refresh. If MODE0/$\overline{\text{RESET}}$ = "H", internal refresh mode is selected. If MODE0/$\overline{\text{RESET}}$ = "L", external refresh mode. The falling edge of MODE0/$\overline{\text{RESET}}$ resets the refresh address counter.
MODE1/ $\overline{\text{RFRQ}}$	38	40	I	**Internal Interval Select/External Refresh Request;** When Internal Refresh mode is selected (MODE0/$\overline{\text{RESET}}$ = "H"), this pin is used as refresh interval selection. If CLK $\geqq$ 15MHz, it must be "L", and if CLK –24 to 25MHz, it must be "H". When External Refresh mode is selected (MODE0/$\overline{\text{RESET}}$ = "L"), this pin is used as refresh request. And the refresh starts when MODE1/$\overline{\text{RERQ}}$ = "L" is strobed by the falling edge of CLK.
$\overline{\text{AS}}$	40	42	I	**Address Strobe;** Memory access starts when $\overline{\text{AS}}$ = "L" is strobed by the falling edge of CLK, and ends at the rising edge of $\overline{\text{AS}}$, that is, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ become "H" (inactive) when $\overline{\text{AS}}$ turns "H" except refresh mode. The $\overline{\text{AS}}$ must be kept "L" until $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths have been satisfied for $\overline{\text{DRAM}}$ specifications.
R/$\overline{\text{W}}$	39	41	I	**Read/Write Control;** This pin is used to select memory read or write mode. If R/$\overline{\text{W}}$ = "H", read mode is selected. If R/$\overline{\text{W}}$ = "L", write mode.
$\overline{\text{CS}}$	42	44	I	**Chip Select;** This pin is used to control the states of output pins except for RDY. When $\overline{\text{CS}}$ = "H", $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and MA (MA0 to MA8) become high impedance state.
BS	41	43	I	**Bank Select;** This pin is used to select either of the two banks of DRAM arrays. If BS = "L", the lower bank ($\overline{\text{RAS}}$0) is selected. If BS = "H", the upper bank ($\overline{\text{RAS}}$1) is selected.
CLK	10	11	I	**Clock input;** This input provides basic timing for the internal logic. 8086 (5MHz) → CLK = 15MHz 8086 (8MHz) → CLK = 24MHz 68000 (8MHz) → CLK = 16MHz 68000 (12.5MHz) → CLK = 25MHz The CLK frequency should be higher or equals to 15MHz.
RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8	1 3 5 7 12 14 16 18 20	2 4 6 8 13 15 17 19 21	I	**Row Address;** These inputs are used to generate memory row address.

I: Input, O*: 3-State output

Table 2 – PIN DESCRIPTION (Continuted)

Symbol	Pin DIP	Pin PLCC	Type	Pin Name and Function
CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8	2 4 6 8 13 15 17 19 21	3 5 7 9 14 16 18 20 22	I	**Column Address;** These inputs are used to generate memory column address.
$\overline{RAS0}$ $\overline{RAS1}$	37 36	39 38	O*	**Row Address Strobe;** These outputs are used by DRAM to strobe Row Address present on MA0 to MA8. Either $\overline{RAS0}$ or $\overline{RAS1}$ is selected by BS. The selected $\overline{RAS}$ is issued after $\overline{AS}$ = "L" is strobed by the falling edge of CLK. In the refresh mode (both Internal and External), both $\overline{RAS0}$ and $\overline{RAS1}$ are issued. These outputs become high impedance state if $\overline{CS}$ = "H". Each output drives maximum 22 DRAMs directly without external driver.
$\overline{CAS0}$ $\overline{CAS1}$	35 34	37 36	O*	**Column Address Strobe;** These outputs are used by DRAM to strobe column address, present on MA0 to MA8. These outputs are issued from the CLK rising edge, which is 1.5 CLK cycles after $\overline{AS}$ = "L" is strobed, with delay time of t_{CASN}. (See Fig. 4 and 5.) These outputs are not controlled by BS, i.e., both $\overline{CAS0}$ and $\overline{CAS1}$ are issued every memory access. In the refresh mode (both Internal and External), these outputs are kept "H". These outputs become high impedance state if $\overline{CS}$ = "H". Each output drives maximum 22 DRAMs directly without external driver.
$\overline{WE}$	22	24	O*	**Write Enable;** This output is used by DRAM to control read or write cycle. This output depends on R/$\overline{W}$ input, i.e., it is asynchronous with CLK. This output drives maximum 44 DRAMs directly without external driver.
RDY	23	25	O	**Ready;** This output identifies whether the memory arrays is refresh mode. If RDY = "L", refresh is excuted. If RDY = "H", refresh is not executed.
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8	33 31 30 29 28 27 26 25 24	35 33 32 31 30 29 28 27 26	O*	**Memory Address;** These outputs are used by DRAM for address inputs, row, column and refresh row address. These outputs can drive maximum 44 DRAMs directly without external driver. These outputs become high impedance state if $\overline{CS}$ = "H".

I: Input, O*: 3-State output, O: Output

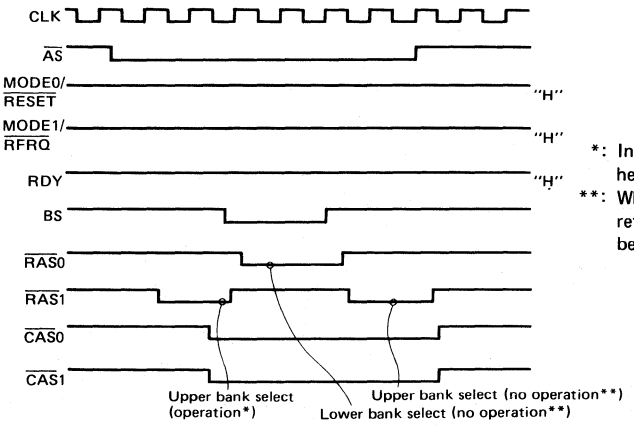
FUNCTIONAL DESCRIPTION

Read/Write Cycle Mode;

The memory read and write cycle starts from $\overline{AS}$ = "L". The selected $\overline{RAS}$ is issued after half cycle period from the falling edge of CLK which strobes $\overline{AS}$ = "L". The $\overline{CAS}$ is issued after 1.5 cycles from $\overline{AS}$ strobed. The $\overline{AS}$ input must satisfy the set up time, T_{ASSL}, referenced to the falling edge of CLK. The address at MA0 to MA8 are changed from row to column at the 3rd rising edge of CLK. The $\overline{WE}$ output depends on R/$\overline{W}$ input, controlled by neither CLK nor $\overline{AS}$, i.e., if R/$\overline{W}$ changes from "H" to "L" in memory cycle ($\overline{AS}$ = "L"), $\overline{WE}$ is changed regardless of states of $\overline{AS}$ and CLK. Therefore, Read-Modify-Write cycle can be executed. Refer to the "APPLICATION" section below.

The bank select (BS) must not change during $\overline{AS}$ = "L" because the $\overline{RAS}$'s are controlled by BS. If BS were changed during $\overline{AS}$ = "L", the both $\overline{RAS}$ ($\overline{RAS0}$ and $\overline{RAS1}$) would be selected during one memory access cycle. Refer to the Fig. 2.

Fig. 2 – BANK SELECTION



*: In the read cycle, the data on upper bank are held valid until $\overline{CAS}$ goes "H".

**: When the DRAM has the "$\overline{CAS}$-before-$\overline{RAS}$" refresh mode, the DRAM executes the $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Refresh Mode;

The MB 1422A provides two types of refresh modes as internal refresh mode and external refresh mode selected by MODE0/$\overline{RESET}$. Both $\overline{RAS0}$ and $\overline{RAS1}$ are issued during refresh mode Both $\overline{CAS0}$ and $\overline{CAS1}$ are set "H" until completion of the refresh cycles.

The refresh addresses are provided by internal refresh counter on MA0 to MA8 before issuing $\overline{RAS}$.

During refresh mode (both internal and external), RDY is set "L" to identify the MB 1422A is in refresh cycle.

When $\overline{AS}$ is brought "L" during RDY = "L", the memory access (both Read and Write Cycle) is ignored and the MB 1422A executes $\overline{RAS}$-only refresh.

1. Internal Refresh Mode;
   The internal refresh mode is selected by MODE0/$\overline{RESET}$ = "H" and executed by internal refresh request.
   In the internal refresh mode, the refresh is automatically taken place by the specified period since internal refresh request signal is generated by the refresh time generator. The internal refresh will be completed within ten CLK cycles, therefore, the RDY remains "L" until ten CLK cycles.
2. External Refresh Mode;
   The external refresh mode is selected by MODE0/$\overline{RESET}$ = "L" and executed when the MODE1/$\overline{REFQ}$ = "L" is strobed by the falling edge of CLK.
   The external refresh will be completed within twelve CLK cycles after MODE1/$\overline{RFRQ}$ = "L" is strobed by the falling of CLK. However, the RDY is kept "L" within ten CLK cycles. Because the first falling edge of CLK after MODE1/$\overline{RFRQ}$ = "L" is used to check the status of $\overline{AS}$ and the second falling edge is used to issue RDY signal.
   If $\overline{AS}$ = "L" is strobed by the first falling edge of CLK, the MB 1422A executes memory access (read or write) first and refresh mode.

Arbitration of memory access and refresh request;

The MB 1422A arbitrates memory access and refresh request, If refresh request, either external or internal, is strobed during memory access cycle, the MB 1422A executes memory access cycle first and refresh cycle. On the other hands, if memory access request is strobed during refresh mode the memory access request will be ignored until the end of refresh cycle.

FUNCTIONAL TRUTH TABLE

BS	READ/WRITE CYCLE		REFRESH CYCLE	
	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS0}$	$\overline{RAS1}$
L	Valid	H	Valid	
H	H	Valid		

$\overline{CS}$	MA0 to MA8	$\overline{RAS0}$ $\overline{RAS1}$	$\overline{CAS0}$ $\overline{CAS1}$	$\overline{WE}$
L	Valid			
H	High-Z			

MODE0/$\overline{RESET}$	MODE1/$\overline{RFRQ}$	Function
H	L	Internal Refresh mode, CLK $\geqq$ 15MHz*
H	H	Internal Refresh mode, CLK = 24 to 25 MHz**
L	$\overline{RFRQ}$	External refresh mode

*: For 8086 (5MHz) and 68000 (8MHz), the refresh is executed once in every 232 CLK cycles.
**: For 8086 (8MHz) and 68000 (12.5MHz), the refresh is executed once in every 372 CLK cycles.

DRAM INTERFACE

Addressing;
The MB 1422A is capable to address directly maximum 512K address with 256K DRAM. Fig. 3 shows the example of interfacing between MPU and MB 1422A for both 64K and 256K DRAM system. The DRAMs require address set-up and hold times on both row and column addresses. The MB 1422A resolves such critical timing requirement. Fig. 4 shows an example of calculation of address set up and hold times.

Fig. 3 – INTERFACING BETWEEN MPU AND DRAM

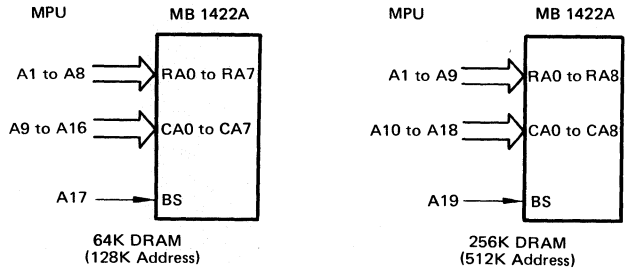
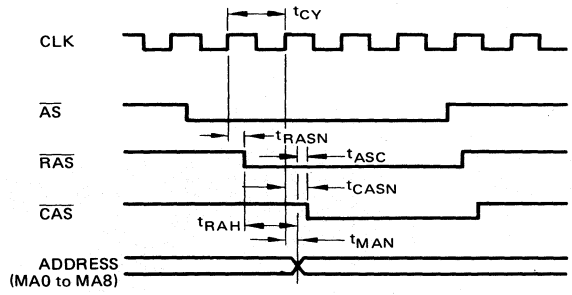


Fig. 4 – EXAMPLE OF ADDRESS SET UP AND HOLD TIME CALCULATION

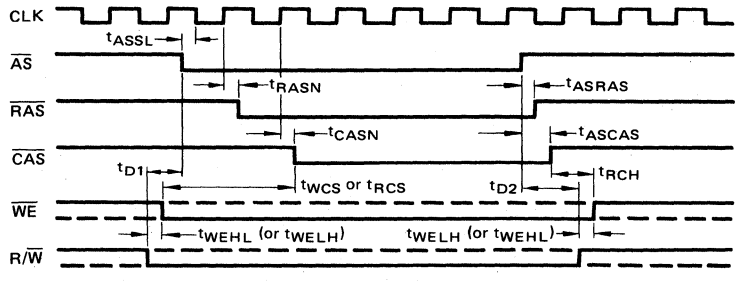


$t_{ASC} = t_{CASN}(Min) - t_{MAN}(Max)$
$t_{RAH} = t_{CY}(Min) + t_{MAN}(Min) - t_{RASN}(Max)$

Read/Write Command;

Since the $\overline{WE}$ depends on R/$\overline{W}$, it must be taken a care to set-up and hold times for Read and Write command. Therefore, R/$\overline{W}$ must be valid before $\overline{CAS}$ = "L", and R/$\overline{W}$ must not be changed until Read or Write command hold time has been satisfied except for read-modify-write cycle. Fig. 5 shows an example of calculation of Read/Write command set up times.

Fig. 5 – READ/WRITE COMMAND SET UP/HOLD TIME



Set Up Time;

$t_{WCS} = (t_{CASN} + 1.5t_{CY} + t_{ASSL}) - (t_{D1} + t_{WEHL})$

$t_{RCS} = (t_{CASN} + 1.5t_{CY} + t_{ASSL}) - (t_{D1} + t_{WELH})$

Hold Time;

$t_{RCH} = t_{D2} - t_{ASCAS} + t_{WEHL}$

Initiallization;

In the single power supplied DRAM which has substrate bias generator, it is necessary 200μs pause time to let substrate stable and after that eight dummy $\overline{RAS}$ cycles must be done for initiallization of internal dynamic circuitly.

Therefore, memory access is not executed correctly until the above pause time and eight dummy cycles have been satisfied. In the case of using internal refresh mode, eight $\overline{AS}$ clocks or eight refresh cycles must be applied after 200μs pause time.

On the other hand, in the case of using external refresh mode eight refresh cycles (keeping MODE1/$\overline{RFRQ}$ = "L" until eight $\overline{RAS}$ = "L" is detected) or eight $\overline{AS}$ cycles must be applied.

Refresh;

The MB 1422A is capable of doing refresh mode for both 2ms/128 cycles and 4 ms/256 cycles.

MPU INTERFACE

The MB 1422A is capable of interfacing with both 8086 and 6800.
The examples of interfacing with these MPU's are shown in Fig. 6 and 7.

Fig. 6 – EXAMPLE OF INTERFACE BETWEEN MB 1422A AND 8086

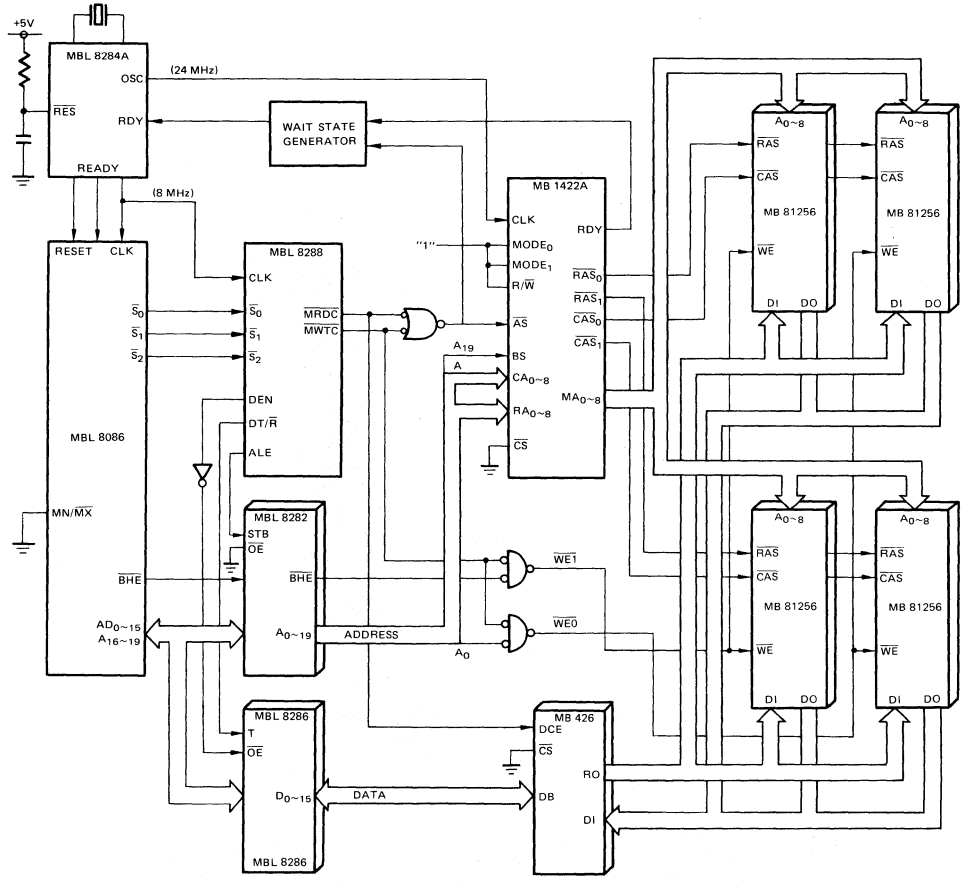
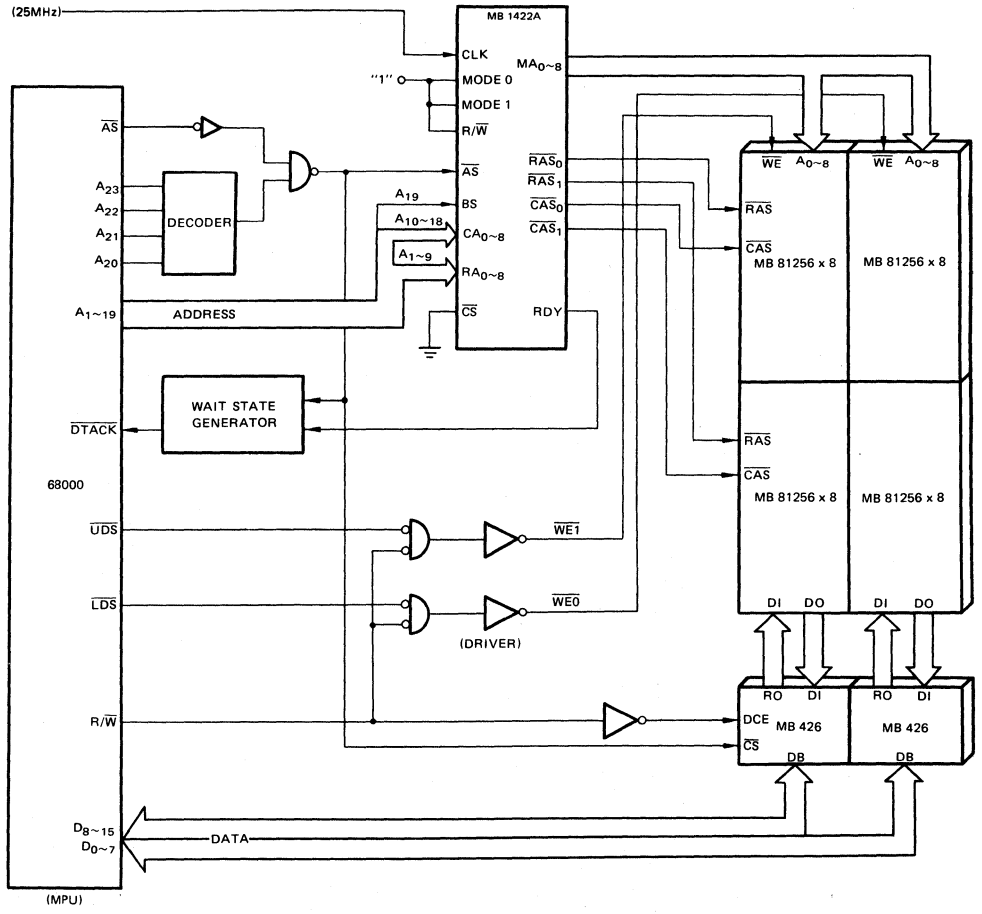


Fig. 7 – EXAMPLE OF INTERFACE BETWEEN MB 1422A AND 68000

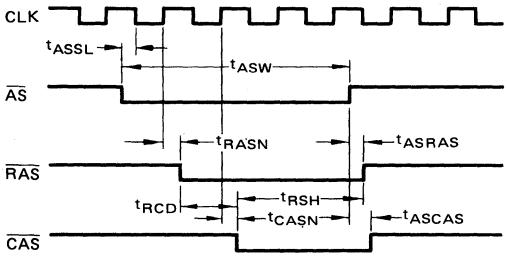


APPLICATION

Memory Access Cycle Time;

Since memory access cycle depends on $\overline{AS}$, the memory cycle time can be controlled by $\overline{AS}$. The minimum cycle time can be calculated with Fig. 8.

Fig. 8 – MEMORY ACCESS CYCLE TIME



Hence, $t_{RCD} = t_{CY} + t_{CASN} - t_{RASN}$
t_{RSH} = 75ns (min) → MB 81256-15

The minimum $\overline{AS}$ Pulse Width must be $t_{RSH} + t_{RCD} + t_{RASN} + 0.5t_{CY} + t_{ASSL} - t_{ASRAS}$.

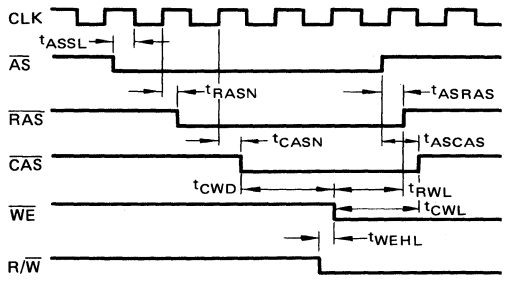
The maximum $\overline{AS}$ pulse width must not be greater than maximum t_{RAS} of DRAM.

Read-Modify-Write;

The MB 1422A provides a capable of read-modify-write and delayed write cycle by delayed write command input on R/$\overline{W}$.

Fig. 9 shows an example of write command on R/$\overline{W}$ for read-modify-write cycle.

Fig. 9 – WRITE COMMAND INPUT FOR READ-MODIFY-WRITE



In the Read-Modify-Write cycle, the write command ($\overline{WE}$) should be delayed with t_{CWD}. Therefore, the write command on the R/$\overline{W}$ should be delayed.

Delay Time of R/$\overline{W}$ from $\overline{AS}$ is;

$t_{ASSL} + 1.5t_{CY} + t_{CASN} + t_{CWD} - t_{WEHL}$.

The t_{RWL} and t_{CWL} must be noticed in the read-modify-write cycle.
Therefore, $\overline{AS}$ must be "L" until delay time of $t_{CWL} - t_{ASCAS}$ and $t_{RWL} - t_{ASRAS}$ have been satisfied.

3

Refresh;

There are two ways for refreshing DRAM in the memory system as cycle steal (or distributed) refresh and burst refresh.

The MB 1422A provides both ways.

In the internal refresh mode, cycle steal refresh is taken place automatically without any external control circuit.

On the other hands, in the external refresh mode, both ways can be used by controlling MODE1/$\overline{\text{RFRQ}}$ input.

1. Cycle Steal Refresh

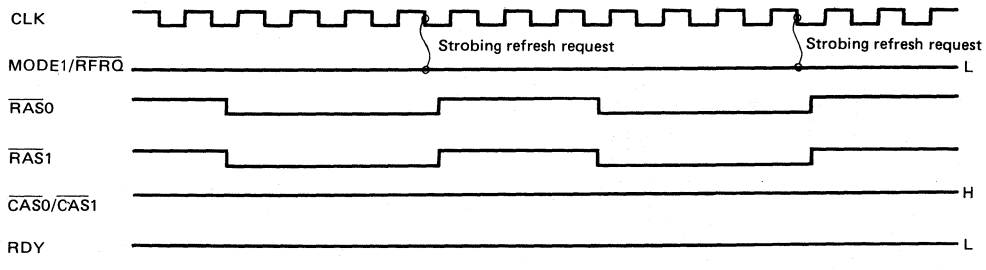
   The cycle steal refresh is taken place by the period divided required refresh period by required refresh cycle, i.e., 4ms/256 = 15.6μs, and the refresh request should be applied at a period of 15.6μs. In the external refresh mode the refresh period counter is necessary for this purpose.

2. Burst Refresh

   The burst refresh is taken place by doing refresh for all required refresh cycles continuously, i.e., the refresh request should be applied at a period of required refresh cycles. When MODE1/$\overline{\text{RFRQ}}$ is kept "L" through all refresh cycles (256 or 128), one refresh cycle will be completed within seven CLK cycles because next refresh request is strobed during the refresh cycle.

   Fig. 10 shows an example of burst refresh cycle with keep MODE1/$\overline{\text{RFRQ}}$ = "L" through the cycle.

Fig. 10 – BURST REFRESH



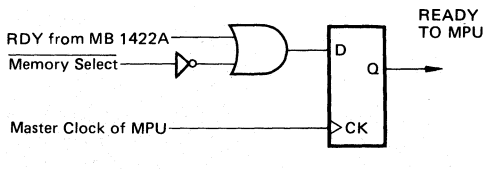
RDY Output;

The MB 1422A issues ready signal to identify whether DRAM array is ready or not. The following cautions are necessary to send RDY to MPU.

- RDY must be sent only when the DRAM array is being accessed.
- RDY must be sent synchronously with MPU operation.
- RDY must be sent before MPU starts operation, and if RDY is issued during MPU operation, RDY must be held until the completion of current MPU operation and then sent to MPU.

The Fig. 11 shows an example of external circuit to send RDY to MPU.

Fig. 11 – EXAMPLE OF RDY INTERFACE TO MPU



In this case, both set up and hold times on READY of MPU must be satisfied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	*V_{CC}	4.5	5.0	5.5	V
Output High Current	I_{OH}	–	–	-3.3	mA
Output Low Current	I_{OL}	–	–	10	mA
Ambient Temperature	T_A	0	–	70	°C

*: **Referenced to GND**

DC CHARACTERISTICS

(Recommended Operation Conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Supply Current		I_{CC}		88*	145	mA	V_{CC} = 5.5V
Input Low Current	Except for CLK and $\overline{CS}$	I_{IL}			-200	μA	V_{CC} = 5.5V, V_{IN} = 0.5V
	CLK, $\overline{CS}$				-400		
Input High Current		I_{IH1}			20	μA	V_{CC} = 5.5V V_{IN} = 2.4V
		I_{IH2}			100		V_{CC} = 5.5V, V_{IN} = 5.5V
Input Clamp Voltage		V_{IC}			-1.5	V	V_{CC} = 4.5V, I_{IN} = -18mA
Output Low Voltage		V_{OL}			0.5	V	V_{CC} = 4.5V, I_{OL} = 10mA
Output High Voltage		V_{OH}	2.4			V	V_{CC} = 4.5V, I_{OH} = -3.3mA
Output Leakage Current (High-Z)		I_{OZ}	-100		100	μA	V_{CC} = 5.5V, V_{OUT} = 0.5V/2.4V
Output Short Circuit Current		I_{OS}	-50	-100*	-200	mA	V_{CC} = 5.5V, V_{OUT} = 0V
Input Low Voltage		V_{IL}	–	–	0.8	V	
Input High Voltage		V_{IH}	2.0	–	–	V	

*: All typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS

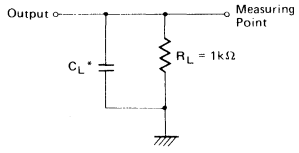
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
$\overline{AS}$ Low Set up Time to CLK	t_{ASSL}	10			ns
$\overline{FRRQ}$ Low Set up Time to CLK	t_{RFRQS}	10			ns
$\overline{RFRQ}$ Low Hold Time to CLK	t_{RFRQH}	10			ns
$\overline{RFRQ}$ High Set up Time to CLK	t_{REFSS}	10			ns
$\overline{AS}$ High Set up Time to CLK	t_{ASSH}	10			ns
BS Set up Time to CLK	t_{BSS}	10			ns
BS Hold Time to $\overline{AS}$	t_{BSH}	10			ns
CLK High Time	t_{WP}	15			ns
CLK Low Time	t_{WN}	15			ns
Delay Time from CLK to $\overline{RAS}$n	t_{RASN}		20	32	ns
Delay Time from $\overline{AS}$ to $\overline{RAS}$n	t_{ASRAS}		18	30	ns
Delay Time from CLK to $\overline{CAS}$n	t_{CASN}		37	52	ns
Delay Time from $\overline{AS}$ to $\overline{CAS}$n	t_{ASCAS}		36	53	ns
Delay Time from RAm to MAm	t_{RAMA}		21	35	ns
Delay Time from CLK to MAm	t_{MAN}		27	42	ns
Delay Time from CAm to MAm	t_{CAMA}		21	35	ns
Delay Time from $\overline{AS}$ to MAm	t_{ASMA}		23	39	ns
Delay Time from R/$\overline{W}$ to $\overline{WE}$	t_{WEHL}		16	25	ns
	t_{WELH}		17	28	ns
Delay Time from CLK to $\overline{RAS}$n (Refresh cycle)	t_{RASRHL}		24	36	ns
	t_{RASRLH}		25	37	ns
Delay Time from CLK to MAm (Refresh cycle)	t_{MAR}		33	51	ns
Delay Time from CLK to RDY (Refresh cycle)	t_{RDYHL}		23	35	ns
	t_{RDYLH}		21	32	ns
Address Enable Time from $\overline{CS}$	t_{PZHMA}		24	43	ns
	t_{PZLMA}		24	41	ns
$\overline{WE}$ Enable Time from $\overline{CS}$	t_{PZHWE}		24	43	ns
	t_{PZLWE}		24	41	ns
$\overline{RAS}$/$\overline{CAS}$ Enable Time from $\overline{CS}$	t_{PZHRC}		20	38	ns
	t_{PZLRC}		23	41	ns
Address Disable Time from $\overline{CS}$	t_{PHZMA}		36	56	ns
	t_{PLZMA}		32	48	ns
$\overline{WE}$ Disable Time from $\overline{CS}$	t_{PHZWE}		36	56	ns
	t_{PLZWE}		32	48	ns
$\overline{RAS}$/$\overline{CAS}$ Disable Time from $\overline{CS}$	t_{PHZRC}		33	48	ns
	t_{PLZRC}		23	39	ns
Column Address to $\overline{CAS}$ Set up Time	t_{ASC}	0			ns
$\overline{RAS}$ Puls Width (Refresh cycle)	t_{WRAS}	150			ns
Delay Time from $\overline{RAS}$ to $\overline{CAS}$	t_{RCA}	25			ns
Row Address Hold Time	t_{RAH}	20			ns

n; 0, 1
m; 0, 1, 2, 4, 5, 6, 7, 8

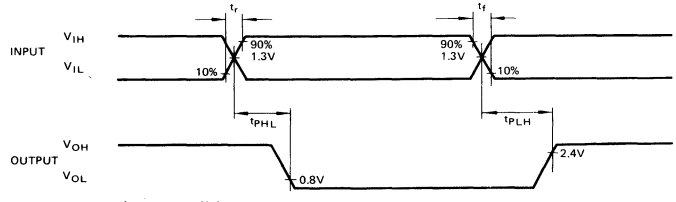
AC CHARACTERISTICS TEST CONDITIONS

1. DELAY TIME



Pin Name	C_L (std)
MA0 to MA8	300pF
$\overline{WE}$	300pF
$\overline{RAS0}$ and $\overline{RAS1}$	200pF
$\overline{CAS0}$ and $\overline{CAS1}$	200pF
RDY	150pF

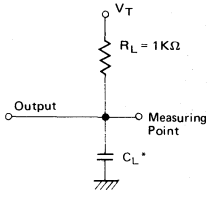
* Including jig capacitance.



Input conditions;

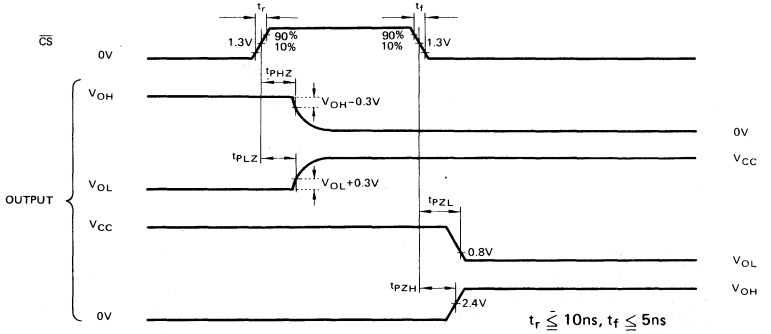
V_{IH} = 3V, V_{IL} = 0V, $t_r \leqq 10ns$, $t_f \leqq 5ns$

2. ENABLE/DISABLE TIME



* Including jig capacitance.

	Symbol	Pin Name	CL (pF)	VT (V)
Disable time measurement	t_{PLZ}	MA0 to MA8, $\overline{WE}$	300	V_{CC}
		$\overline{RAS}$, $\overline{CAS}$	200	
	t_{PHZ}	MA0 to MA8, $\overline{WE}$	300	0
		$\overline{RAS}$, $\overline{CAS}$	200	
Enable time measurement	t_{PZL}	MA0 to MA8, $\overline{WE}$	300	V_{CC}
		$\overline{RAS}$, $\overline{CAS}$	200	
	t_{PZH}	MA0 to MA8, $\overline{WE}$	300	0
		$\overline{RAS}$, $\overline{CAS}$	200	



$t_r \leqq 10ns$, $t_f \leqq 5ns$

Delay time calcuration

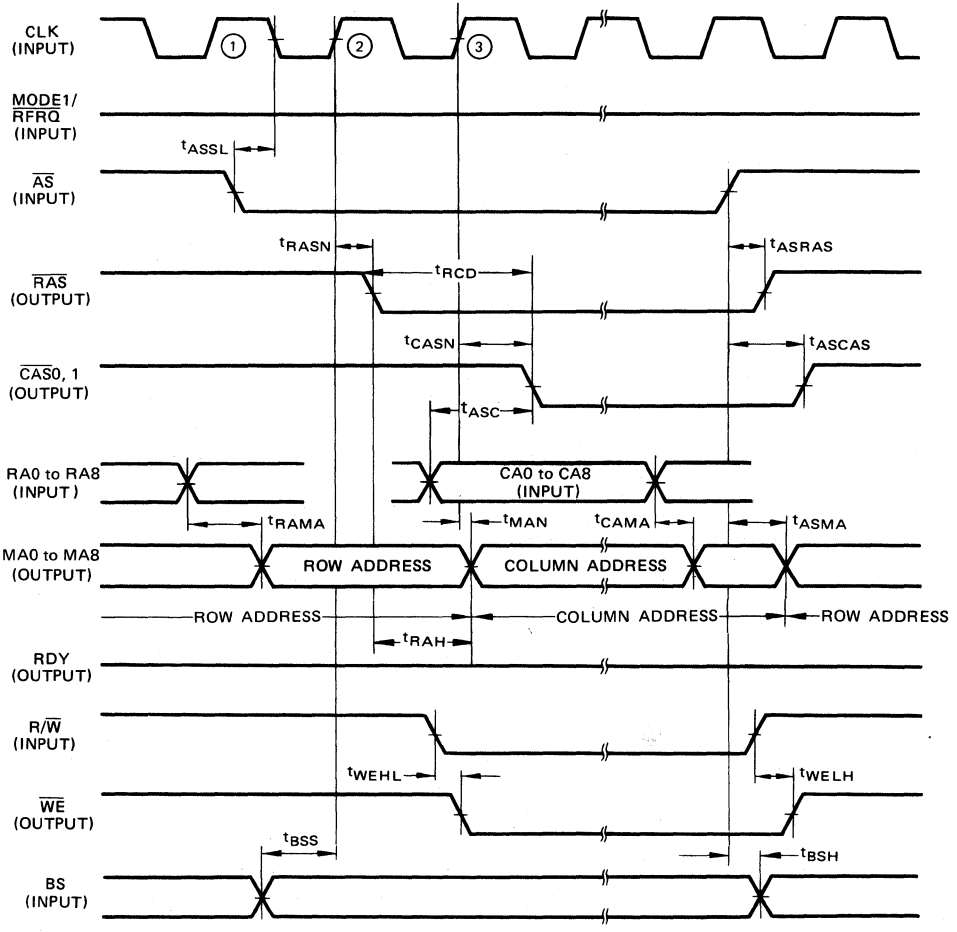
When the load capacitance is different from the standard value shown above, the delay time is specified according to the following equation.

$t_{pd(CL)} = t_{pd(Std)} + 0.04 \times \triangle C_L$, $\triangle C_L = C_L - C_{L(Std)}$

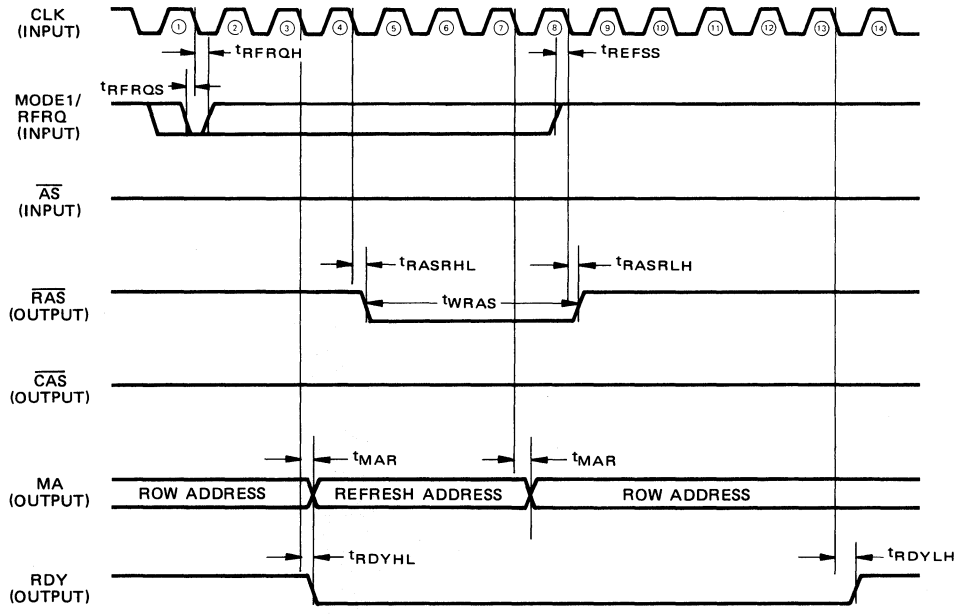
Unit: t_{pd} = ns

C_L = pF

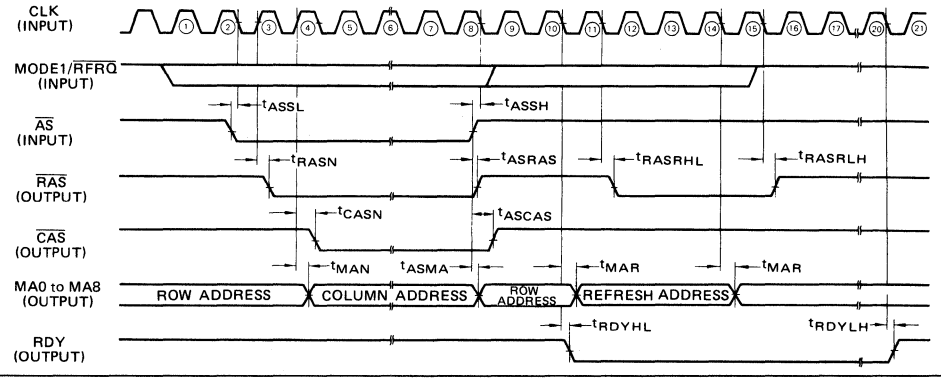
READ/WRITE CYCLE TIMING DIAGRAM



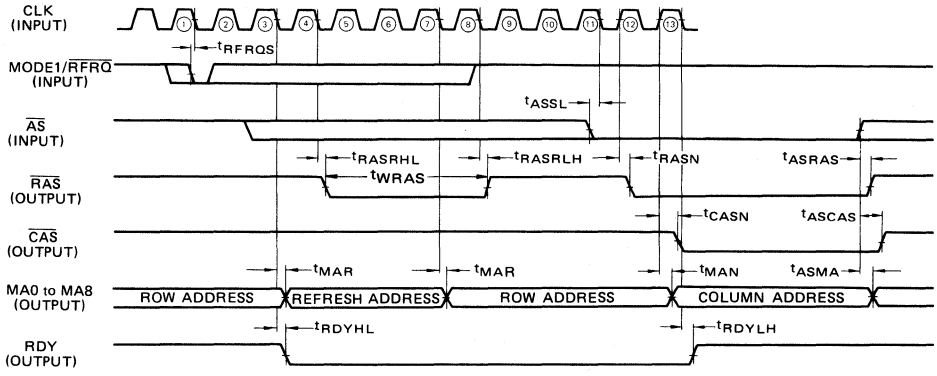
EXTERNAL REFRESH CYCLE TIMING DIAGRAM



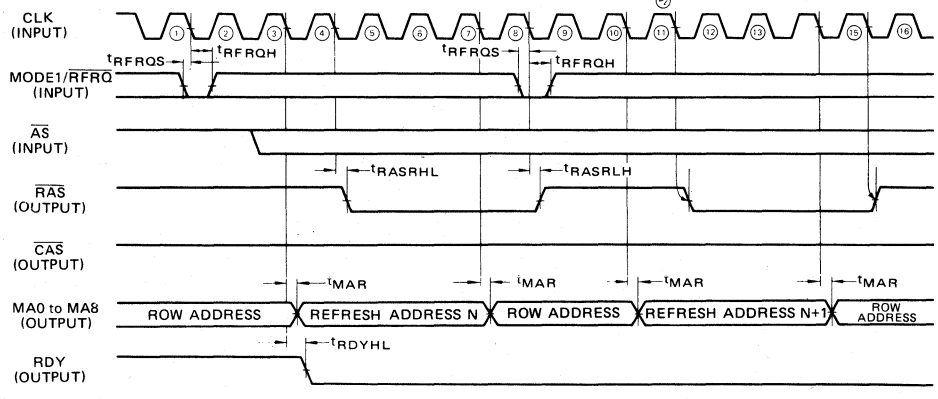
READ/WRITE REFRESH CYCLE



REFRESH READ/WRITE CYCLE



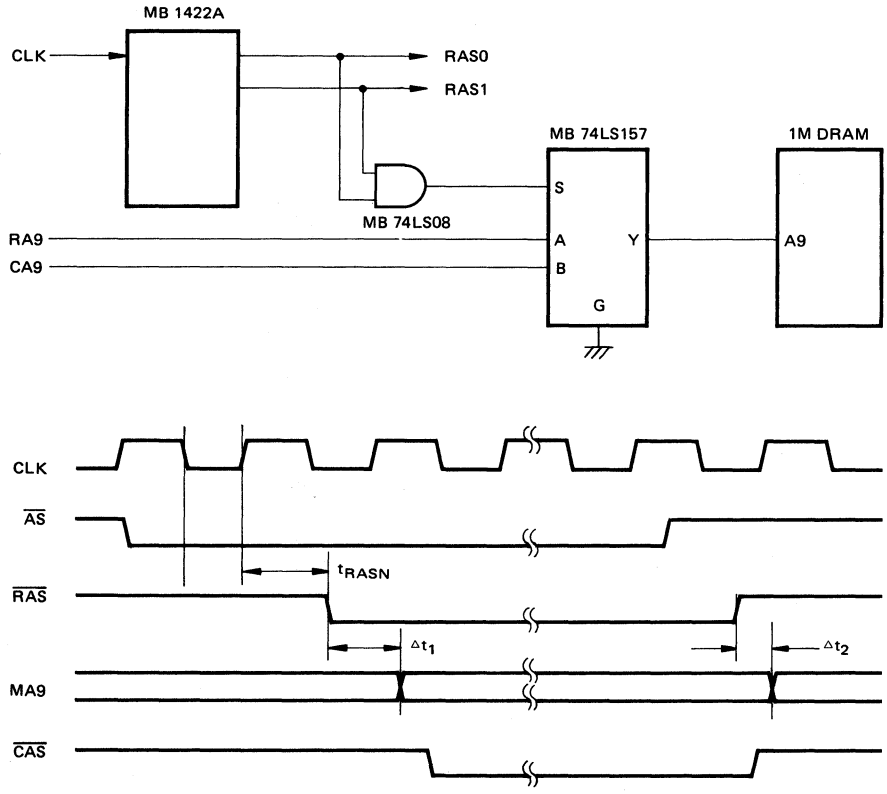
BURST REFRESH CYCLE



APPLICATION FOR 1M DRAM

The Fujitsu MB 1422A is designed to refresh all nine bits of memory addresses (MA0 to MA8). It can also, control 1M DRAMs by adding some external circuits.
Refer to the application circuits described below.

Fig. 12 – ADDITIONAL EXTERNAL CIRCUIT

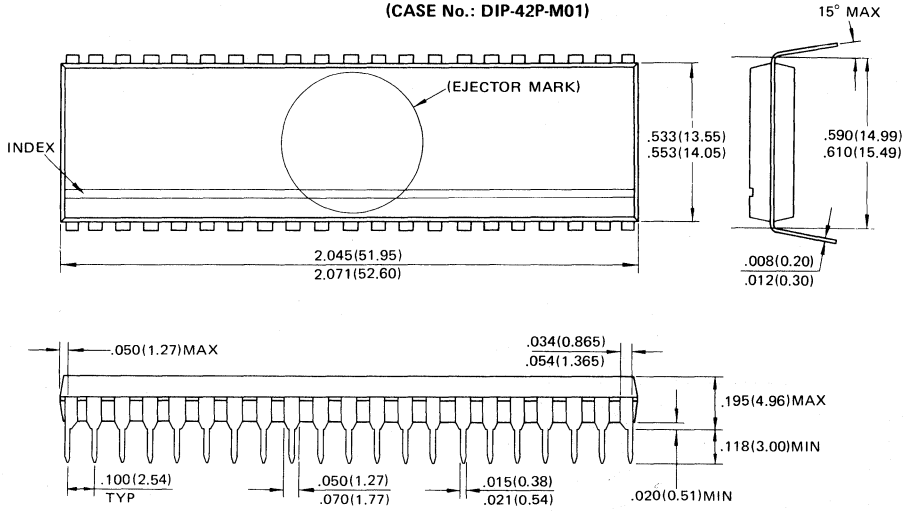


$\Delta t1 = t_{PHL}$ (LS08) + t_{PLH} or t_{PHL} (LS157) $\geqq t_{RAH}$ (Row Address Hold Time)
$\Delta t2 = t_{PLH}$ (LS08) + t_{PLH} or t_{PHL} (LS157)

3

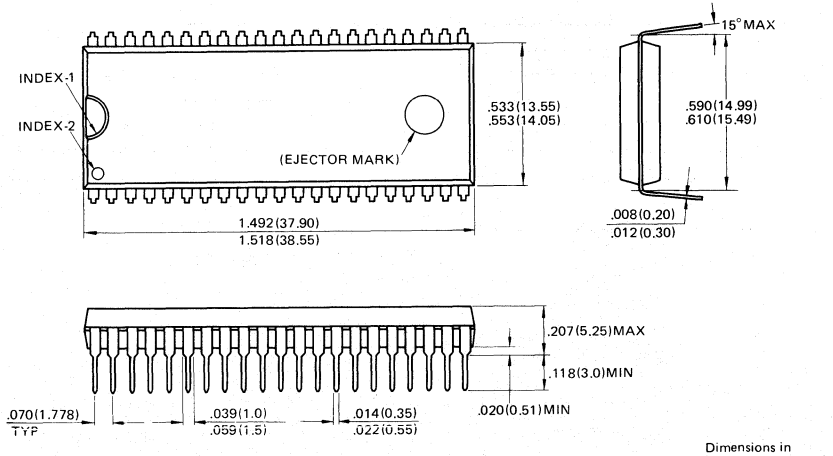
PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



Dimensions in inches (millimeters)

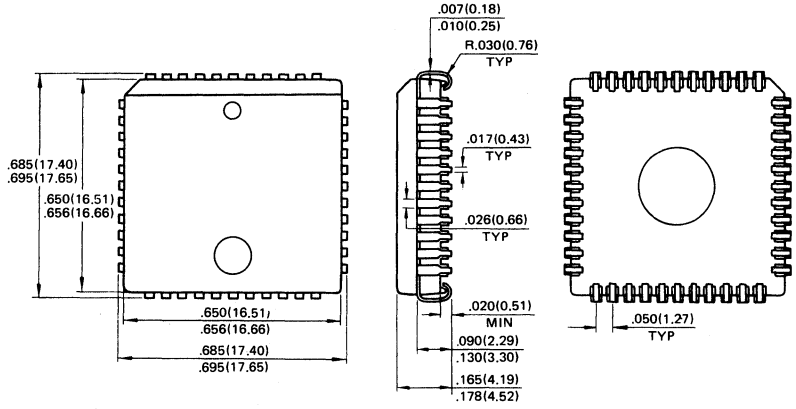
42-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-42P-M02)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

44-LEAD PLASTIC CHIP CARRIER
(CASE No.: LCC-44P-M01)



Dimensions in
inches (millimeters)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	15	RA5	29	MA5
2	RA0	16	CA5	30	MA4
3	CA0	17	RA6	31	MA3
4	RA1	18	CA6	32	MA2
5	CA1	19	RA7	33	MA1
6	RA2	20	CA7	34	VCC
7	CA2	21	RA8	35	MA0
8	RA8	22	CA8	36	CAS1
9	CA3	23	GND	37	CAS0
10	MODE0/RESET	24	WE	38	RAS1
11	CLK	25	RDY	39	RAS0
12	GND	26	MA8	40	MODE1/RFRQ
13	RA4	27	MA7	41	R/W
14	CA4	28	MA6	42	AS
				43	BS
				44	CS