FUJITSU

16 BIT ERROR CHECKING & CORRECTION

MB1426

April, 1986
Edition 1.0

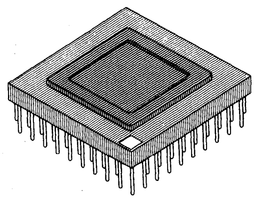
PRELIMINARY

DESCRIPTION

The MB1426 Error Checking and Correction (ECC) device is designed to enhance memory reliability in 16-bit systems. Using a modified Hamming Single-Error-Correction/Double-Error-Detection (SEC/DED) code, the ECC can find and correct all single-bit errors and detect all double-bit errors. The MB1426 is a TTL device fabricated in low-power Schottky and is housed in a 64-pin Pin-Grid-Array (PGA) package.

FEATURES

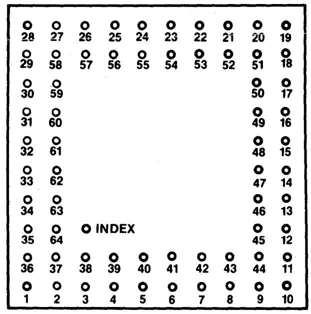
- Detects and corrects all single-bit errors
- Detects all double-bit errors
- On-chip latches for memory-read, check-bit, and syndrome data
- Separate busses for CPU and memory data
- Direct read/write by ECC-through mode
- Low power Schottky TTL for high performance
- Single +5V supply



PGA-64C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENTS



No.	I/O	Name	No.	I/O	Name	No.	I/O	Name	No.	I/O	Name
01	B	CD08	17	B	CB1	33	I	$\overline{\text{PWC0}}$	49	B	CB4
02	I	$\overline{\text{PWC1}}$	18	B	CB2	34	B	CD14	50	B	CB5
03	B	CD07	19	B	MD01	35	B	CD12	51	B	MD00
04	B	CD05	20	B	MD03	36	B	CD10	52	B	MD02
05	B	CD04	21	B	MD04	37	B	CD09	53	B	MD05
06	B	CD03	22	B	MD06	38	I	$\overline{\text{ECCTH}}$	54		GND
07	B	CD01	23	B	MD07	39	B	CD06	55	B	MD09
08	O	$\overline{\text{ERR}}$	24	B	MD08	40		GND	56	B	MD11
09	O	$\overline{\text{MERR}}$	25	B	MD10	41	B	CD02	57	B	MD13
10	T	STCB0	26	B	MD12	42	B	CD00	58	B	MD15
11	T	STCB1	27	B	MD14	43	I	ERREN	59	I	RCLK
12	T	STCB2	28	I	$\overline{\text{BSCNT}}$	44	I	$\overline{\text{EN}}$	60	O	$\overline{\text{PERR}}$
13	T	STCB3	29	B	P1	45	I	$\overline{\text{SLE}}$	61		VCC
14	T	STCB4	30	O	$\overline{\text{PERR1}}$	46	I	$\overline{\text{RST}}$	62	B	CD15
15	T	STCB5	31	B	P0	47		VCC	63	B	CD13
16	B	CB0	32	O	$\overline{\text{PERR0}}$	48	B	CB3	64	B	CD11

B: Bidirectional pin
I: Input pin
O: Output pin

PIN DESCRIPTIONS

Pin No.	Designator	Function
33 2	$\overline{PWC0}$ $\overline{PWC1}$	Partial Write Control/Read Write Control: These pins are used to control read write and they are also used to control the partial write. If both $\overline{PWC0}$ and $\overline{PWC1}$ = "H" the read operation is selected. If both $\overline{PWC0}$ and $\overline{PWC1}$ = "L" the word write operation is selected. In the partial write mode, if $\overline{PWC0}$ = "L" and $\overline{PWC1}$ = "H", the lower byte (MD0 to MD7) is written CPU data and the upper byte (MD8 to MD15) is written memory data which is latched during previous read operation. On the other hand, if $\overline{PWC0}$ = "H" and $\overline{PWC1}$ = "L" the lower byte is written memory data and the upper byte is written CPU data.
59	RCLK	Read Data Latch Clock: This pin is used to strobe the read data from memory and latch into the internal read data latch. The rising edge of RCLK strobes read data from MD00/MD15 and check bits from CB0/CB5. In the read cycle, data is strobed on the rising of RCLK.
45	$\overline{SLE}$	Syndrome Latch Enable: This pin is used to latch syndrome bits into the internal syndrome latch. The falling edge of $\overline{SLE}$ strobes and latches the syndrome bits until $\overline{RST}$ = "L".
46	$\overline{RST}$	Syndrome Latch Reset: This pin is used to reset syndrome latch. If $\overline{RST}$ = "L", the syndrome latch is reset and the latch is enabled to accept next string of syndrome bits.
43	$\overline{ERREN}$	Error Enable: This pin is used to enable $\overline{ERR}$ and $\overline{MERR}$ outputs. If $\overline{ERREN}$ = "L", $\overline{ERR}$ and $\overline{MERR}$ are set "H" and disabled.
44	$\overline{EN}$	Syndrome Output Enable: This pin is used to enable syndrome outputs (STCB0 and STCB5). If $\overline{EN}$ = "L", STCB0/STCB5 are enabled. If $\overline{EN}$ = "H", STCB0/STCB5 are disabled and in the high-impedance state.
38	$\overline{ECCTH}$	ECC Through: This pin is used to enable the ECC-through mode. If $\overline{ECCTH}$ = "L", ECC-through mode is enabled and the read or write cycle is executed without regard to the ECC function. When ECC is utilized, the $\overline{ECCTH}$ pin must be "H".
28	$\overline{BSCNT}$	Bus Control: This pin is used to control the operating mode of data pins CD00/CD15 and MD00/MD15, also to disable $\overline{PERR0}$, $\overline{PERR1}$ and $\overline{PERR}$. If $\overline{BSCNT}$ = "L" all data pins are in the input mode and $\overline{PERR0}$, $\overline{PERR1}$ and $\overline{PERR}$ are disabled (set "H"). If $\overline{BSCNT}$ = "H", the operating mode of these data pins is controlled by the states of $\overline{PWC0}$, and $\overline{PWC1}$, and $\overline{PERR0}$, $\overline{PERR1}$ and $\overline{PERR}$ are enabled corresponding the the state of $\overline{PWC0}$ and $\overline{PWC1}$.
42 7 41 6	CD00 CD01 CD02 CD03	CPU Data: These pins have a common I/O capability and are connected to the CPU data bus. In the write cycle, these pins are in the input mode, that is, the CPU data is input to these pins and

3

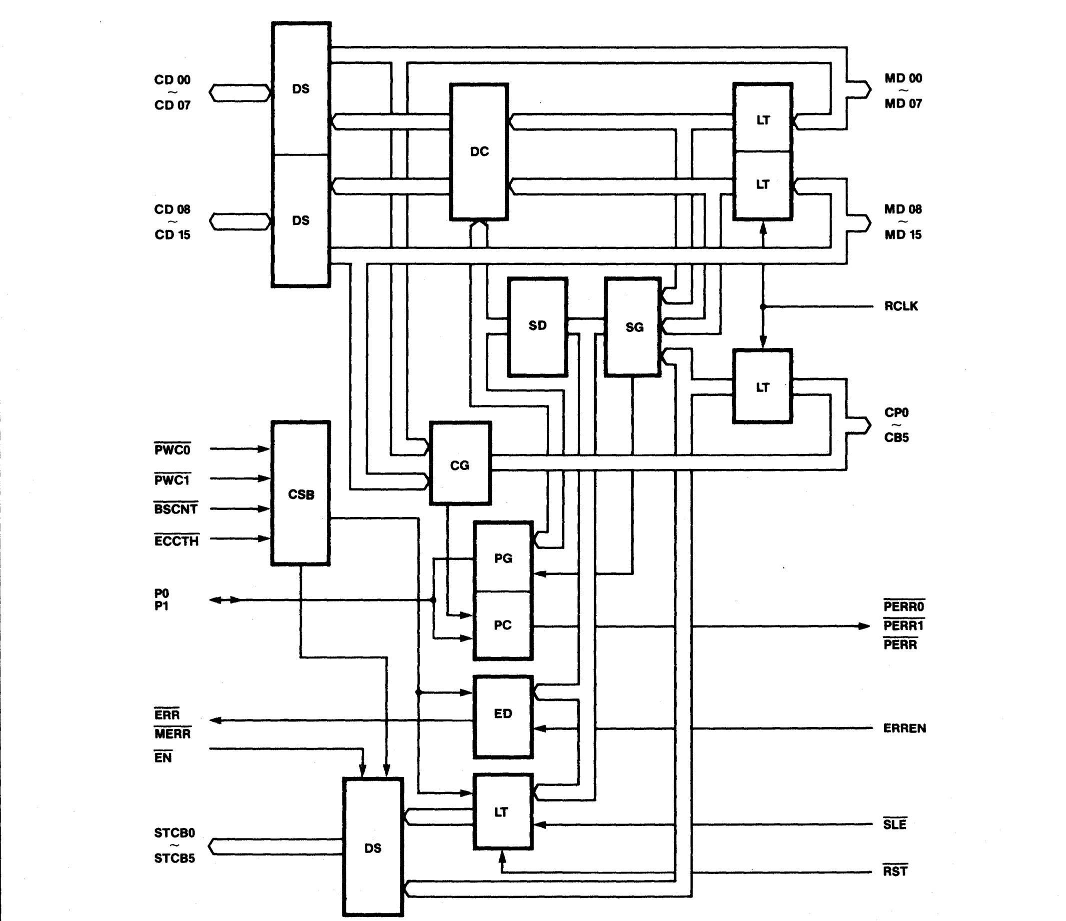
PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
5 4 39 3 1 37 36 64 35 63 34 62	CD04 CD05 CD06 CD07 CD08 CD09 CD10 CD11 CD12 CD13 CD14 CD15	output to memory through MD00/MD15. In a read cycle, these pins are in the output mode, that is, memory data from MD00/MD15 is output to the CPU via these pins.
51 19 52 20 21 53 22 23 24 55 25 56 16 57 27 58	MD00 MD01 MD02 MD03 MD04 MD05 MD06 MD07 MD08 MD09 MD10 MD11 MD12 MD13 MD14 MD15	Memory Data: These pins have a common I/O capability and they are connected to the memory data bus. In a write cycle, these pins are in the output mode, that is, CPU data from CD00/CD15 is output to memory through these pins. In a read cycle, these pins are in the input mode, that is, memory data is input to these pins and output through CD00/CD15.
31 29	P0 P1	Parity Bit: These pins have a common I/O capability and P0 and P1 correspond, respectively, to the lower byte and the upper byte. The parity bit from the CPU should be odd parity.
16 17 18 48 49 50	CB0 CB1 CB2 CB3 CB4 CB5	Check Bit: These pins have a common I/O capability and are connected to the check bit memory I/O line. In a write cycle, check bit data is generated by the check bit generator using CPU data; the check-bit pattern is output to check bit memory, that is, during a write cycle, these pins operate in the output mode. In a read cycle, the check-bit pattern from memory is input to these pins, that is, during a read cycle, these pins operate in the input mode.
10 11 12 13 14 15	STCB0 STCB1 STCB2 STCB3 STCB4 STCB5	Syndrome-Through Check Bit: These pins output the syndrome bits when read or partial write is selected. These outputs are used to analyze an error bit in the data word (CD00/CD15) and in the check bits (CB0/CB5). In the ECC-through mode, these pins output the check bits from memory.
8	$\overline{ERR}$	Error: This pin outputs the error flag when any single- or multiple-bit error is detected.

PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
9	$\overline{MERR}$	Multiple Error: This pin outputs the multiple error flag when a multiple-bit error is detected.
32 30 60	$\overline{PERR0}$ $\overline{PERR1}$ $\overline{PERR}$	Parity Error: These pins output a parity error flag when parity error occurs on CPU data. If $\overline{PERR0}$ = "L", a parity error on CD00/CD07 and P0 occurs. If $\overline{PERR1}$ = "L", a parity error on CD8/CD15 and P1 occurs. $\overline{PERR} = \overline{PERR0} \cdot \overline{PERR1}$.

BLOCK DIAGRAM



DS: Data Selector
DC: Data Corrector
LT : Latch
ED: Error Detector
SD: Syndrome Decoder
SG: Syndrome Generator
CSB: Control Signal Buffer
CG: Check Bit Generator
PG: Parity Generator
PC: Parity Checker

ANALYSIS OF BLOCK DIAGRAM

DS (Data Selector): Selects memory-read or memory-write data.

DC (Data Corrector): Corrects a single-bit error by using syndrome decoder.

LT (Latches): Latches memory-read, check-bit, and syndrome data.

ED (Error Detector): Detects single-bit or double-bit errors of memory-read data (MD00/MD15 and CB0/CB5). Single-bit or double-bit errors are determined, respectively, by the states of $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$.

SG (Syndrome Generator): Generates a syndrome-bit pattern to check memory-read data.

SD (Syndrome Decoder): Decodes syndrome-bit pattern of Syndrome Generator. When a single-bit error is detected, locates error bit and inverts the parity bit.

CSB (Control Signal Buffer): Buffers all control signals.

CG (Check Bit Generator): Generates check bit for checking memory-write data.

PG (Parity Generator): Generates odd parity bit for bus data.

PC (Parity Checker): Checks odd parity bit for bus data.

SDS (Syndrome Data Selector): Selects syndrome data or memory-check bit.

FUNCTIONAL DESCRIPTION

The error-detecting and error-correcting capabilities of the MB1426 ECC provides the user with a high order of confidence in memory reliability. Using a modified Hamming SEC/DED code, the ECC is able to detect and correct all single-bit errors and to detect all double-bit errors, even those containing consecutive strings of 0s and 1s. The detect/correct cycle for single-bit errors occurs without interrupting the CPU. Error flags notify the user when an error is detected.

The MB1426 has on-chip latches for memory-read, check-bit, and syndrome data; latching of the memory data allows the user to execute a partial (byte) write. To further enhance transmission reliability, a parity generator and checker is available to the user. A brief description of the read, write, and partial-write capabilities are described in subsequent paragraphs; for a detailed analysis of operating principles, refer to the Functional Truth Tables.

Read Cycle

The read cycle is executed by setting $\overline{\text{BSCNT}}$, $\overline{\text{PWC0}}$, and $\overline{\text{PWC1}}$ to the High state. The data and check bits from memory are read out and latched on the rising edge of RCLK; the latched data is sent to the syndrome generator and data corrector. The syndrome bit pattern is generated and decoded by the syndrome decoder; the decoded results are then sent to the data corrector.

If a single-bit error is detected, the $\overline{\text{ERR}}$ flag is raised and the error is corrected by the data corrector; the corrected data is output to CD00/CD15. When a single-bit error is detected and $\overline{\text{SLE}}$ is driven Low, the falling edge triggers the syndrome latches; this latched data is output to STCB0/STCB5 when $\overline{\text{EN}}$ is driven Low. Because data is held in the syndrome latches until $\overline{\text{RST}}$ is driven Low, "$\overline{\text{RST}}$ = L" should be executed before the syndrome data is used to identify the error-bit location.

If multiple-bit errors or a bit string (0s or 1s) error is detected, both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$ flags are raised and the latched memory data is output to CD00/CD15. For these cases, the data correction cycle is not executed.

In the read cycle, odd parity bits for bytes MD00/MD07 and MD08/MD15, respectively, are output to P0 and P1.

Write Cycle

Write capabilities of the MB1426 include both word write and partial (byte) write; either operation can be selected by setting $\overline{\text{PWC0}}$ and $\overline{\text{PWC1}}$ to the proper states—see Truth Tables that follow. If the CPU is capable of parity coding, the parity bits of P0 and P1 are utilized and, in both the word and paritial-byte write modes, the parity bits are checked.

The word write mode is executed by setting both $\overline{\text{PWC0}}$ and $\overline{\text{PWC1}}$ to the Low state. In the word-write mode, CPU data from CD00/CD15 is transferred to the check-bit generator and to MD00/MD15. Data appearing at MD00/MD15 is output and written into memory. The check-bit generator uses the CPU data to generate the check bits and these are output to CB0/CB5. The CPU and check-bit data are written into memory during the same write cycle.

The partial write mode is executed by setting either $\overline{\text{PWC0}}$ or $\overline{\text{PWC1}}$ to the Low state. If $\overline{\text{PWC0}}$ is Low and $\overline{\text{PWC1}}$ is High, the partial write is performed on byte CD00/CD07; in reverse states, byte CD08/CD15 is affected. Before a partial write is executed, the memory and check-bit data must be latched by setting $\overline{\text{BBSCNT}}$ to the Low state; this action puts CD00/CD15, MD00/MD15, P0, and P1 in the input mode and avoids data output to the CPU and memory.

The 8-bits of CPU data to be written to memory and the data to be read from memory are sent to the check-bit generator and to MD00/MD15; the data on MD00/MD15 is written into memory. Check bits are generated from 8-bits of CPU data and 8-bits of memory data and the check bits are then output to CB0/CB5. The partial write operation can be summarized as follows:

- Set $\overline{\text{BBSCNT}}$ Low and latch the 16-bit memory data and 6 check bits by executing a read cycle.
- Set either $\overline{\text{PWC0}}$ or $\overline{\text{PWC1}}$ Low and execute a write cycle. (In this case, BSCNT should be High to change MD00/MD15 from the input to the output mode.)
- Check bits are generated by 8 bits of CPU data and 8 bits of memory data.

FUNCTIONAL TRUTH TABLES

CPU Bus/Memory Bus Control

$\overline{BSCNT}$	$\overline{PWC0}$	$\overline{PWC1}$	CD00 to CD07, P0	CD08 to CD15, P1	MD00 to MD07	MD08 to MD15	Function
H	H	H	Output	Output	Input	Input	Read
	L	H	Input	Input	Output[1]	Output[2]	Partial Write
	H	L	Input	Input	Output[2]	Output[1]	
	L	L	Input	Input	Output	Output	Write
L	X	X	Input	Input	Input	Input	No function

Notes:
1. The CPU data is written into memory.
2. Memory data from previous read cycle is written into memory.

Syndrome Output Control

$\overline{ECCTH}$	$\overline{PWC0}$	$\overline{PWC1}$	$\overline{EN}$	CB0 to CB5	STCB0 to STCB5	Function
H	H	H	L	Input	Syndrome	Read
	L	H		Output	Syndrome	Partial Write
	H	L		Output		
	L	L		Output		Write
L	X	X		Input	Check Bit	ECC-Through
X	X	X	H		High-Z	

Hamming Code

Check Bit	CPU Data																Function
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
CB0		X		X		X		X		X		X		X		X	Odd
CB1			X	X			X	X			X	X			X	X	Odd
CB2					X	X	X	X	X	X	X		X			X	Even
CB3	X	X	X	X	X	X	X	X	X								Odd
CB4	X	X	X		X			X					X	X	X	X	Even
CB5	X								X	X	X	X	X	X	X	X	Odd

FUNCTIONAL TRUTH TABLES (continued)

Check Bit Generation

$CB0 = \overline{CD01 + CD03 + CD05 + CD07 + CD09 + CD11 + CD13 + CD15}$

$CB1 = \overline{CD02 + CD03 + CD06 + CD07 + CD10 + CD11 + CD14 + CD15}$

$CB2 = CD04 + CD05 + CD06 + CD07 + CD08 + CD09 + CD10 + CD12 + CD15$

$CB3 = \overline{CD00 + CD01 + CD02 + CD03 + CD04 + CD05 + CD06 + CD07 + CD08}$

$CB4 = CD00 + CD01 + CD02 + CD04 + CD07 + CD12 + CD13 + CD14 + CD15$

$CB5 = \overline{CD00 + CD08 + CD09 + CD10 + CD11 + CD12 + CD13 + CD14 + CD15}$

Syndrome Decode

Syndrome (STCB)	Error Bit																						No Error
	Memory Bus Data (MD)																Check Bit (CB)						
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	0	1	2	3	4	5	
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	0	0	0	0
2	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0
3	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0
4	1	1	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0
5	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0

Error Detection and Correction

$\overline{ERR}$	$\overline{MERR}$	Message	Detect	Correct
H	H	No Error	—	—
L	H	Single Bit Error	Yes	Yes
L	L	Multiple Bit Error	Yes	No

Error Flag Control

<table>
<tr><th>ERREN</th><th>$\overline{ECCTH}$</th><th>$\overline{PWC0}$</th><th>$\overline{PWC1}$</th><th>$\overline{ERR}$
$\overline{MERR}$</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td rowspan="3">disable</td></tr>
<tr><td>X</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">1</td><td>0</td><td>1</td><td rowspan="3">enable</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>

Parity Error Flag Control

BSCNT	PWC0	PWC1	PERR0	PERR1	PERR
H	H	H	H	H	H
	L	H	enable	H	enable
	H	L	H	enable	
	L	L	enable		
L	X	X	H	H	H

H: Disable state

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_I	-0.5 to 5.5	V
Output Voltage	V_O	-0.5 to 5.5	V
Operating Temperature	T_{OP}	–25 to 85	°C
Storage Temperature	T_{STG}	-55 to 125	°C

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output High Current	I_{OH}			-3.3	mA
Output Low Current	I_{OL}			10	mA
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply Current		I_{CC}		240	400	mA	V_{CC} = 5.5V
Input Low Current	Except for PWC0, PWC1, ECCTH	I_{IL}			-200	µA	V_{CC} = 5.5V, V_{IN} = 0.5V
	PWC0, PWC1, ECCTH				-400		
Input High Current		I_{IH1}			20	µA	V_{CC} = 5.5V, V_{IN} = 2.4V
		I_{IH2}			100		V_{CC} = 5.5V, V_{IN} = 5.5V
Input Clamp Voltage		V_{IC}			-1.5	V	V_{CC} = 4.5V, I_I = –18mA
Output Low Voltage		V_{OL}			0.5	V	V_{CC} = 4.5V, I_{OL} = 10mA
Output High Voltage		V_{OH}	2.4			V	V_{CC} = 4.5V, I_{OH} = –3.3mA
Output Leakage Current (High-Z)		I_{OZ}	-100		100	µA	V_{CC} = 5.5V, V_I = 0.5V/2.4V
Output Short Circuit Current		I_{OS}		-60		mA	V_{CC} = 5.5V, V_O = 0V
Input Low Voltage		V_{IL}			0.8	V	
Input High Voltage		V_{IH}	2.0			V	

AC CHARACTERISTICS (continued)

(Recommended operating conditions and AC test conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay Time from RCLK to CD, P0, P1	t_{CKCD}		35	57	ns
Delay Time from RCLK to $\overline{ERR}$	t_{CKER}		22	37	ns
Delay Time from RCLK to $\overline{MERR}$	t_{CKMER}		25	42	ns
Delay Time from ERREN to $\overline{ERR}$, $\overline{MERR}$	t_{EREN}		11	21	ns
MD Set Up Time referenced to RCLK	t_{MDCKS}	15			ns
MD Hold Time referenced to RCLK	t_{MDCKH}	10			ns
CB Set Up Time referenced to RCLK	t_{CBCKS}	15			ns
CB Hold Time referenced to RCLK	t_{CBCKH}	10			ns
Disable Time of MD from $\overline{PWC0}/\overline{PWC1}$	t_{MDZD}		15	26	ns
Disable Time of CB from $\overline{PWC0}/\overline{PWC1}$	t_{CBZD}		15	26	ns
Enable Time of CD, P0, P1 from $\overline{PWC0}/\overline{PWC1}$	t_{CDZE}		22	36	ns
Delay Time from CD to MD	t_{CDMD}		16	27	ns
Delay Time from CD to CB	t_{CDCB}		21	34	ns
Delay Time from CD to $\overline{PERR0}/\overline{PERR1}$	t_{CDPEN}		22	35	ns
Delay Time from CD to $\overline{PERR}$	t_{CDPER}		23	38	ns
Delay Time from P0/P1 to $\overline{PERR0}/\overline{PERR1}$	t_{PPEN}		12	22	ns
Delay Time from P0/P1 to $\overline{PERR}$	t_{PPER}		14	26	ns
Enable Time of MD from $\overline{PWC0}/\overline{PWC1}$	t_{MDZE}		20	32	ns
Enable Time of CD from $\overline{PWC0}/\overline{PWC1}$	t_{CBZE}		20	32	ns
Disable Time of CD, P0, P1 from $\overline{PWC0}/\overline{PWC1}$	t_{CDZD}		15	26	ns
Delay Time from $\overline{PWC0}/\overline{PWC1}$ to $\overline{PERR0}$, $\overline{PERR1}$	t_{PWPEN}		10	18	ns
Delay Time from $\overline{PWC0}/\overline{PWC1}$ to $\overline{PERR}$	t_{PWPER}		12	22	ns
Enable Time of MD from $\overline{BSCNT}$	t_{BCMDZE}		20	35	ns
Delay Time from $\overline{SLE}$ to STCB	t_{SLEST}[1]		23	37	ns
Enable Time of STCB from $\overline{EN}$	t_{STZE}[1]		15	24	ns
RCLK Set Up Time referenced to $\overline{SLE}$	t_{SSL}[1]	44			ns
Delay Time from MD to CD	t_{MDCDTH}[2]		21	34	ns
Delay Time from MD to P0, P1	t_{MDPTH}[2]		28	48	ns
Delay Time from CB to STCB	t_{CBSTTH}[2]		18	30	ns
RCLK Set Up Time referenced to $\overline{PWC0}$, $\overline{PWC1}$	t_{CKS}[3]	57			ns
$\overline{PWC0}$, $\overline{PWC1}$ Set Up Time referenced to $\overline{BSCNT}$	t_{SBC}[3]	10			ns
Delay Time from PWC0/PWC1 to CD	t_{SCD}[3]		15	26	ns

AC CHARACTERISTICS (continued)

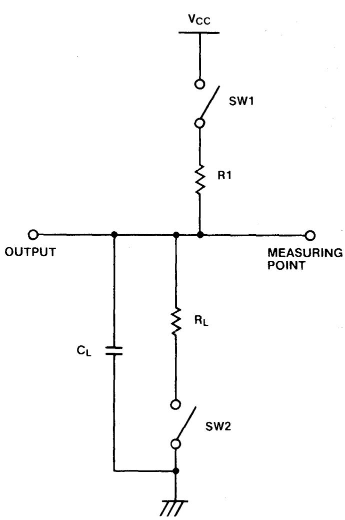
(Recommended operating conditions and AC test conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RCLK Pulse Width	t_{WCK}	20			ns
RST Pulse Width	t_{WRST}	20			ns
SLE Pulse Width	WSLE	20			ns

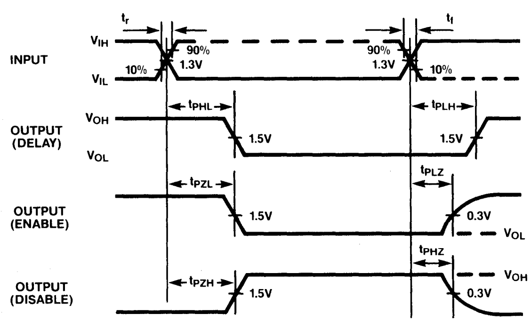
Notes:
1. Syndrome Latch
2. ECC-Through Mode
3. Partial Write Mode

AC TEST CONDITONS

Output Load:



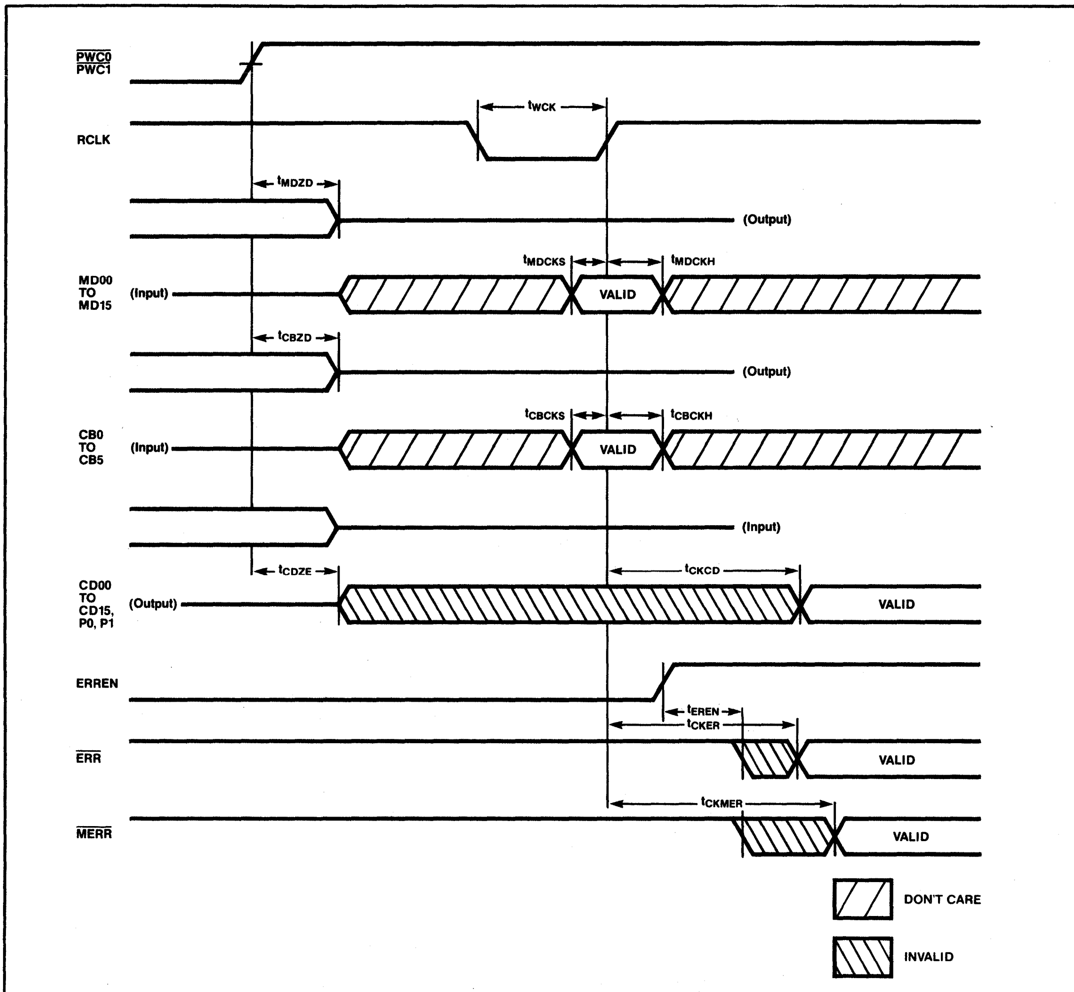
Timing Waveform:



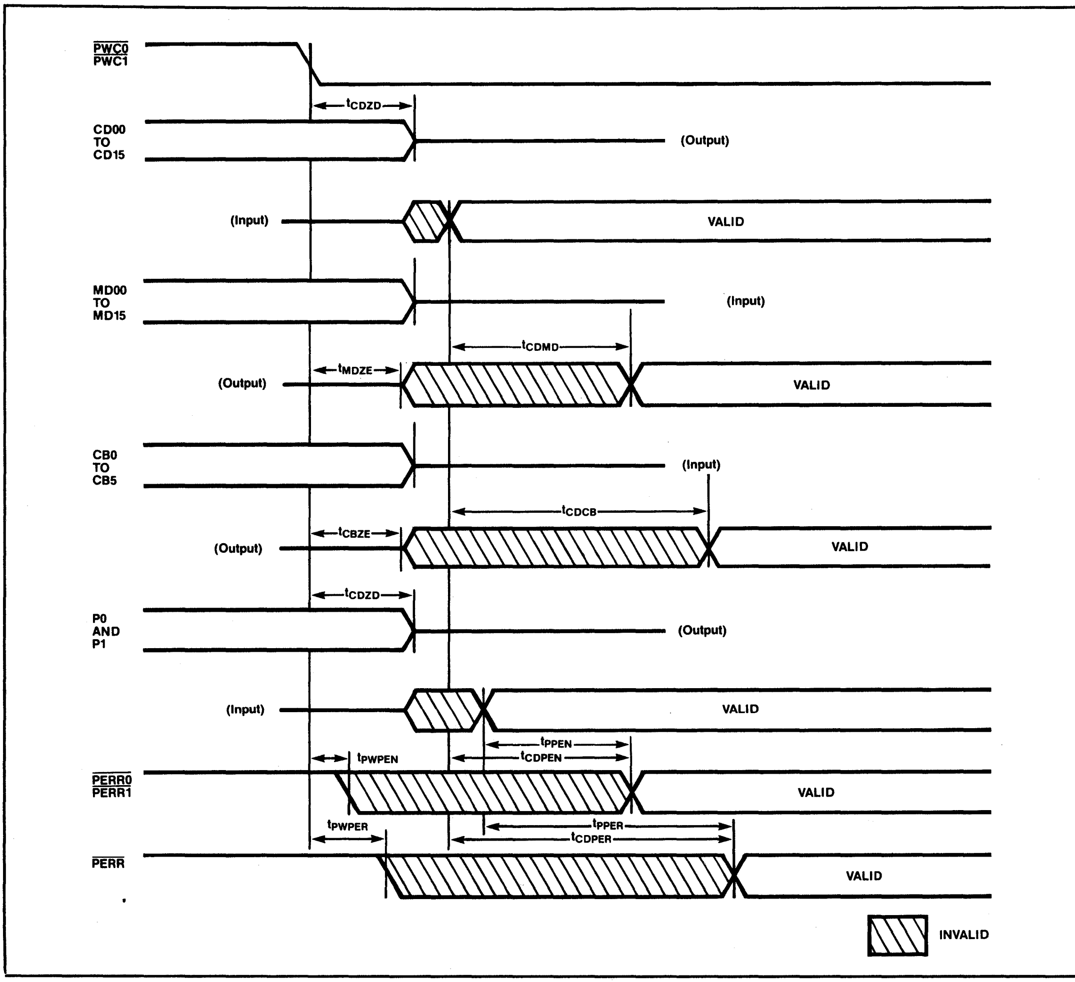
V_{IH} = 3V, V_{IL} = 0V, tr = 10ns, tf = 5ns

Parameter	Symbol	RL(Ω)	R1(Ω)	CL(pF)	SW1	SW2
Delay Time	t_{PLH} t_{PHL}	1.0K	—	50	Off	On
Enable Time	t_{PLZ} t_{PHZ}	1.0K	0.5K	5	On Off	On On
Disable Time	t_{PZL} t_{PZH}	1.0K	0.5K	50	On Off	On On

TIMING DIAGRAMS
Read Mode



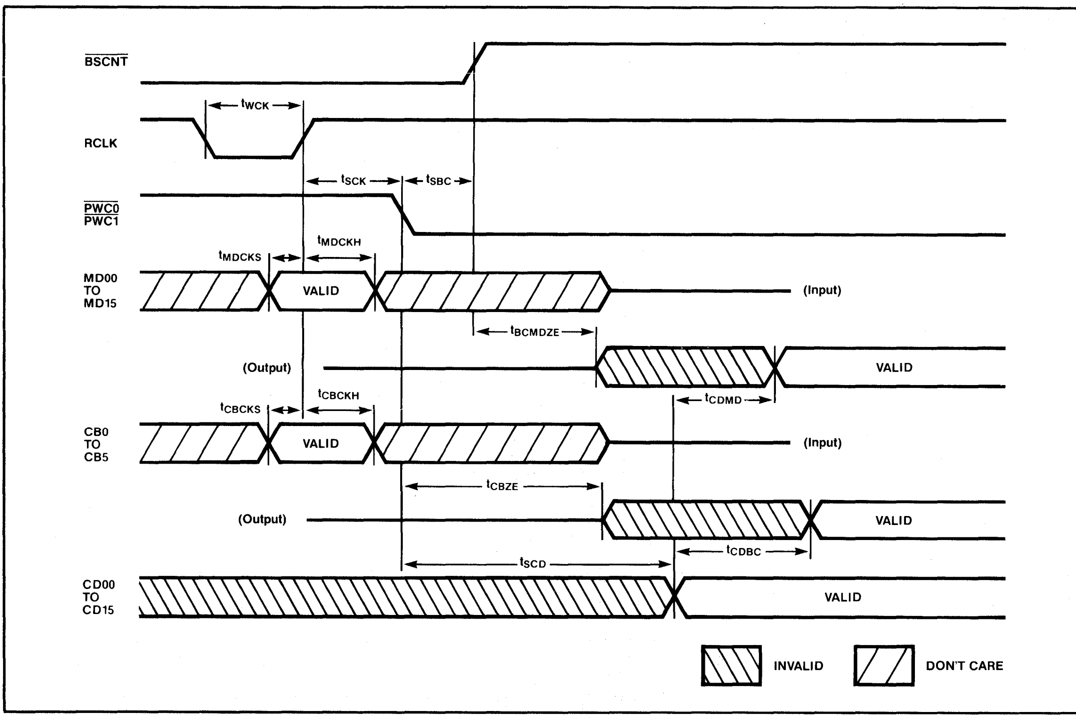
TIMING DIAGRAMS (continued)
Write Mode (Word Write)



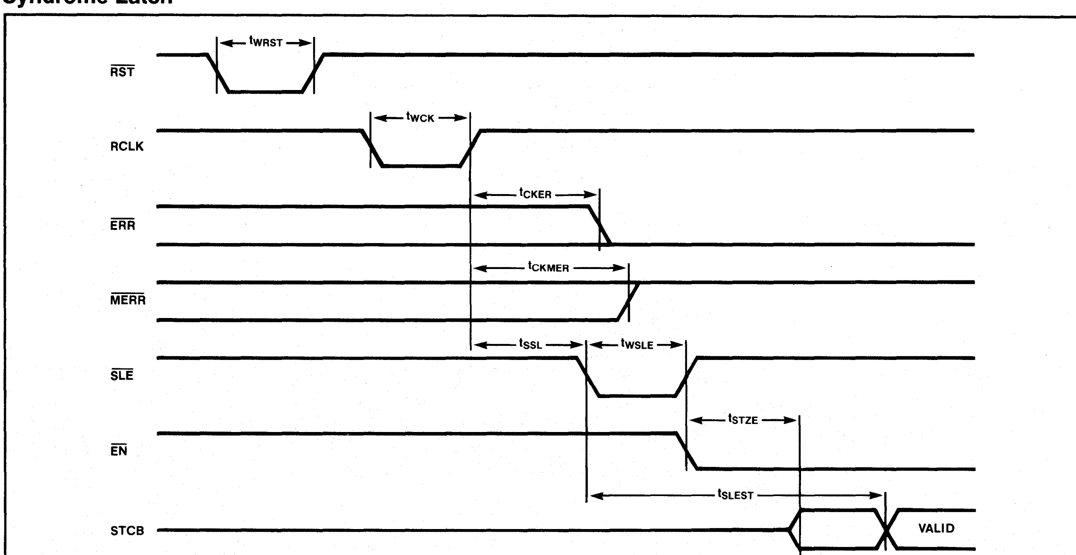
3

TIMING DIAGRAMS (continued)

Partial Write Mode (Byte Write)

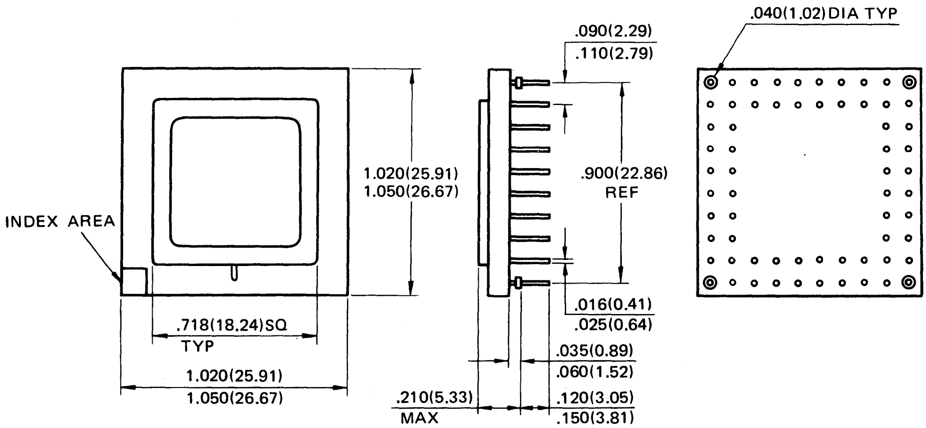


Syndrome Latch



PACKAGE DIMENSIONS

64-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
(PGA-64C-A01)



Dimensions in
inches (millimeters)