Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

MB1509

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 400MHz PRESCALER

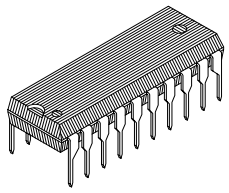
The Fujitsu MB1509 is a 400MHz dual serial input PLL (Phase Locked) frequency synthesizer designed for cordless telephone application.

The MB1509 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

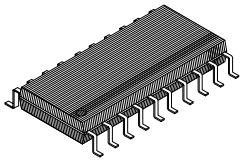
The MB1509 incorporates two 400 MHz dual modulus prescalers to enable implemention of a pulse swallow function.

It operates supply voltage of 3.0V typ. and dissipates 8mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 400MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 8mA typ, @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin dual in line package (Suffix: -P)
  Plastic 20-pin flat package (Suffix: -PF)

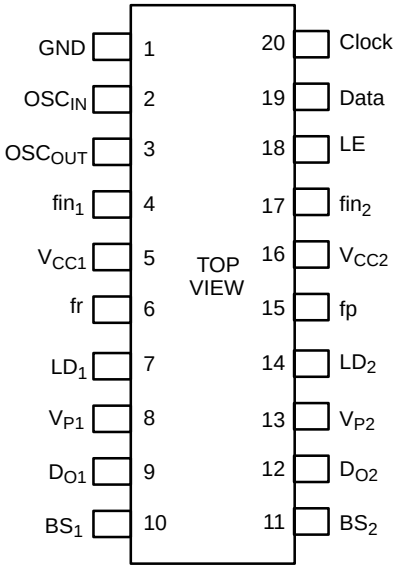


PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



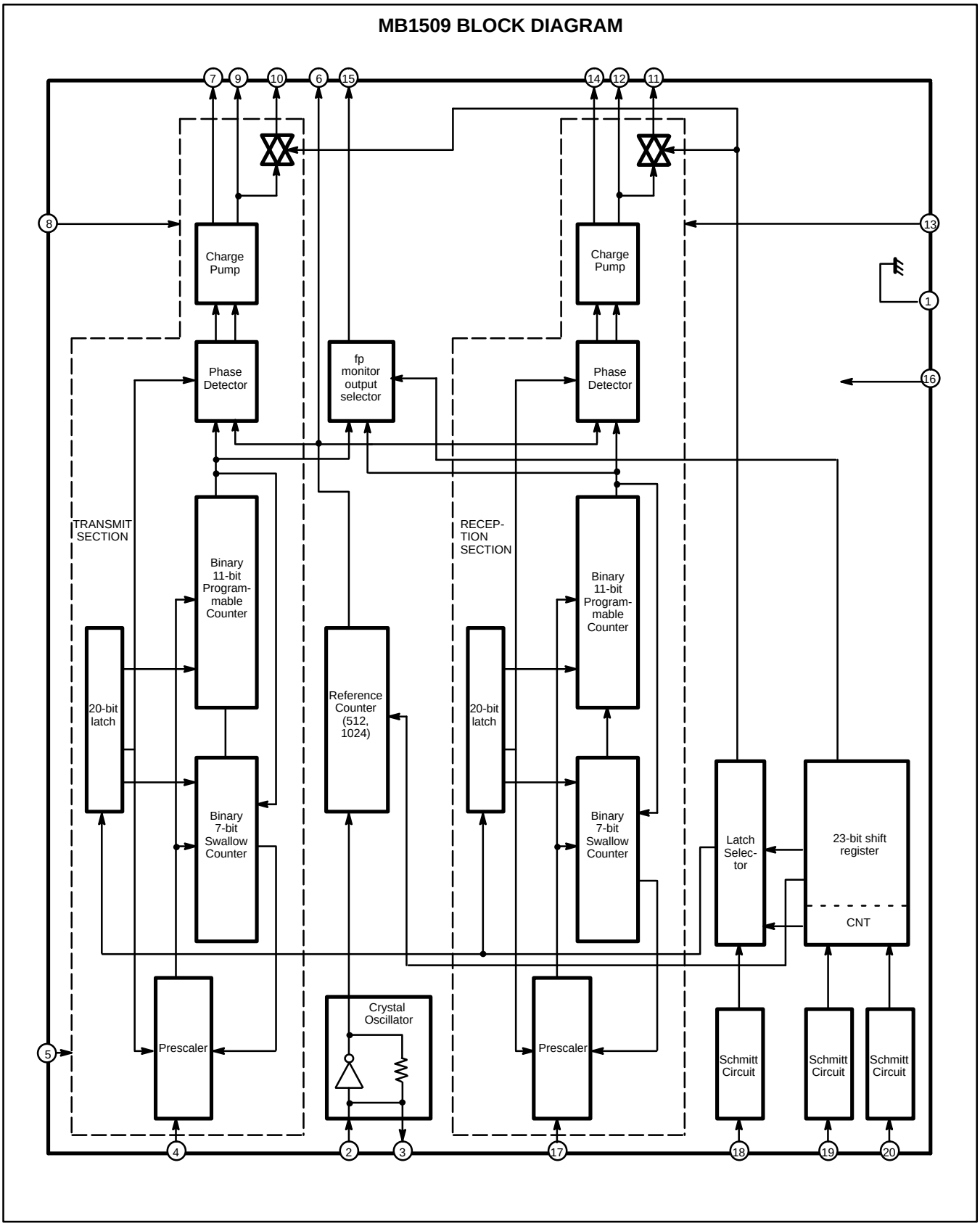
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1509 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 400MHz dual modulus prescaler (Divide ratio: 32/33, 64/65)
- Charge pump

COMMON BLOCK

- 23-bit shift register
- Programmable divider consisting of:
  Reference counter (Divide ratio: 512, 1024)
  (Divide frequency = 25kHz, 12.5kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fin_1</td><td>I</td><td>Prescaler input pin of transmit section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>–</td><td>Power supply voltage input pin of transmit section.
When power is OFF, latched data of transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output.</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section.
<table><tr><td>Condition</td><td>LD pin output level</td></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of transmit section.</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of reception section.</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section.
<table><tr><td>Condition</td><td>LD pin output level</td></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output.
This pin outputs divided frequency of transmit section or reception section depending upon FP bit setting.
<table><tr><td>FP bit</td><td>Output</td></tr><tr><td>H</td><td>Transmit section (fp1)</td></tr><tr><td>L</td><td>Reception section (fp2)</td></tr></table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of reception section and reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section. The connection with VCO should be AC conneciton.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog swith becomes ON.
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmit section or reception section depending upon a control data. Control bit data: H → Latch of transmit section; L → Latch of reception section
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

M: Preset divide ratio of dual modulus prescaler (32 or 64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (512 or 1024)

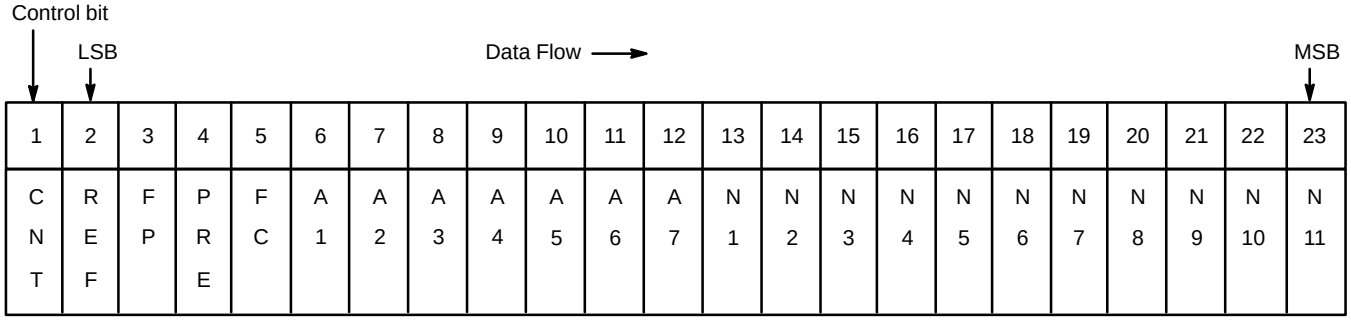
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of transmit section and programmable divider of reception section are controlled individually.
Serial data of binary data is input into Data pin.
On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of transmit section or the latch of reception section depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of transmit section
L	Latch of reception section

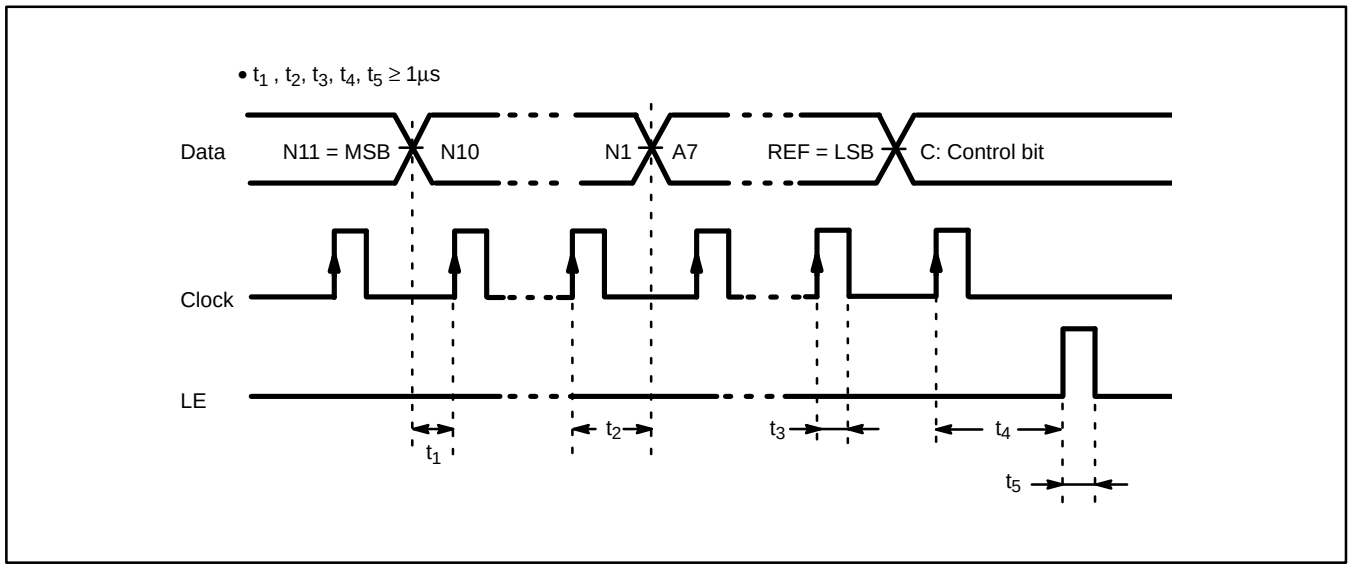
SHIFT REGISTER CONFIGURATION



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	REF	FP	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
PRE : Divide ratio of the prescaler setting bit (32/33 or 64/65)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CNT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the clock shifts one bit of the data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

PRE : DIVIDE RATIO (P) OF THE PRESCALER SETTING BIT
H = 32/33
L = 64/65

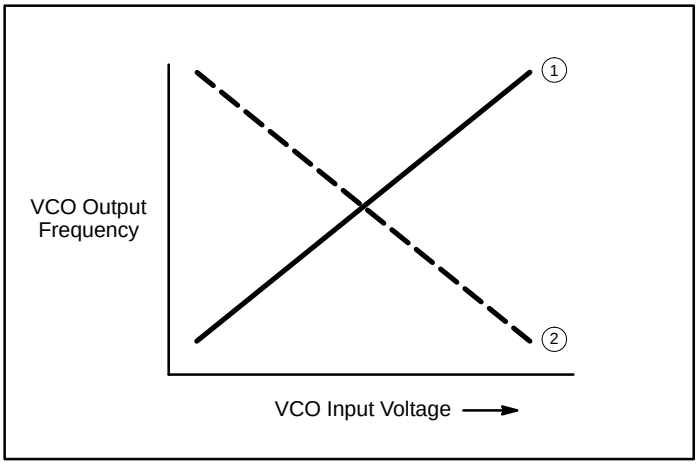
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 512 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section.

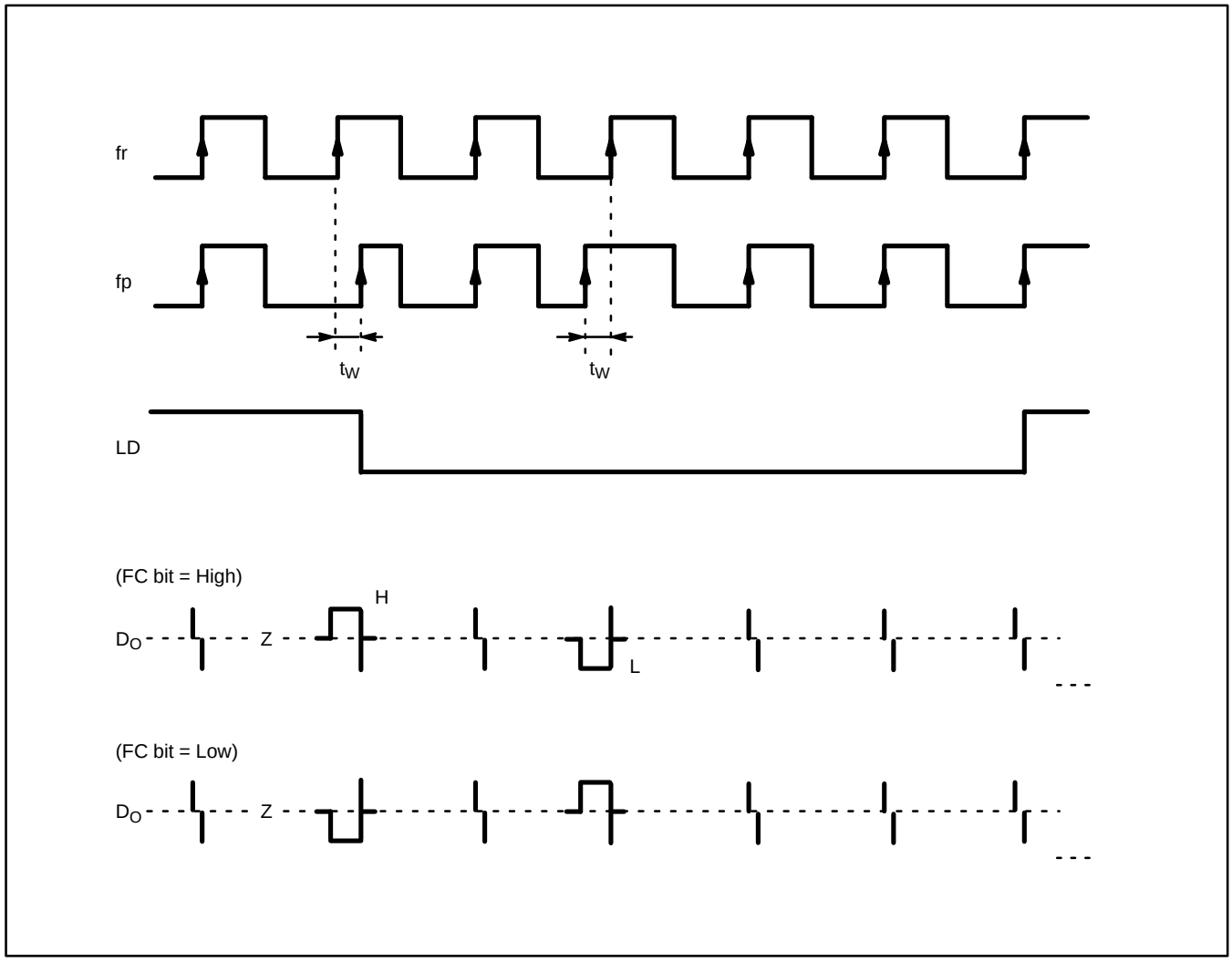
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO poratity, FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



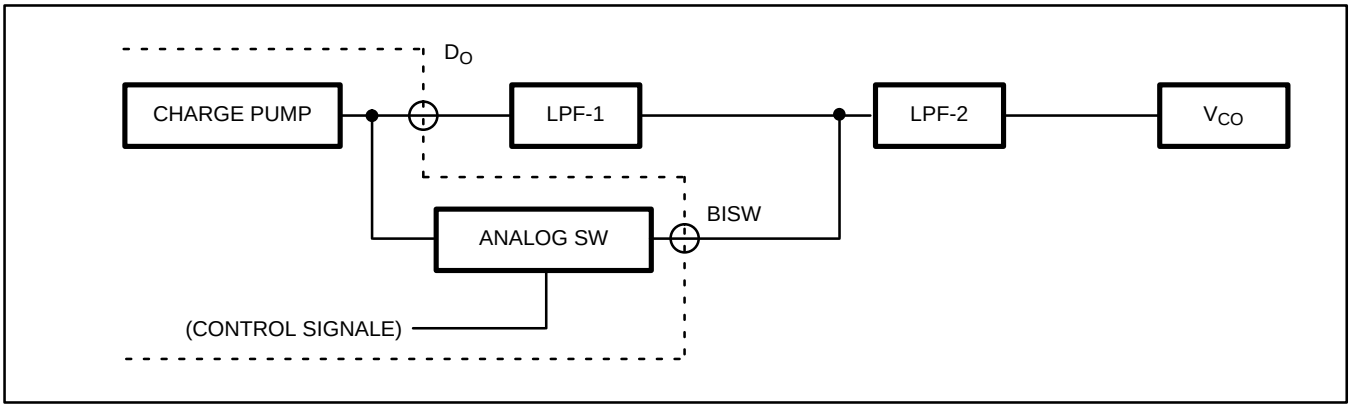
Note:
- Phase difference detection range = –2π to +2π
- LD output becomes low when phase difference is t_W or more.
  LD output becomes high when phase difference less than t_W is reperated 3 times or more.
  (e. g. t_W = 625 to 1250 ns, foscin = 12.8 MHz)
- Spike apperance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending up the VCO characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pin output the charge pump output (D_{01}, D_{02}). When analog switch is OFF, BS pin is set to high impedance.

	Control data = H Divide ratio of transmit section is set		Control data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

When a analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	–	8.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	–40	–	+85	°C	

HANDLING PRECAUTIONS

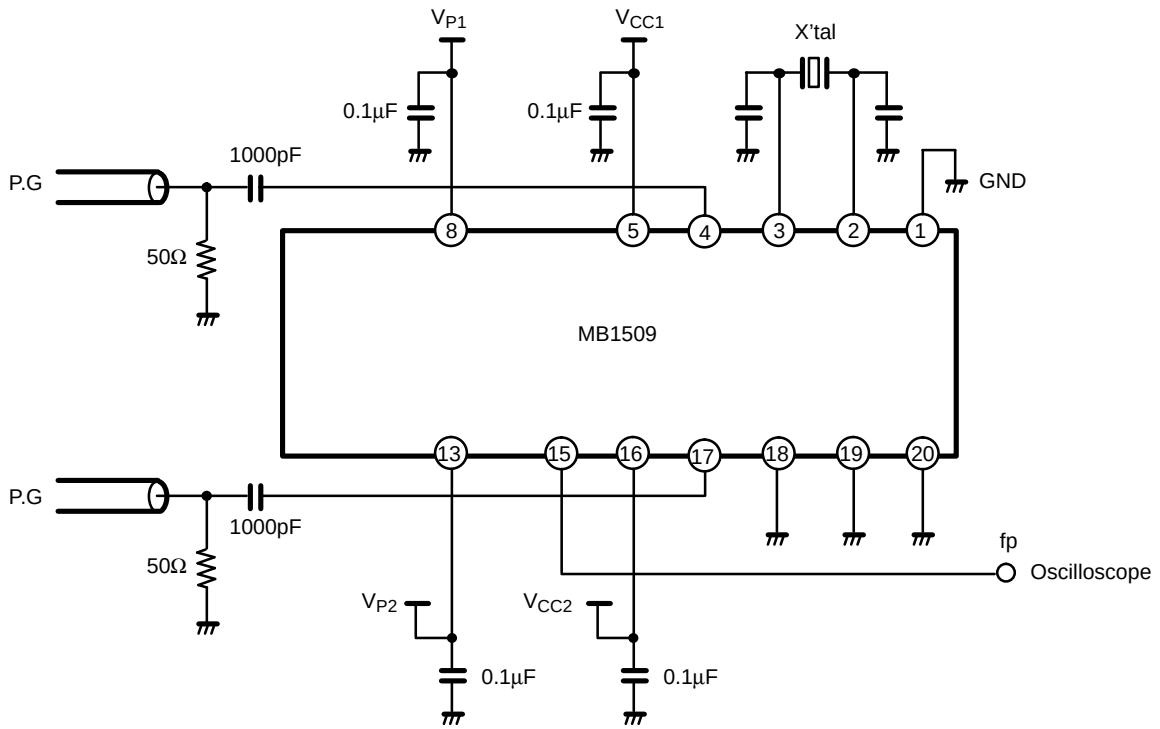
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

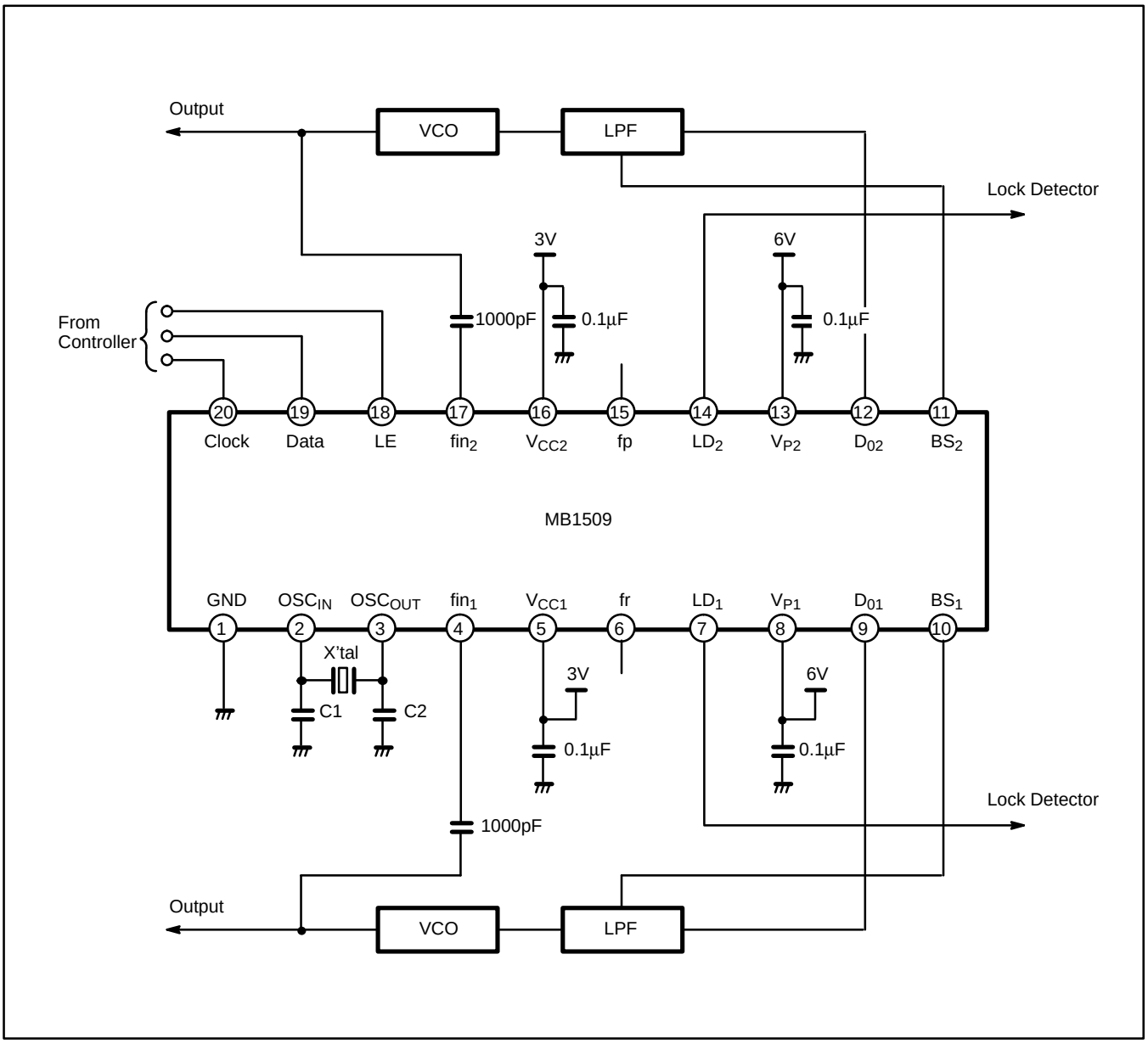
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current∗		I_{CC1}	Reception section is active.	–	4.0	–	mA
		I_{CC2}	Transmit/reception section are active.	–	8.0	12.0	
Operating Frequency∗∗	fin	fin1	P = 64/65	10	–	400	MHz
		fin2	P = 32/33	10	–	200	
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	Pfin	V_{CC} = 2.7 to 4.0V, 50Ω	–10	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	2	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High–level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High–level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High–impedance Cutoff Current	D_O	I_{OFF}	V_P = V_{CC} to 8.0V	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

Notes: ∗: fin = 400MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
∗∗: AC coupling. Minimum operating frequency is measured with capacitor 1000pF.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



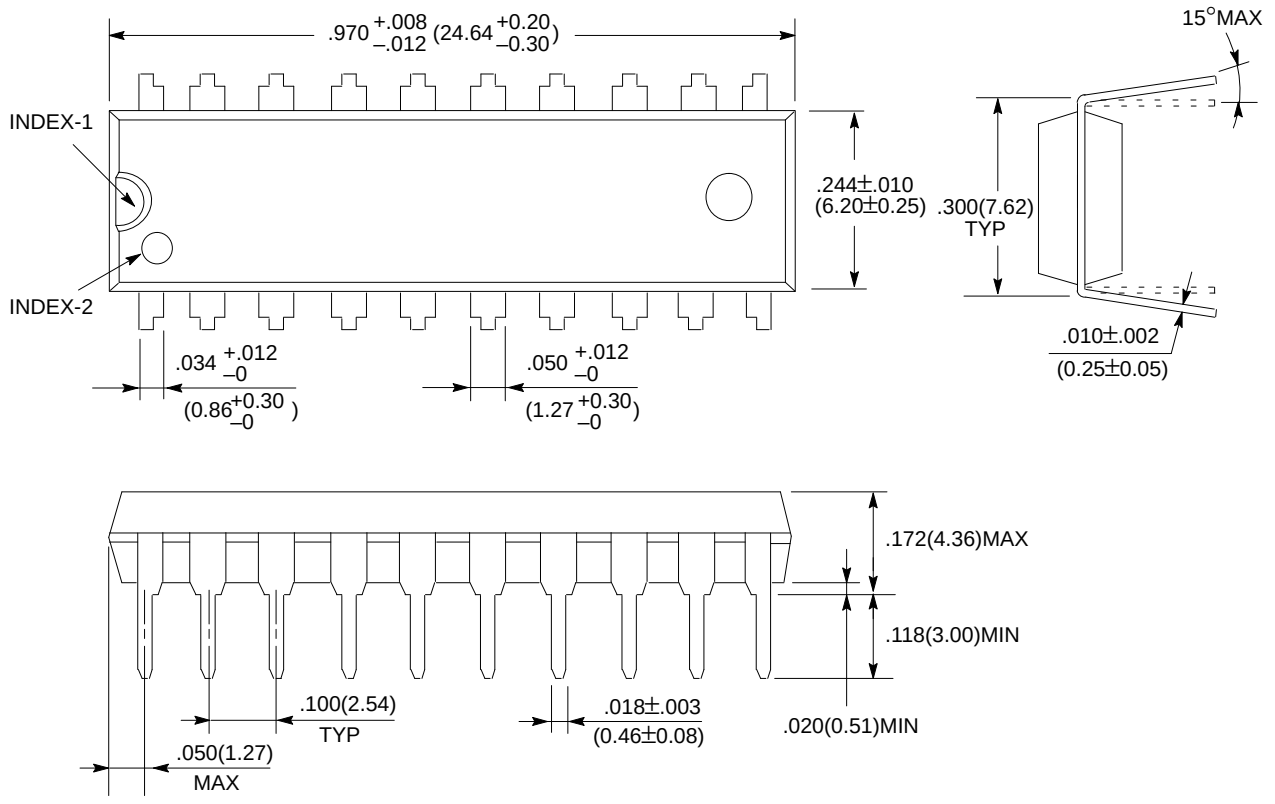
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8 V max.
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : involve the schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

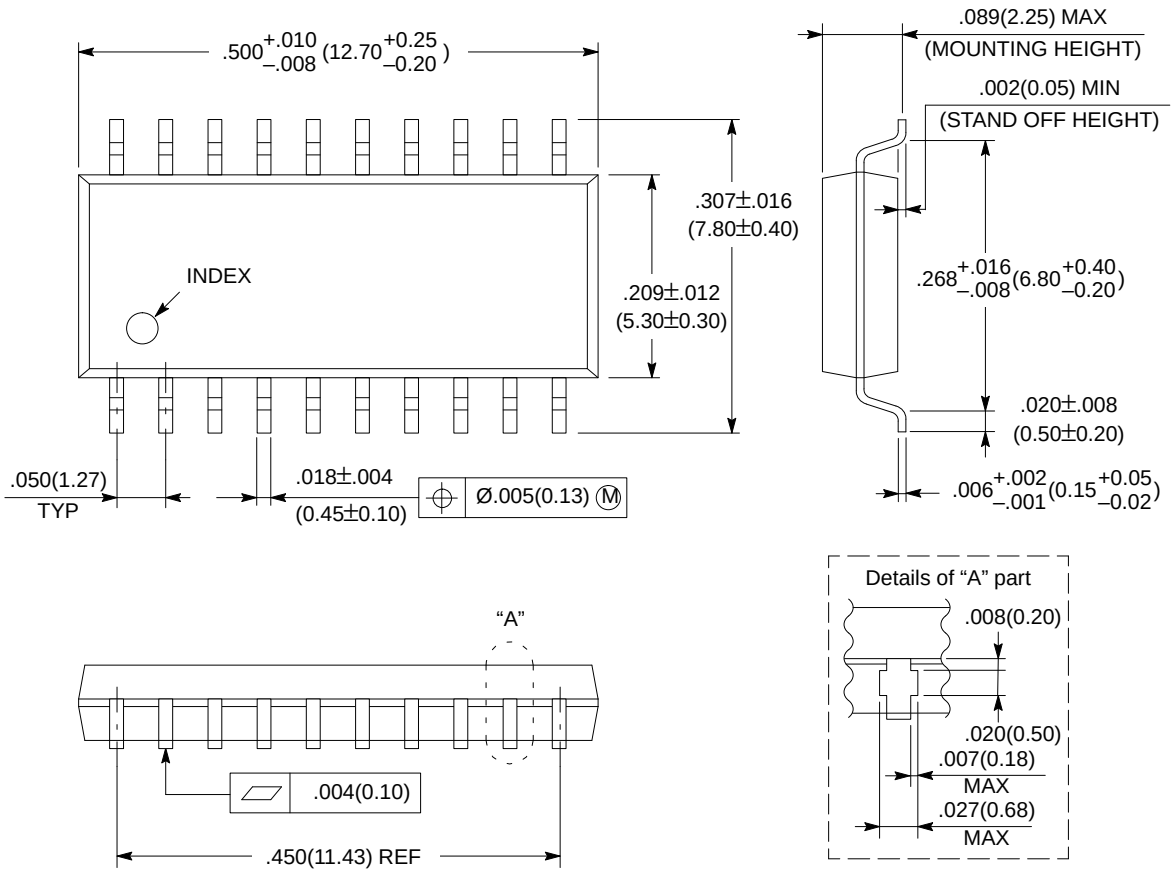
20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Dimensions in
inches (millimeters)

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