DS04–21316–1E

FUJITSU

DATA SHEET

MB1513

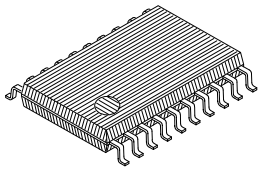
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTIONS (1.1GHz)

The Fujitsu MB1513 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.

The MB1513 is configured of a 1.1 GHz dual-modulus prescaler with selectable 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and an intermittent operation control circuit that selects the stand-by or operating mode depending on the power-save control input state (PS).

The MB1513 operates from a single +5 V supply. Fujitsu's advanced process technology achieves an I_{CC} of 8mA, typical. The stand-by mode current consumption is just 100µA.



PLASTIC PACKAGE
(FPT-20P-M03)

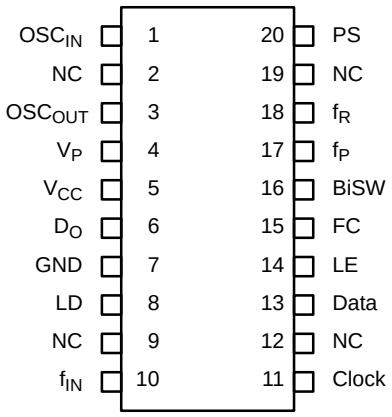
FEATURES

- High operating frequency : f_{IN} = 1.1GHz (V_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modulus prescaler with selectable 128/129 divider ratio
- Low supply current : I_{CC} = 8 mA typ. at 5V
- Power-saving stand-by mode : 100µA typ.
- Serial input, 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter : 0 to 127
  – Binary 11-bit programmable counter : 16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  – Binary 14-bit programmable reference counter: 8 to 16,383
  – 1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lockup
- On-chip charge pump minimizes system component count
- Wide operating temperature range: –40 to +85°C
- Plastic 20–pin shrink small outline package (Suffix: PFV)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

(TOP VIEW)

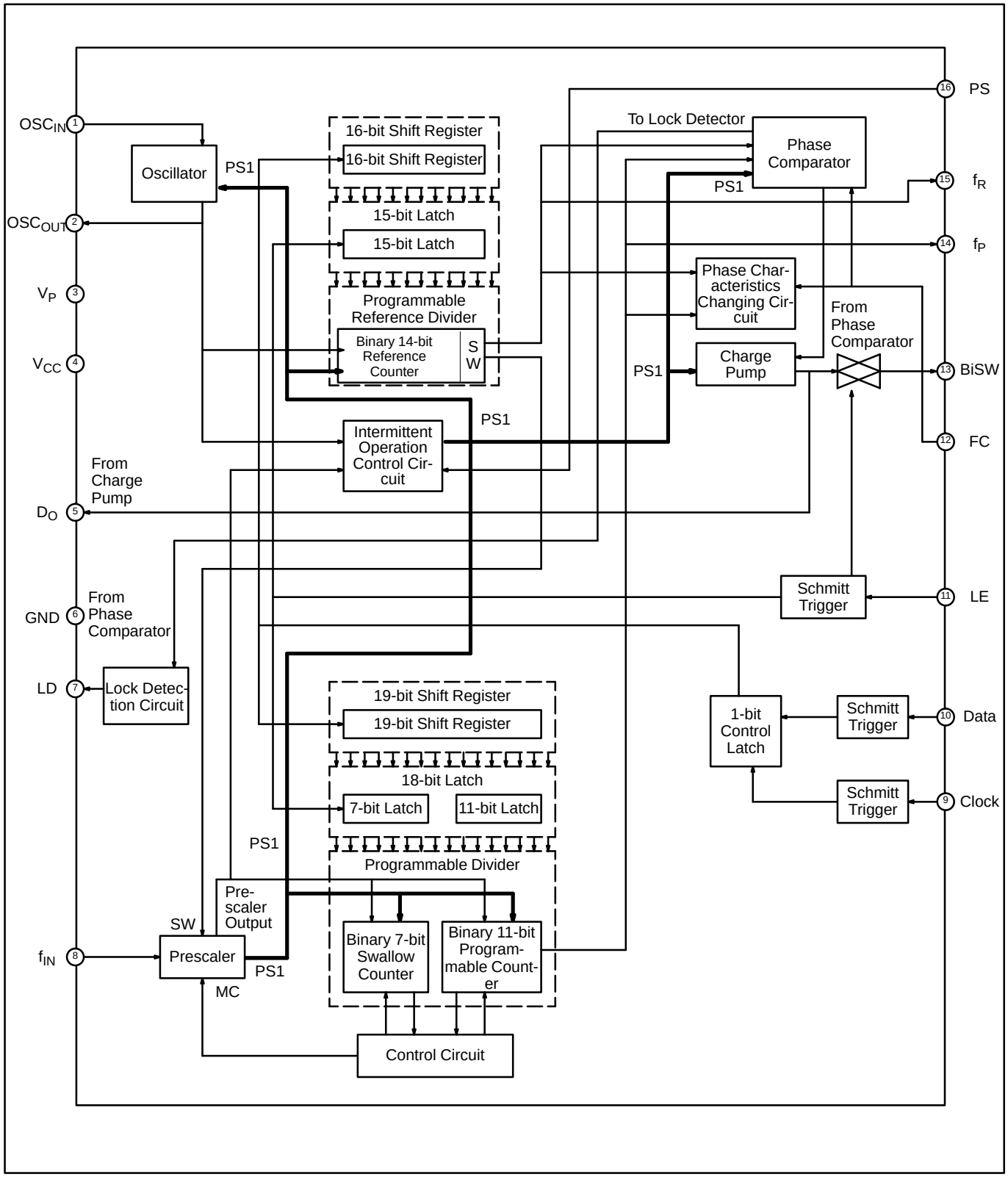


ABSOSUTE MAXIMUM RATINGS(See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	$V_{CC} \le V_P \le 10.0$	V
Output Voltage	V_O	–0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin.
2	NC	–	No connection
3	OSC_{OUT}	O	Oscillator output An external crystal is connected to this pin.
4	V_P	–	Power supply input for charge pump and analog switch
5	V_{CC}	–	Power supply
6	D_O	O	Charge pump output The phase of the charge pump is reversed depending on the FC input.
7	GND	–	Ground
8	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked.
9	NC	–	No connection
10	f_{IN}	I	Prescaler input An external VCO is AC-coupled to this pin.
11	Clock	I	Clock input for 19-bit and 16-bit shift registers One bit of data is shifted into the registers on the rising edge of the clock. A Schmitt trigger circuit is involved.
12	NC	–	No connection
13	Data	I	Binary serial data input The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 15-bit latch. When the control bit is low, data is transmitted to the 18-bit latch. A Schmitt trigger circuit is involved.
14	LE	I	Load enable signal input When LE is high, the contents of the shift register are transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin. A Schmitt trigger circuit is involved.
15	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and the phase comparator are reversed. The FC input signal is also used to control the fOUT pin (test pin) of f_R or f_P.
16	BiSW	O	Analog switch output Usually, BiSW is in the high-impedance state. When the switch is on (LE is high), the charge pump is connected to the BiSW pin.
17	f_P	O	Programmable counter output monitor pins
18	f_R	O	Reference counter output monitor pin
19	NC	–	No connection
20	PS	I	Power save signal input Set low when the system is operating (never use pin 20 as it is opened) PS = High : Operation mode PS = Low : Stand-by mode

FUNCTIONAL DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

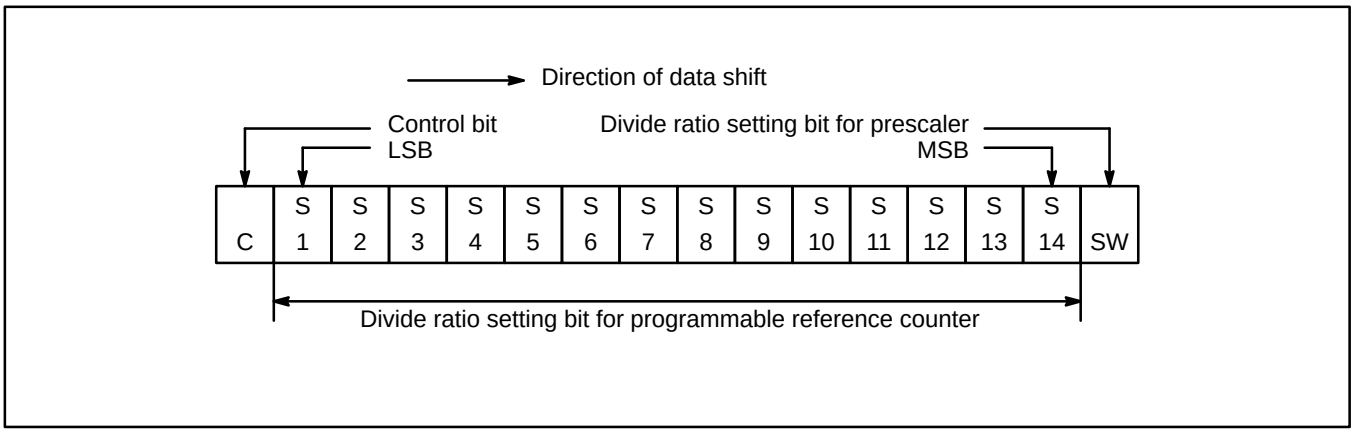
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of prescaler (128)

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched, depending on the control as follows:

Control Data	Destination of Serial Data
H	15-bit latch
L	18-bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The 16-bit serial data format is shown below:



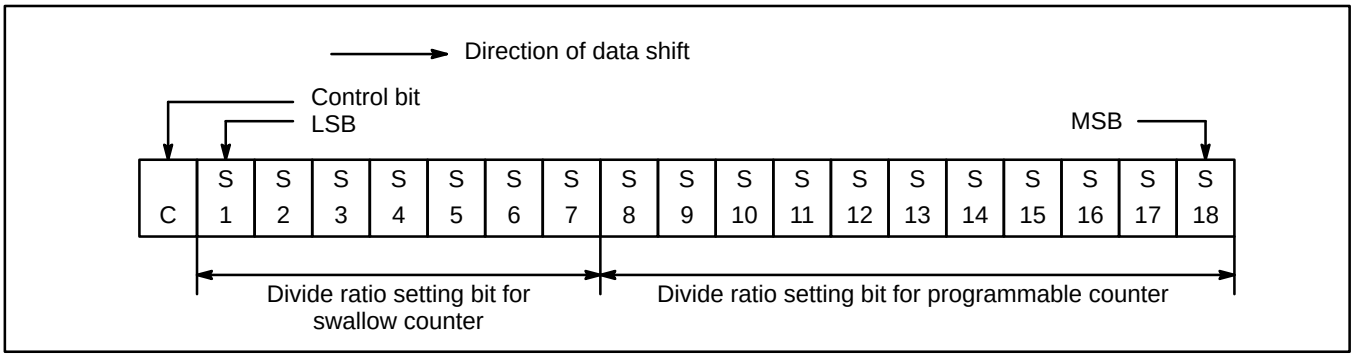
- 14-bit programmable reference counter divide ratio

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited
2. SW: This bit selects the divide ratio of the prescaler
   SW Low: 128 or 129
   (SW must be always be low.)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383)
4. C: Control bit: Set high
5. Data is input from the MSB.

(b) Programmable divider divide ratio
The programmable divider consists of a 19-bit shift register, 18-bit latch, 7-bit swallow counter, and an 11-bit programmable counter. The 19-bit serial data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

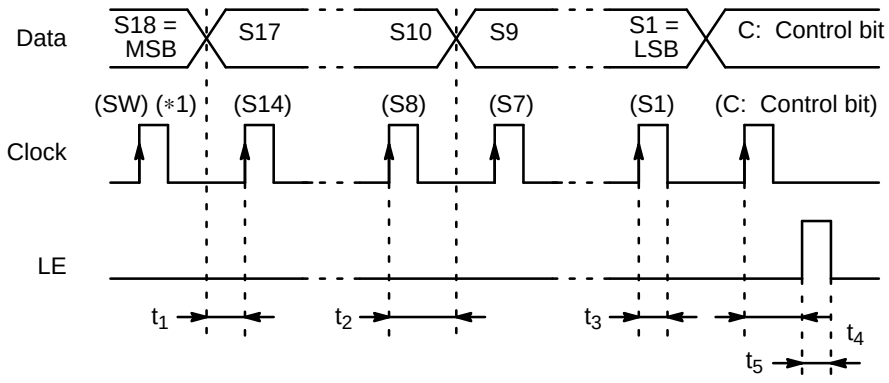
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 16 to 2,047)

Notes: 1. Divide ratios less than 16 are prohibited for 11–bit programmable counters
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127)
3. S8 to S18: These bits select the divide ratio of programmable counter (16 to 2,047)
4. C: Control bit: (Set low)
5. Data is input from the MSB.

Serial data input timing

- t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
  t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



∗1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or starting the internal circuits according to their necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost. To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting the phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enters the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS = High)
  All circuits are operating, and PLL operation is normal.
- Stand-by mode (PS = Low)
  Circuits that do not affect operation are powered-down to save power.
  The current in the power save state is typically 100µA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage-controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

Relationship between FC input and phase characteristics

The FC pin controls the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

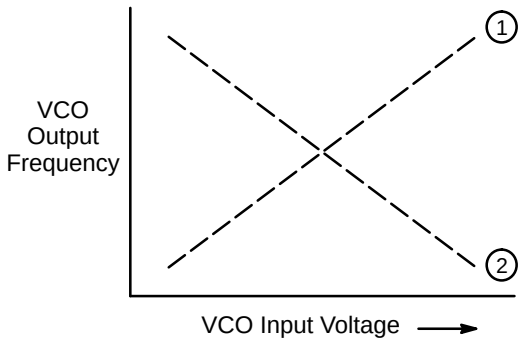
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (∗1)	Z (∗1)

∗1: High impedance

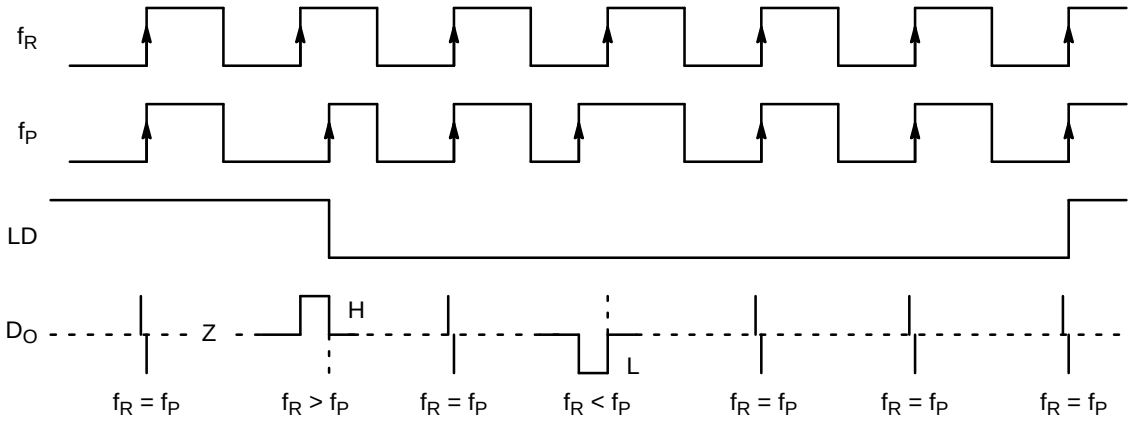
When designing a synthesizer, the FC pin setting depends on the VCO characteristics.

∗: When the VCO characteristics are similar to ① , set FC high or open.

∗: When the VCO characteristics are similar to ② , set FC low.



Phase comparator output waveform (FC = High)



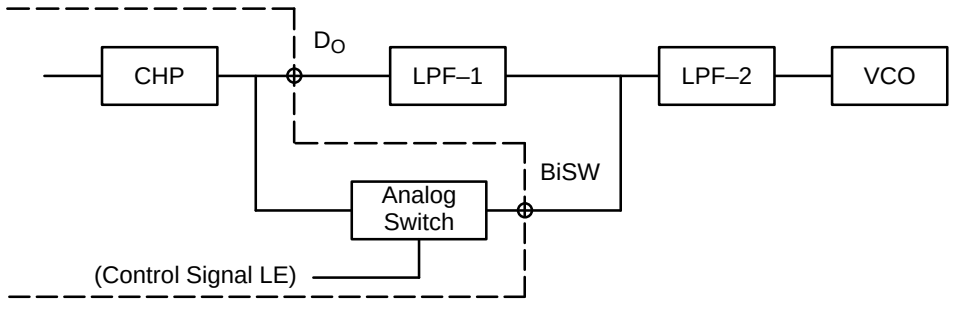
Notes:
1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. The spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, a spike might not appear, depending on the charge pump characteristics.
4. LD is low when the phase difference is tw or more. LD is high when the phase difference is tw or less for three or more continuous cycles (when f_{OSCIN} = 12.8 MHz, tw = 625 to 1,250 ns).

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (D_O) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$			V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

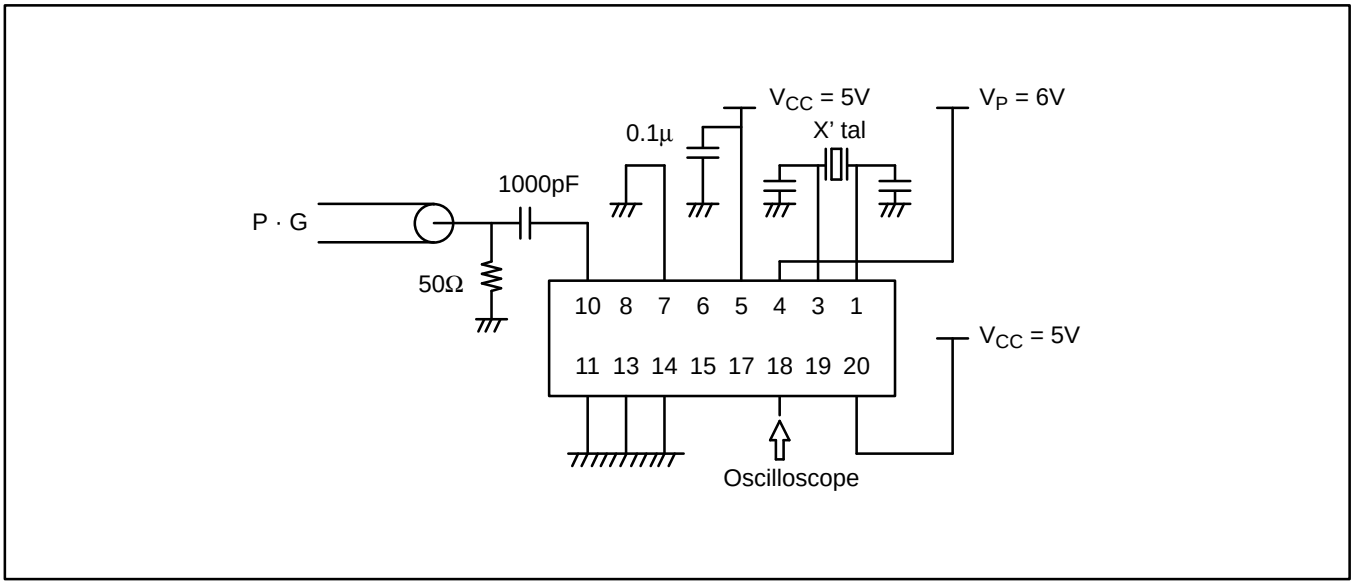
HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

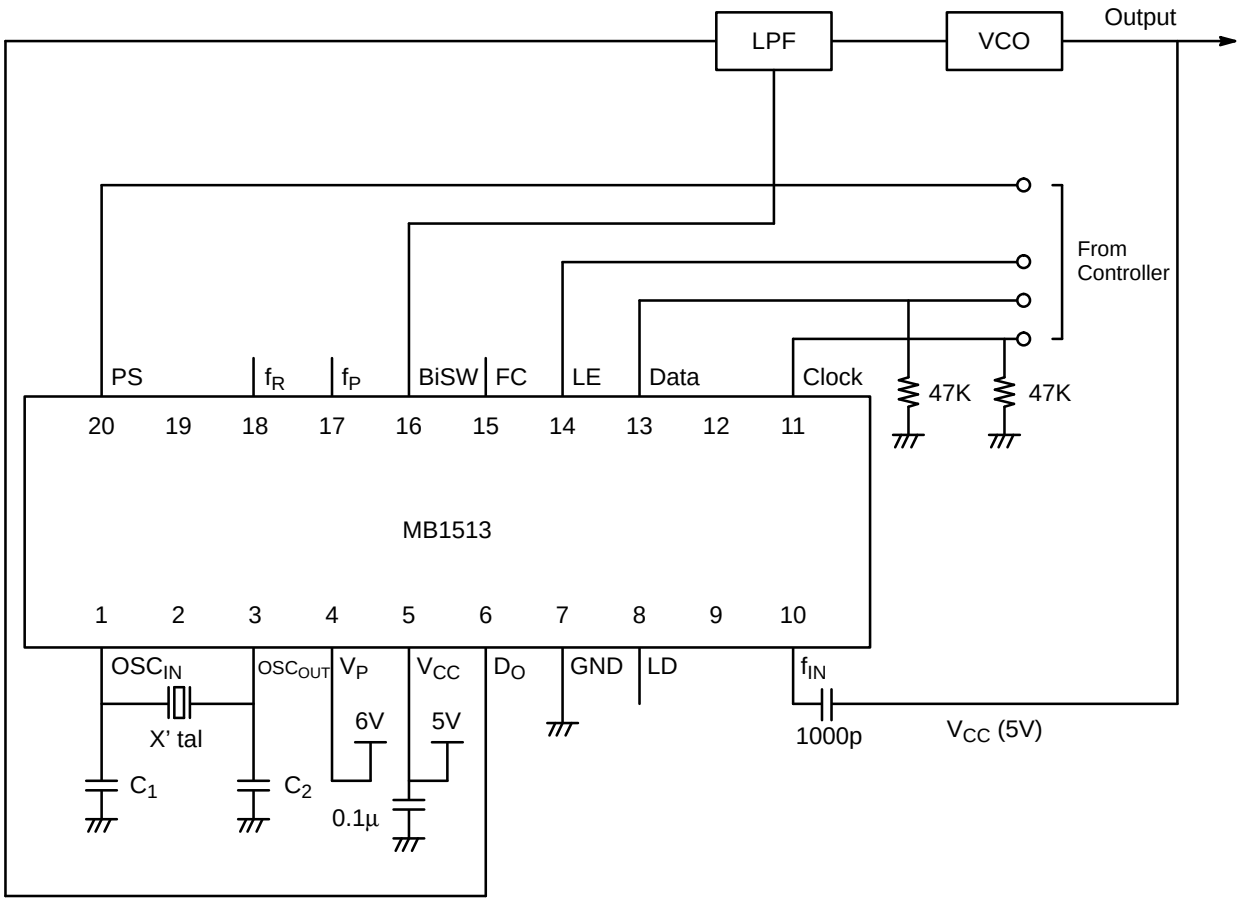
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply Current		I_{CC}	–	8.0	–	mA	With f_{IN} = 1.1GHz, OSC_{IN} = 12MHz, V_{CC} = 5.0V
Stand-by Current		IPS	–	100	–	µA	–
Operating Frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling.The minimum operating frequency is measured with a 1000pF capacitor connected
	OSC_{IN}	f_{OSC}	–	12	20	MHz	–
Input Sensitivity	f_{IN}	$V_{f\ IN}$	–10	–	6	dBm	–
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	–
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7+0.4	–	–	V	–
Low-level Input Voltage		V_{IL}	–	–	V_{CC} x 0.3–0.4	V	–
High-level Input Current	Data Clock LE	I_{IH}	–	1.0	–	µA	–
Low-level Input Current		I_{IL}	–	–1.0	–	µA	–
	FC	I_{FC}	–	–60	–	µA	–
Input Current	OSC_{IN}	I_{OSC}	–	±50	–	µA	–
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	–	–	V	V_{CC} = 5V
Low-level Output Voltage		V_{OL}	–	–	0.4	V	–
High-impedance Cut off Current	D_O	I_{OFF}	–	–	1.1	µA	V_{DO} = GND to 8V $V_{CC} \leq V_P \leq 8V$
Output Current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	–
		I_{OL}	1.0	–	–	mA	–
Analog Switch ON Resistance		R_{ON}	–	25	–	Ω	–

TEST CIRCUIT
(FOR MEASURING PRESCALER INPUT SENSITIVITY)



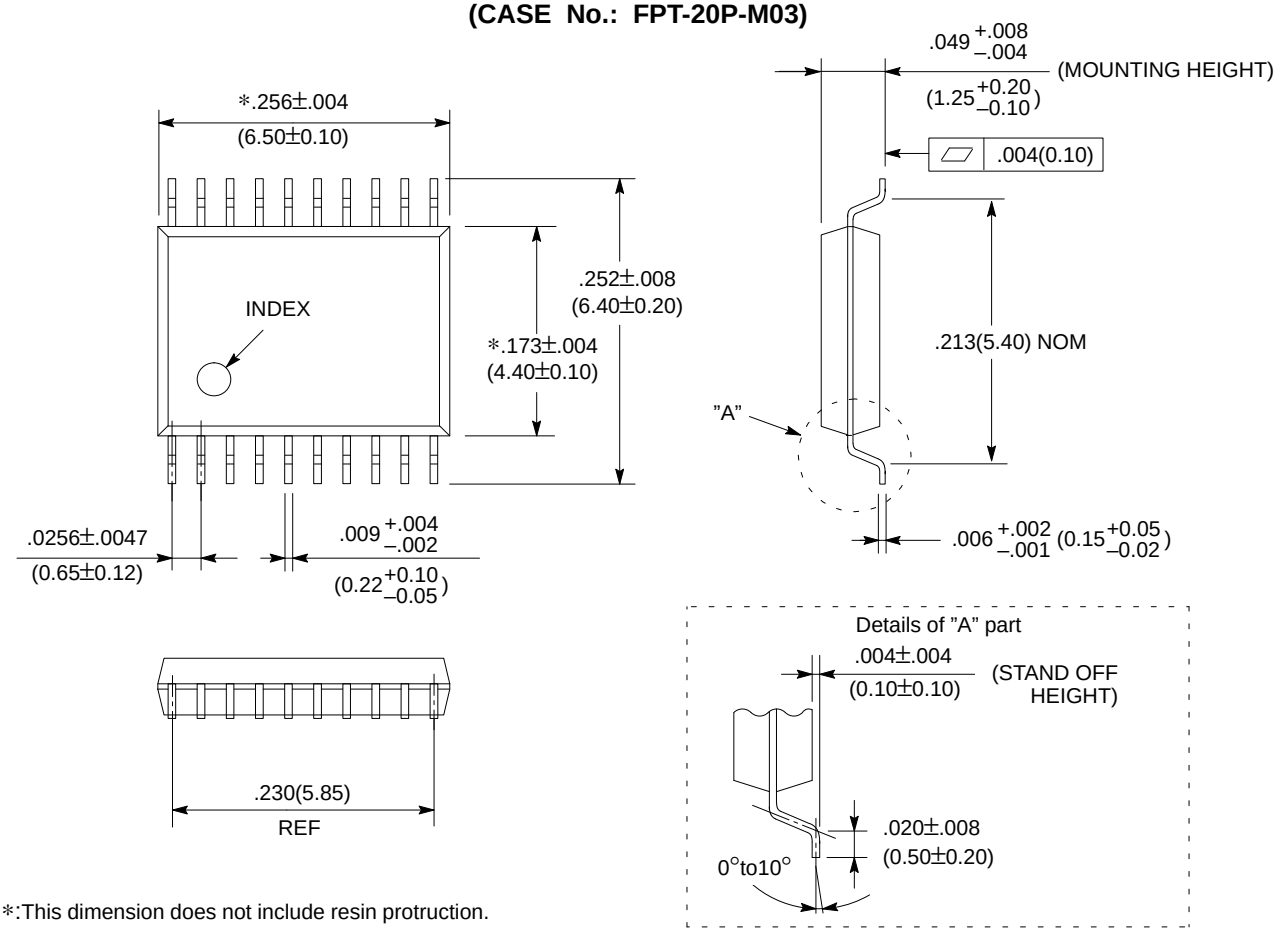
APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8V
C_1, C_2 : Depend on the crystal parameters

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)