DS04–21321–1aE

FUJITSU

DATA SHEET

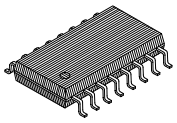
MB15A02 ASSP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

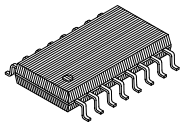
LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1GHZ PRESCALER

The Fujitsu MB15A02, utilizing Bi-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB15A02 contains a 1.1GHz two modulus prescaler that can select either a 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase reverse function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, and programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).
It operates supply voltage of 5V typ. and achieves very low supply current of 7mA typ. realized through the use of Fujitsu Advanced Process Technology.

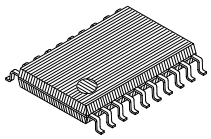
- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=–10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC}=7mA typ.
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  – Binary 14-bit programmable reference counter: 6 to 16,383
  – 1-bit switch counter (SW) sets divide ratio of prescaler
- Two types of phase detector output
  – On-chip charge pump (Bipolar type)
  – Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16–pin Plastic SOP Package
  16–pin and 20–pin Plastic SSOP Packages



PLASTIC PACKAGE
FPT-16P–M05



PLASTIC PACKAGE
FPT-16P–M06



PLASTIC PACKAGE
FPT-20P–M03

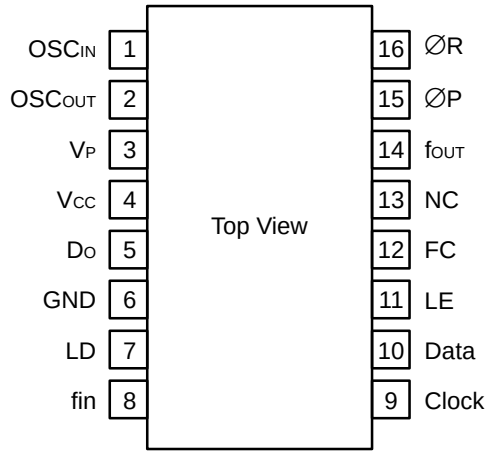
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V	
	V_P	V_{CC} to 8.0	V	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V	∅P pin
Open-drain Voltage	V_{OOP}	–0.5 to 6.0	V	
Output Current	I_{OUT}	±10	mA	
Storage Temperature	T_{STG}	–55 to +125	°C	

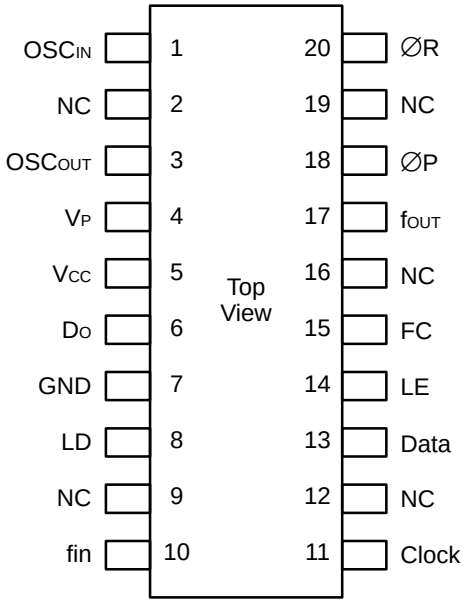
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

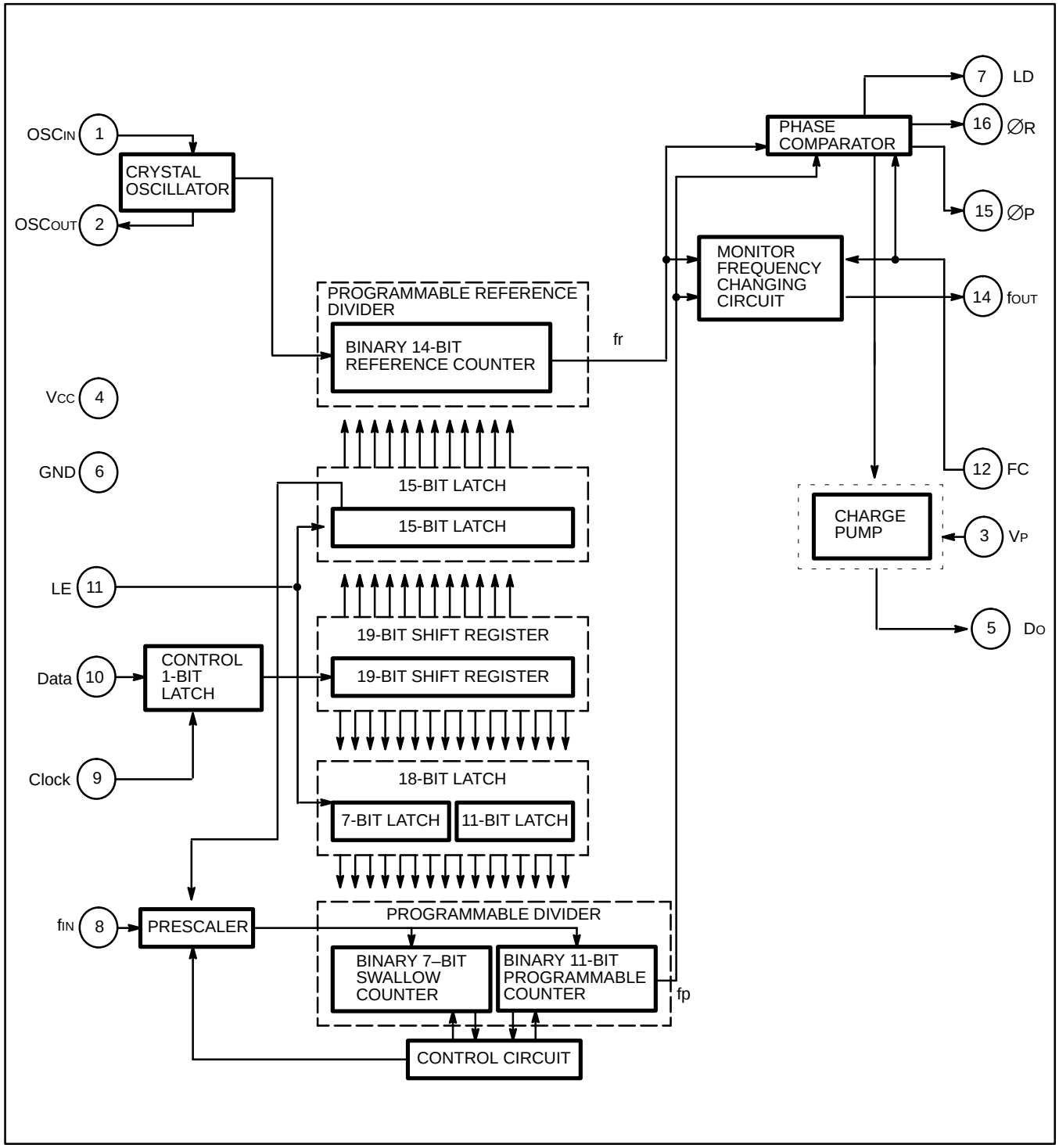


(FPT–16P–M06)
(FPT–16P–M05)



(FPT–20P–M03)

BLOCK DIAGRAM



Note : Pin numbers are based on SOP/SSOP 16–pin packages.

PIN DESCRIPTION

Pin No.		Pin Name	I/O	Description
SOP–16P SSOP–16P	SSOP–20P			
1 2	1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	4	V_P	–	Power supply pin for charge pump. When the internal charge pump is not used, V_P pin needs to be connected to V_{CC}.
4	5	V_{CC}	–	Power supply pin.
5	6	D_O	O	Charge pump output.
6	7	GND	–	Ground.
7	8	LD	O	Phase comparator output. Normally this pin outputs high level. When there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into shift register.
10	13	Data	I	Binary serial data input. The last bit of data is a control bit. When this bit is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	14	LE	I	Load enable input (with internal pull up resistor). When LE is high, the data stored in shift register is transferred into latch according to the control bit.
12	15	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of phase comparator is reversed. FC input signal is also used to select fout pin (test pin) output, fr or fp.
13	2,9,12,16,19	NC	–	No connection
14	17	f_{OUT}	O	Minitor pin of phase comparator input. fout pin outputs either programmable reference divider output (fr) or programmable divider output (fp) according to FC pin input level. FC=H: It is the same as fr output level. FC=L: It is the same as fp output level.
15	18	∅P	O	Outputs for external charge pump. The characteristics are reversed according to FC input. ∅P pin is N-channel open drain output.
16	20	∅R	O	Outputs for external charge pump. ∅R pin is CMOS output.

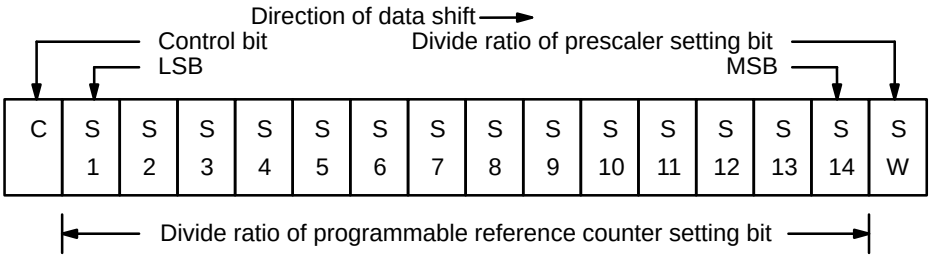
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift register and when load enable pin is high level or open, stored data is transferred into latch according to the control bit.
Control data ”H” data is transferred into 15-bit latch.
Control data ”L” data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit programmable reference counter. Serial 16-bit data format is shown below.



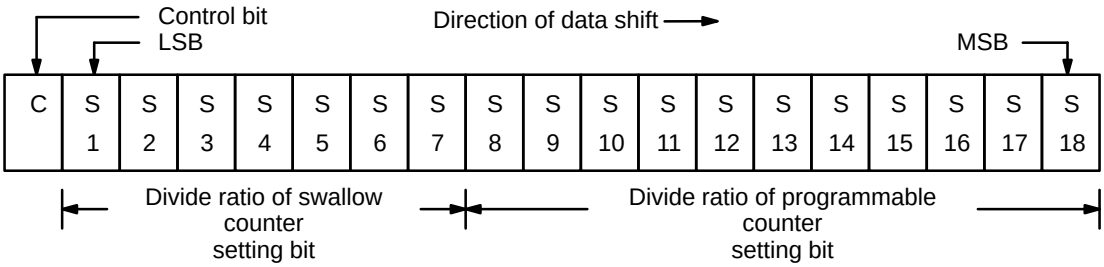
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 6 is prohibited.
Divide ratio: 6 to 16,383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets at high level).
Start data input with MSB first.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2,047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit.
C: Control bit (sets at low level).
Data input with MSB first.

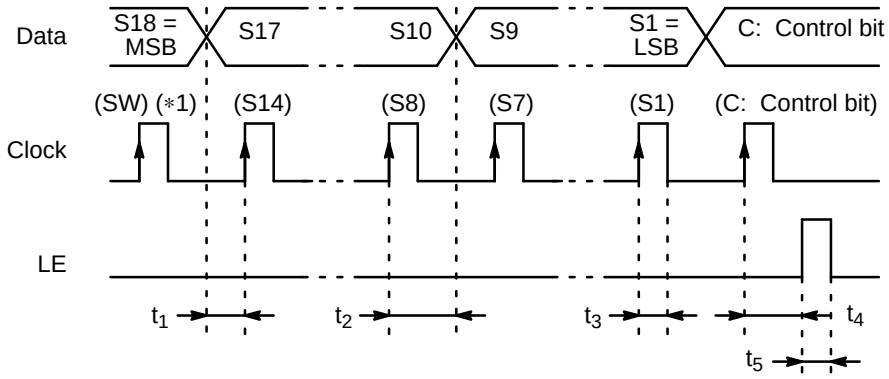
PULSE SWALLOW FUNCTION

$f_{VCO} = [(PxN)+A] \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (6 to16,383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

Serial data input timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 800ns) : LE pulse width



∗1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

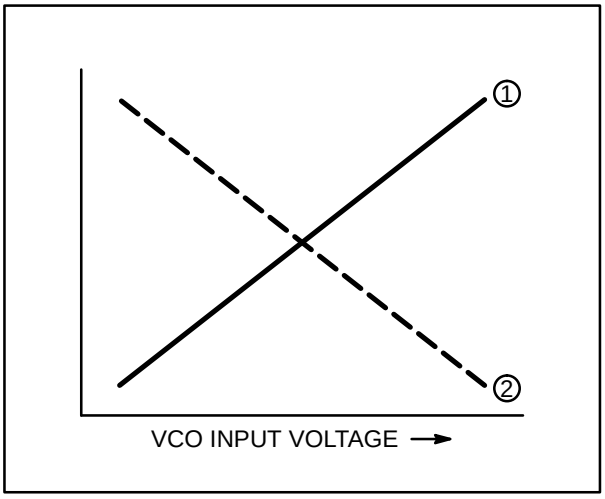
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (∅R, ∅P) are reversed depending upon FC pin input level. Also, monitor pin (fout) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ∅R, ∅P) and FC input level are shown below.

	FC=H or open				FC=L			
	DO	**∅R**	**∅P**	**fout**	**DO**	**∅R**	**∅P**	**fout**
fr>fp	H	L	L	(fr)	L	H	Z	(fp)
fr<fp	L	H	Z	(fr)	H	L	L	(fp)
fr=fp	Z	L	Z	(fr)	Z	L	Z	(fp)

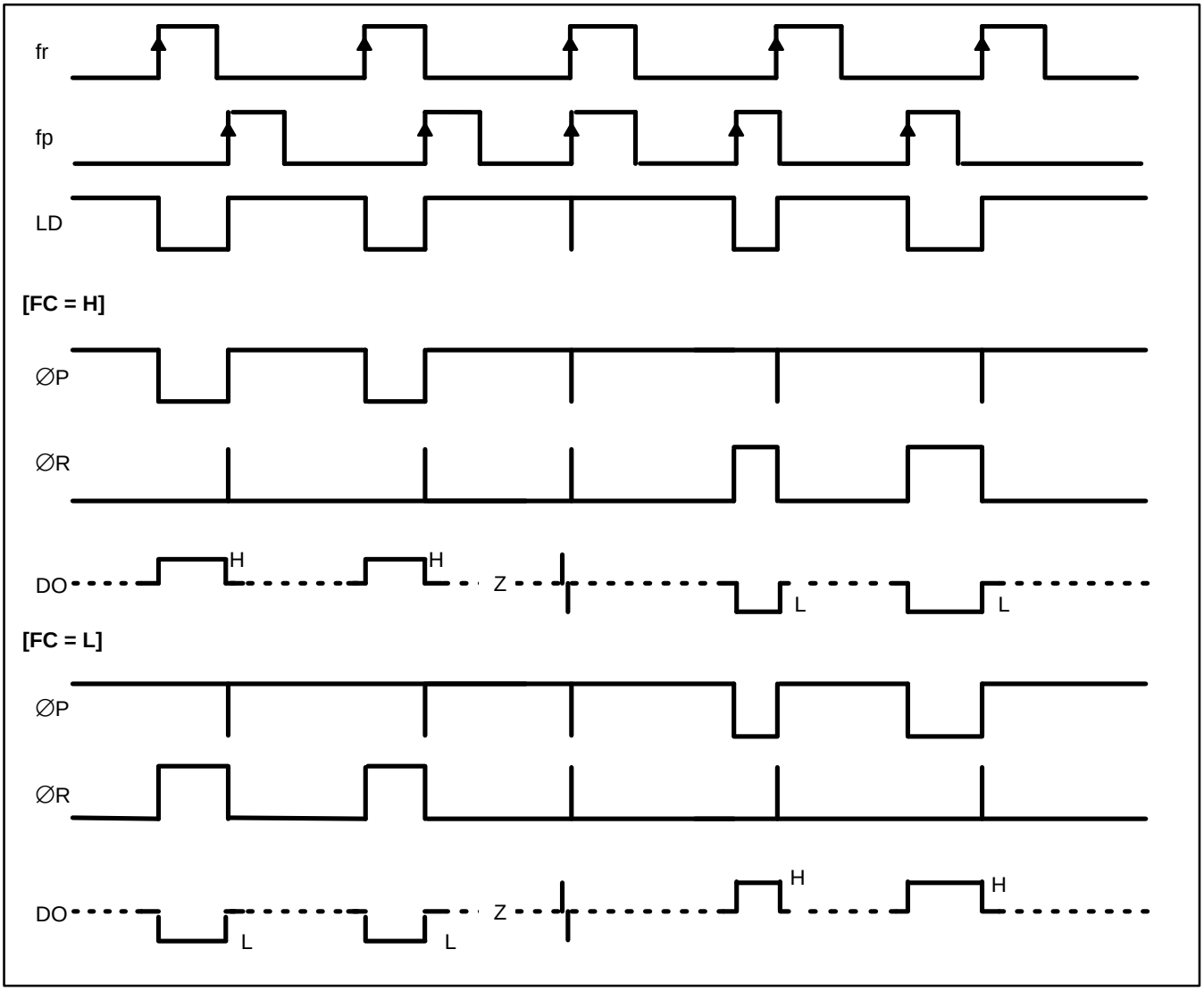
Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.

OUTPUT WAVEFORM



NOTE: Phase error detection range: –2π to +2π

RECOMMENDED OPERATING CONDITIONS

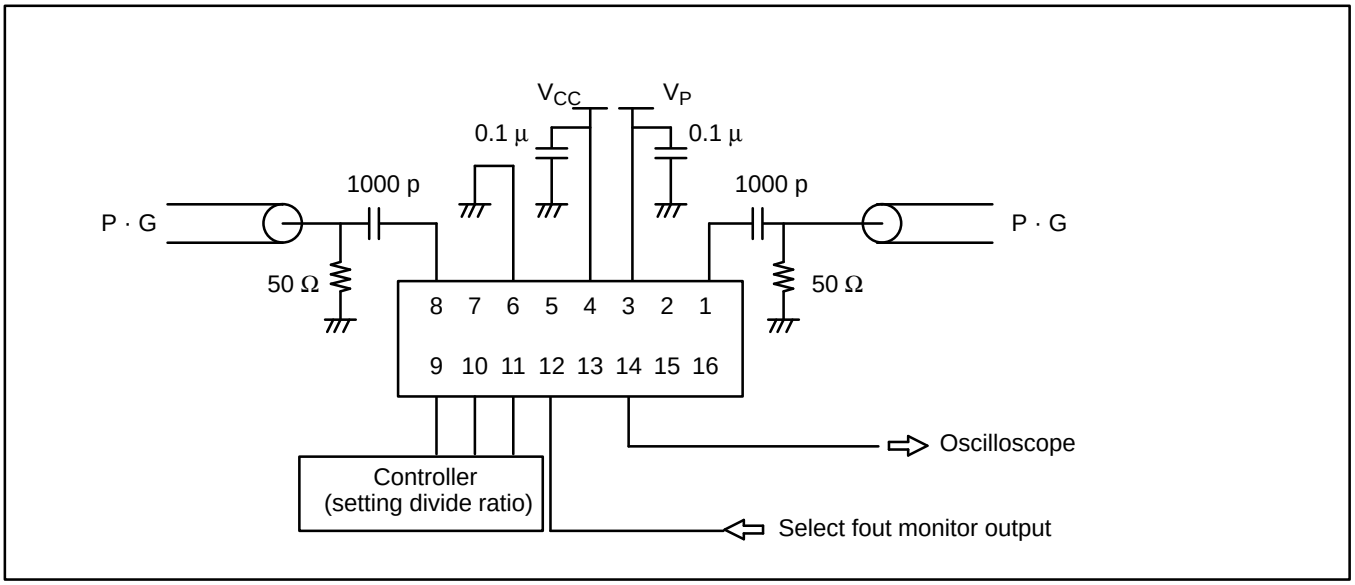
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	–	6.0	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	Ta	–40	–	85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Power Supply Current		I_{CC}	–	7.0	–	mA	*1
Operating Frequency	fin	fin	10	–	1100	MHz	*2
	OSC_{IN}	f_{OSC}	–	12	20	MHz	
Input Sensitivity	fin	Pfin	–10	–	6	dBm	50Ω system
	OSC_{IN}	V_{OSC}	0.5	–	–	V_{PP}	
High-level Input Voltage	Clock, Data, LE	V_{IH}	V_{CC}x0.7	–	–	V	
Low-level Input Voltage		V_{IL}	–	–	V_{CC}x0.3	V	
High-level Input Current	Data Clock	I_{IH}	–	–	1.0	µA	
Low-level Input Current		I_{IL}	–	–	–1.0	µA	
Input Current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
	LE, FC	I_{LE}	–	–60	–	µA	
High-level Output Voltage	∅R, LD	V_{OH}	4.4	–	–	V	V_{CC}=5V, I_{OH} = –1.0mA
Low-level Output Voltage	∅R, ∅P, LD	V_{OL}	–	–	0.4	V	V_{CC}=5V, I_{OL} = 1.0mA
High impedance Cutoff Current	D_O, ∅P	I_{OFF}	–	–	1.1	µA	V_P=V_{CC} to 6V V_{OOP}=GND to 6V
Output Current	∅R, LD	I_{OH}	–1.0	–	–	mA	V_{CC}=5V
	∅R, ∅P, LD	I_{OL}	–	–	1.0	mA	V_{CC}=5V

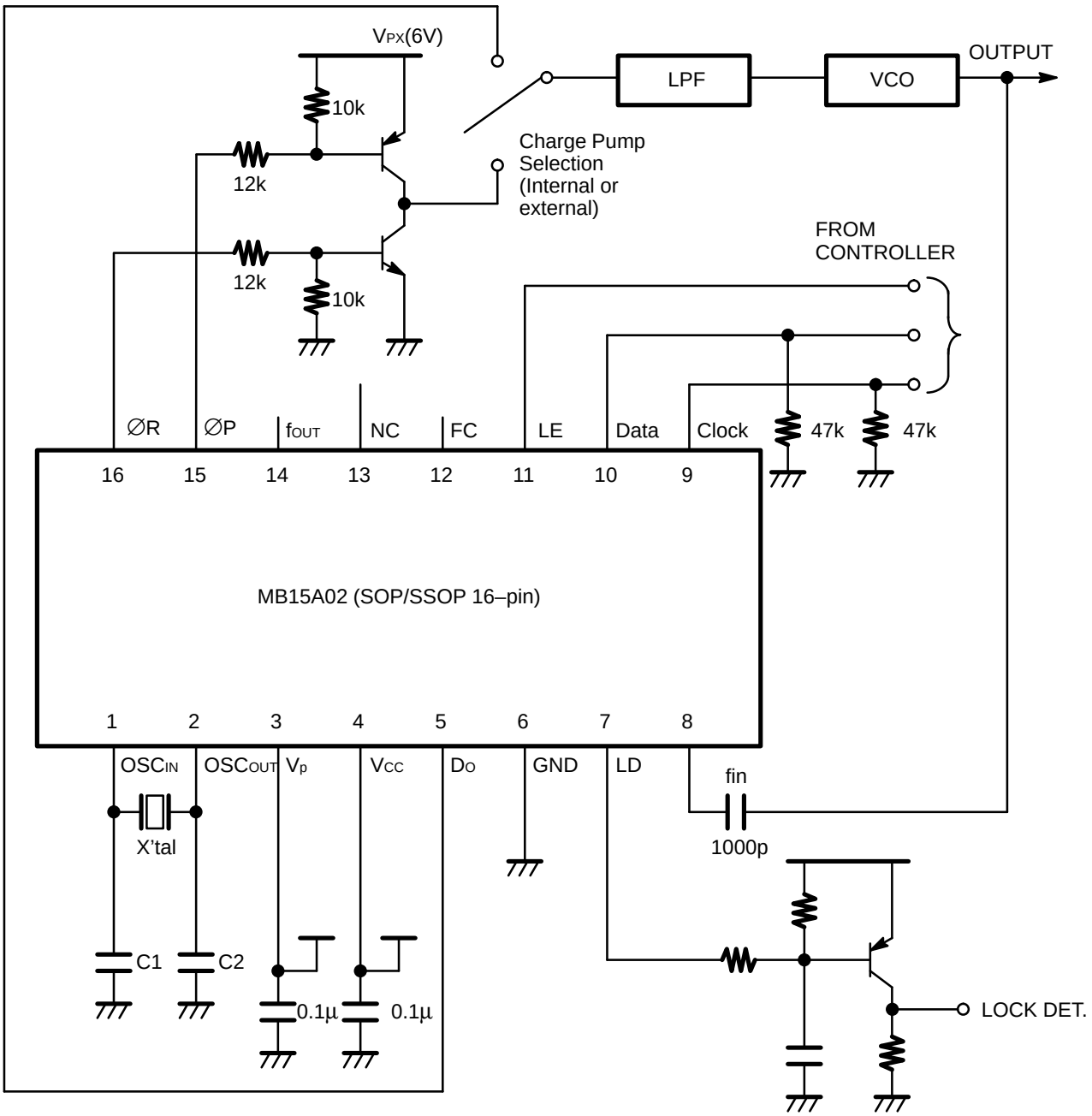
*1: fin=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. In locked state.
*2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



Note : Pin numbers are based on SOP/SSOP 16–pin packages.

TYPICAL APPLICATION EXAMPLE



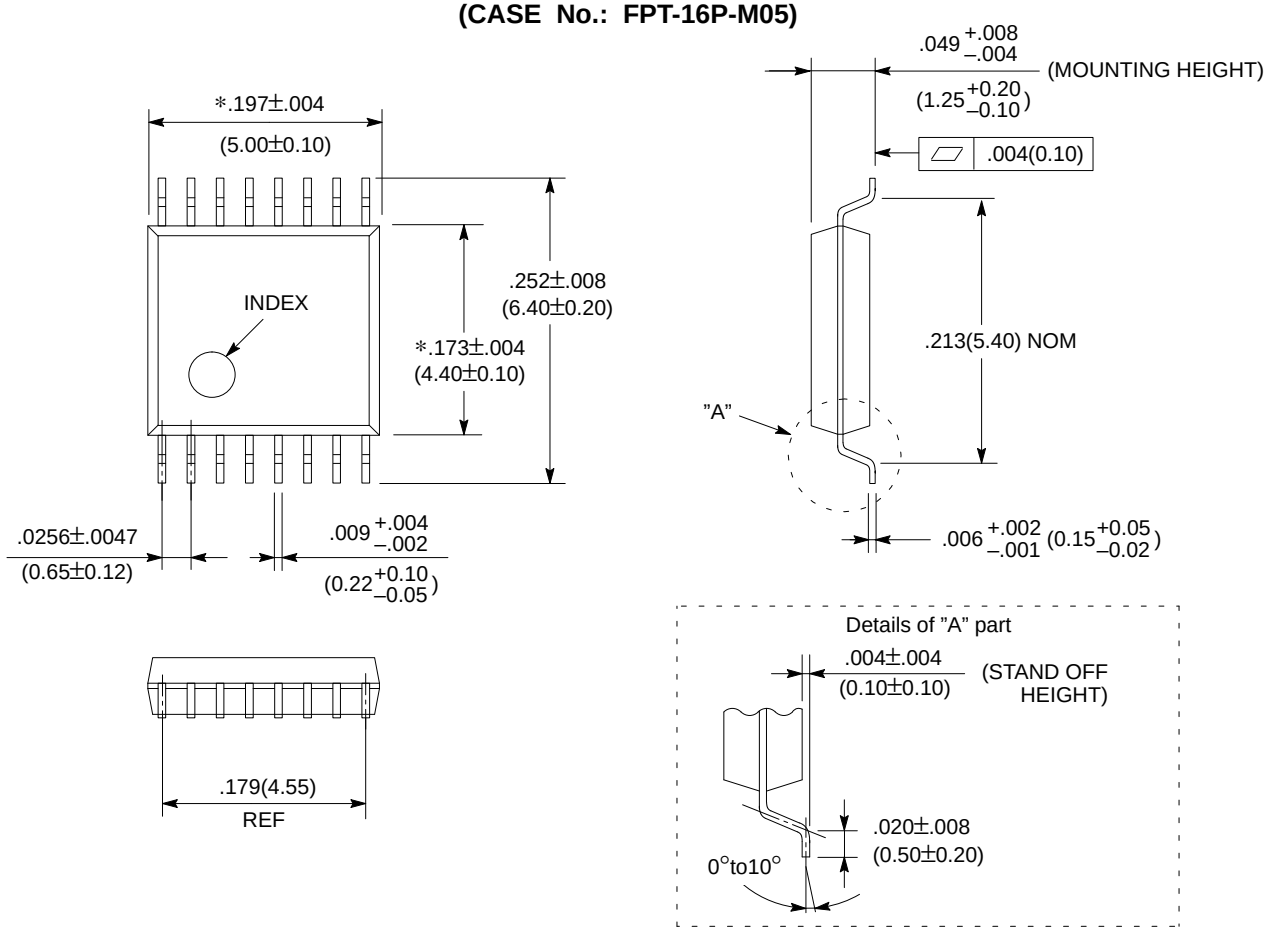
VPX : 6V max.
VP : When internal charge pump is not used, VP pin needs to be connected to VCC.
C1, C2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output
ØR : CMOS output

ORDERING INFORMATION

Part Number	Package
MB15A02PF	Plastic SOP, 16–pin FTP–16P–M06
MB15A02PFV1	Plastic SSOP, 16–pin FTP–16P–M05
MB15A02PFV2	Plastic SSOP, 20–pin FTP–20P–M03

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)

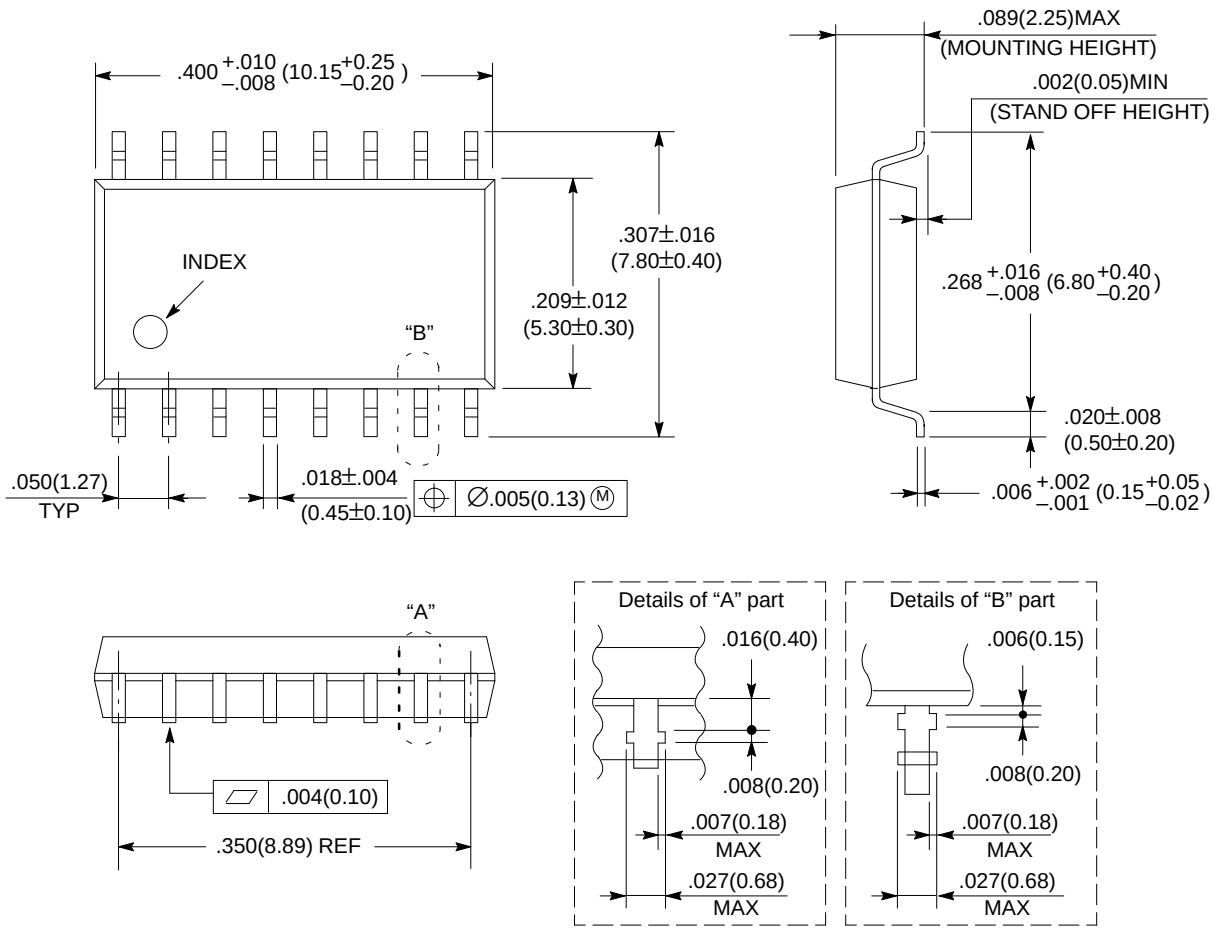


*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

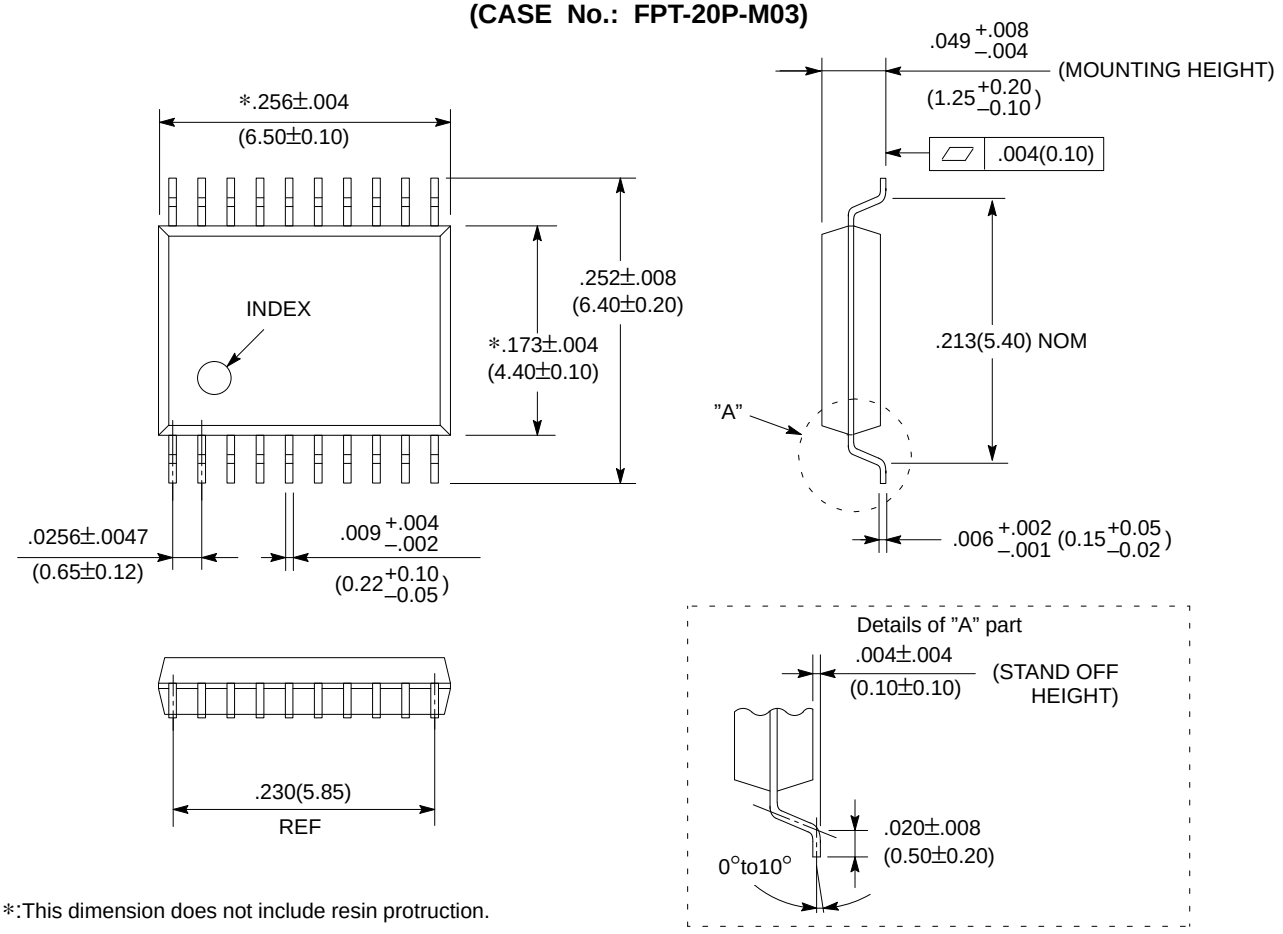
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

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