FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21353–1E

*ASSP*

# Dual Serial Input PLL Frequency Synthesizer

## MB15F02L



### ■ DESCRIPTION

The Fujitsu MB15F02L is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.2 GHz and a 250 MHz prescalers. A 64/65 or a 128/129 for the 1.2 GHz prescaler, and a 16/17 or a 32/33 for 250 MHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 4.0 mA typ. at a supply voltage of 3.0 V.

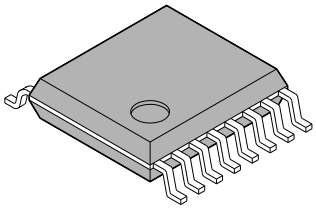
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F02L is ideally suitable for digital mobile communications, such as GSM (Global System for Mobile Communications).

### ■ FEATURES

- High frequency operation RF synthesizer: 1.2 GHz max. / IF synthesizer: 250 MHz max.
- Low power supply voltage: $V_{CC}$ = 2.7 to 3.6 V
- Very Low power supply current : $I_{CC}$ = 4.0 mA typ. ($V_{CC}$ = 3 V)
- Power saving function : Supply current at power saving mode Typ.0.1 µA ($V_{CC}$ = 3 V), Max.10 µA ($I_{PS1}$ = $I_{PS2}$)
- Dual modulus prescaler : 1.2 GHz prescaler (64/65,128/129) , 250 MHz prescaler (16/17,32/33)
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 5 to 2,047
- On–chip high performance charge pump circuit and phase comparator, achieving high–speed lock–up and low phase noise
- On–chip phase control for phase comparator
- Wide operating temperature: Ta = –40 to 85°C

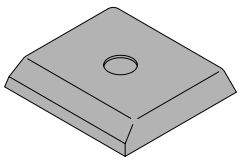
### ■ PACKAGES

16-pin, Plastic SSOP



(FPT-16P-M05)

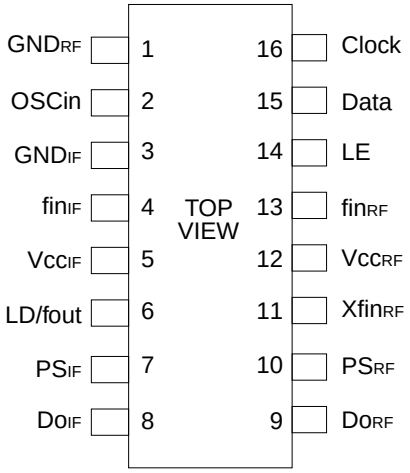
16-pin, Plastic BCC



(LCC-16P-M03)

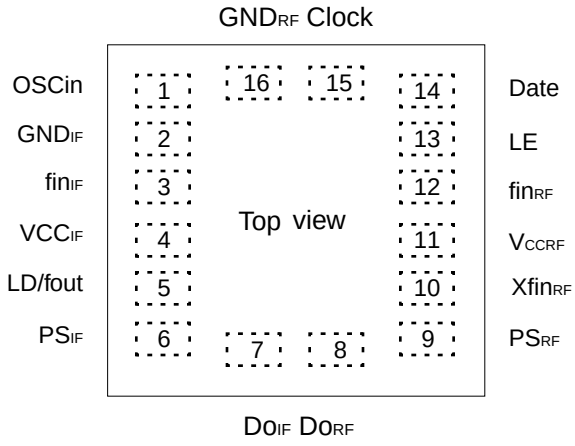
## ■ PIN ASSIGNMENTS

**SSOP-16 pin**




(FPT-16P-M05)

**BCC-16 pin**

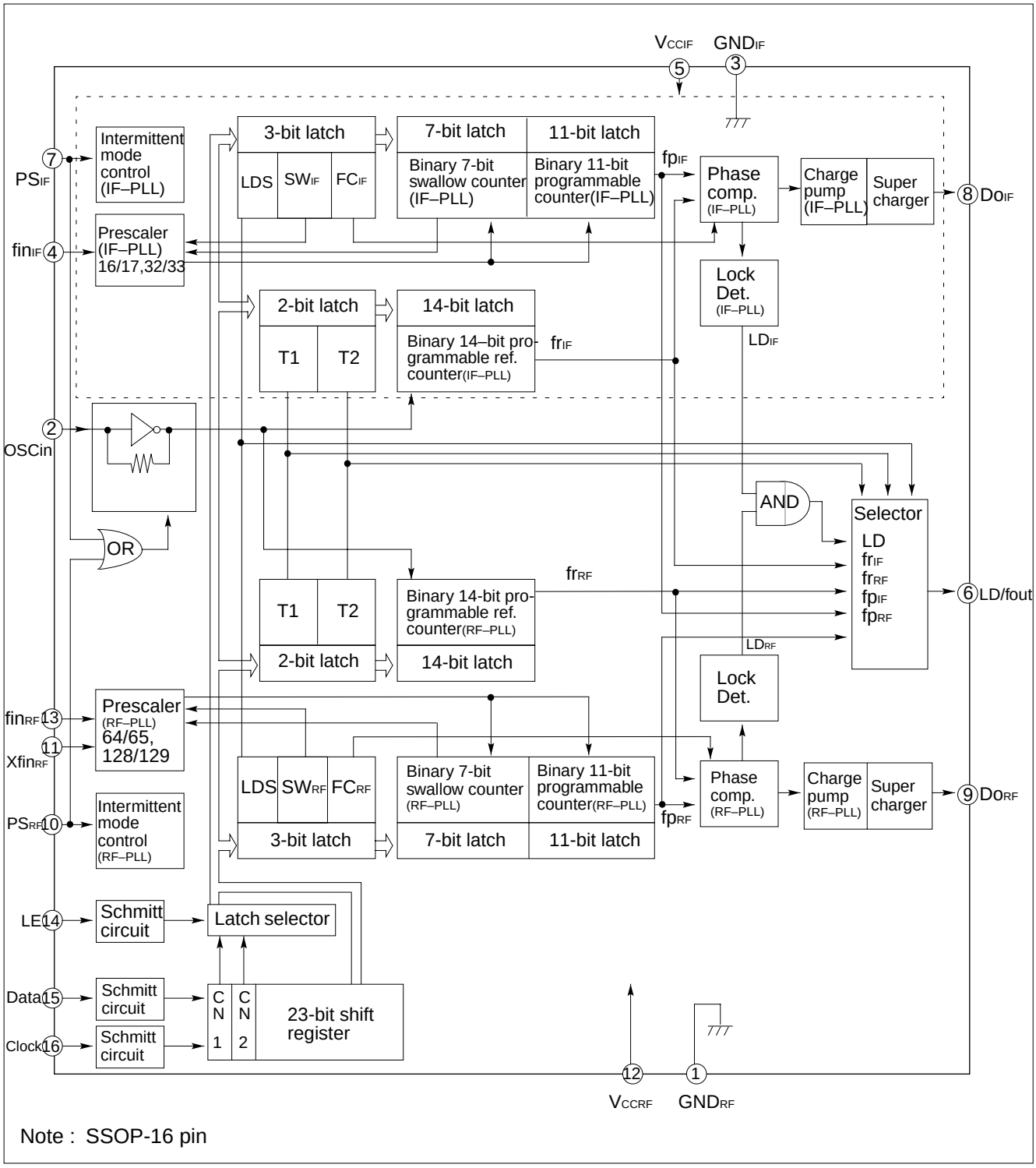



(LCC-16P-M03)

## ■ PIN DESCRIPTIONS

| Pin no. | | Pin name | I/O | Descriptions |
|---|---|---|---|---|
| SSOP | BCC | | | |
| 1 | 16 | $GND_{RF}$ | – | Ground for RF-PLL section. |
| 2 | 1 | OSCin | I | The programmable reference divider input. TCXO should be connected with a AC coupling capacitor. |
| 3 | 2 | $GND_{IF}$ | – | Ground for the IF-PLL section. |
| 4 | 3 | $fin_{IF}$ | I | Prescaler input pin for the IF-PLL.<br>The connection with VCO should be AC coupling. |
| 5 | 4 | $V_{CCIF}$ | – | Power supply voltage input pin for the IF-PLL section. |
| 6 | 5 | LD/fout | O | Lock detect signal output (LD) / phase comparator monitoring output (fout)<br>The output signal is selected by a LDS bit in a serial data.<br>LDS bit = “H” ; outputs fout signal<br>LDS bit = “L” ; outputs LD signal |
| 7 | 6 | $PS_{IF}$ | I | Power saving mode control for the IF-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.)<br>$PS_{IF}$ = “H” ; Normal mode<br>$PS_{IF}$ = “L” ; Power saving mode |
| 8 | 7 | $D_{OIF}$ | O | Charge pump output for the IF-PLL section.<br>Phase characteristics of the phase detector can be reversed by FC-bit. |
| 9 | 8 | $DO_{RF}$ | O | Charge pump output for the RF-PLL section.<br>Phase characteristics of the phase detector can be reversed by FC-bit. |
| 10 | 9 | $PS_{RF}$ | I | Power saving mode control for the RF-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.)<br>$PS_{RF}$ = “H” ; Normal mode<br>$PS_{RF}$ = “L” ; Power saving mode |
| 11 | 10 | $Xfin_{RF}$ | I | Prescaler complimentary input for the RF-PLL section.<br>This pin should be grounded via a capacitor. |
| 12 | 11 | $V_{CCRF}$ | – | Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled. |
| 13 | 12 | $fin_{RF}$ | I | Prescaler input pin for the RF-PLL.<br>The connection with VCO should be AC coupling. |
| 14 | 13 | LE | I | Load enable signal input (with the schmitt trigger circuit.)<br>When LE is “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data. |
| 15 | 14 | Data | I | Serial data input (with the schmitt trigger circuit.)<br>A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data. |
| 16 | 15 | Clock | I | Clock input for the 23-bit shift register (with the schmitt trigger circuit.)<br>One bit data is shifted into the shift register on a rising edge of the clock. |

## ■ BLOCK DIAGRAM




Note : SSOP-16 pin

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Rating | | Unit | Remark |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power supply voltage | $V_{CC}$ | –0.5 | +4.0 | V | |
| Input voltage | $V_I$ | –0.5 | $V_{CC}$ +0.5 | V | |
| Output voltage | $V_O$ | –0.5 | $V_{CC}$ +0.5 | V | |
| Output current | $I_O$ | –10 | +10 | mA | Except Do output |
| | $I_{do}$ | –25 | +25 | mA | Do output |
| Storage temperature | $T_{STG}$ | –55 | +125 | °C | |

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | $V_{CC}$ | 2.7 | 3.0 | 3.6 | V | |
| Input voltage | $V_I$ | GND | – | $V_{CC}$ | V | |
| Operating temperature | Ta | –40 | – | +85 | °C | |

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

**Handling Precautions**

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

## ■ ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.7 to 3.6 V, Ta = –40 to +85°C)

| Parameter | | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Power supply current | | $I_{CCIF}$*1 | $fin_{IF}$ = 250 MHz, fosc = 12 MHz | – | 1.5 | – | mA |
| | | $I_{CCRF}$*2 | $fin_{RF}$ = 1200 MHz, fosc = 12 MHz | – | 2.5 | – | |
| Power saving current | | $I_{PSIF}$ | $V_{CCIF}$ current at $PS_{IF}$ = "L" | – | 0.1*3 | 10 | µA |
| | | $I_{PSRF}$ | $V_{CCRF}$ current at $PS_{IF/RF}$ = "L" | – | 0.1*3 | 10 | |
| Operating frequency | $fin_{IF}$*4 | $fin_{IF}$ | IF-PLL | 50 | – | 250 | MHz |
| | $fin_{RF}$*4 | $fin_{RF}$ | RF-PLL | 100 | – | 1200 | |
| | OSCin | $f_{OSC}$ | – | 3 | – | 40 | |
| Input sensitivity | $fin_{IF}$ | $Vfin_{IF}$ | IF-PLL, 50 Ω termination | –10 | – | +2 | dBm |
| | $fin_{RF}$ | $Vfin_{RF}$ | RF-PLL, 50 Ω termination | –10 | – | +2 | dBm |
| | OSCin | $V_{OSC}$ | – | 0.5 | – | $V_{CC}$ | Vp-p |
| Input voltage | Data, Clock, LE | $V_{IH}$ | Schmitt trigger input | $V_{CC} \times 0.7 + 0.4$ | – | – | V |
| | | $V_{IL}$ | Schmitt trigger input | – | – | $V_{CC} \times 0.3 – 0.4$ | |
| | $PS_{IF}$, $PS_{RF}$ | $V_{IH}$ | – | $V_{CC} \times 0.7$ | – | – | V |
| | | $V_{IL}$ | – | – | – | $V_{CC} \times 0.3$ | |
| Input current | Data, Clock, LE, $PS_{IF}$, $PS_{RF}$ | $I_{IH}$*5 | – | –1.0 | | +1.0 | µA |
| | | $I_{IL}$*5 | – | –1.0 | – | +1.0 | |
| | OSCin | $I_{IH}$ | – | 0 | – | +100 | µA |
| | | $I_{IL}$*5 | – | –100 | – | 0 | |
| Output voltage | LD/fout | $V_{OH}$ | $V_{CC}$ = 3.0 V, $I_{OH}$ = –1.0 mA | $V_{CC}$ – 0.4 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$ = 3.0 V, $I_{OL}$ = 1.0 mA | – | – | 0.4 | |
| | $Do_{IF}$, $Do_{RF}$ | $V_{DOH}$ | $V_{CC}$ = 3.0 V, $I_{DOH}$ = –1.0 mA | $V_{CC}$ – 0.4 | – | – | V |
| | | $V_{DOL}$ | $V_{CC}$ = 3.0 V, $I_{DOL}$ = 1.0 mA | – | – | 0.4 | |
| High impedance cutoff current | $Do_{IF}$, $Do_{RF}$ | $I_{OFF}$ | $V_{CC}$ = 3.0 V, $V_{OFF}$ = GND to $V_{CC}$ | – | – | 3.0 | nA |
| Output current | LD/fout | $I_{OH}$*5 | $V_{CC}$ = 3.0 V | –1.0 | – | – | mA |
| | | $I_{OL}$ | $V_{CC}$ = 3.0 V | – | – | 1.0 | |
| | $Do_{IF}$, $Do_{RF}$ | $I_{DOH}$*5 | $V_{CC}$ = 3.0 V, $V_{DOH}$ = 2.0 V, Ta = 25°C | –11 | – | –6 | mA |
| | | $I_{DOL}$ | $V_{CC}$ = 3.0 V, $V_{DOL}$ = 1.0 V, Ta = 25°C | 8 | – | 15 | |

*1: Conditions ; $V_{CCIF}$ = 3 V, Ta = 25°C, in locking state.

*2: Conditions ; $V_{CCRF}$ = 3 V, Ta = 25°C, in locking state.

*3: fosc = 12.8 MHz , $V_{CC}$ = 3.0 V, Ta = 25°C

*4: AC coupling with a 1000 pF capacitor connected.

*5: The symbol "–" (minus) means direction of current flow.

## ■ FUNCTIONAL DESCRIPTIONS

### 1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \ (A < N)$

$f_{VCO}$: Output frequency of external voltage controlled oscillator (VCO)
M: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$)
$f_{OSC}$: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

### 2. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

**Table1. Control Bit**

| Control bit | | Destination of serial data |
|---|---|---|
| CN1 | CN2 | |
| L | L | The programmable reference counter for the IF-PLL. |
| H | L | The programmable reference counter for the RF-PLL. |
| L | H | The programmable counter and the swallow counter for the IF-PLL |
| H | H | The programmable counter and the swallow counter for the RF-PLL |

### (1) Shift Register Configuration

• **Programmable Reference Counter**

LSB ↓ Data Flow → MSB ↓

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CN1 | CN2 | T1 | T2 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 | R13 | R14 | X | X | X | X | X |

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table.3]
X : Dummy bits(Set “0” or “1”)
**Note:** Data input with MSB first.

• **Programmable Counter**

LSB ← Data Flow → MSB

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CN1 | CN2 | LDS | SW IF/RF | FC IF/RF | A1 | A2 | A3 | A4 | A5 | A6 | A7 | N1 | N2 | N3 | N4 | N5 | N6 | N7 | N8 | N9 | N10 | N11 |

CNT1, 2 : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW IF/RF : Divide ratio setting bit for the prescaler (16/17 or 32/33 for the IF-PLL, 64/65 or 128/129 for the RF-PLL) [Table. 6]
FC IF/RF : Phase control bit for the phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]

**Note:** Data input with MSB first.

## (2) Data Setting

### Table2. Binary 14-bit Programmable Reference Counter Data Setting

| Divide ratio (R) | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 16383 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Divide ratio less than 5 is prohibited.

### Table3. Test Purpose Bit Setting

| T1 | T2 | LD/fout pin state |
|---|---|---|
| L | L | Outputs $fr_{IF.}$ |
| H | L | Outputs $fr_{RF.}$ |
| L | H | Outputs $fp_{IF.}$ |
| H | H | Outputs $fp_{RF.}$ |

**Table4. Binary 11-bit Programmable Counter Data Setting**

| Divide ratio (N) | N 11 | N 10 | N 9 | N 8 | N 7 | N 6 | N 5 | N 4 | N 3 | N 2 | N 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| . | . | . | . | . | . | . | . | . | . | . | . |
| 2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Divide ratio less than 5 is prohibited.

**Table5. Binary 7-bit Swallow Counter Data Setting**

| Divide ratio (A) | A 7 | A 6 | A 5 | A 4 | A 3 | A 2 | A 1 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| . | . | . | . | . | . | . | . |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Divide ratio (A) range = 0 to 127

**Table6. Prescaler Data Setting**

| | | SW = "H" | SW = "L" |
|---|---|---|---|
| **Prescaler divide ratio** | **IF-PLL** | 16/17 | 32/33 |
| | **RF-PLL** | 64/65 | 128/129 |

**Table7. Phase Comparator Phase Switching Data Setting**

| | $FC_{IF,RF}$ = H | $FC_{IF,RF}$ = L |
|---|---|---|
| | $DO_{IF,RF}$ | |
| fr > fp | H | L |
| fr = fp | Z | Z |
| fr < fp | L | H |
| VCO polarity | (1) | (2) |

Note:
- Z = High-impedance
- Depending upon the VCO and LPF polarity, FC bit should be set.

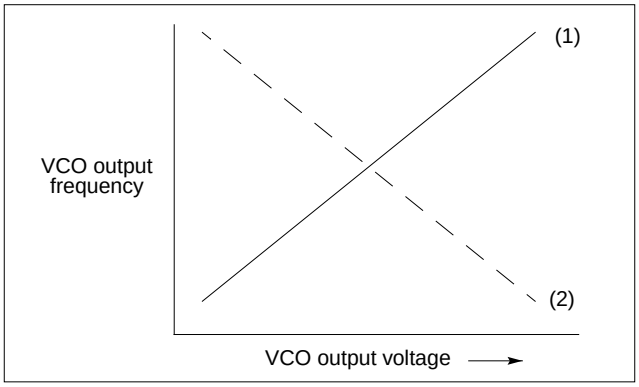


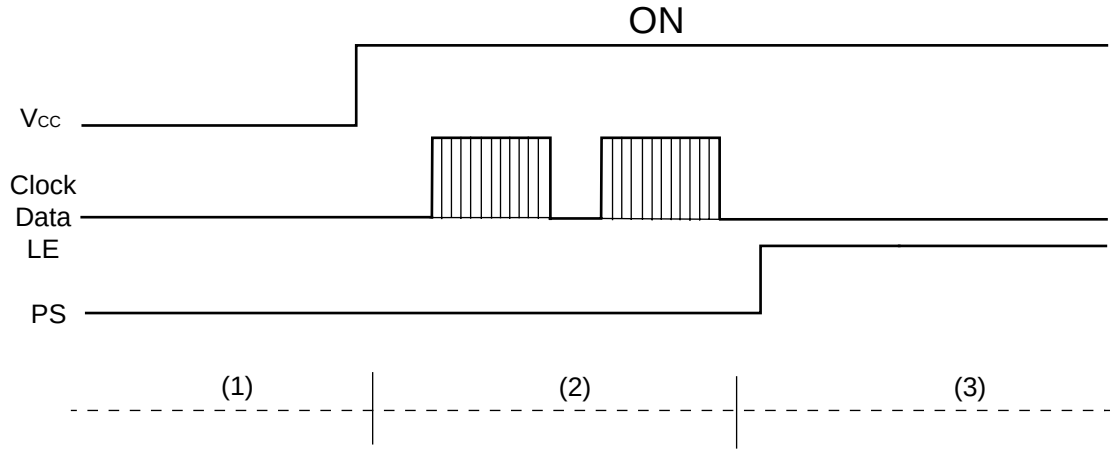

**Table8. LD/fout Output Select Data Setting**

| LDS | LD/fout output signal |
|---|---|
| H | fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals |
| L | LD signal |

## 3. Power Saving Mode (Intermittent Mode Control Circuit)

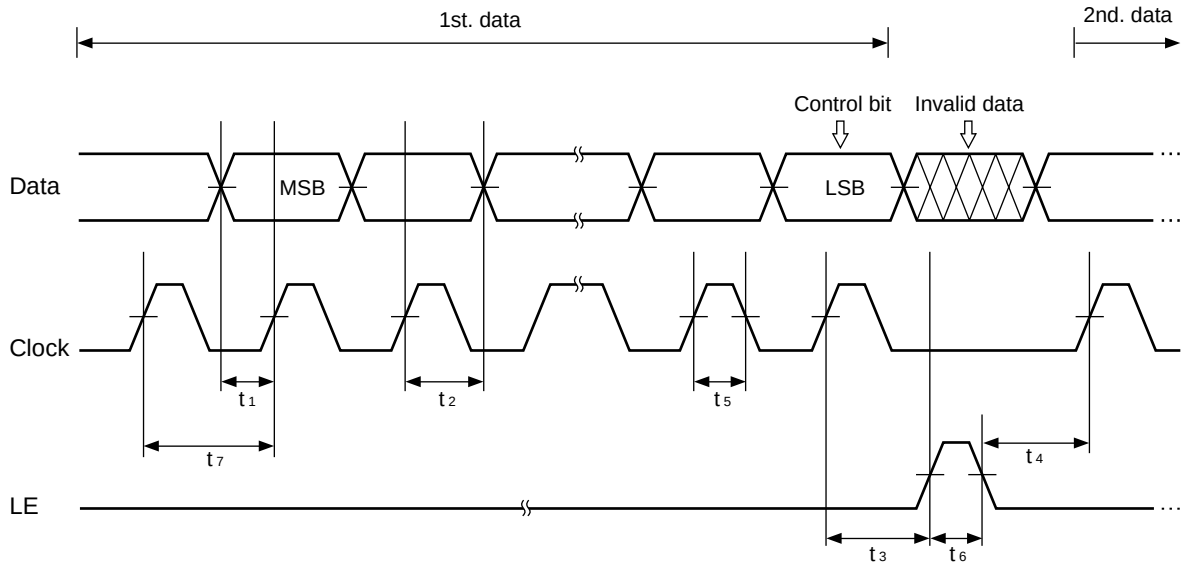
Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL (RF-PLL) enters into power saving mode resultant current consumption can be limited to 10 μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode.
In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (fr) and comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up. Thus keeping the loop locked.
*PS pin must be set "L" at Power-ON.*
Allow 1 μs after frequency stabilization on power-up for exiting the power saving mode (PS: L to H)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10 μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

| $PS_{IF}$ | $PS_{RF}$ | IF-PLL counters | RF-PLL counters | OSC input buffer |
|---|---|---|---|---|
| L | L | OFF | OFF | OFF |
| H | L | ON | OFF | ON |
| L | H | OFF | ON | ON |
| H | H | ON | ON | ON |




(1) PS = L (power saving mode) at Power-ON
(2)Set serial data after power supply remains stable.
(3)Release saving mode(PS : L → H) after setting serial data.

## 4. Serial Data Input Timing

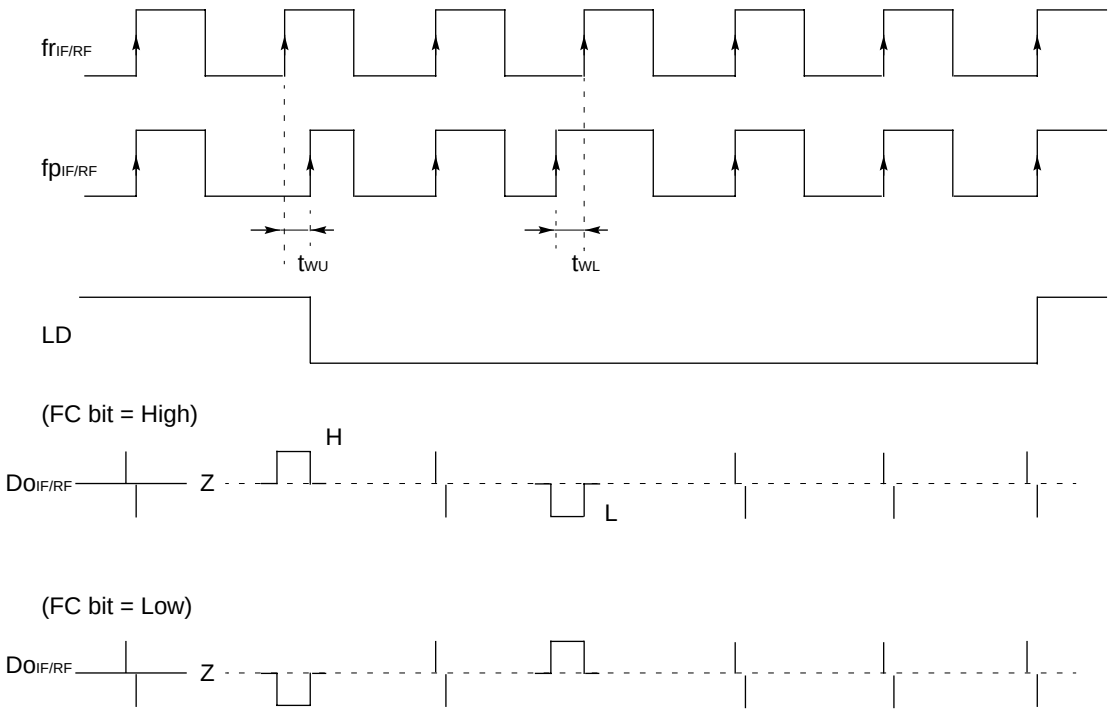



On rising edge of the clock, one bit of the data is transferred into the shift register.

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| t1 | 20 | – | – | ns |
| t2 | 20 | – | – | ns |
| t3 | 30 | – | – | ns |
| t4 | 20 | – | – | ns |

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| t5 | 30 | – | – | ns |
| t6 | 100 | – | – | ns |
| t7 | 100 | – | – | ns |
| | | | | |

## ■ PHASE DETECTOR OUTPUT WAVEFORM

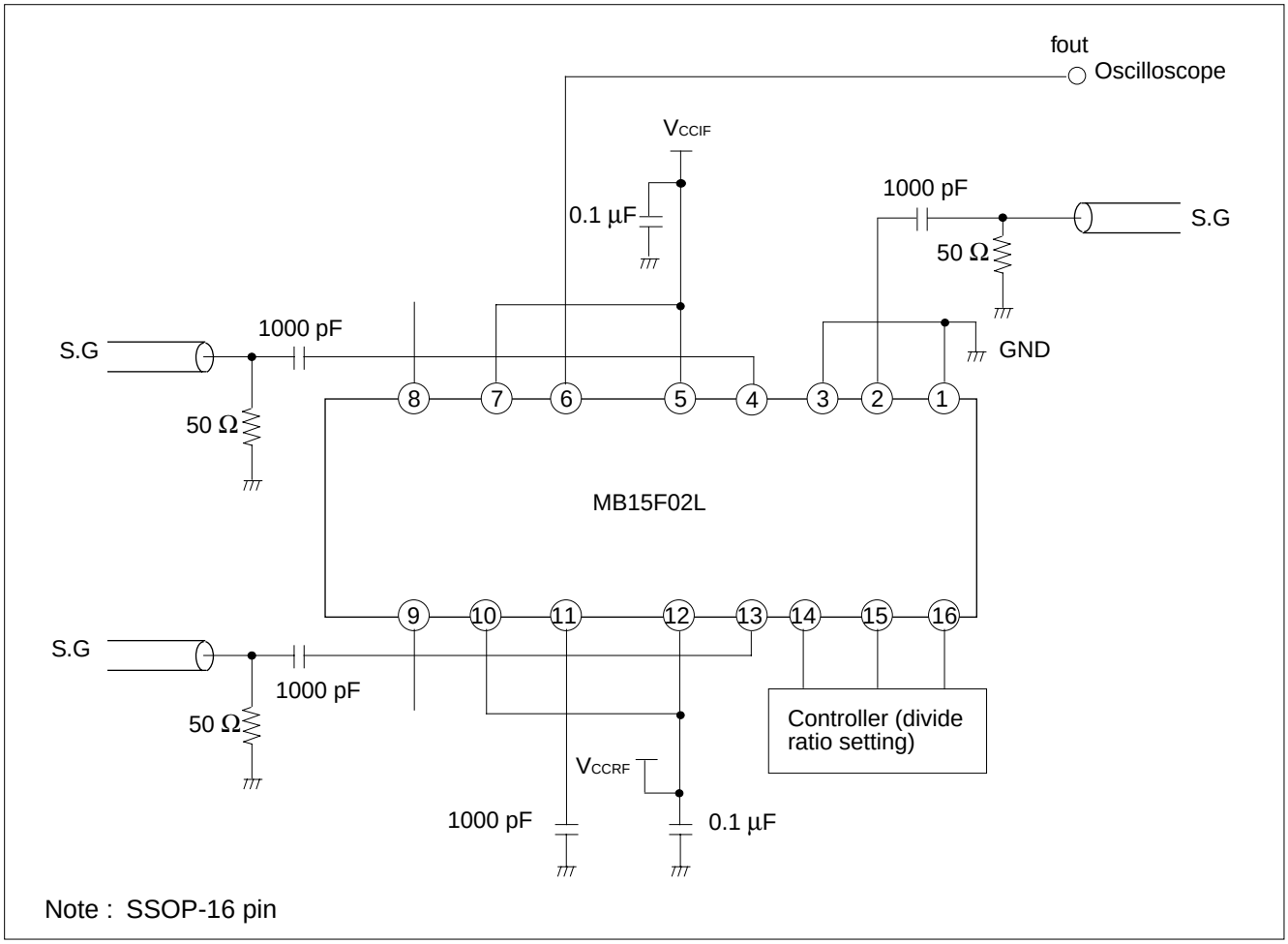



### LD Output Logic Table

| IF-PLL section | RF-PLL section | LD output |
|---|---|---|
| Locking state / Power saving state | Locking state / Power saving state | H |
| Locking state / Power saving state | Unlocking state | L |
| Unlocking state | Locking state / Power saving state | L |
| Unlocking state | Unlocking state | L |

Note:
- Phase error detection range = –2π to +2π
- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is $t_{WU}$ or more.
- LD output becomes high when phase error is $t_{WL}$ or less and continues to be so for three cycles or more.
- $t_{WU}$ and $t_{WL}$ depend on OSCin input frequency as follows.
  $t_{WU} \geq 4/fosc$: i.e. $t_{WU} \geq 312.5$ ns when foscin = 12.8 MHz
  $t_{WL} \leq 8/fosc$: i.e. $t_{WL} \leq 625.0$ ns when foscin = 12.8 MHz

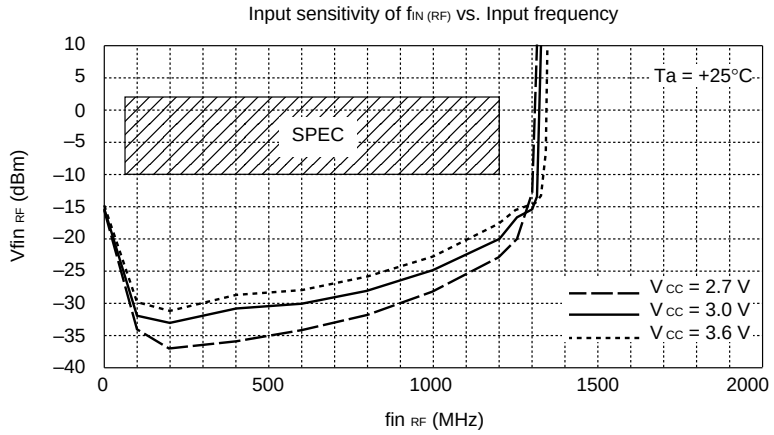
## ■ TEST CIRCUIT (fin, $OSC_{IN}$ Input Sensitivity Test)

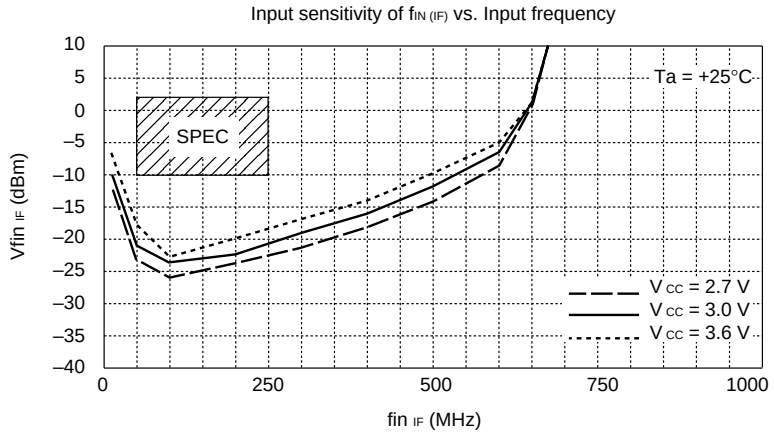



Note : SSOP-16 pin

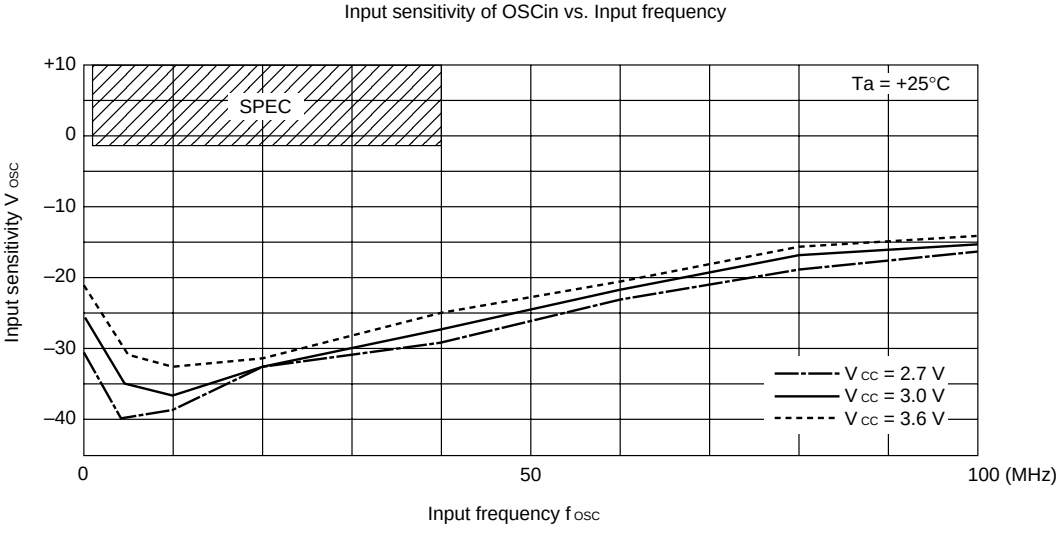
## ■ TYPICAL CHARACTERISTICS

### 1. fin Input Sensitivity

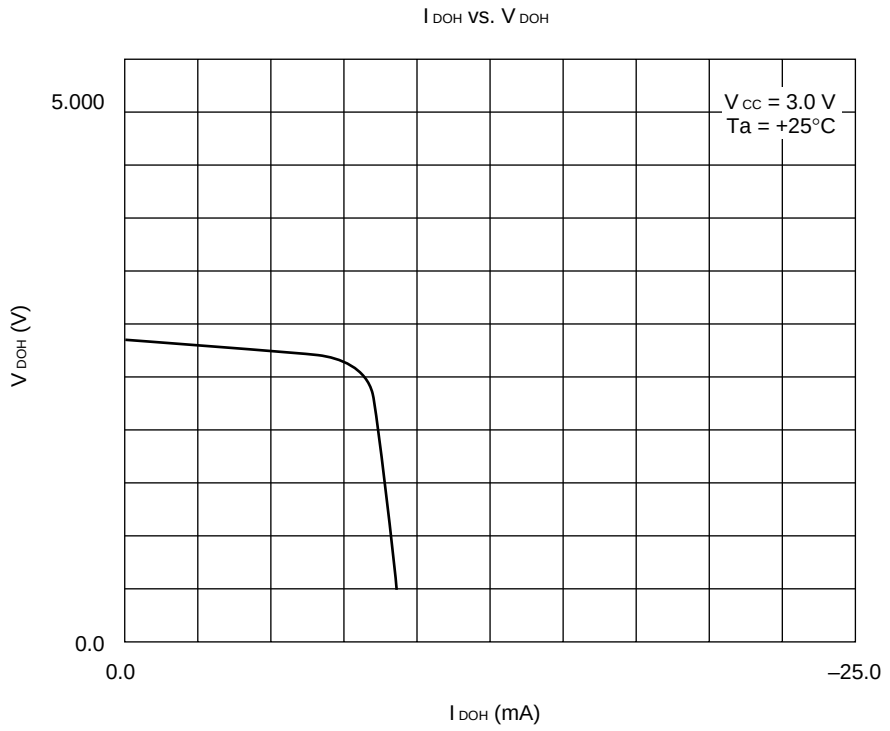


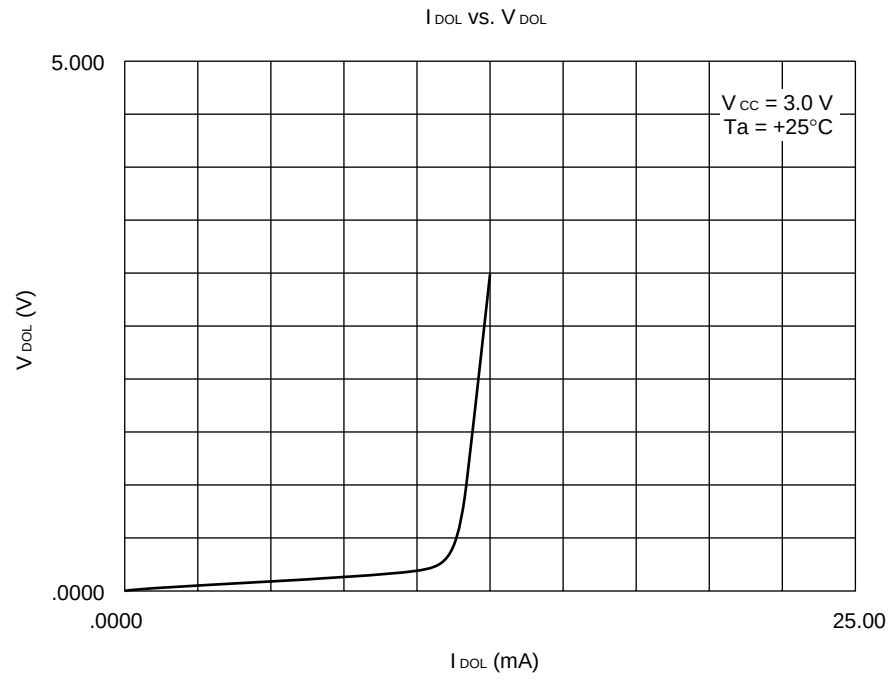




### 2. OSCin Input Sensitivity



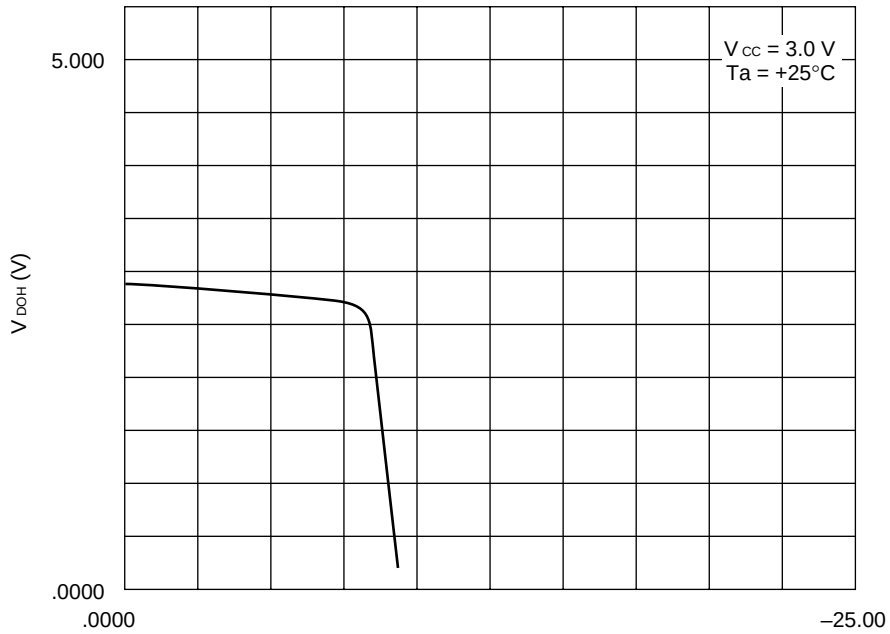
## 3. $D_{ORF}$ Output Current



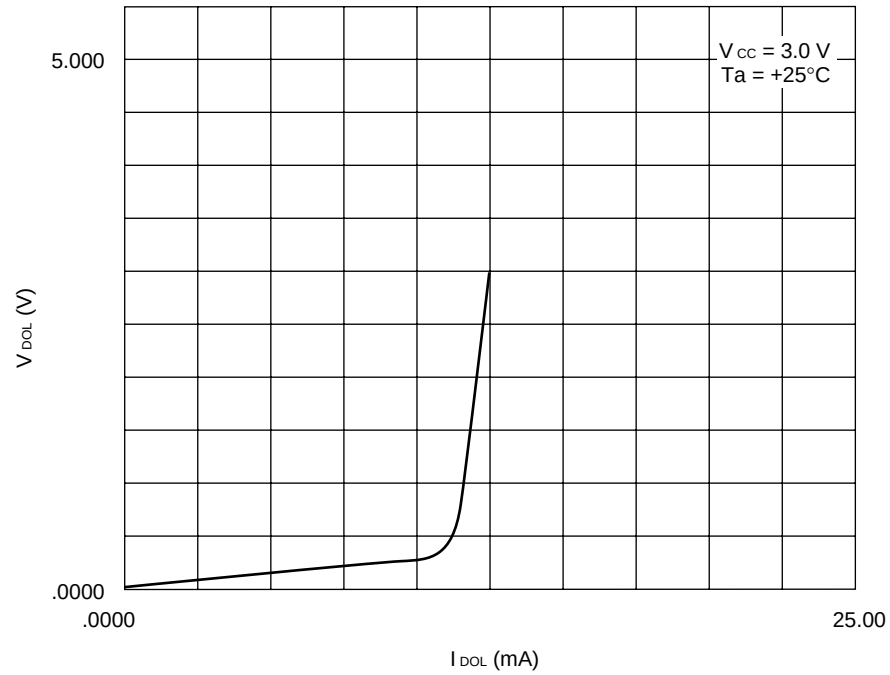



## 4. $D_{OIF}$ Output Current

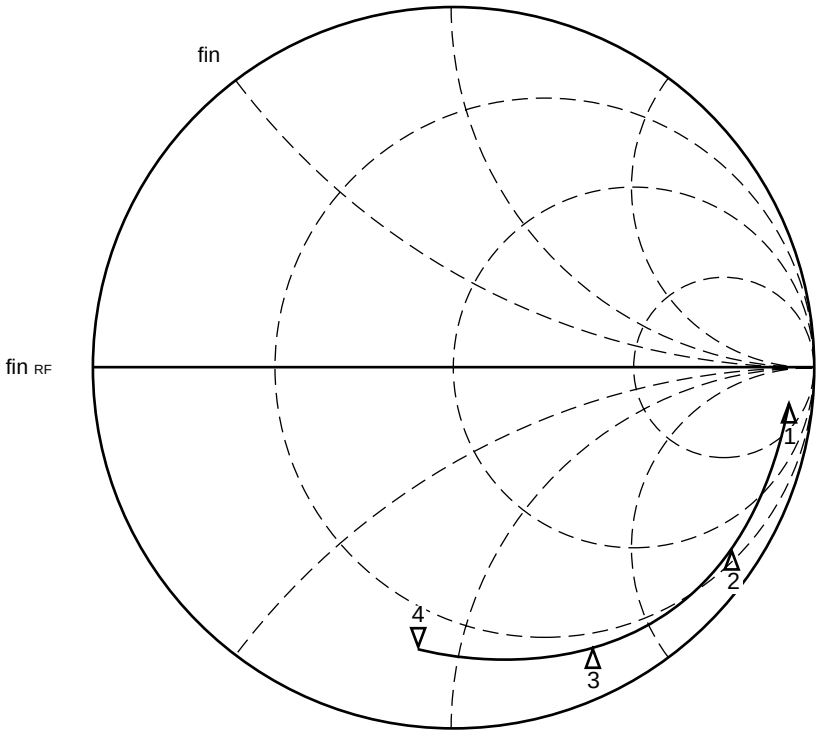
$I_{DOH}$ vs. $V_{DOH}$




$I_{DOL}$ vs. $V_{DOL}$



## 5. fin Input Impedance

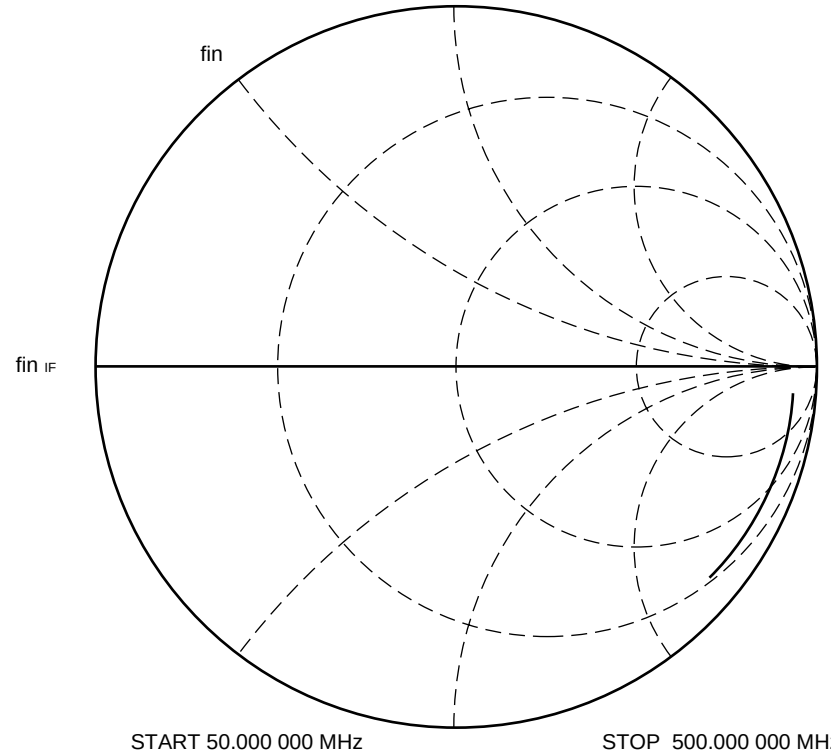



1 : 309 Ω
–640.13 Ω
100 MHz

2 : 29.773 Ω
–186.98 Ω
400 MHz

3 : 12.648 Ω
–83.883 Ω
800 MHz

4 : 10.252 Ω
–43.703 Ω
1.2 GHz

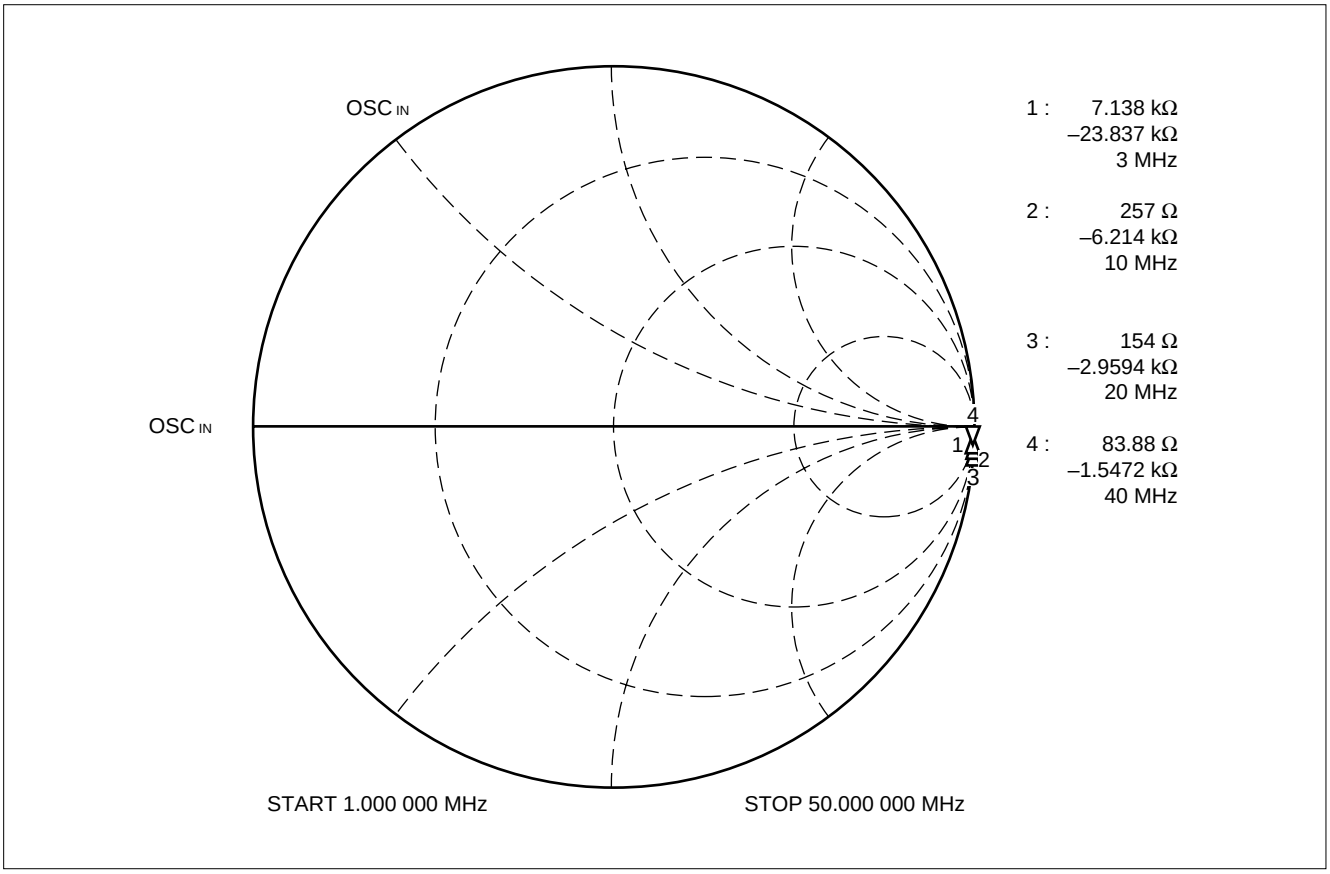



1 : 791.22 Ω
–907.56 Ω
50 MHz

2 : 89.189 Ω
–378.02 Ω
200 MHz

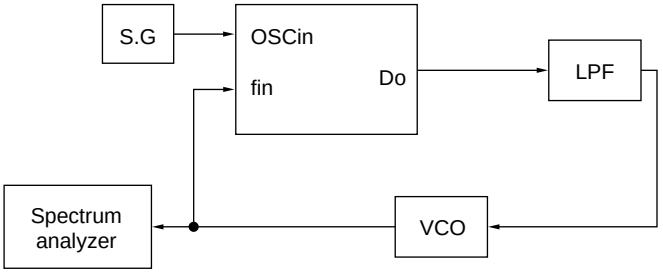
3 : 58.797 Ω
–304.36 Ω
250 MHz

## 6. $OSC_{IN}$ Input Impedance

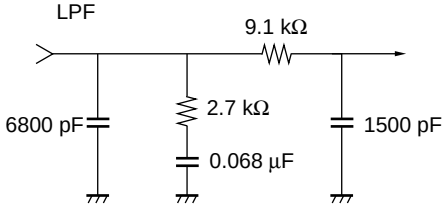


## ■ REFERENCE INFORMATION (Lock Up Time, Phase Noise, Reference Leakage)

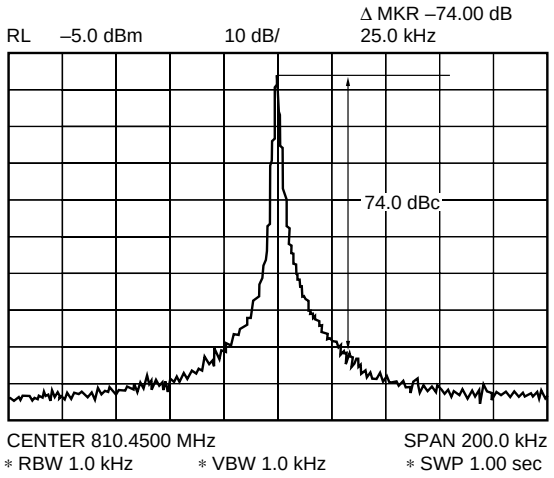
Test Circuit



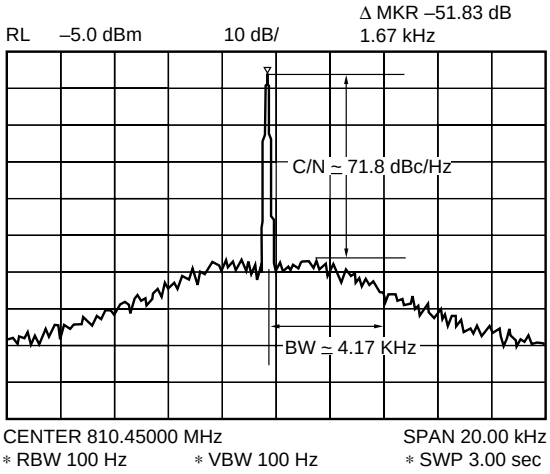

$f_{VCO}$ = 810.45 MHz
$K_V$ = 17 MHz/V
fr = 25 kHz
$f_{OSC}$ = 14.4 MHz
LPF



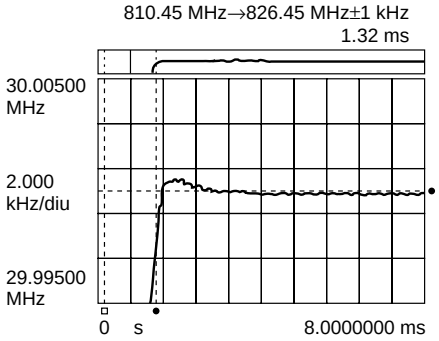

PLL reference leakage

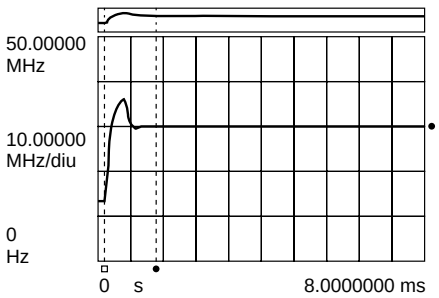



PLL phase noise

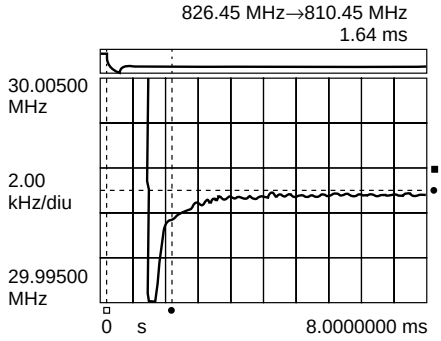


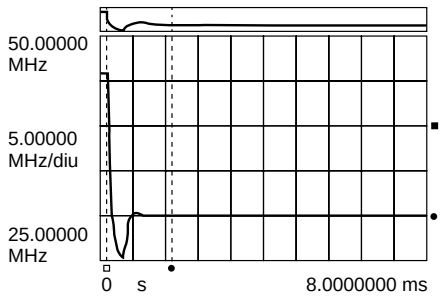

PLL lock up time



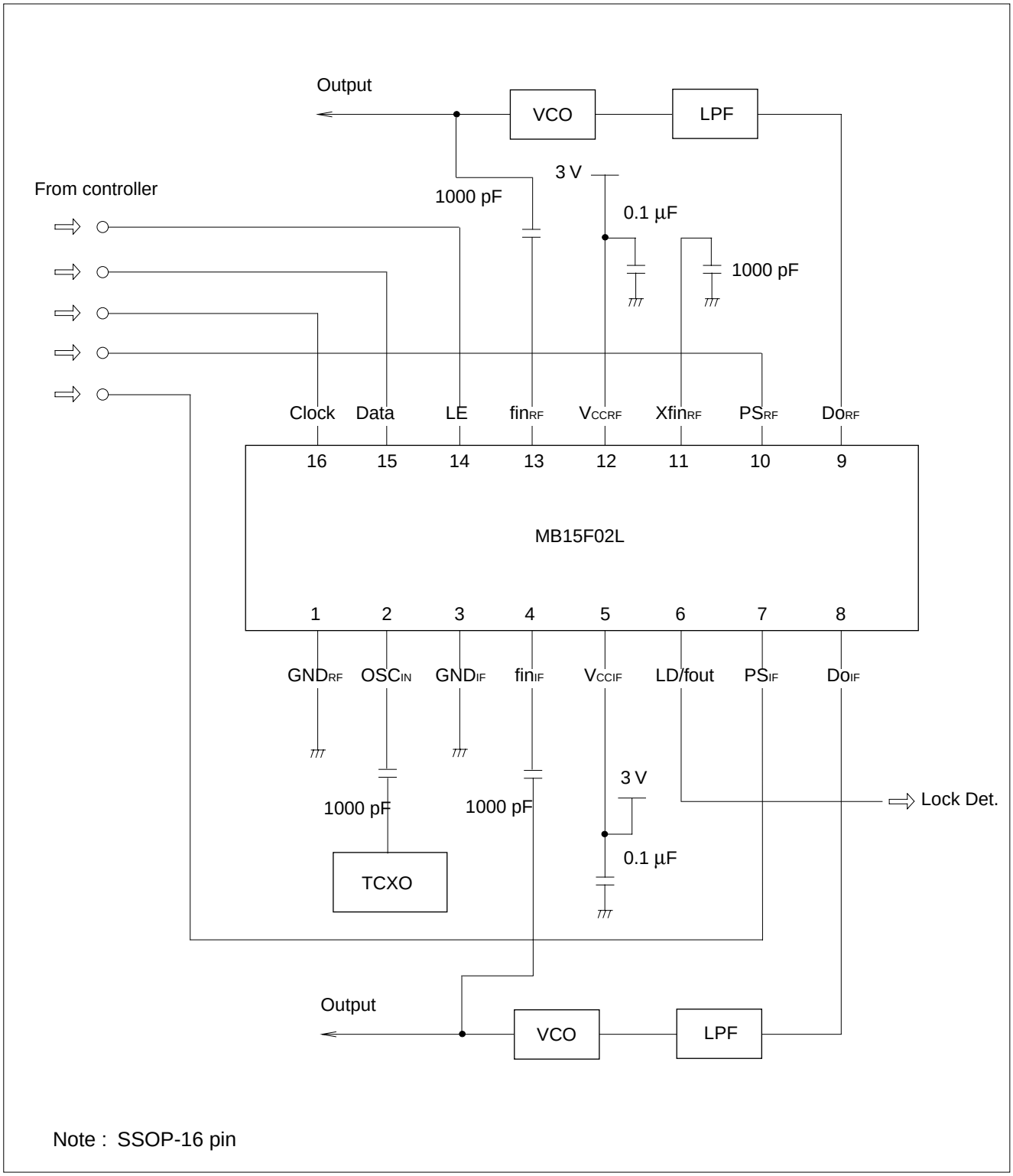




PLL lock up time



## ■ APPLICATION EXAMPLE




Note : SSOP-16 pin

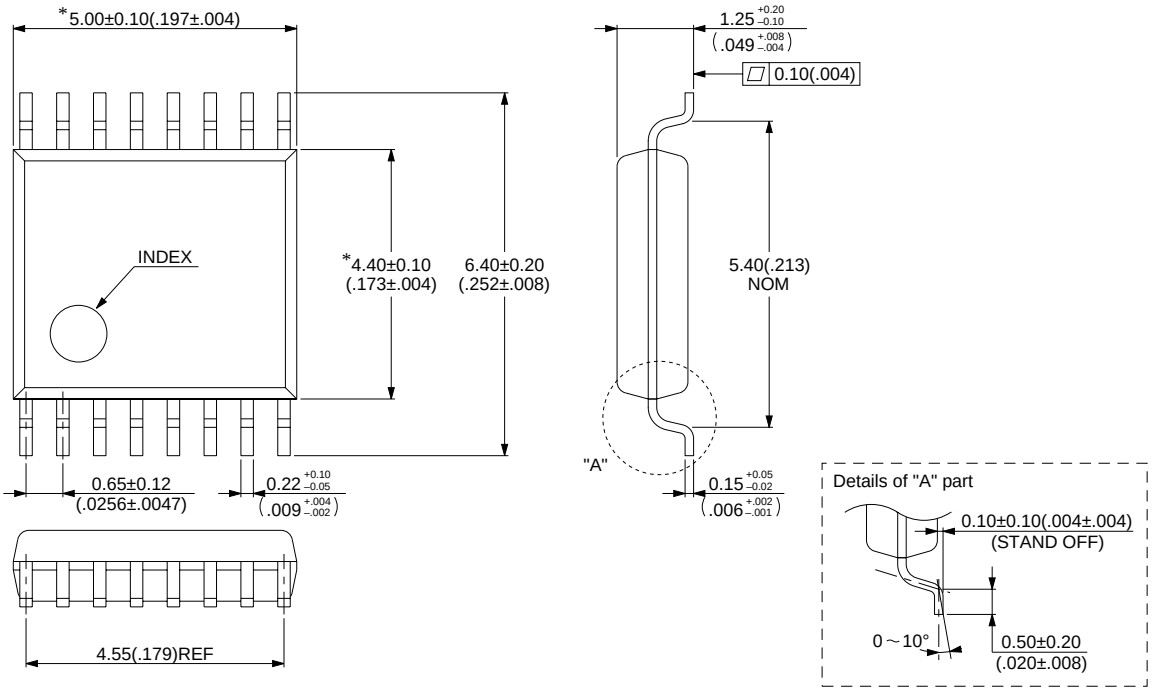
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB15F02LPFV1 | 16 pin, Plastic SSOP<br>(FPT-16P-M05) | |
| MB15F02LPV | 16 pin, Plastic BCC<br>(LCC-16P-M03) | |

## ■ PACKAGE DIMENSIONS

16 pins, Plastic SSOP
(FPT-16P-M05)

*: These dimensions do not include resin protrusion.



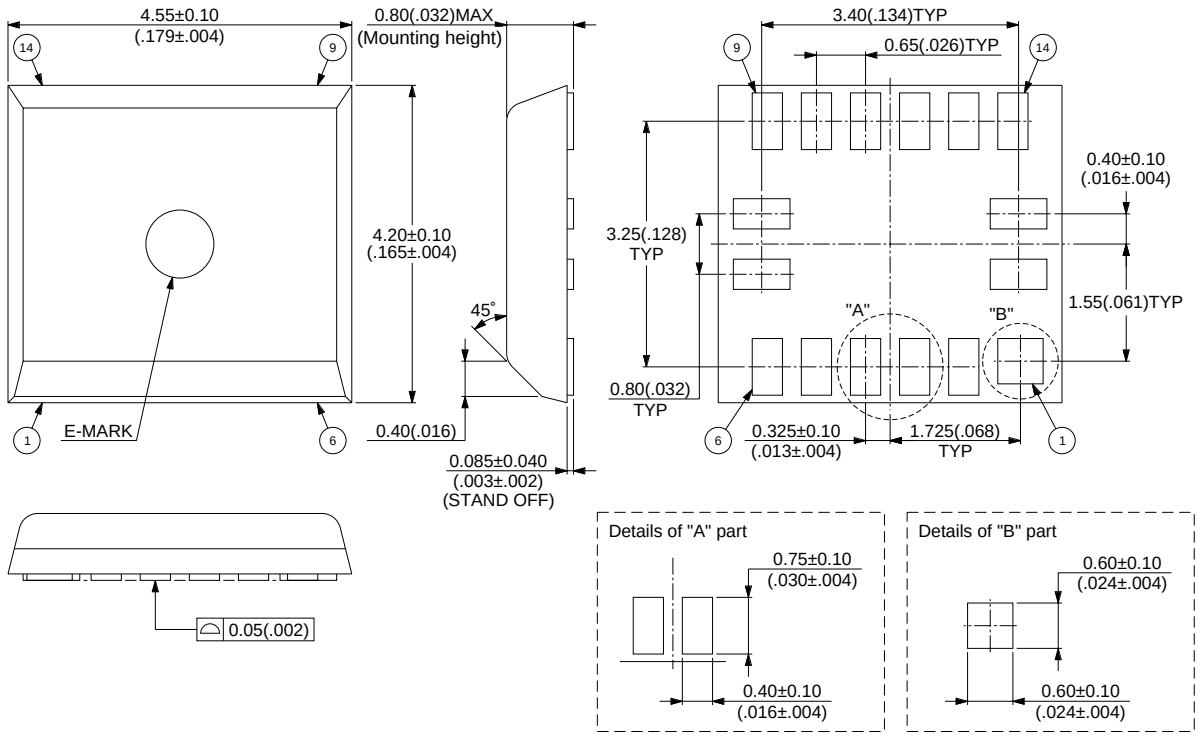



Dimensions in mm (inches).

*(Continued)*

*(Continued)*

16 pins, Plastic BCC
(LCC-16P-M03)






Dimensions in mm (inches).

# FUJITSU LIMITED

*For further information please contact:*

**Japan**
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

**North and South America**
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

**Europe**
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

**Asia Pacific**
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

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