FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21376-2E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F73UV

■ DESCRIPTION

The Fujitsu MB15F73UV is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2250 MHz and a 600 MHz prescalers. A 64/65 or a 128/129 for the 2250 MHz prescaler, and a 8/9 or a 16/17 for the 600 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

The BiCMOS process is used, as a result a supply current is typically 3.2 mA at 2.7 V. The supply voltage range is from 2.4 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial data. The data format is the same as the previous one MB15F03SL, MB15F73SP/UL. Fast locking is achieved for adopting the new circuit.

MB15F73UV is in the new small package (BCC18), which decreases a mount area of MB15F73UV about 50% comparing with the former BCC20 (for dual PLL) .

MB15F73UV is ideally suited for wireless mobile communications, such as CDMA and PCS.

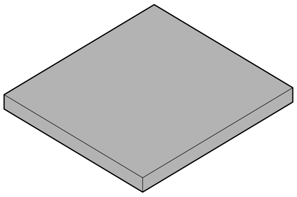
■ FEATURES

- High frequency operation : RF synthesizer : 2250 MHz Max
  : IF synthesizer : 600 MHz Max
- Low power supply voltage : V_{CC} = 2.4 V to 3.6 V
- Ultra low power supply current : I_{CC} = 3.2 mA Typ
  (V_{CC} = 2.7 V, Ta = +25 °C, SW_{IF} = SW_{RF} = 0 in IF/RF locking state)

(Continued)

■ PACKAGES

18-pin plastic BCC



(LCC-18P-M05)

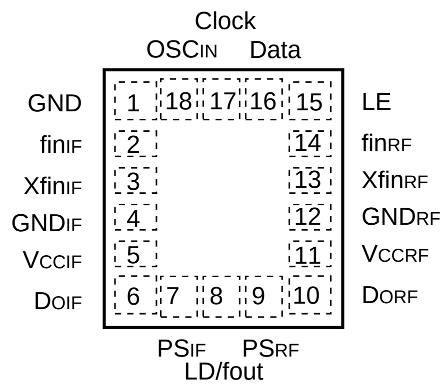
FUJITSU

(Continued)

- Direct power saving function : Power supply current in power saving mode
  Typ 0.1 μA (V_{CC} = 2.7 V, Ta = +25 °C)
  Max 10 μA (V_{CC} = 2.7 V)
- Software selectable charge pump current : 1.5 mA/6.0 mA Typ
- Dual modulus prescaler : 2250 MHz prescaler (64/65 or128/129) /600 MHz prescaler (8/9 or 16/17)
- 23 bit shift register
- Serial input binary 14-bit programmable reference divider : R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter : 0 to 127
  - Binary 11-bit programmable counter : 3 to 2,047
- Built-in high-speed tuning, low-noise phase comparator, current-switching type constant current circuit
- On-chip phase control for phase comparator
- On-chip phase comparator for fast lock and low noise
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Operating temperature : Ta = –40 °C to +85 °C
- Serial data format compatible with MB15F73UL
- Ultra small Package Bcc18 (2.4 mm x 2.7 mm x 0.45 mm)

■ PIN ASSIGNMENTS

(BCC-18)
TOP VIEW

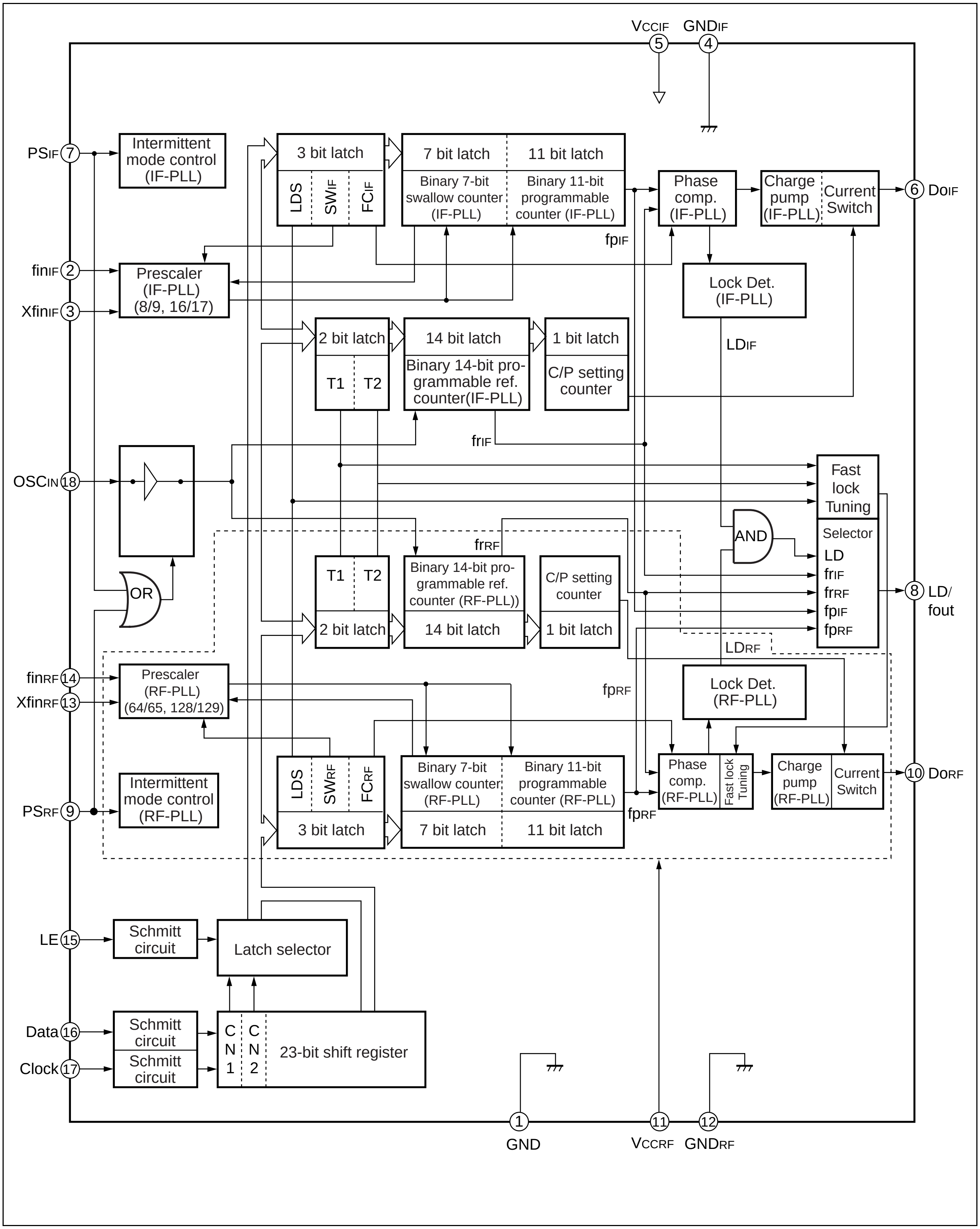


(LCC-18P-M05)

■ PIN DESCRIPTION

Pin no. BCC	Pin name	I/O	Descriptions
1	GND	—	Ground pin for OSC input buffer and the shift register circuit.
2	fin_{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
3	$Xfin_{IF}$	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
4	GND_{IF}	—	Ground pin for the IF-PLL section.
5	V_{CCIF}	—	Power supply voltage input pin for the IF-PLL section, the shift register and the oscillator input buffer.
6	Do_{IF}	O	Charge pump output for the IF-PLL section.
7	PS_{IF}	I	Power saving mode control pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{IF} = “H” ; Normal mode/PS_{IF} = “L” ; Power saving mode
8	LD/fout	O	Lock detect signal output (LD) /phase comparator monitoring output (fout) pin. The output signal is selected by LDS bit in a serial data. LDS bit = “H” ; outputs fout signal/LDS bit = “L” ; outputs LD signal
9	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{RF} = “H” ; Normal mode/PS_{RF} = “L” ; Power saving mode
10	Do_{RF}	O	Charge pump output for the RF-PLL section.
11	V_{CCRF}	—	Power supply voltage input pin for the RF-PLL section.
12	GND_{RF}	—	Ground pin for the RF-PLL section
13	$Xfin_{RF}$	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
14	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be via AC coupling.
15	LE	I	Load enable signal input pin (with the schmitt trigger circuit) When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
16	Data	I	Serial data input pin (with the schmitt trigger circuit) Data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
17	Clock	I	Clock input pin for the 23-bit shift register (with the schmitt trigger circuit) One bit data is shifted into the shift register on a rising edge of the clock.
18	OSC_{IN}	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min	Max	
Power supply voltage		V_{CC}	–0.5	4.0	V
Input voltage		V_I	–0.5	V_{CC} + 0.5	V
Output voltage	LD/fout	V_O	GND	V_{CC}	V
	Do_{IF}, Do_{RF}	V_{DO}	GND	V_{CC}	V
Storage temperature		Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.4	2.7	3.6	V	$V_{CCRF} = V_{CCIF}$
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	–40	—	+85	°C	

Notes :
- V_{CCRF}, V_{CCIF} must supply equal voltage.
  Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF}, V_{CCIF} to keep them equal.
  It is recommended that the non-use PLL is controlled by power saving function.
- Although this device contains an anti-static element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device.
  - When storing and transporting the device, put it in a conductive case.
  - Before handling the device, confirm the (jigs and) tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on working bench.
  - Before fitting the device into or removing it from the socket, turn the power supply off.
  - When handling (such as transporting) the device mounted board, protect the leads with a conductive sheet.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current		I_{CCIF} *1	fin_{IF} = 480 MHz V_{CCIF} = 2.7 V	0.8	1.2	1.7	mA
		I_{CCRF} *1	fin_{RF} = 2000 MHz V_{CCRF} = 2.7 V	1.3	2.0	2.8	mA
Power saving current		I_{PSIF}	PS_{IF} = PS_{RF} = “L”	—	0.1 *2	10	µA
		I_{PSRF}	PS_{IF} = PS_{RF} = “L”	—	0.1 *2	10	µA
Operating frequency	fin_{IF} *3	fin_{IF}	IF PLL	50	—	600	MHz
	fin_{RF} *3	fin_{RF}	RF PLL	200	—	2250	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	–15	—	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	–15	—	+2	dBm
Input available voltage	OSC_{IN}	V_{OSC}	—	0.5	—	1.5	V_{P-P}
“H” level input voltage	Data LE Clock	V_{IH}	Schmitt triger input	0.7 V_{CC} + 0.4	—	—	V
“L” level input voltage		V_{IL}	Schmitt triger input	—	—	0.3 V_{CC} – 0.4	V
“H” level input voltage	PS_{IF} PS_{RF}	V_{IH}	—	0.7 V_{CC}	—	—	V
“L” level input voltage		V_{IL}	—	—	—	0.3 V_{CC}	V
“H” level input current	Data LE Clock PS	I_{IH} *4	—	–1.0	—	+1.0	µA
“L” level input current		I_{IL} *4	—	–1.0	—	+1.0	µA
“H” level output voltage	LD/ fout	V_{OH}	V_{CC} = 2.7 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
“L” level output voltage		V_{OL}	V_{CC} = 2.7 V, I_{OL} = 1 mA	—	—	0.4	V
“H” level output voltage	Do_{IF} Do_{RF}	V_{DOH}	V_{CC} = 2.7 V, I_{DOH} = –0.5 mA	V_{CC} – 0.4	—	—	V
“L” level output voltage		V_{DOL}	V_{CC} = 2.7 V, I_{DOL} = 0.5 mA	—	—	0.4	V
High impedance cutoff current	Do_{IF} Do_{RF}	I_{OFF}	V_{CC} = 2.7 V V_{OFF} = 0.5 V to Vcc – 0.5 V	—	—	2.5	nA
“H” level output current	LD/ fout	I_{OH} *4	V_{CC} = 2.7 V	—	—	–1.0	mA
“L” level output current		I_{OL}	V_{CC} = 2.7 V	1.0	—	—	mA

(Continued)

(Continued)

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition		Value			Unit
					Min	Typ	Max	
"H" level output current	Do_{IF} *8 Do_{RF}	I_{DOH} *4	V_{CC} = 2.7 V, V_{DOH} = Vcc / 2, Ta = +25 °C	CS bit = "1"	–8.2	–6.0	–4.1	mA
				CS bit = "0"	–2.2	–1.5	–0.8	mA
"L" level output current	Do_{IF} *8 Do_{RF}	I_{DOL}	V_{CC} = 2.7 V, V_{DOL} = Vcc / 2, Ta = +25 °C	CS bit = "1"	4.1	6.0	8.2	mA
				CS bit = "0"	0.8	1.5	2.2	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = Vcc / 2		—	3	—	%
	vs V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ Vcc – 0.5 V		—	10	—	%
	vs Ta	I_{DOTA} *7	–40 °C ≤ Ta ≤ +85 °C, V_{DO} = Vcc / 2		—	5	—	%

*1 : Conditions ; fosc = 12.8 MHz, Ta = +25 °C, SW = "0" in locking state.

*2 : V_{CCIF} = V_{CCRF} = 2.7 V, fosc = 12.8 MHz, Ta = +25 °C, in power saving mode.
PS_{IF} = PS_{RF} = GND
V_{IH} = V_{CC}, V_{IL} = GND (at CLK, Data, LE)

*3 : AC coupling. 1000 pF capacitor is connected under the condition of Min operating frequency.

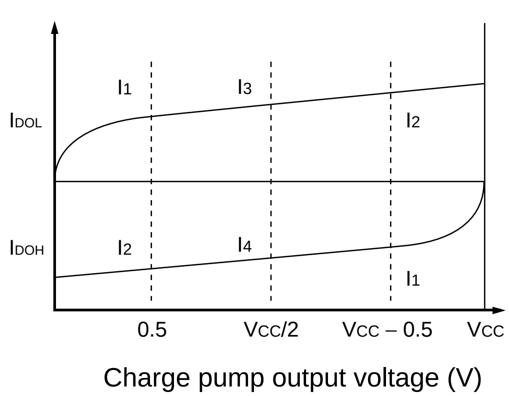
*4 : The symbol "–" (minus) means the direction of current flow.

*5 : V_{CC} = 2.7 V, Ta = +25 °C ($||I_3| - |I_4||$) / [($|I_3| + |I_4|$) / 2] × 100 (%)

*6 : V_{CC} = 2.7 V, Ta = +25 °C [($||I_2| - |I_1||$) / 2] / [($|I_1| + |I_2|$) / 2] × 100 (%) (Applied to both I_{DOL} and I_{DOH})

*7 : V_{CC} = 2.7 V, [$||I_{DO}(+85\ °C)| - |I_{DO}(-40\ °C)||$ / 2] / [$|I_{DO}(+85\ °C)| + |I_{DO}(-40\ °C)|$ / 2] × 100 (%) (Applied to both I_{DOL} and I_{DOH})

*8 : When Charge pump current is measured, set LDS = "0" , T1 = "0" and T2 = "1".



■ FUNCTIONAL DESCRIPTION

1. Pulse swallow function

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (8 or 16 for IF-PLL, 64or 128 for RF-PLL)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$, $A < N$)
f_{OSC} : Reference oscillation frequency (OSC_{IN} input frequency)
R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

The serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.
The serial data of binary data is entered through Data pin.
On rising edge of Clock, one bit of the serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable reference counter for the RF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration

• **Programmable Reference Counter**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CS : Charge pump current select bit
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383)
T1, T2 : LD/fout output setting bit
CN1, CN2 : Control bit
X : Dummy bits (Set “0” or “1”)

Note : Data input with MSB first.

• Programmable Counter

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	$SW_{IF/RF}$	$FC_{IF/RF}$	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127)
N1 to N11 : Divide ratio setting bits for the programmable counter (3 to 2,047)
LDS : LD/fout signal select bit
$SW_{IF/RF}$: Divide ratio setting bit for the prescaler (IF : SW_{IF}, RF : SW_{RF})
$FC_{IF/RF}$: Phase control bit for the phase detector (IF : FC_{IF}, RF : FC_{RF})
CN1, 2 : Control bit

Note : Data input with MSB first.

(2) Data setting

• Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 11-bit Programmable Counter Data Setting

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited

• Binary 7-bit Swallow Counter Data Setting

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

- Prescaler Data Setting

Divide ratio	SW = "1"	SW = "0"
Prescaler divide ratio IF-PLL	8/9	16/17
Prescaler divide ratio RF-PLL	64/65	128/129

- Charge Pump Current Setting

Current value	CS
±6.0 mA	1
±1.5 mA	0

- LD/fout output Selectable Bit Setting

LD/fout pin state		LDS	T1	T2
LD output		0	0	0
		0	1	0
		0	1	1
fout output	fr_{IF}	1	0	0
	fr_{RF}	1	1	0
	fp_{IF}	1	0	1
	fp_{RF}	1	1	1

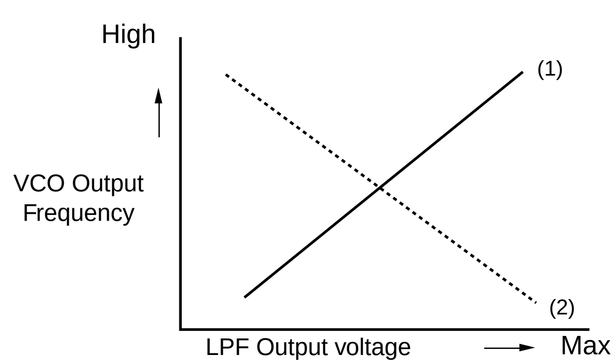
- Phase Comparator Phase Switching Data Setting

Phase comparator input	FC_{IF}, FC_{RF} = "1"	FC_{IF}, FC_{RF} = "0"
	Do_{IF}, Do_{RF}	Do_{IF}, Do_{RF}
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.

(1) VCO polarity FC = "1"
(2) VCO polarity FC = "0"



Note : Give attention to the polarity for using active type LPF.

3. Power Saving Mode (Intermittent Mode Control Circuit)

Status	PS pin
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

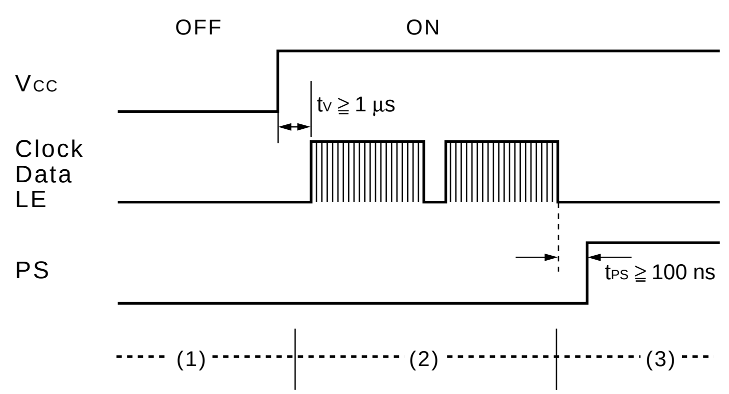
For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparaor output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

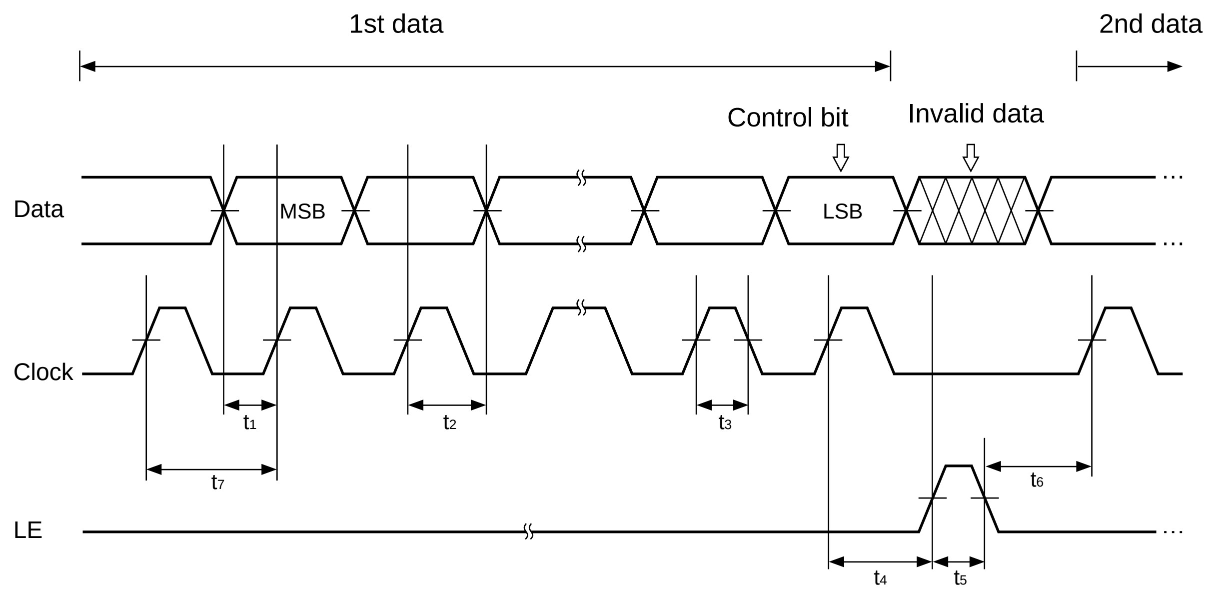
Notes :
- When power (VCC) is first applied, the device must be in standby mode, PS = Low, for at least 1 µs.
- Serial data input are done after the power supply becomes stable, and then the power saving mode is released after completed the data input.



(1) PS = L (power saving mode) at Power-ON
(2) Set serial data at least 1 µs after the power supply becomes stable ($V_{CC} \geq 2.2$ V) .
(3) Release power saving mode (PS_{IF}, PS_{RF} : “L” → “H”) at least 100 ns later after setting serial data.

4. Serial Data Data Input Timing

Divide ratio is performed through a serial interface using the Data pin, Clock pin, and LE pin.
Setting data is read into the shift register at the rise of the Clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

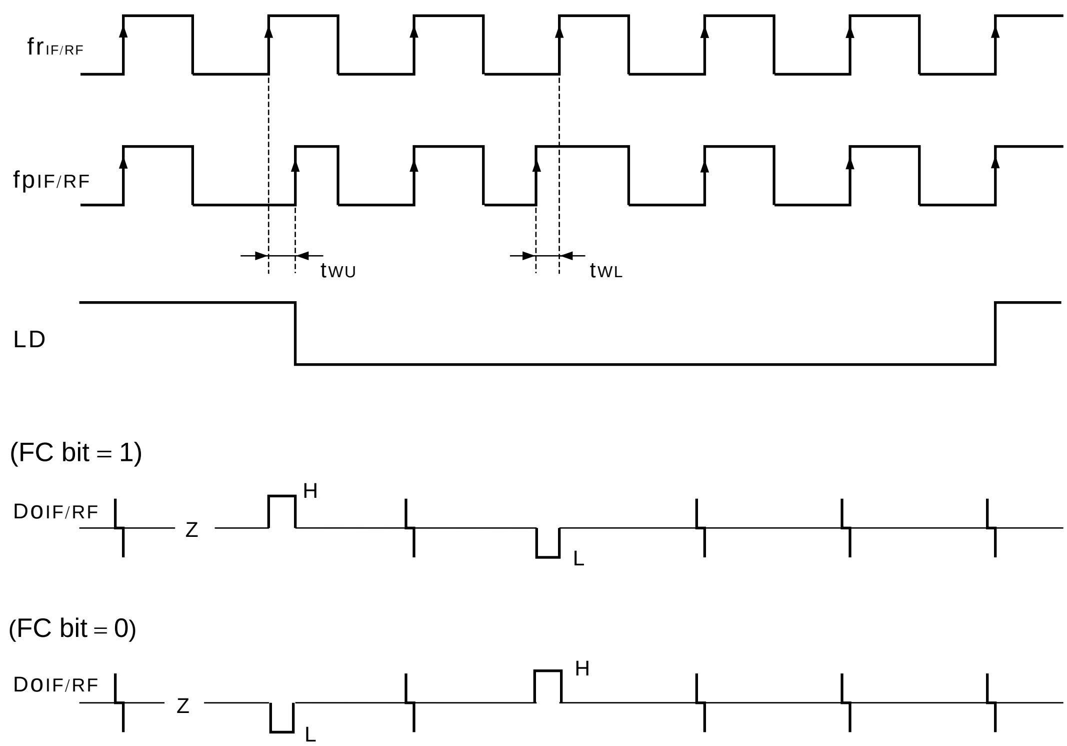


Parameter	Min	Typ	Max	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

Parameter	Min	Typ	Max	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note : LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



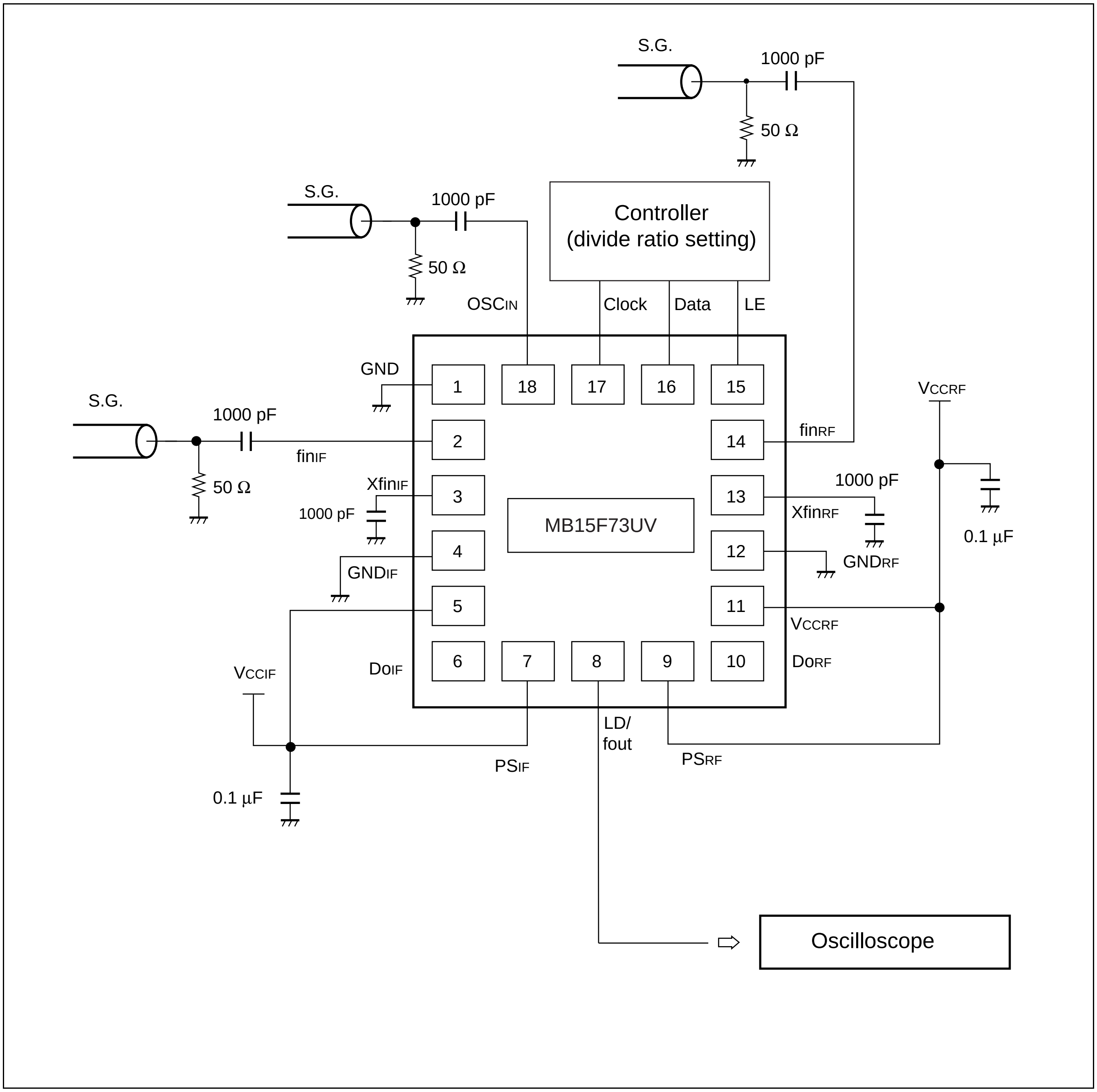
- LD Output Logic

IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes :
- Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{IF/RF}$ signals during locking state are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.

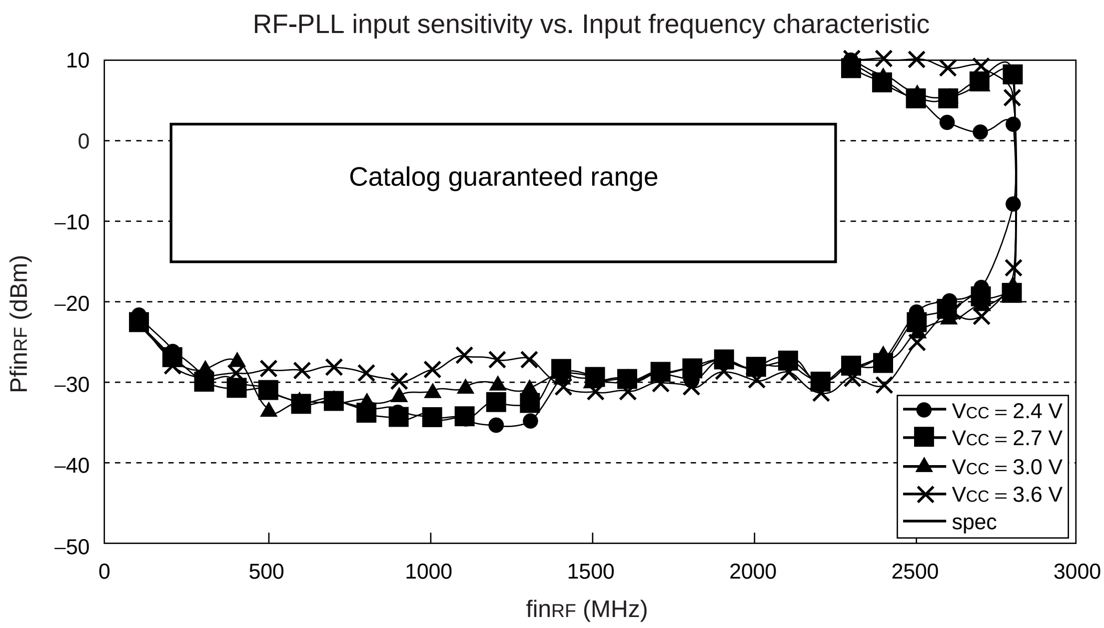
  $t_{WU} \geq 2/fosc$: e.g. $t_{WU} \geq 156.3$ ns when fosc = 12.8 MHz
  $t_{WU} \leq 4/fosc$: e.g. $t_{WL} \leq 312.5$ ns when fosc = 12.8 MHz

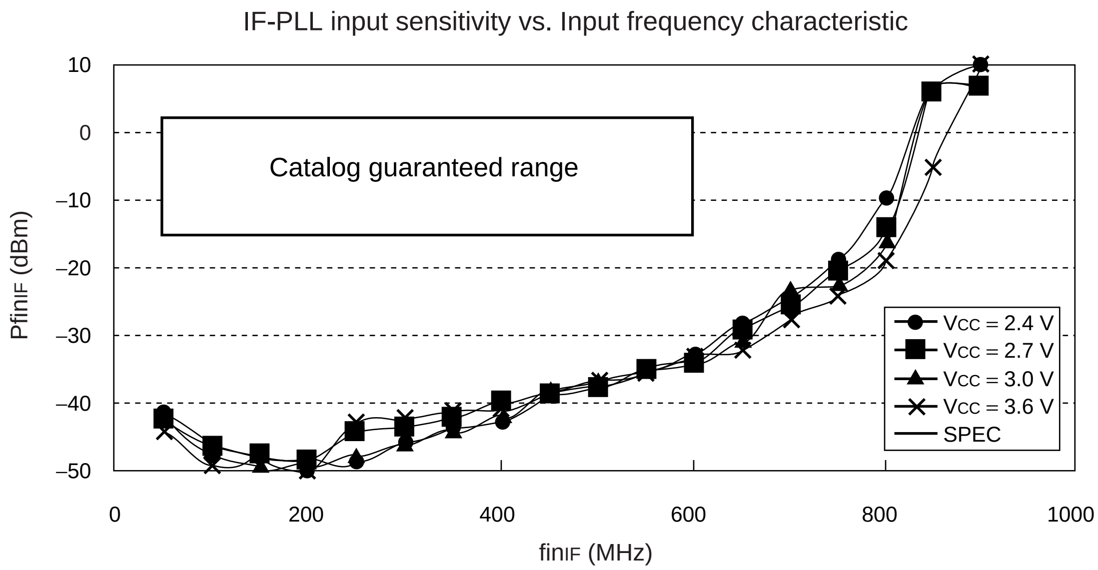
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC$_{IN}$)



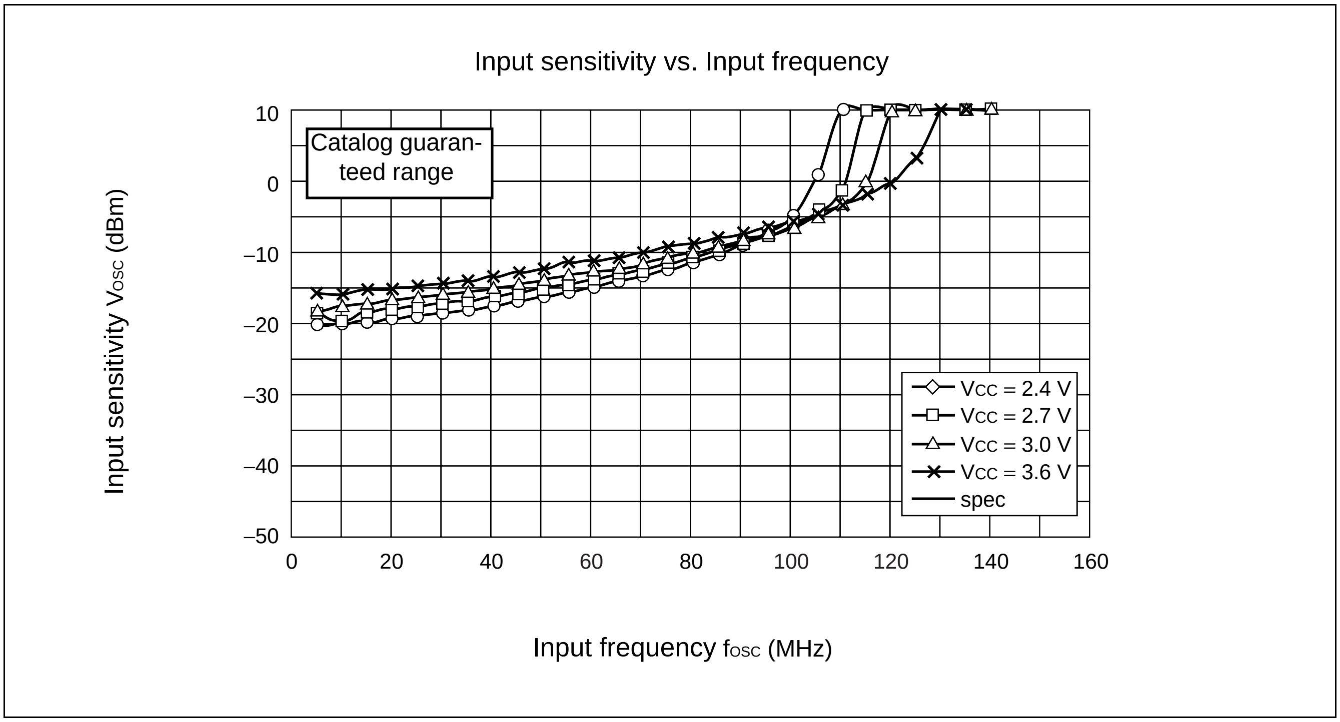
■ TYPICAL CHARACTERISTICS

1. fin input sensitivity





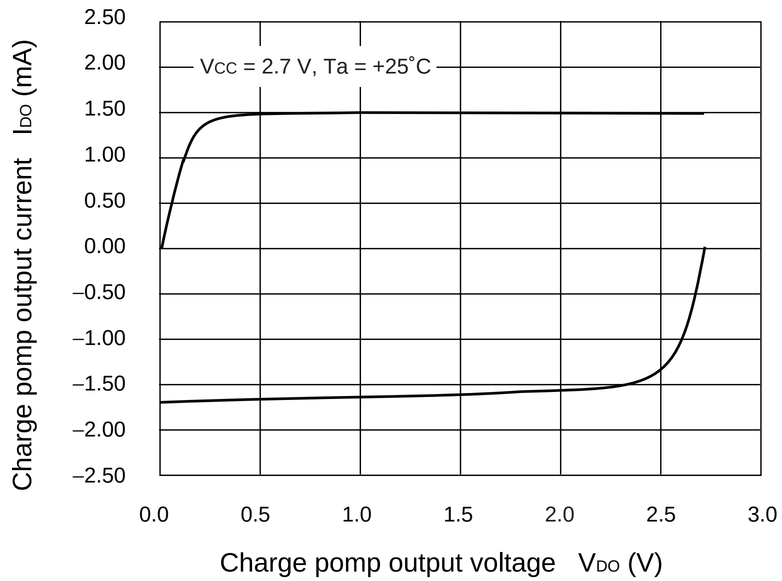
2. OSC_{IN} input sensitivity



3. RF/IF-PLL Do output current

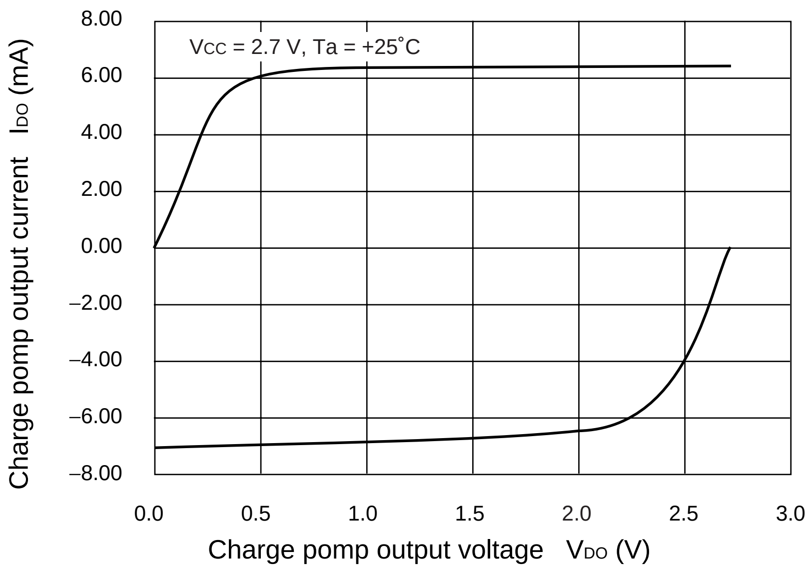
- CP = 1.5 mA

Charge Pomp Output Voltage vs. Charge Pomp Output Current



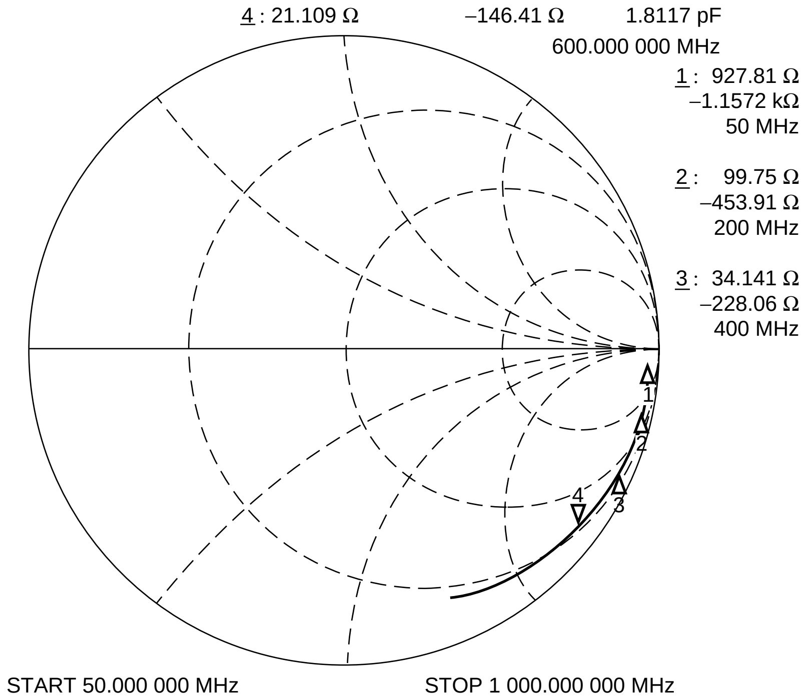
- CP = 6.0 mA

Charge Pomp Output Voltage vs. Charge Pomp Output Current

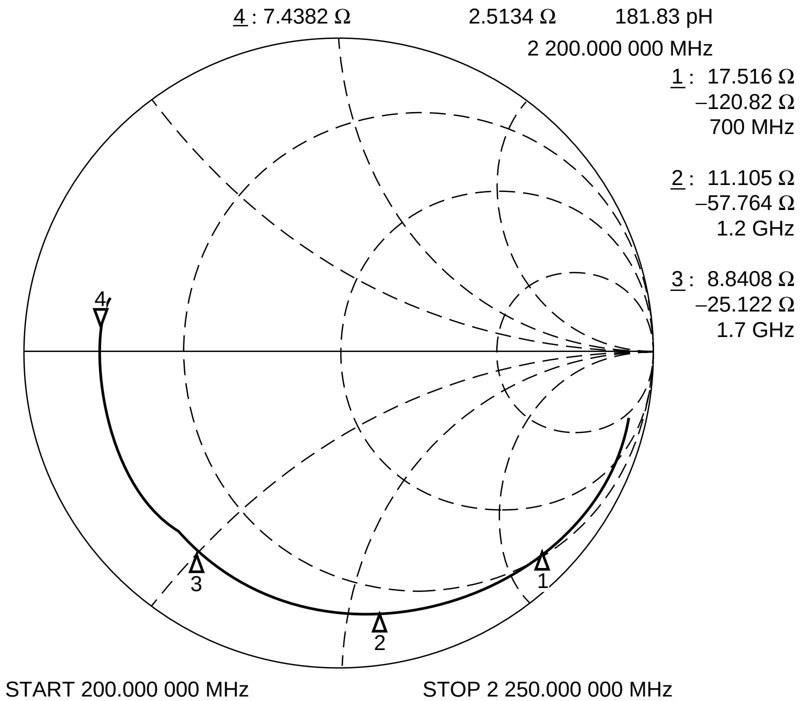


4. fin input impedance

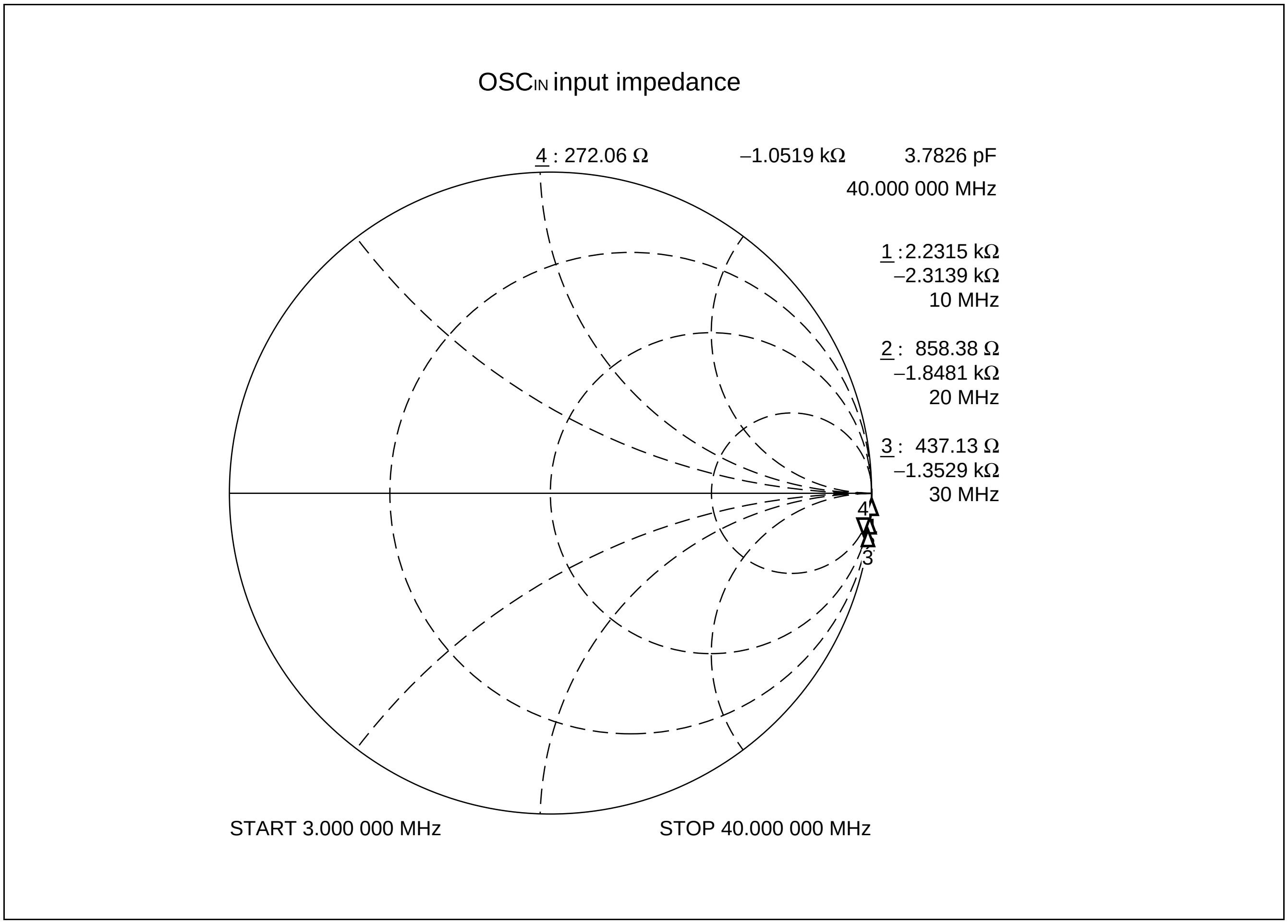
finIF input impedance



finRF input impedance

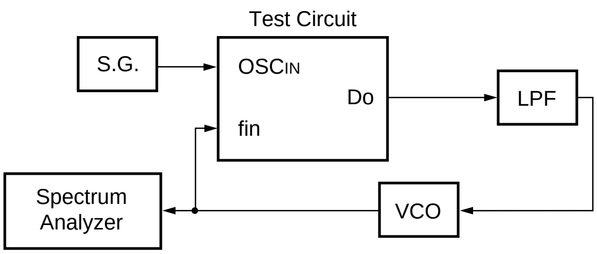


5. OSC$_{IN}$ input impedance

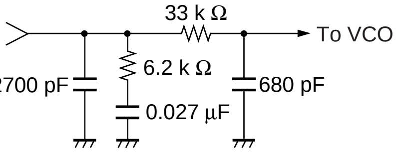


■ REFERENCE INFORMATION

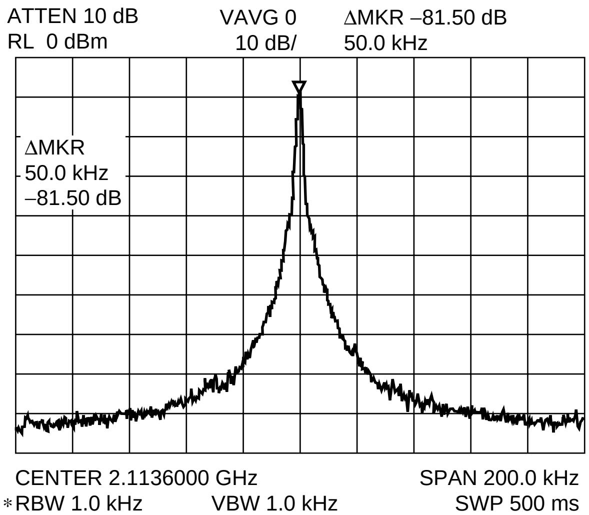
(for Lock-up Time, Phase Noise and Reference Leakage)



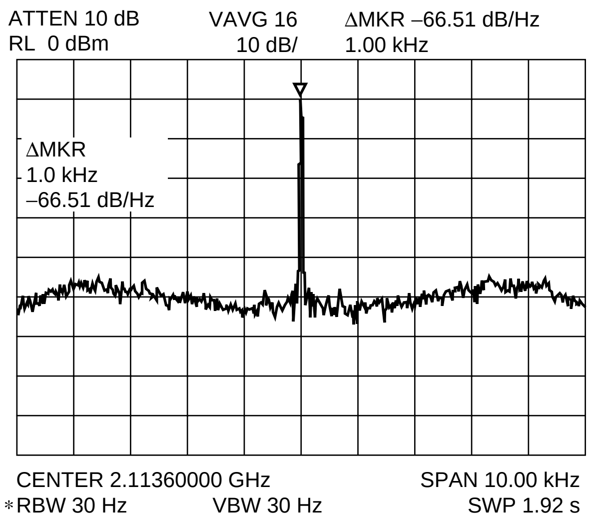
fVCO = 2113.6 MHz VCC = 2.7 V
KV = 50 MHz/V VVCO = 2.8 V
fr = 50 kHz Ta = + 25 °C
fosc = 19.2 MHz CP : 1.5 mA mode
LPF



• PLL Reference Leakage



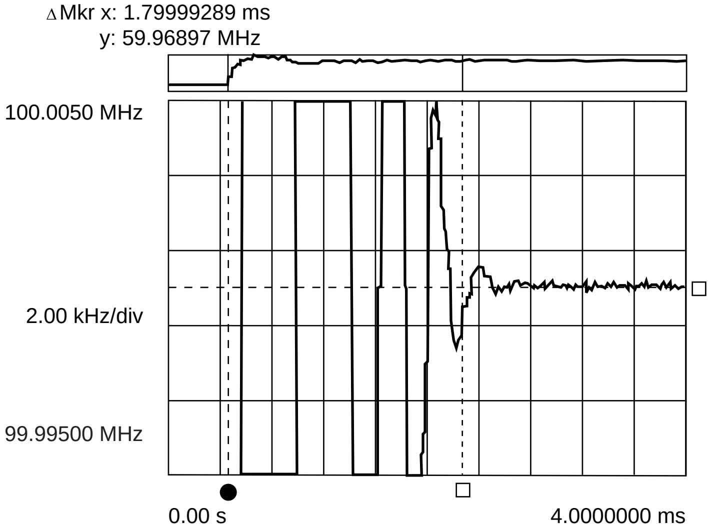
• PLL Phase Noise



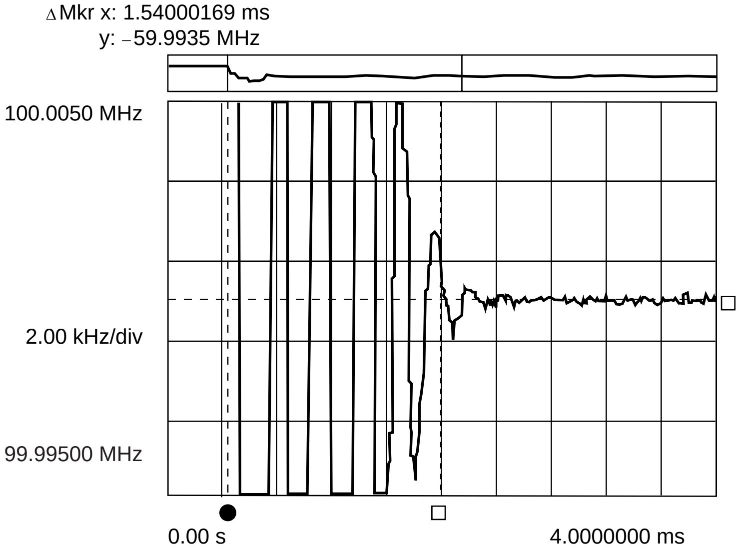
(Continued)

(Continued)

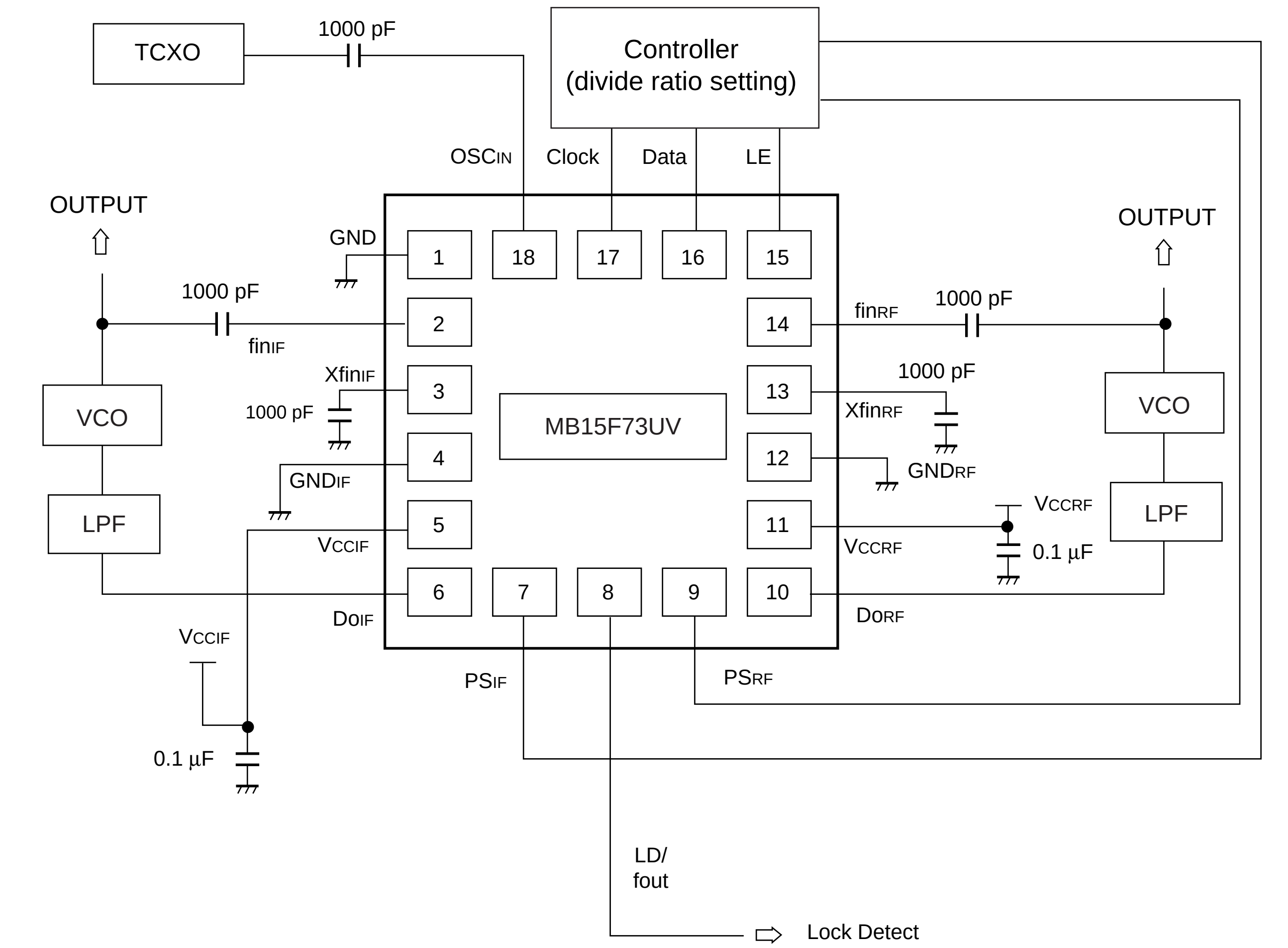
PLL Lock Up time
2113.6 MHz→2173.6 MHz ± 1 kHz
L ch→H ch 1.80 ms



PLL Lock Up time
2173.6 MHz→2113.6 MHz ± 1 kHz
H ch→L ch 1.54 ms



■ APPLICATION EXAMPLE



Note : Clock, Data, LE : The schmitt trigger circuit is provided (insert a pull-down or pull-up register to prevent oscillation when open-circuit in the input) .

■ USAGE PRECAUTIONS

(1) V_{CCRF} and V_{CCIF} must be equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

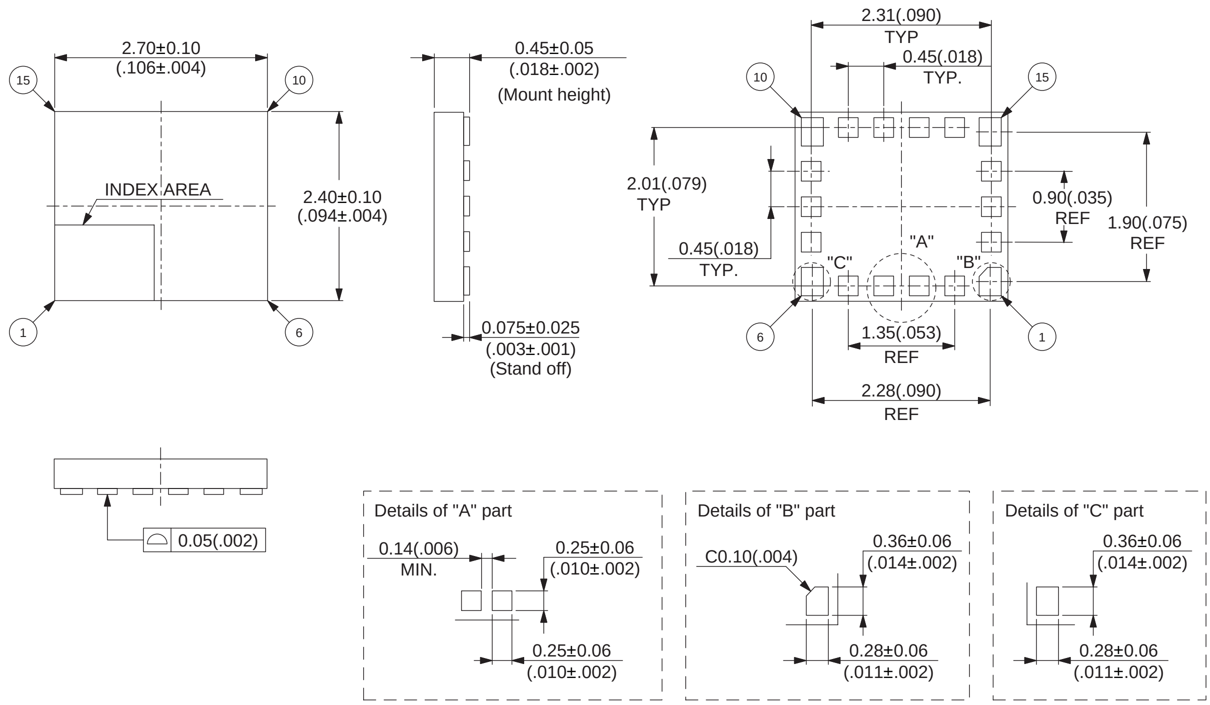
(2) To protect against damage by electrostatic discharge, note the following handling precautions :
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F73UVPVB	18-pin plastic BCC (LCC-18P-M05)	

■ PACKAGE DIMENSIONS

18-pin plastic BCC
(LCC-18P-M05)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

FUJITSU LIMITED

F0312