FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27228-2E

ASSP

For Power Supply Applications (General Purpose DC/DC Converter)

2-Channel DC/DC Converter IC
with Overcurrent Protection Symmetrical-Phase Type

MB3886

■ DESCRIPTION

The MB3886 is a symmetrical-phase type of two-channel, DC/DC converter IC using pulse width modulation (PWM) , incorporating an overcurrent protection circuit (requiring no current sense resistor) and an overvoltage protection circuit. Providing high output driving capabilities, the MB3886 is suitable for down-conversion.
The MB3886 adopts both synchronous rectification to provide high efficiency and symmetrical phasing (two anti-phase triangular waves) which contributes to making the input capacitor small.
The MB3886 contains a 5-volt regulator resulting in a reduced number of components used. It also contains a variety of protection features which output the protection status upon detection of an overvoltage or overcurrent while reducing the number of external protective devices required.
The result is an ideal built-in power supply for driving products with high speed CPU's such as home TV game devices and notebook PC's.
This product is covered by US Patent Number 6,147,477.

■ FEATURES

- Overcurrent protection circuit (requiring no current sense resistor) and overvoltage protection circuit
- Power-supply voltage range : 5.5 V to 18 V
- Synchronous rectification system providing high efficiency
- PSIG pins (open-drain) to output the protection status

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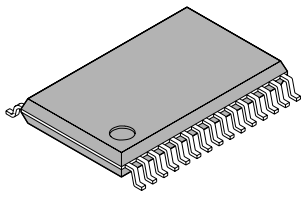
■ PACKAGE

30-pin plastic SSOP



(FPT-30P-M02)

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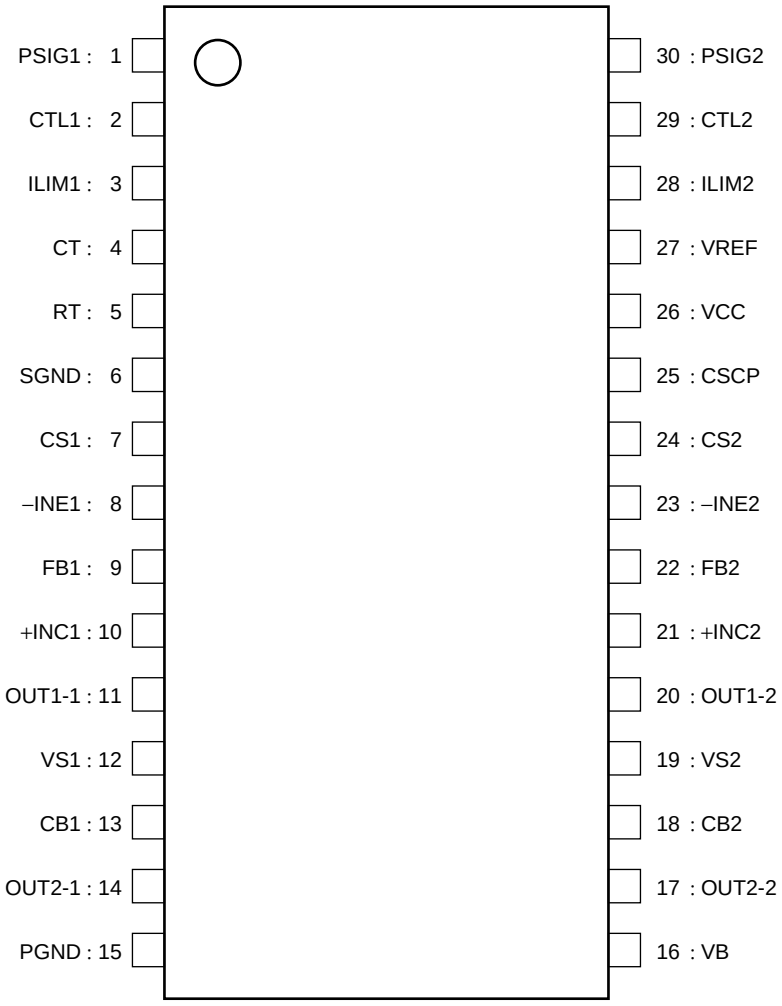
- Symmetrical-phase system reducing the input capacitor loss
- Built-in channel control function
- Reference voltage : 3.5 V ± 1%
- Error amplifier threshold voltage : 1.25 V ± 1% (0 °C to 85 °C)
- Oscillator frequency range : 10 kHz to 500 kHz
- Built-in circuit for load-independent soft-start and discharge control
- Totem-pole type output for N-ch MOSFET

■ PIN ASSIGNMENT

(TOP VIEW)



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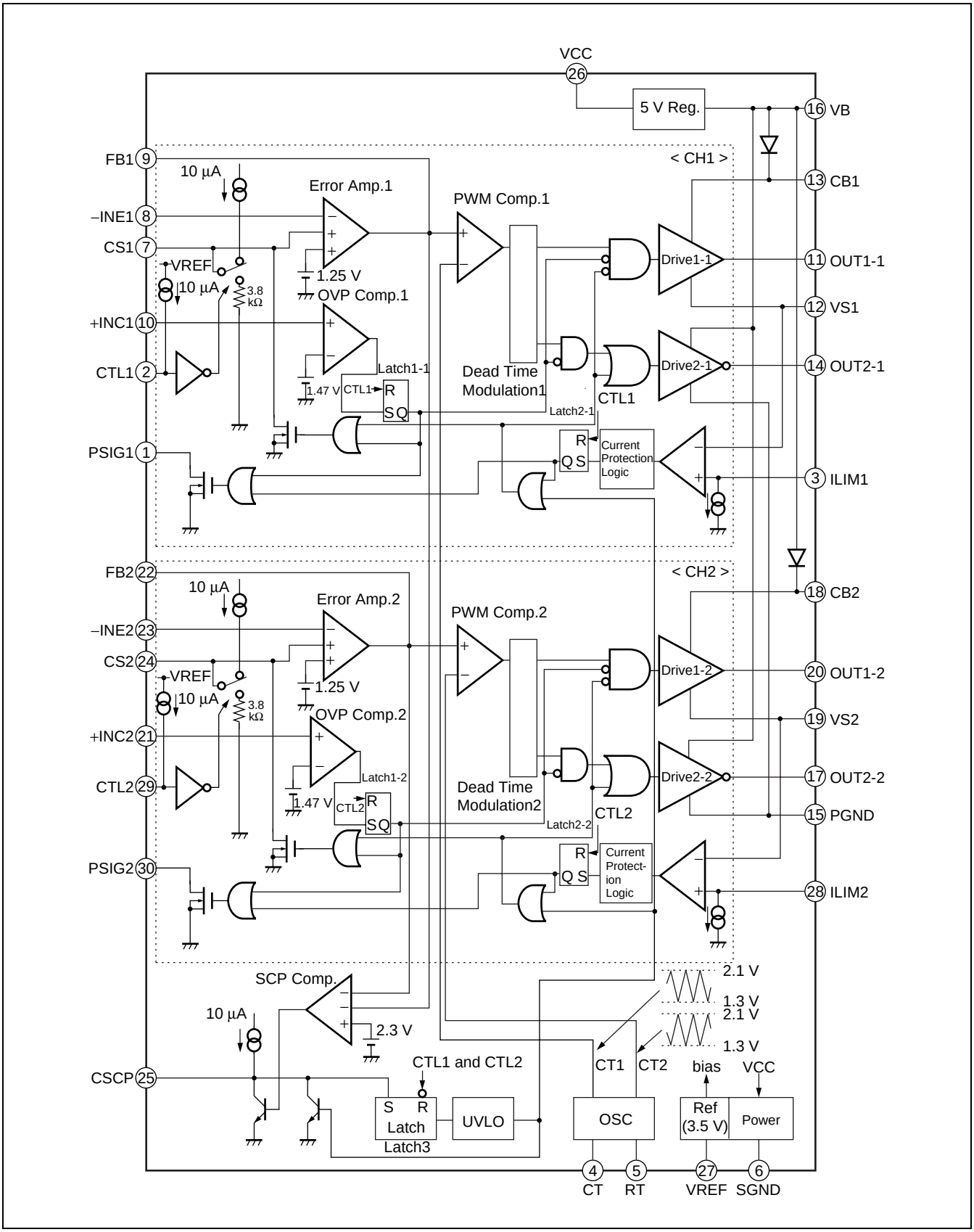
■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	PSIG1	O	CH1 protection status output terminal
2	CTL1	I	CH1 control terminal “H” level : CH1 ON state “L” level : CH1 OFF state and protection status reset
3	ILIM1	I	CH1 overcurrent detection resistor connection terminal
4	CT	—	Triangular waveform oscillation frequency setting capacitor connection terminal
5	RT	—	Triangular waveform oscillation frequency setting resistor connection terminal
6	SGND	—	Ground terminal
7	CS1	—	CH1 soft-start capacitor connection terminal
8	–INE1	I	CH1 error amp. inverting input terminal
9	FB1	O	CH1 error amp. output terminal
10	+INC1	I	CH1 overvoltage comparator noninverting input terminal
11	OUT1-1	O	CH1 totem-pole output terminal (External main-side FET gate drive)
12	VS1	—	CH1 external main-side FET source connection terminal
13	CB1	—	CH1 boot capacitor connection terminal Connect a capacitor between the CB1 and VS1 terminals.
14	OUT2-1	O	CH1 totem-pole output terminal (External synchronous-rectification-side FET gate drive)
15	PGND	—	Ground terminal
16	VB	O	Output circuit bias output terminal
17	OUT2-2	O	CH2 totem-pole output terminal (External synchronous-rectification-side FET gate drive)
18	CB2	—	CH2 boot capacitor connection terminal Connect a capacitor between the CB2 and VS2 terminals.
19	VS2	—	CH2 external main-side FET source connection terminal
20	OUT1-2	O	CH2 totem-pole output terminal (External main-side FET gate drive)
21	+INC2	—	CH2 overvoltage comparator noninverting input terminal
22	FB2	O	CH2 error amp. output terminal
23	–INE2	I	CH2 error amp. inverting input terminal
24	CS2	—	CH2 soft-start capacitor connection terminal
25	CSCP	—	Timer-latch short-circuit protection capacitor connection terminal
26	VCC	—	Reference voltage, control circuit power supply terminal
27	VREF	O	Reference voltage output terminal
28	ILIM2	I	CH2 overcurrent detection resistor connection terminal
29	CTL2	I	CH2 control terminal “H” level : CH2 ON state “L” level : CH2 OFF state and protection status reset
30	PSIG2	O	CH2 protection status output terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power-supply voltage	V_{CC}	—	—	20	V
Boot voltage	V_{CB}	CB terminal	—	25	V
Output current	I_O	—	—	120	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1 / f_{OSC} × Duty)	—	800	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	770*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power-supply voltage	V_{CC}	—	5.5	12	18	V
Boot voltage	V_{CB}	CB terminal	—	—	23	V
Reference voltage output current	I_{OR}	VREF terminal	−1	—	0	mA
Bias output current	I_{OB}	VB terminal	−1	—	0	mA
Input voltage	V_{IN}	−INE terminal	0	—	V_{CC} − 1.8	V
	V_{INC}	+INC terminal	0	—	V_{CC}	V
	V_{CTL}	CTL terminal	0	—	V_{REF}	V
Output voltage	V_{PSIG}	PSIG terminal	0	—	15	V
Output current	I_O	—	−100	—	100	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1 / fosc × Duty)	−700	—	700	mA
Oscillator frequency	f_{OSC}	—	10	290	500	kHz
Timing resistor	R_T	—	6.8	9.1	12	kΩ
Timing capacitor	C_T	—	150	330	15000	pF
Boot capacitor	C_B	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	VREF terminal	—	0.1	1.0	µF
Bias output capacitor	C_{VB}	VB terminal	1.0	4.7	10	µF
Soft-start capacitor	C_S	—	—	0.1	1	µF
Short-circuit detection capacitor	C_{SCP}	—	—	0.01	1	µF
Overcurrent detection setting resistor	R_{LIM}	—	0.1	1	10	kΩ
Operating ambient temperature	Ta	—	−30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Values			Unit
					Min	Typ	Max	
1. Reference Voltage Block [Ref]	Output voltage	V_{REF}	27	Ta = +25 °C	3.465	3.500	3.535	V
		$\Delta V_{REF}/V_{REF}$	27	Ta = 0 °C to +85 °C	—	0.5*	—	%
	Input stability	Line	27	VCC = 5.5 V to 18 V	—	1	10	mV
	Load stability	Load	27	VREF = 0 mA to –1 mA	—	3	10	mV
	Short-circuit output current	Ios	27	VREF = 2 V	–28	–14	–7	mA
2. Bias Voltage Block [VB]	Output voltage	V_B	16	—	5.0	5.1	5.2	V
3. Triangular Waveform Oscillator Block [OSC]	Oscillator frequency	f_{OSC}	4	RT = 9.1 kΩ, CT = 330 pF	260	290	320	kHz
	Frequency/ temperature variation	$\Delta f_{OSC}/f_{OSC}$	4	Ta = 0 °C to 85 °C	—	1*	—	%
4. Undervoltage (VCC) Lockout Circuit Block [UVLO]	Threshold voltage	V_{TH}	26	VCC = ↓	4.7	4.9	5.1	V
	Hysteresis width	V_H	26	—	—	0.35*	—	V
	Reset voltage	V_{RST}	26	—	1.7	2.1	2.5	V
5. Short-circuit Protection Circuit Block [SCP]	Threshold voltage	V_{TH}	25	—	0.63	0.68	0.73	V
	Input source current	I_{CSCP}	25	—	–14	–10	–6	µA
6. Overcurrent Protection Circuit Block [OCP]	ILIM terminal input current	I_{LIM}	3, 28	RT = 9.1 kΩ	106	118	130	µA
	Offset voltage	V_{IO}	3, 28	—	—	1*	—	mV
7. Overvoltage Protection Circuit Block [OVP]	Threshold voltage	V_{TH}	10, 21	+INC = ↓	1.44	1.47	1.50	V
	Input bias current	I_B	10, 21	+INC = 0 V	–200	–30	—	nA
8. Latches Block [Latch1 to Latch3]	Reset voltage	V_{RST}	2, 29	CTL = ↓	0.8	1.4	2	V
9. Protection Status Output Circuit Block [PSIG]	Output leakage current	I_{LEAK}	1, 30	PSIG = 5 V	—	—	40	µA
	Output low-level voltage	V_{OL}	1, 30	PSIG = 1 mA	—	0.1	0.4	V

* : Typical design value

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(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Values			Unit
					Min	Typ	Max	
10. Soft-start Circuit Block [CS]	Charge current	I_{CS}	7, 24	—	–14	–10	–6	µA
11. Error Amp. Block [Error Amp.]	Threshold voltage	V_{TH1}	8, 23	FB = 1.7 V, Ta = +25 °C	1.241	1.2500	1.259	V
		V_{TH2}	8, 23	FB = 1.7 V, Ta = 0 °C to 85 °C	1.2375	1.2500	1.2625	V
	Input bias current	I_B	8, 23	–INE = 0 V	–200	–20	—	nA
	Voltage gain	A_V	9, 22	DC	60	100	—	dB
	Frequency bandwidth	BW	9, 22	A_V = 0 dB	—	1500*	—	kHz
	Output voltage	V_{FBH}	9, 22	—	2.4	2.7	—	V
		V_{FBL}	9, 22	—	—	0.8	1.0	V
	Output source current	I_{SOURCE}	9, 22	FB = 1.7 V	—	–100	–45	µA
	Output sink current	I_{SINK}	9, 22	FB = 1.7 V	1.5	9.0	—	mA
12. PWM Comparator Block [PWM Comp.]	Threshold voltage	V_{TL}	9, 22	Duty cycle = 0%	1.2	1.3	—	V
		V_{TH}	9, 22	Duty cycle = Dtr	—	2.02	2.2	V
13. Dead Time Control Block [DTC]	Maximum duty cycle	Dtr	11, 20	RT = 9.1 kΩ, CT = 330 pF	73	78	83	%
14. Output Block [Drive]	Output current (main side)	$I_{SOURCE1}$	11, 20	Duty ≤ 5% (t = 1 / fosc × Duty)	—	–700*	—	mA
		I_{SINK1}	11, 20	Duty ≤ 5% (t = 1 / fosc × Duty)	—	900*	—	mA
	Output voltage (main side)	V_{OH1}	11, 20	OUT1 = –100 mA, CB = 13.5 V, VS = 12 V	V_{CB} – 2.5	V_{CB} – 0.9	—	V
		V_{OL1}	11, 20	OUT1 = 100 mA, CB = 13.5 V, VS = 12 V	—	V_S + 0.9	V_S + 1.4	V
	Output current (synchronous rectification side)	$I_{SOURCE2}$	14, 17	Duty ≤ 5% (t = 1 / fosc × Duty)	—	–750*	—	mA
		I_{SINK2}	14, 17	Duty ≤ 5% (t = 1 / fosc × Duty)	—	900*	—	mA
	Output voltage (synchronous rectification side)	V_{OH2}	14, 17	OUT2 = –100 mA	2.5	4.1	—	V
		V_{OL2}	14, 17	OUT2 = 100 mA	—	1.0	1.4	V

* : Typical design value

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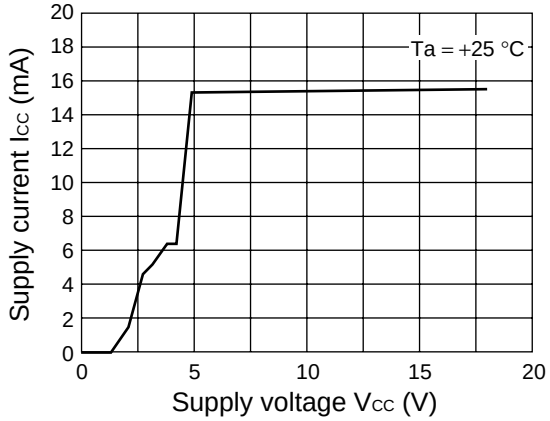
(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

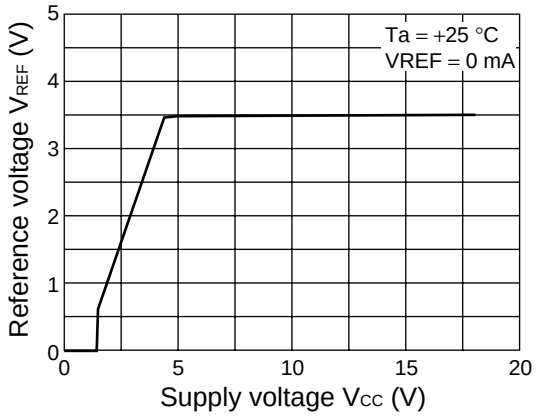
Parameter		Sym-bol	Pin No.	Conditions	Values			Unit
					Min	Typ	Max	
14. Output Block [Drive]	Diode voltage	V_D	13, 18	VB = 10 mA	—	0.9	1.1	V
	Dead time	t_D	11, 14 20, 17	OUT1 = OUT2 = OPEN, VS = 0 V	30	100	170	ns
15. Channel control Block [CTL]	Output ON condition	V_{ON}	2, 29	Output ON state	2	—	V_{REF}	V
	Output OFF condition	V_{OFF}	2, 29	Output OFF state	0	—	0.8	V
	Input current	I_{CTL}	2, 29	—	–14	–10	–6	µA
16. General	Power-supply current	I_{CC}	26	—	—	15	23	mA

■ TYPICAL CHARACTERISTICS

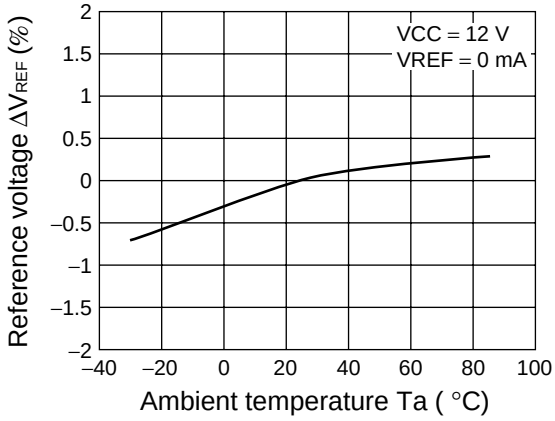
Supply Current vs. Supply Voltage



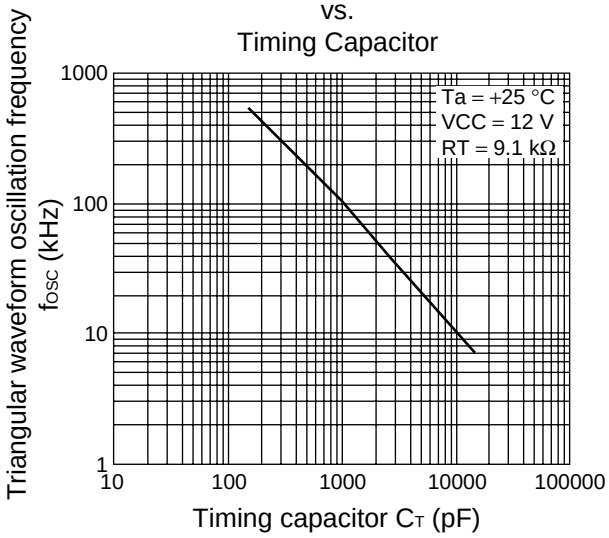
Reference Voltage vs. Supply Voltage



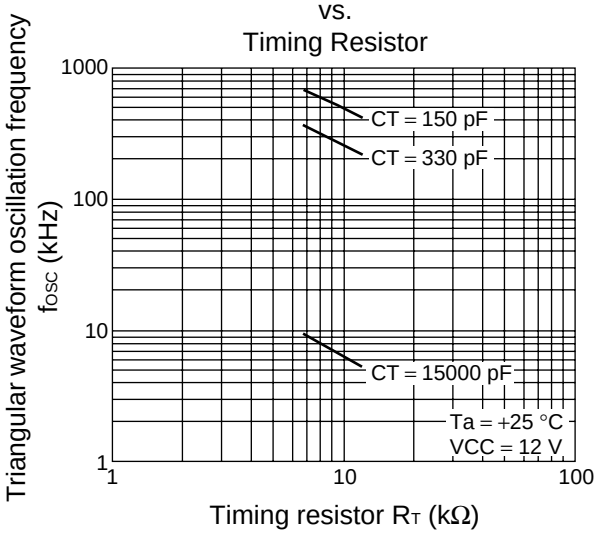
Reference Voltage vs. Ambient Temperature



Triangular Waveform Oscillation Frequency vs. Timing Capacitor



Triangular Waveform Oscillation Frequency vs. Timing Resistor



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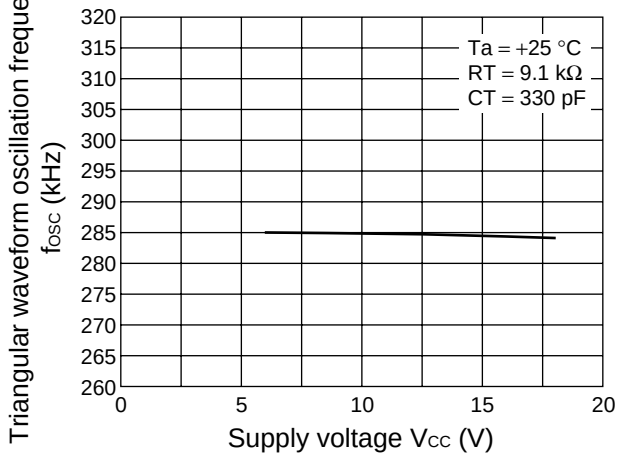
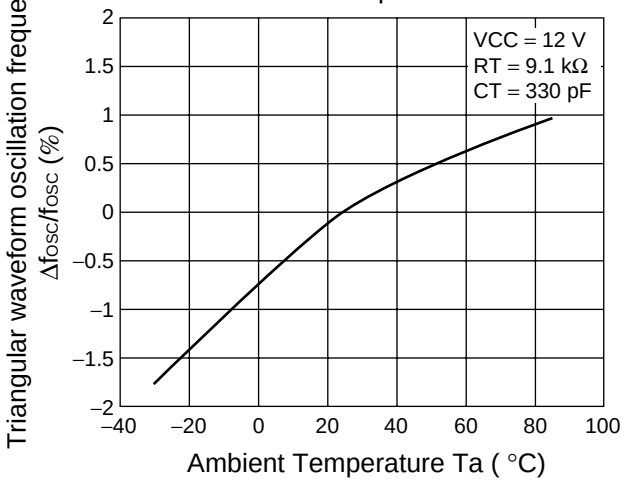
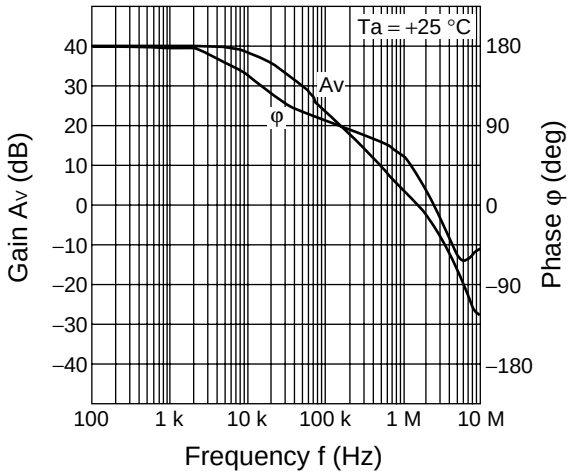
Triangular Waveform Oscillation Frequency vs. Supply Voltage

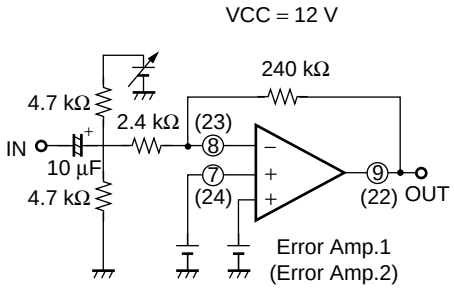


Triangular Waveform Oscillation Frequency vs. Ambient Temperature

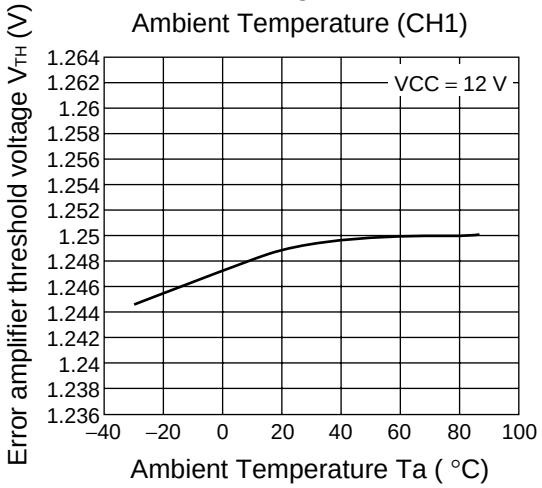


Error Amp. Gain/Phase vs. Frequency (CH1)

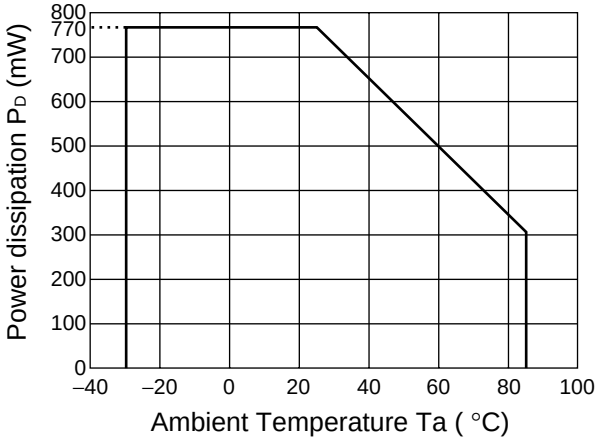




Error Amp. Threshold Voltage vs. Ambient Temperature (CH1)



Power Dissipation vs. Ambient Temperature



■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Functions

(1) Reference voltage Block

The reference voltage circuit generates a temperature-compensated reference voltage (typically 3.5 V) using the voltage supplied from the power supply terminal (pin 26) . The voltage is used as the reference voltage for the IC's internal circuitry.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VREF terminal (pin 27) .

(2) Triangular waveform oscillator Block

The triangular waveform oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 4) and RT terminal (pin 5) to generate oscillating triangular waveforms CT1 (amplitude of 1.3 V to 2.1 V) and CT2 (amplitude of 1.3 V to 2.1 V in antiphase with CT1) . The symmetrical-phase system using the two opposite-phase triangular waves reduces the input ripple current, resulting in a smaller input capacitor.

The oscillating triangular waveforms are input to the IC's internal PWM comparator and can be output to an external device through the CT terminal.

(3) Error Amp. Block (Error Amp.)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. It supports a wide range of in-phase input voltages from 0 V to "Vcc – 1.8 V", allowing easy setting from the external power supply.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverting input terminal of the error amplifier, enabling stable phase compensation to be provided for the system.

(4) PWM comparator Block (PWM Comp.)

The PWM comparator is a voltage-pulse width modulator that controls the output duty depending on the input voltage.

Main side : Turns the output transistor on in the intervals in which the error amplifier output voltage is higher than the triangular wave voltage.

Synchronous rectification sides : Turns the output transistor on in the intervals in which the error amplifier output voltage is lower than the triangular wave valtage.

(5) Output Block

The output circuits on the main side and on the synchronous rectification side are both in the totem pole configuration, capable of driving an external N-ch MOS FET.

In addition, because the output drive ability (700 mA Max : Duty ≤ 5%) is high, the gate – source capacity is large and the FET of low ON resistor can be used.

2. Channel Control Function

Channels are turned on and off depending on the voltage levels at the CTL1 terminal (pin 2) and CTL2 terminal (pin 29).

Channel On/Off Setting Conditions

CTL terminal voltage level		Channel output state	
CTL1	**CTL2**	**CH1**	**CH2**
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

3. Protective Functions

(1) Timer-Latch Short-Circuit Protection Circuit Block

The short-circuit detection comparator (SCP Comp.) provided for the two channels detects the output voltage level and, if either channel output voltage falls below the short-circuit detection voltage, the timer circuit is actuated to start charging the external capacitor Cscp connected to the CSCP terminal (pin 25) .

When the capacitor voltage reaches about 0.68 V, the circuit turns off the output transistor and sets the dead time to 100%.

Once the protection circuit is actuated, it can be reset by turning the power supply off and on again. (See “SETTING THE TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.)

(2) Undervoltage Lockout Circuit Block

The transient state or a momentary drops in supply voltage, which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the undervoltage lockout circuit detects the internal reference voltage level with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 25) at the “L” level.

System operation is restored when the supply voltage reaches the threshold voltage of the undervoltage lockout circuit.

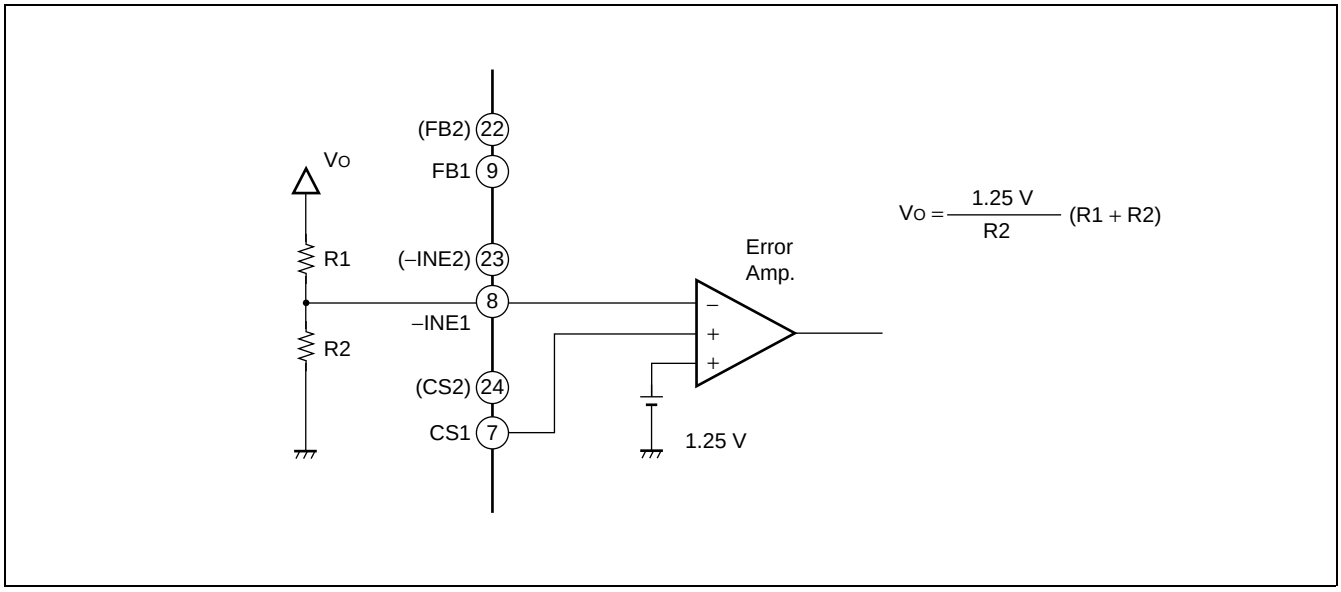
(3) Overcurrent Protection Circuit

The overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET’s drain and source by the main-side FET ON resistor and sets the latch to fix the main and synchronous rectification outputs of the relevant channel at the “L” level. The detection current value can be set by resistor R_{LIM1} connected between the main-side FET’s drain and the ILIM1 terminal (pin 3) and resistor R_{LIM2} connected between the drain and the ILIM2 pin (pin 28) . (See “SETTING THE OVERCURRENT DETECTION CURRENT”.)

(4) Overvoltage Protection Circuit (OVP)

When the overvoltage detection comparator (OVP Comp.) provided for each channel detects the output voltage level exceeding its threshold voltage, the overvoltage protection circuit sets the latch to fix only the main output of the relevant channel at the “L” level and the synchronous-rectification output at the “H” level. (See “SETTING THE OVERVOLTAGE DETECTION VOLTAGE”.)

■ SETTING THE OUTPUT VOLTAGE



CH1, 2

■ SETTING THE OSCILLATION FREQUENCY

The oscillation frequency can be set by connecting the timing capacitor (C_T) to the CT terminal (pin 4) and timing resistor (R_T) to the RT terminal (pin 5) .

Oscillation frequency : f_{osc}

$$f_{osc}\ (kHz) \fallingdotseq \frac{870000}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START AND DISCHARGE TIMES

To prevent surge currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} and C_{S2}) to the CS1 terminal (pin 7) for channel 1 and the CS2 terminal (pin 24) for channel 2, respectively.

Setting the each control terminals (CTL1 and CTL2) from “L” to “OPEN” switches SW1 and SW2 from B to A to charge the external soft-start capacitors (C_{S1} and C_{S2}) connected to the CS1 and CS2 terminals at 10 μA.

The error amplifier output (FB1 or FB2) is determined by comparison between the lower one of the potentials at two noninverting input terminals (1.25 V CS terminal voltages) and the inverting input terminal voltage (–INE) . The FB terminal voltage during the soft-start period is therefore determined by comparison between the –INE terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged. The soft-start time is obtained from the following equation :

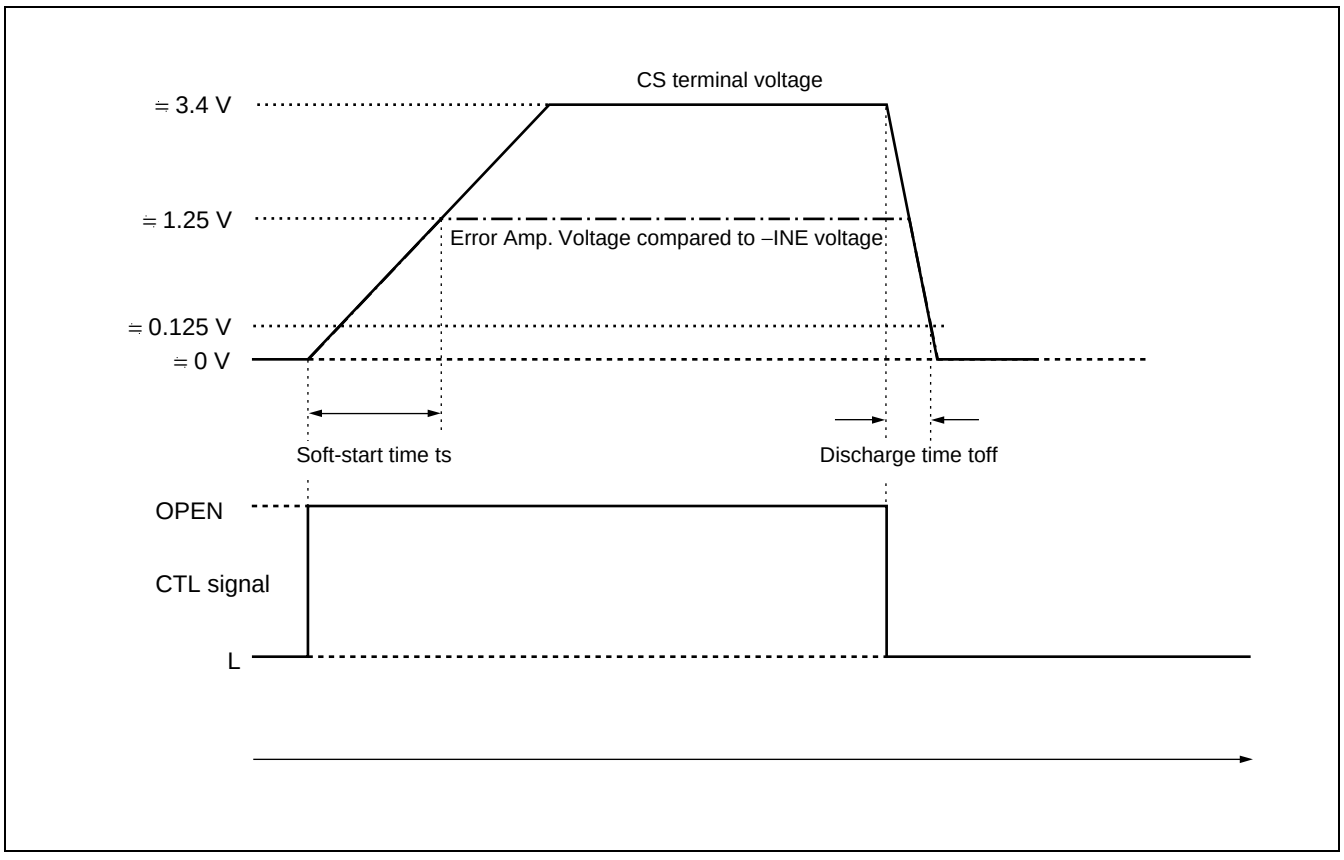
Soft-start time : ts (time to output 100%)

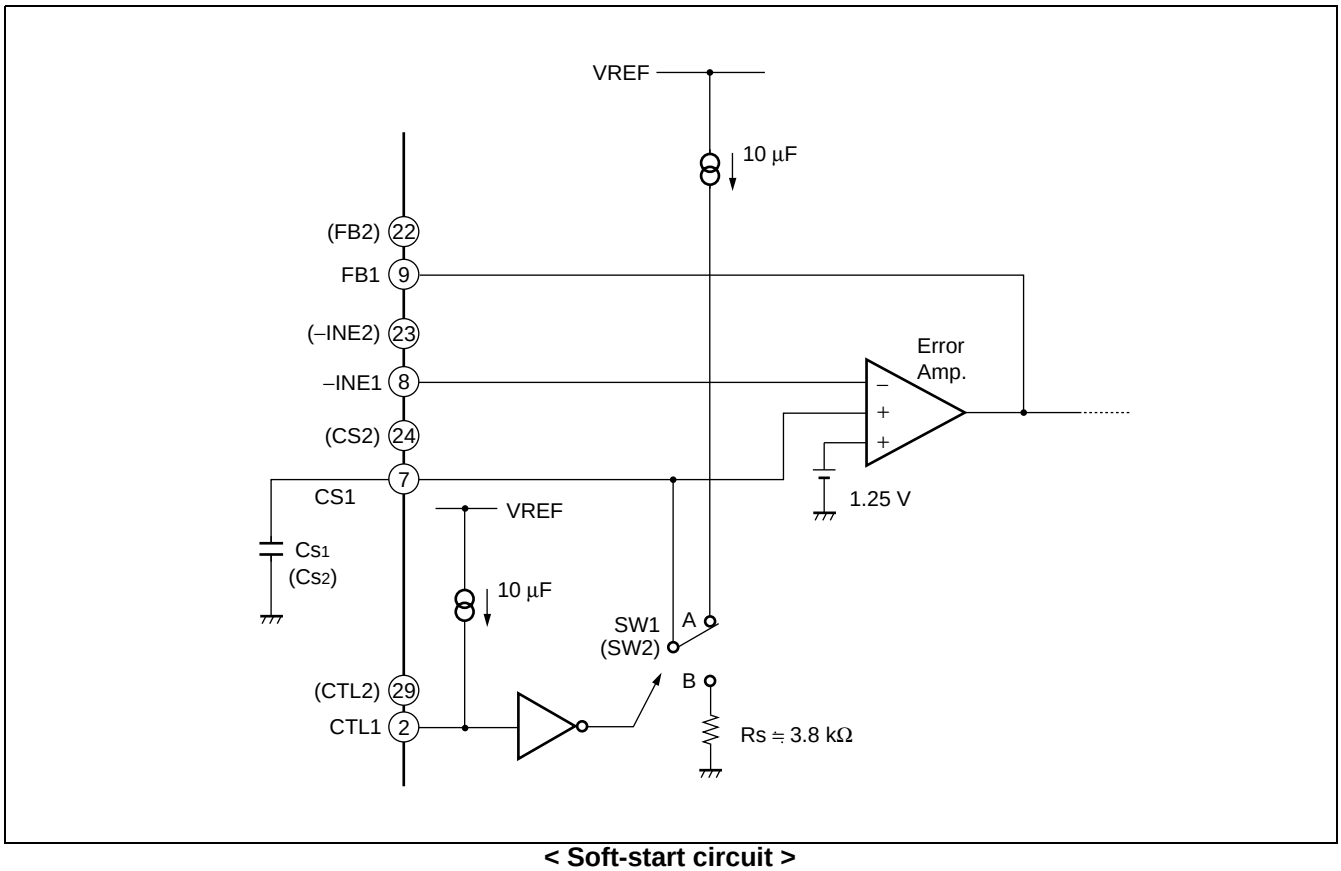
$$ts\ (s) \fallingdotseq 0.125 \times C_S\ (\mu F)$$

Setting the each control terminals (CTL1 and CTL2) from “OPEN” to “L” switches SW1 and SW2 from A to B. Then the IC discharges the soft-start capacitors (C_{S1} and C_{S2}) charged at about 3.4 V using the internally set discharge resistor ($Rs \fallingdotseq 3.8\ k\Omega$) and lowers the output voltage with a time constant of about 1/10 of the soft-start time regardless of the DC/DC converter load current. The discharge time is obtained from the following equation :

Discharge time : toff (time to output 10%)

$$toff\ (s) \fallingdotseq 0.0126 \times C_S\ (\mu F)$$

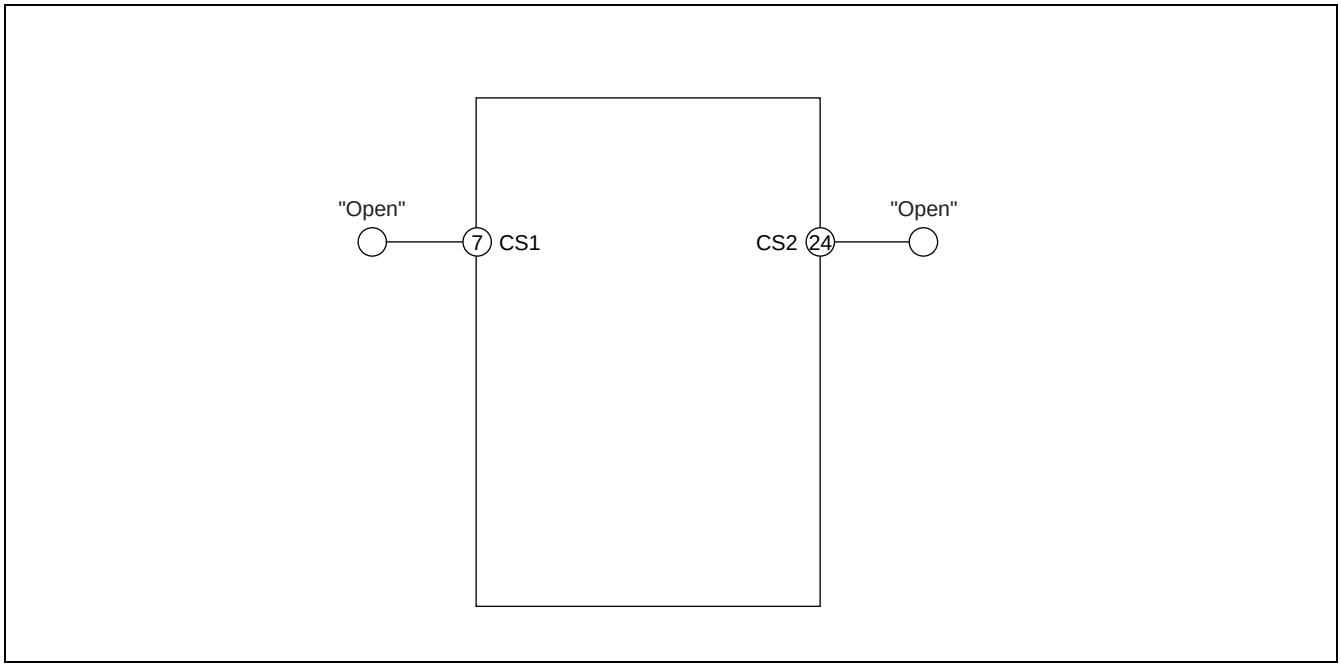




< Soft-start circuit >

■ TREATMENT OF UNUSED CS PINS

When the soft-start function is not used, the CS1 terminal (pin 7) and CS2 terminal (pin 22) should be left open.



< Operation Without Soft-Start Setting >

■ SETTING THE OVERCURRENT DETECTION CURRENT

The overcurrent protection circuit is actuated upon completion of the soft-start period. If an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET's drain and source by the main-side FET ON resistor (RON) and sets the latch to fix the main and synchronous rectification outputs of the relevant channel at the "L" level. At the same time, the circuit fixes the PSIG1 terminal (pin 1) at the "L" level when the overcurrent is detected on CH1 or the PSIG2 terminal (pin 30) at the "L" level when it is detected on CH2. The detection current value can be set by the resistors (R_{LIM1} and R_{LIM2}) connected between the main-side FET's drain and the ILIM1 terminal (pin 3) /ILIM2 terminal (pin 28) , respectively. Note that the overcurrent protection circuit works for each channel separately.

Detection current value : I_{OCP}

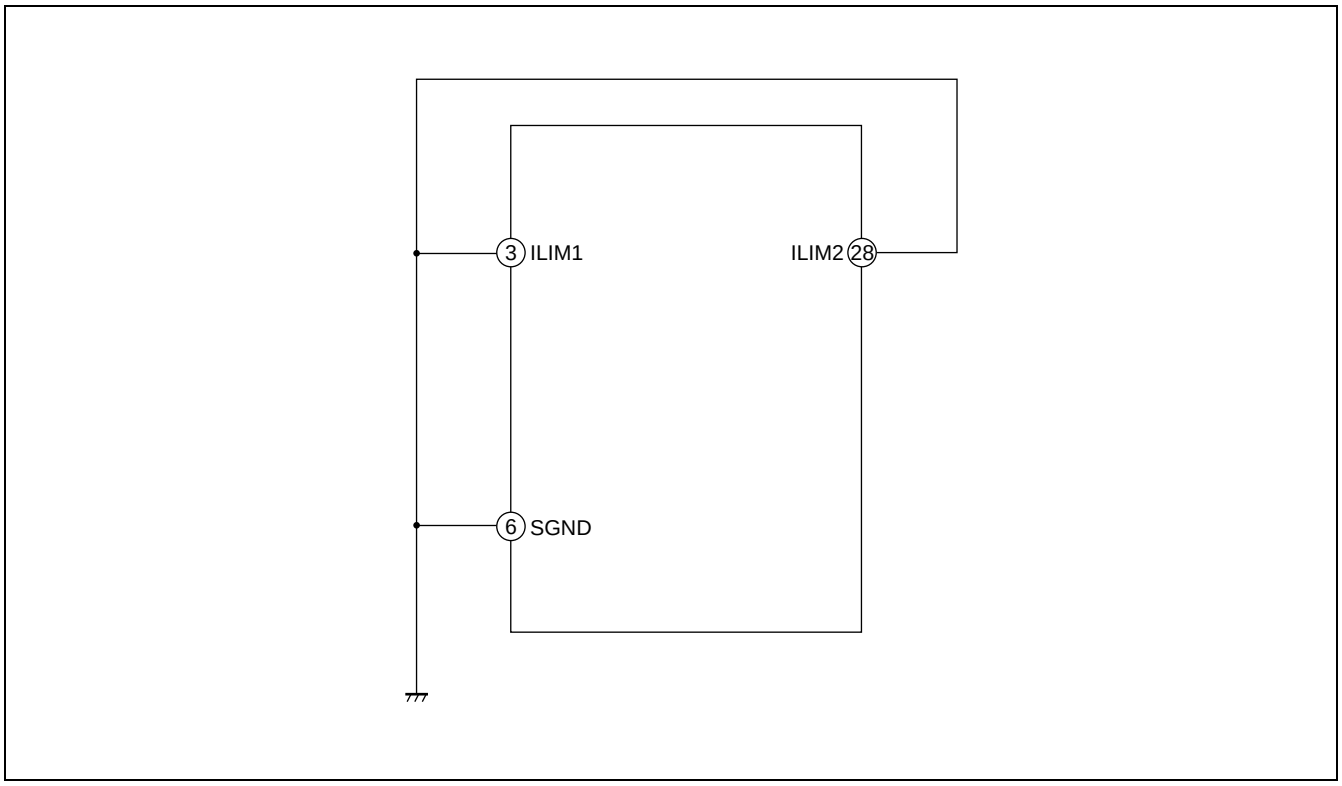
$$I_{OCP}\ (A) \fallingdotseq \frac{I_{LIM}\ (A) \times R_{LIM}\ (\Omega)}{Ron\ (\Omega)} - \frac{(Vin\ (V) - Vo\ (V)) \times Vo\ (V)}{2 \times Vin\ (V) \times f_{OSC}\ (Hz) \times L\ (H)}$$

RON : Main-side FET ON resistor, Vin : Input voltage, Vo : DC/DC converter output voltage

f_{OSC} : Oscillation frequency, L : Coil inductance

■ TREATMENT OF UNUSED ILIM PINS

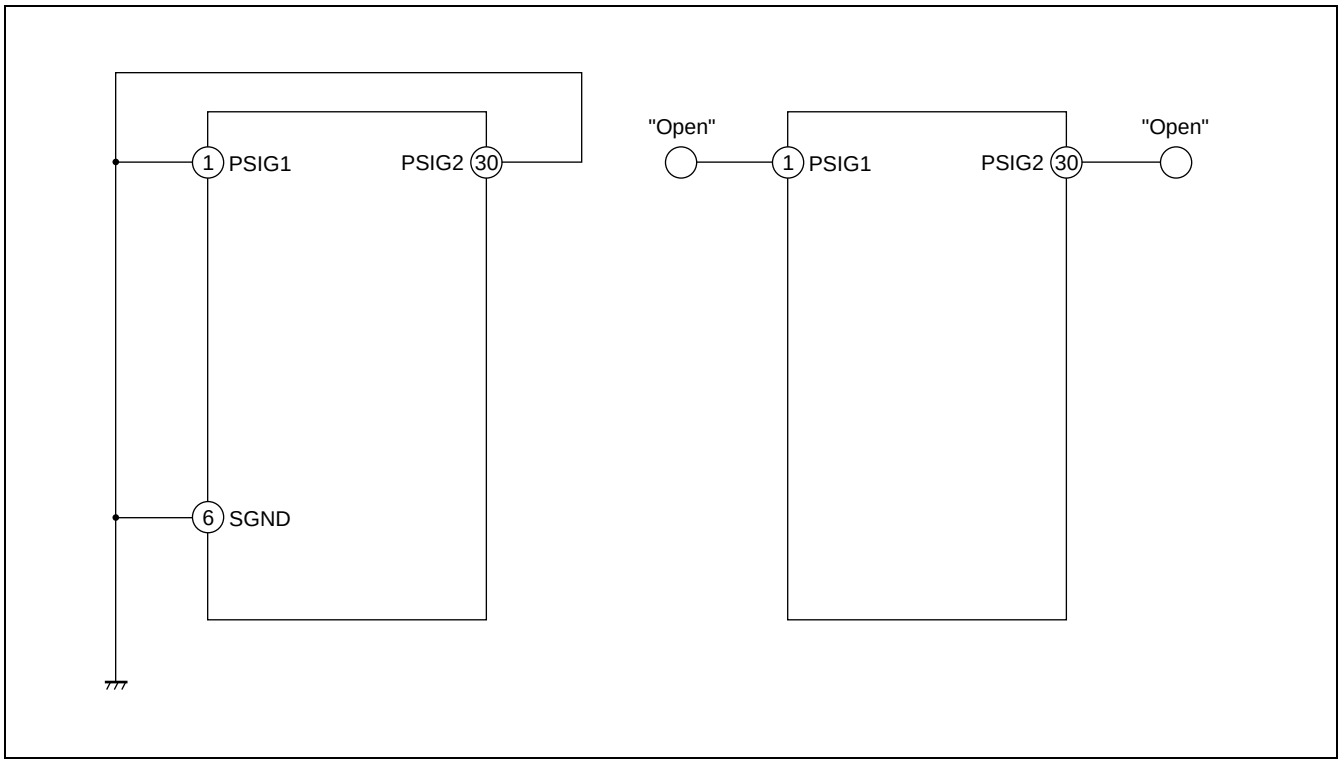
When the overcurrent protection circuit is not used, the ILIM1 terminal (pin 3) and ILIM2 terminal (pin 28) should be shorted to the SGND terminal (pin 6) using the shortest possible connection.



< Operation Without Using the ILIM Terminals >

■ TREATMENT OF UNUSED PSIG PINS

When the PSIG terminals are not used, the PSIG1 terminal (pin 1) and PSIG2 terminal (pin 30) should be shorted or open to the SGND terminal (pin 6) .



< Operation Without Using the PSIG Terminals >

■ SETTING THE TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage.

While the DC/DC converter load conditions are stable on both channels, the short-circuit detection comparator keeps its output at the "H" level and the CSCP terminal (pin 25) remains at the input standby voltage ($V_{STB} \fallingdotseq 50$ mV) .

If a load condition changes rapidly due to a short circuit of the load, causing the output voltage to drop, the short-circuit detection comparator changes its output to the "L" level. This causes the external short-circuit protection capacitor Cscp connected to the CSCP terminal to be charged at 10 μA.

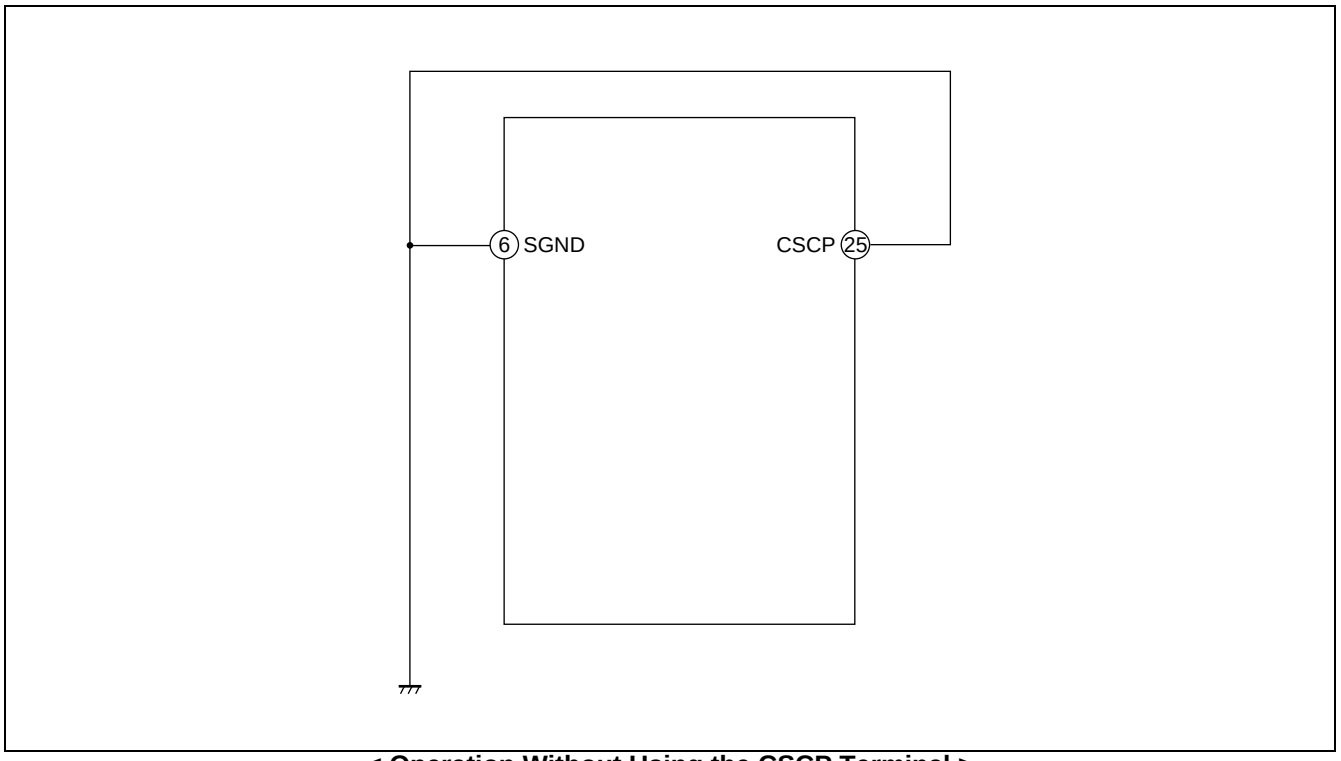
Short-circuit detection time : tscp

$$tscp\ (s) \fallingdotseq 0.068 \times Cscp\ (\mu F)$$

When the capacitor Cscp is charged to the threshold voltage ($V_{TH} \fallingdotseq 0.68$ V) , the protection circuit sets the latch and turns off the external FET (setting the dead time to 100%) . At this time, the latch input is closed and the CSCP terminal is held at the input latch voltage ($V_I \fallingdotseq 50$ mV) . The protection circuit shuts off both channels even when a short circuit is detected on only either.

■ PROCESSING WITHOUT USING THE CSCP TERMINAL

When the timer-latch short-circuit protection circuit is not used, the CSCP terminal (pin 25) should be shorted to SGND using the shortest possible connection.



< Operation Without Using the CSCP Terminal >

■ SETTING THE OVERVOLTAGE DETECTION VOLTAGE

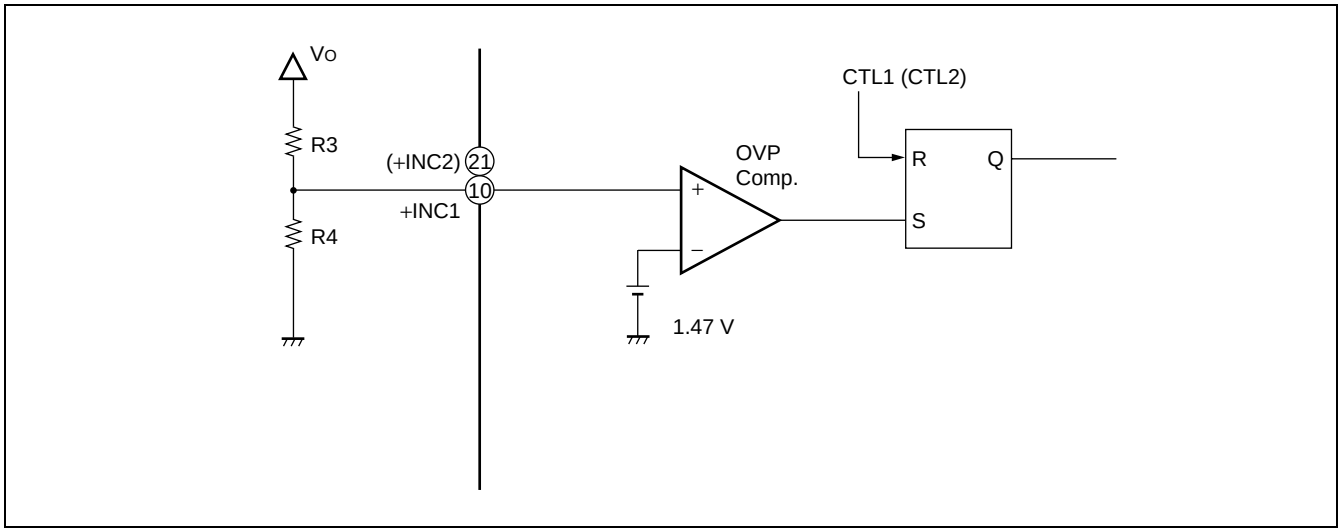
An overvoltage output from the DC/DC converter can be detected by connecting external resistors from the DC/DC converter output voltage to the +INC1 terminal (pin 10) and +INC2 terminal (pin 21) of the overvoltage comparators (OVP Comp. 1 and 2) .

When the DC/DC converter output voltage rises and the detection voltage exceeds the setting voltage, the output of the overvoltage comparator (OVP Comp. 1, 2) becomes the “H” level and the latch is set to fix only the main output of the relevant channel at the “L” level and the synchronous-rectification output at the “H” level. At the same time, the overvoltage protection circuit fixes the PSIG1 terminal (pin 1) at the “L” level when the overvoltage is detected on CH1 or the PSIG2 terminal (pin 30) at the “L” level when it is detected on CH2. Note that the overvoltage protection circuit works for each channel separately.

Overvoltage detection voltage : V_{OVP}

V_{OVP} (V) ≒ 1.47 × (R3 (Ω) + R4 (Ω)) / R4 (Ω)

To reset the actuated protection circuit, either set the CTL1 terminal (pin 2) or CTL2 terminal (pin 29) to the “L” level, or decrease the V_{CC} voltage to the reset voltage (1.7 V Min) or less.



■ OUTPUT STATES DURING PROTECTION CIRCUIT OPERATION

The table below lists the output states with individual protection circuits actuated.

Output terminal / Protection circuit		CH1			CH2		
		OUT1-1	**OUT2-1**	**PSIG1**	**OUT1-2**	**OUT2-2**	**PSIG2**
Overcurrent protection circuit	CH1	L	L	L	Active	Active	H
	CH2	Active	Active	H	L	L	L
Overvoltage protection circuit	CH1	L	H	L	Active	Active	H
	CH2	Active	Active	H	L	H	L
Short-circuit protection circuit	CH1	L	L	H	L	L	H
	CH2	L	L	H	L	L	H

■ RESETTING THE LATCH OF EACH PROTECTION CIRCUIT

When each protection circuit (overvoltage, overcurrent, or short-circuit protection circuit) detects an abnormal state or event, it sets the latch to fix the output at the “L” level. The PSIG1 terminal (pin 1) or PSIG2 terminal (pin 30) is fixed at the “L” level when the overvoltage or overcurrent protection circuit detects an overvoltage or overcurrent.

When a protection circuit operates, the latch can be released by reentering the power supply or setting the CTL1 terminal (pin 2) or CTL2 terminal (pin 29) to the “L” level.

The overvoltage and overcurrent protection circuits work for each channel separately. Use the CTL1 and CTL2 terminals to unlatch CH1 and CH2, respectively.

The short-circuit protection circuit fixes the outputs of both channels upon detection of a short circuit even on either. Set both of the CTL1 and CTL2 terminals to the “L” level to unlatch the two channels.

Unlatching Conditions

Operation circuit	**CTL1**	**CTL2**	**Channels unlatched**	
			CH1	**CH2**
Overcurrent protection circuit Overvoltage protection circuit	OPEN	OPEN	×	×
	L	OPEN	○	×
	OPEN	L	×	○
	L	L	○	○
Short-circuit protection circuit	OPEN	OPEN	×	
	L	OPEN	×	
	OPEN	L	×	
	L	L	○	

○ : Unlatched, × : Not unlatched

■ NOTE ON IC'S INTERNAL POWER CONSUMPTION

The oscillation frequency of an IC and the total gate charge of FETs largely affects the internal dissipation of the IC.

Pay attention to the following point with respect to the internal power consumption of the IC when applications are used.

I_B (mean current) is obtained from the following equation, assuming Qg1 and Qg2 as the total gate charges applied to the gate capacitors ($Ciss_1$, $Ciss_2$, $Crss_1$, $Crss_2$) of external FETs Q1 and Q2.

Current per channel

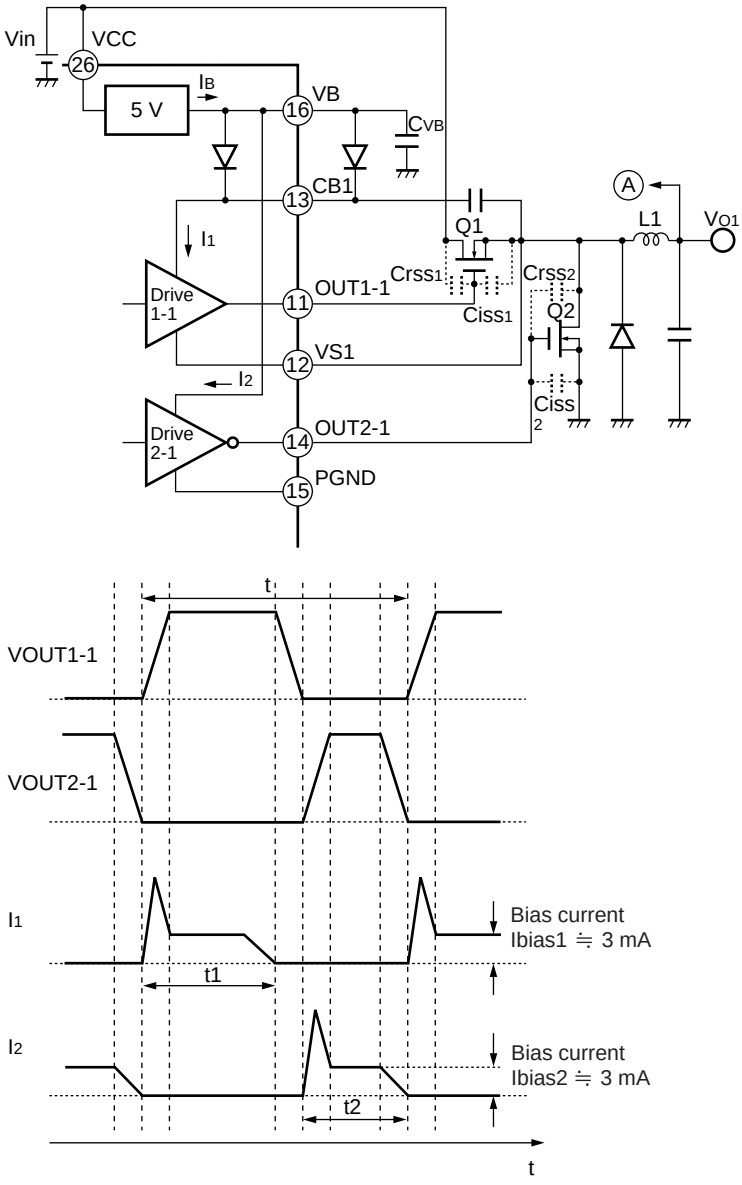
$$I_B\ (A) = I_1 + I_2$$

$$\fallingdotseq Ibias_1 \times \frac{t1}{t} + \frac{Qg_1}{t} + Ibias_2 \times \frac{t2}{t} + \frac{Qg_2}{t} \qquad (Ibias_1 = Ibias_2 \fallingdotseq 3\ mA)$$

As the current consumption by the IC, excluding I_B, is about 15 mA, the power consumption is obtained from the following equation :

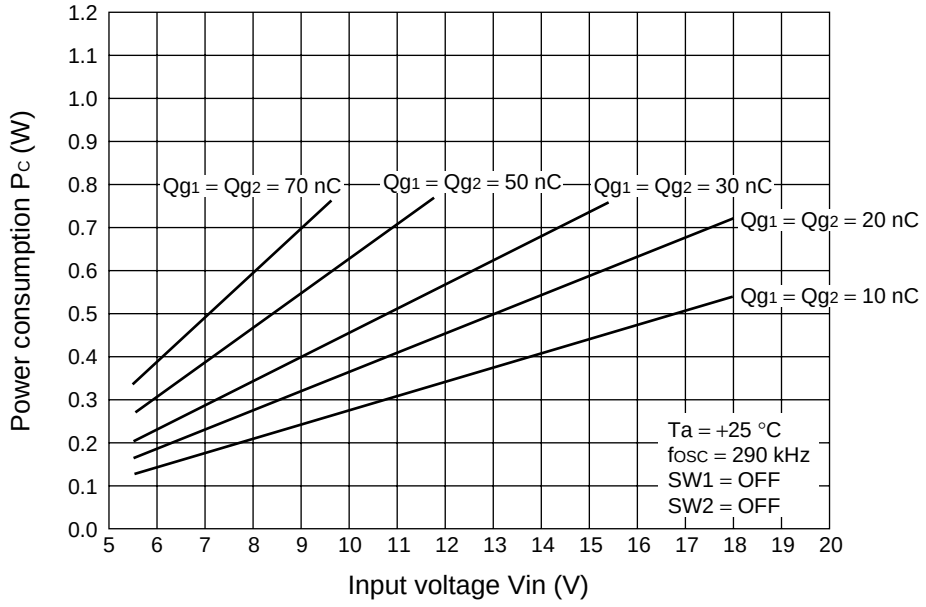
Power consumption : Pc

$$Pc\ (W) = 0.015 \times V_{CC}\ (V) + 2 \times V_{CC}\ (V) \bullet I_B\ (A) - V_B\ (V) \bullet I_B\ (A)$$

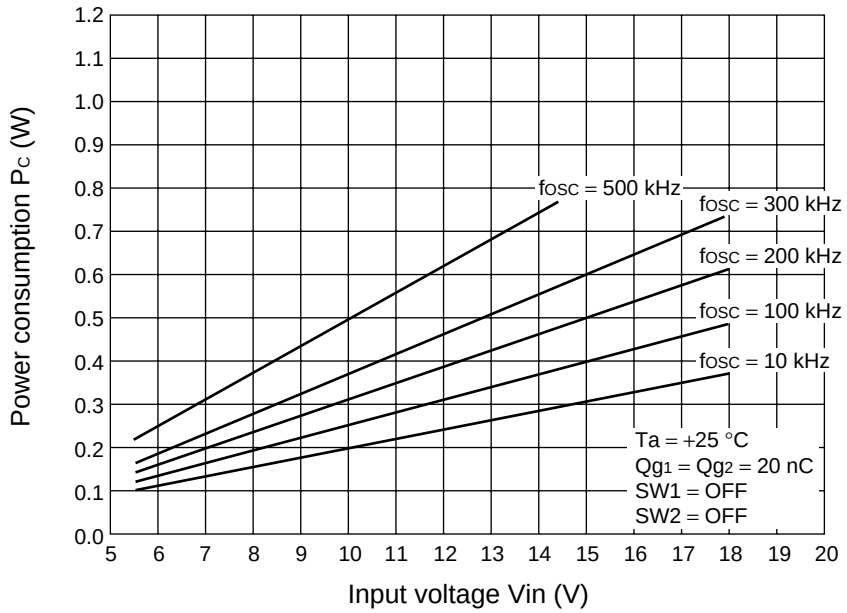


See “Power Consumption vs. Input Voltage” on the next page as a reference and use the above method of obtaining the power consumption to design your application of the IC taking account of the “Power Dissipation vs. Ambient Temperature” characteristic in the “TYPICAL CHARACTERISTICS” section.

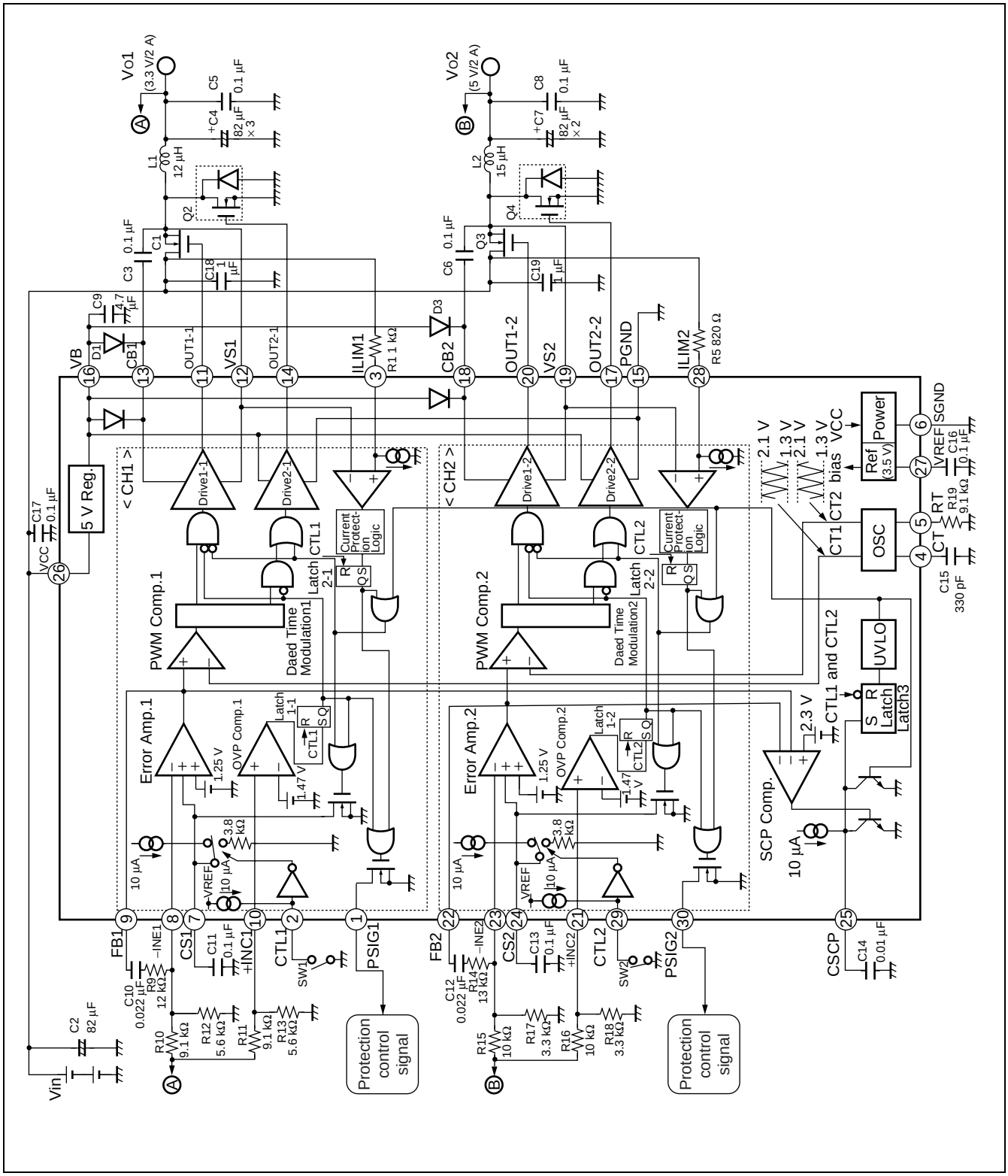
Power Consumption vs. Input Voltage (Qg Parameters)



Power Consumption vs. Input Voltage (fosc Parameter)



■ SAMPLE CIRCUIT



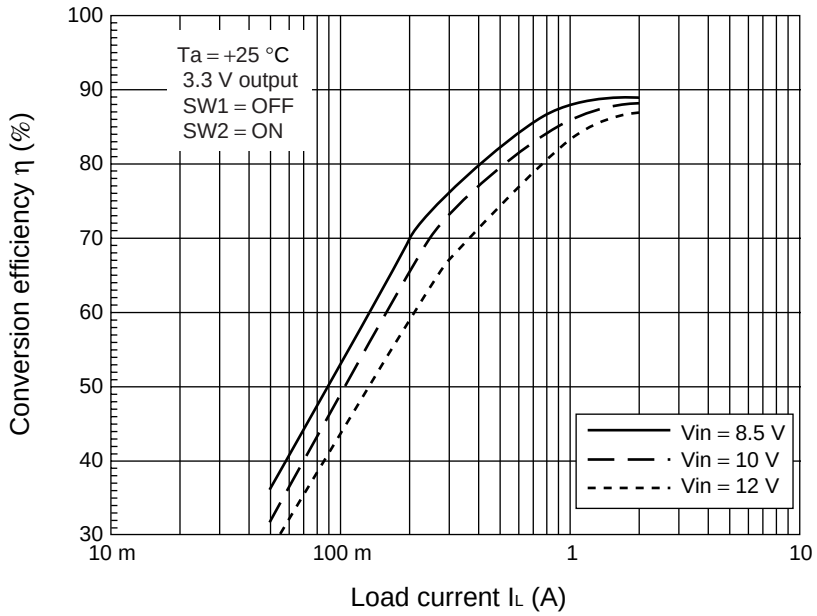
■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q3 Q2, Q4	FET FETKY™	VDS = 30 V, Qg = 17 nC (Max) VDS = 30 V, Qg = 14 nC (Max)		IR IR	IRF7807 IRF7807D1
D1, D3	Diode	VF = 0.3 V (Max) , IF = 1 A		ROHM	RB495D
L1 L2	Coil Coil	12 μH 15 μH	3.5 A, 21 mΩ 2.8 A, 25.9 mΩ	SUMIDA TDK	CDRH125-120 SLF12555T-150M2R8
C2	OS-CON™	82 μF	16 V	SANYO	16SVP82M
C3, C5, C6, C8	Ceramics Condenser	0.1 μF	16 V	KYOCERA	CM21W5R104K16
C4	OS-CON™	82 μF × 3	6.3 V	SANYO	6SVP82M
C7	OS-CON™	82 μF × 2	6.3 V	SANYO	6SVP82M
C9	Ceramics Condenser	4.7 μF	10 V	MURATA	GRM42-6B475K10
C10	Ceramics Condenser	0.022 μF	25 V	MURATA	GRM39B473K25
C11, C13, C16	Ceramics Condenser	0.1 μF	16 V	KYOCERA	CM21W5R104K16
C12	Ceramics Condenser	0.022 μF	25 V	MURATA	GRM39B223K25
C14	Ceramics Condenser	0.01 μF	50 V	MURATA	GRM39B103K50
C15	Ceramics Condenser	330 pF	50 V	MURATA	GRM39R331K50
C17	Ceramics Condenser	0.1 μF	25 V	MURATA	GRM39F104Z25
C18, C19	Ceramics Condenser	1 μF	16 V	MURATA	GRM40B105K16
R1	Resistor	1 kΩ	1/16 W	KOA	RK73G1J102D
R5	Resistor	820 Ω	1/16 W	KOA	RK73G1J821D
R9	Resistor	12 kΩ	1/16 W	KOA	RK73G1J123D
R10, R11	Resistor	9.1 kΩ	1/16 W	KOA	RK73G1J912D
R12, R13	Resistor	5.6 kΩ	1/16 W	KOA	RK73G1J562D
R14	Resistor	13 kΩ	1/16 W	KOA	RK73G1J223D
R15, R16	Resistor	10 kΩ	1/8 W	KYOCERA	CR21-103F
R17, R18	Resistor	3.3 kΩ	1/16 W	KOA	RK73G1J332D
R19	Resistor	9.1 kΩ	1/16 W	KOA	RK73G1J912D

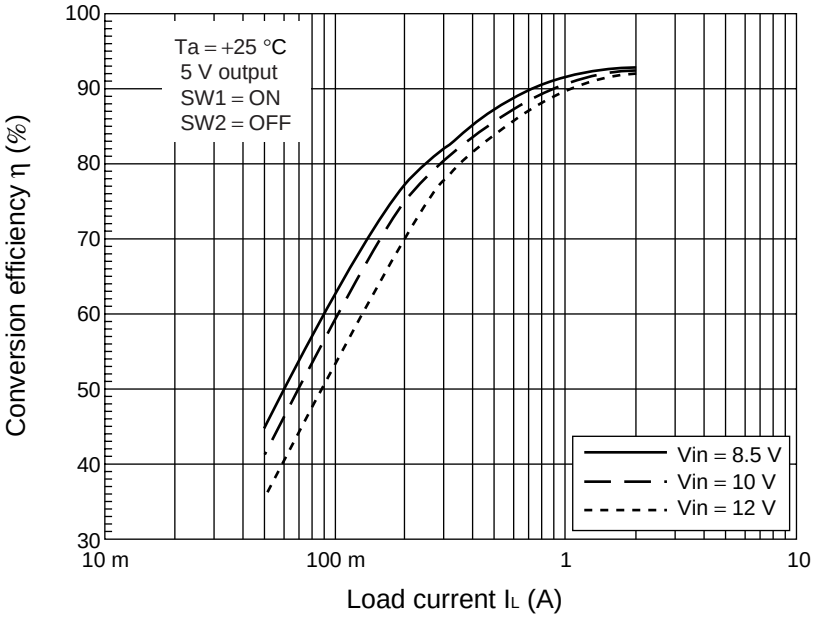
Note : IR : International Rectifier Corp.
ROHM : ROHM CO., LTD.
SUMIDA : Sumida Electric Co., Ltd.
TDK : TDK Corporation
SANYO : SANYO Electric Co., Ltd.
KYOCERA : Kyocera Corporation
MURATA : Murata Manufacturing Co., Ltd.
KOA : KOA Corporation
FETKY is a trademark of International Rectifier Corp.
OS-CON is a trademark of SANYO Electric Co., Ltd.

■ REFERENCE DATA

Conversion Efficiency vs. Load Current (CH1)



Conversion Efficiency vs. Load Current (CH2)



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools, and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage.
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

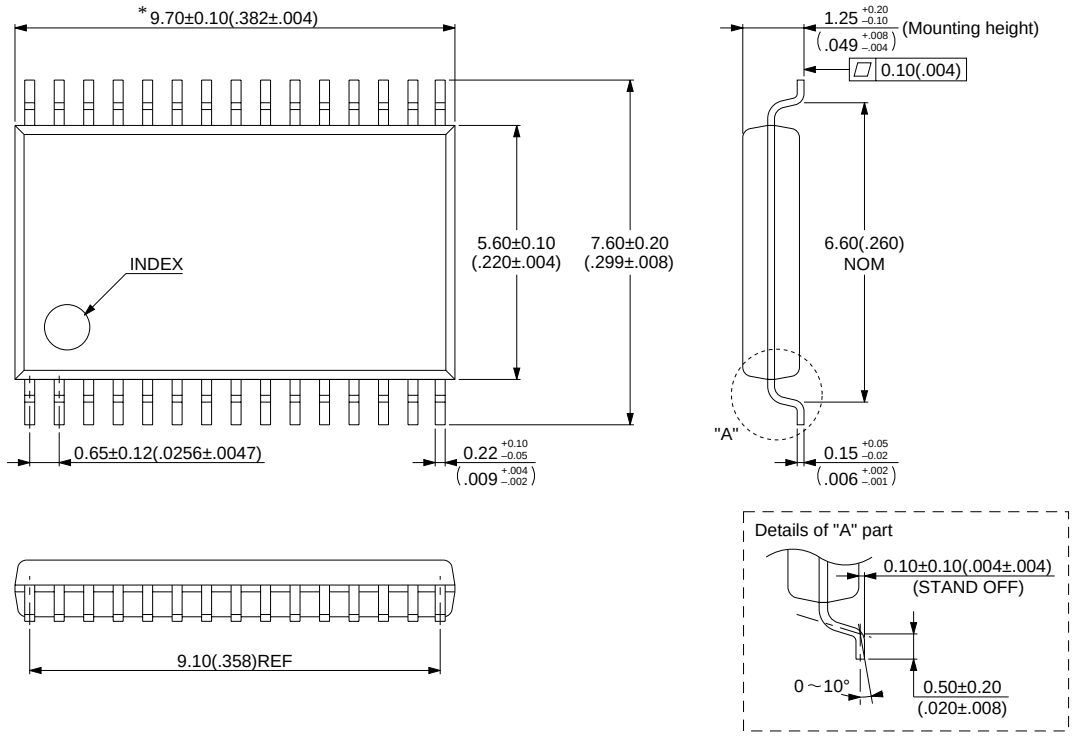
■ ORDERING INFORMATION

Model name	Package	Remarks
MB3886PFV	30-pin plastic SSOP (FPT-30P-M02)	

■ PACKAGE DIMENSION

30-pin plastic SSOP
(FPT-30P-M02)

* : This dimension does not include resin protrusion.



Dimensions in mm (inches)

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