

ASSP For Power Management Applications (General Purpose DC/DC Converter)

2-ch DC/DC Converter IC with Overcurrent Protection

MB39A104

■ DESCRIPTION

The MB39A104 is a 2-channel DC/DC converter IC using pulse width modulation (PWM), incorporating an overcurrent protection circuit (requiring no current sense resistor). This IC is ideal for down conversion.

Operating at high frequency reduces the value of coil.

This is ideal for built-in power supply such as LCD monitors and ADSL.

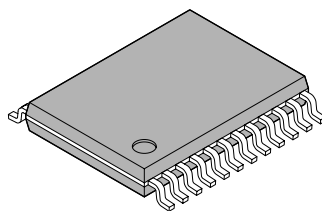
This product is covered by US Patent Number 6,147,477.

■ FEATURES

- Built-in timer-latch overcurrent protection circuit (requiring no current sense resistor)
- Power supply voltage range : 7 V to 19 V
- Reference voltage : 5.0 V \pm 1 %
- Error amplifier threshold voltage : 1.24 V \pm 1 %
- High-frequency operation capability : 1.5 MHz (Max)
- Built-in standby function: 0 μ A (Typ)
- Built-in soft-start circuit independent of loads
- Built-in totem-pole type output for Pch MOS FET

■ PACKAGE

24-pin plastic SSOP



(FPT-24P-M03)

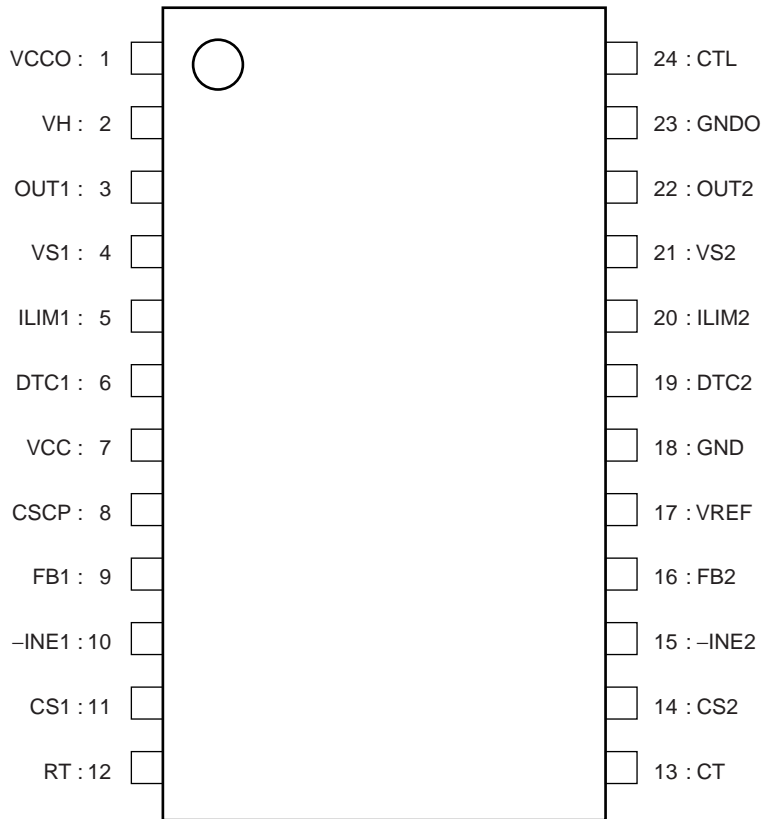
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MB39A104

■ PIN ASSIGNMENTS

(TOP VIEW)



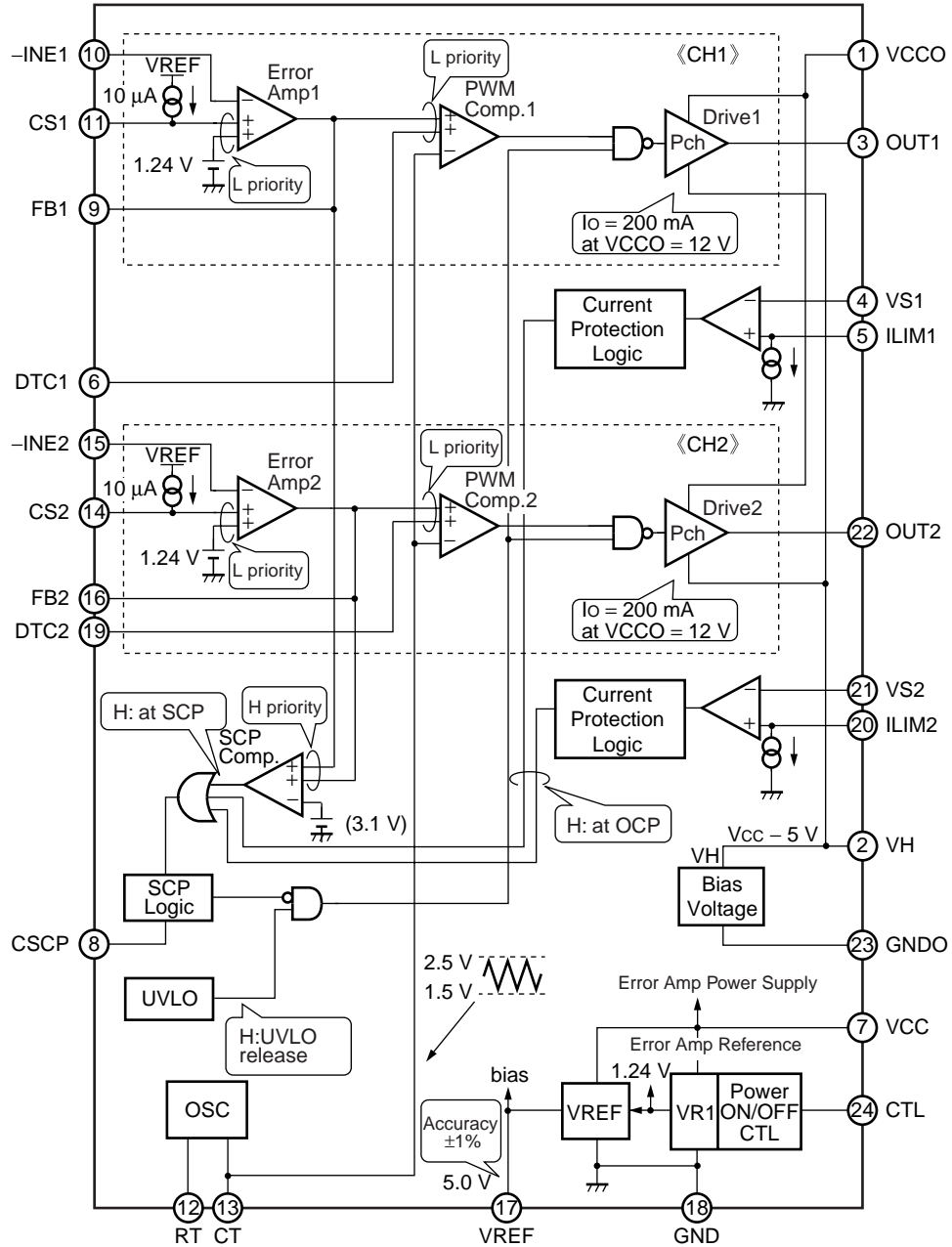
(FPT-24P-M03)

■ PIN DESCRIPTION

| Pin No. | Symbol | I/O | Descriptions |
|---------|--------|-----|---|
| 1 | VCCO | — | Output circuit power supply terminal (Connect to same potential as VCC pin.) |
| 2 | VH | O | Power supply terminal for FET drive circuit ($VH = V_{CC} - 5\text{ V}$) |
| 3 | OUT1 | O | External Pch MOS FET gate drive terminal |
| 4 | VS1 | I | Overcurrent protection circuit input terminal |
| 5 | ILIM1 | I | Overcurrent protection circuit detection resistor connection terminal. Set overcurrent detection reference voltage depending on external resistor and internal current resource ($110\ \mu\text{A}$ at $RT = 24\ \text{k}\Omega$) |
| 6 | DTC1 | I | PWM comparator block (PWM) input terminal. Compares the lowest voltage among FB1 and DTC terminals with triangular wave and controls output. |
| 7 | VCC | — | Power supply terminal for reference power supply and control circuit (Connect to same potential as the VCCO terminal) |
| 8 | CSCP | — | Timer-latch short-circuit protection capacitor connection terminal |
| 9 | FB1 | O | Error amplifier (Error Amp 1) output terminal |
| 10 | -INE1 | I | Error amplifier (Error Amp 1) inverted input terminal |
| 11 | CS1 | — | Soft-start capacitor connection terminal |
| 12 | RT | — | Triangular wave oscillation frequency setting resistor connection terminal |
| 13 | CT | — | Triangular wave oscillation frequency setting capacitor connection terminal |
| 14 | CS2 | — | Soft-start capacitor connection terminal |
| 15 | -INE2 | I | Error amplifier (Error Amp 2) inverted input terminal |
| 16 | FB2 | O | Error amplifier (Error Amp 2) output terminal |
| 17 | VREF | O | Reference voltage output terminal |
| 18 | GND | — | Output circuit ground terminal (Connect to same potential as GNDO terminal.) |
| 19 | DTC2 | I | PWM comparator block (PWM) input terminal. Compares the lowest voltage among FB2 and DTC terminals with triangular wave and controls output. |
| 20 | ILIM2 | I | Overcurrent protection circuit detection resistor connection terminal. Set overcurrent detection reference voltage depending on external resistor and internal current resource ($110\ \mu\text{A}$ at $RT = 24\ \text{k}\Omega$) |
| 21 | VS2 | I | Overcurrent protection circuit input terminal |
| 22 | OUT2 | O | External Pch MOS FET gate drive terminal |
| 23 | GNDO | — | Output circuit ground terminal (Connect to same potential as GND terminal.) |
| 24 | CTL | I | Power supply control terminal. Setting the CTL terminal at "L" level places IC in the standby mode. |

MB39A104

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|----------------------|------------------|---|--------|------|------|
| | | | Min | Max | |
| Power supply voltage | V _{CC} | VCC, VCCO terminal | — | 20 | V |
| Output current | I _O | OUT1, OUT2 terminal | — | 60 | mA |
| Output peak current | I _{OP} | Duty ≤ 5% (t = 1/f _{osc} × Duty) | — | 700 | mA |
| Power dissipation | P _D | T _a ≤ +25 °C | — | 740* | mW |
| Storage temperature | T _{STG} | — | -55 | +125 | °C |

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|------------------------------------|------------------|---|-------|-----|-----------------------|------|
| | | | Min | Typ | Max | |
| Power supply voltage | V _{CC} | VCC, VCCO terminal | 7 | 12 | 19 | V |
| Reference voltage output current | I _{REF} | VREF terminal | -1 | — | 0 | mA |
| VH output current | I _{VH} | VH terminal | 0 | — | 30 | mA |
| Input voltage | V _{INE} | -INE1, -INE2 terminal | 0 | — | V _{CC} - 0.9 | V |
| | V _{DTC} | DTC1, DTC2 terminal | 0 | — | V _{CC} - 0.9 | V |
| Control input voltage | V _{CTL} | CTL terminal | 0 | — | 19 | V |
| Output current | I _O | OUT1, OUT2 terminal | -45 | — | +45 | mA |
| Output Peak current | I _{OP} | Duty ≤ 5% (t = 1/f _{osc} × Duty) | -450 | — | +450 | mA |
| Oscillation frequency | f _{OSC} | Overcurrent detection by ON resistance of FET | 100 | 500 | 1000 | kHz |
| | | * | 100 | 500 | 1500 | kHz |
| Timing capacitor | C _T | — | 39 | 100 | 560 | pF |
| Timing resistor | R _T | — | 11 | 24 | 130 | kΩ |
| VH terminal capacitor | C _{VH} | VH terminal | — | 0.1 | 1.0 | μF |
| Soft-start capacitor | C _S | CS1, CS2 terminal | — | 0.1 | 1.0 | μF |
| Short-circuit detection capacitor | C _{SCP} | CSCP terminal | — | 0.1 | 1.0 | μF |
| Reference voltage output capacitor | C _{REF} | VREF terminal | — | 0.1 | 1.0 | μF |
| Operating ambient temperature | T _a | — | -30 | +25 | +85 | °C |

* : See“ ■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY”.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 12 V, VREF = 0 mA, Ta = +25 °C)

| Parameter | Symbol | Pin No | Conditions | Value | | | Unit | |
|--|--------------------------------------|--------------------------|------------|---------------------------|-------|-------|-------|-----|
| | | | | Min | Typ | Max | | |
| 1. Reference voltage block [REF] | Output voltage | V _{REF} | 17 | Ta = +25 °C | 4.95 | 5.00 | 5.05 | V |
| | Output voltage temperature variation | $\Delta V_{REF}/V_{REF}$ | 17 | Ta = 0 °C to +85 °C | — | 0.5* | — | % |
| | Input stability | Line | 17 | VCC = 7 V to 19 V | — | 3 | 10 | mV |
| | Load stability | Load | 17 | VREF = 0 mA to -1 mA | — | 1 | 10 | mV |
| | Short-circuit output current | I _{OS} | 17 | VREF = 1 V | -50 | -25 | -12 | mA |
| 2. Under voltage lockout protection circuit block [UVLO] | Threshold voltage | V _{TLH} | 17 | VREF = $\bar{\uparrow}$ | 2.6 | 2.8 | 3.0 | V |
| | | V _{THL} | 17 | VREF = $\bar{\downarrow}$ | 2.4 | 2.6 | 2.8 | V |
| | Hysteresis width | V _H | 17 | — | — | 0.2* | — | V |
| 3. Short-circuit detection block [SCP Logic] | Threshold voltage | V _{TH} | 8 | — | 0.68 | 0.73 | 0.78 | V |
| | Input source current | I _{CSCP} | 8 | — | -1.4 | -1.0 | -0.6 | μA |
| | Reset voltage | V _{RST} | 17 | VREF = $\bar{\downarrow}$ | 2.4 | 2.6 | 2.8 | V |
| 4. Short-circuit detection block [SCP Comp] | Threshold voltage | V _{TH} | 8 | — | 2.8 | 3.1 | 3.4 | V |
| 5. Triangular wave oscillator block [OSC] | Oscillation frequency | f _{osc} | 13 | CT = 100 pF, RT = 24 kΩ | 450 | 500 | 550 | kHz |
| | Frequency temperature variation | $\Delta f_{osc}/f_{osc}$ | 13 | Ta = 0 °C to +85 °C | — | 1* | — | % |
| 6. Soft-start block [CS1, CS2] | Charge current | I _{CS} | 11, 14 | CS1 = CS2 = 0 V | -14 | -10 | -6 | μA |
| 7. Error amplifier block [Error Amp1, Error Amp2] | Threshold voltage | V _{TH} | 9, 16 | FB1 = FB2 = 2 V | 1.227 | 1.240 | 1.253 | V |
| | Input bias current | I _B | 10, 15 | -INE1 = -INE2 = 0 V | -120 | -30 | — | nA |
| | Voltage gain | A _V | 9, 16 | DC | — | 100* | — | dB |

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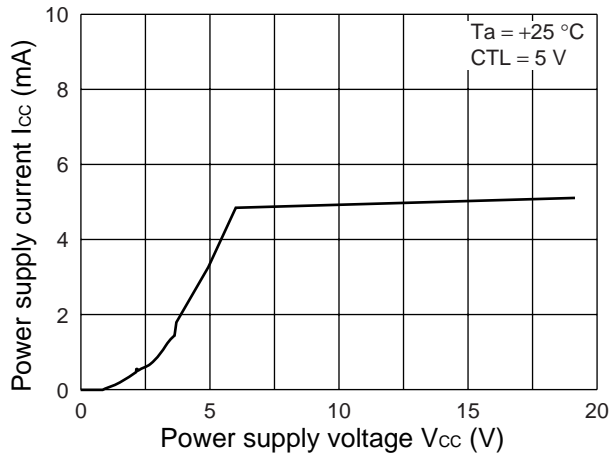
(VCC = VCCO = 12 V, VREF = 0 mA, Ta = +25 °C)

| Parameter | Symbol | Pin No. | Conditions | Value | | | Unit | |
|--|-----------------------------|--------------|-----------------|--|--------------|--------------|--------------|----------|
| | | | | Min | Typ | Max | | |
| 8. Error amplifier block [Error Amp1, Error Amp2] | Frequency bandwidth | BW | 9, 16 | $A_v = 0$ dB | — | 1.6* | — | MHz |
| | Output voltage | V_{OH} | 9, 16 | — | 4.7 | 4.9 | — | V |
| | | V_{OL} | 9, 16 | — | — | 40 | 200 | mV |
| | Output source current | I_{SOURCE} | 9, 16 | FB1 = FB2 = 2 V | — | -2 | -1 | mA |
| Output sink current | I_{SINK} | 9, 16 | FB1 = FB2 = 2 V | 150 | 200 | — | μ A | |
| 9. PWM comparator block [PWM Comp.1, PWM Comp.2] | Threshold voltage | V_{T0} | 6, 19 | Duty cycle = 0 % | 1.4 | 1.5 | — | V |
| | | V_{T100} | 6, 19 | Duty cycle = Dtr | — | 2.5 | 2.6 | V |
| | Input current | I_{DTC} | 6, 19 | DTC1 = DTC2 = 0.4 V | -2.0 | -0.6 | — | μ A |
| 10. Overcurrent protection circuit block [OCP1, OCP2] | ILIM terminal input current | I_{LIM} | 5, 20 | RT = 24 k Ω , CT = 100 pF | 99 | 110 | 121 | μ A |
| | Offset voltage | V_{IO} | 5, 20 | — | — | 1 * | — | mV |
| 11. Bias voltage block [VH] | Output voltage | V_H | 2 | VCC = VCCO = 7 V to 19 V VH = 0 mA to 30 mA | $V_{CC-5.5}$ | $V_{CC-5.0}$ | $V_{CC-4.5}$ | V |
| 12. Output block [Drive1, Drive2] | Output source current | I_{SOURCE} | 3, 22 | OUT1 to OUT4 = 7 V, Duty \leq 5 % ($t = 1/f_{osc} \times Duty$) | — | -300 | — | mA |
| | Output sink current | I_{SINK} | 3, 22 | OUT1 to OUT4 = 12 V, Duty \leq 5 % ($t = 1/f_{osc} \times Duty$) | — | 350 | — | mA |
| | Output ON resistor | R_{OH} | 3, 22 | OUT1 = OUT2 = -45 mA | — | 8.0 | 12.0 | Ω |
| | | R_{OL} | 3, 22 | OUT1 = OUT2 = 45 mA | — | 6.5 | 9.7 | Ω |
| 13. Control block [CTL] | CTL input voltage | V_{IH} | 24 | IC Active mode | 2 | — | 19 | V |
| | | V_{IL} | 24 | IC Standby mode | 0 | — | 0.8 | V |
| | Input current | I_{CTLH} | 24 | CTL = 5 V | — | 50 | 100 | μ A |
| | | I_{CTLL} | 24 | CTL = 0 V | — | — | 1 | μ A |
| 14. General | Standby current | I_{CCS} | 1, 17 | CTL = 0 V | — | 0 | 10 | μ A |
| | Power supply current | I_{CC} | 1, 17 | CTL = 5 V | — | 4.0 | 6.0 | mA |

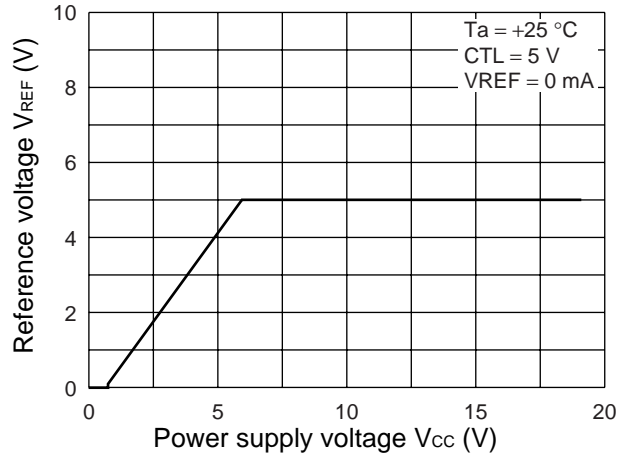
*: Standard design value.

■ TYPICAL CHARACTERISTICS

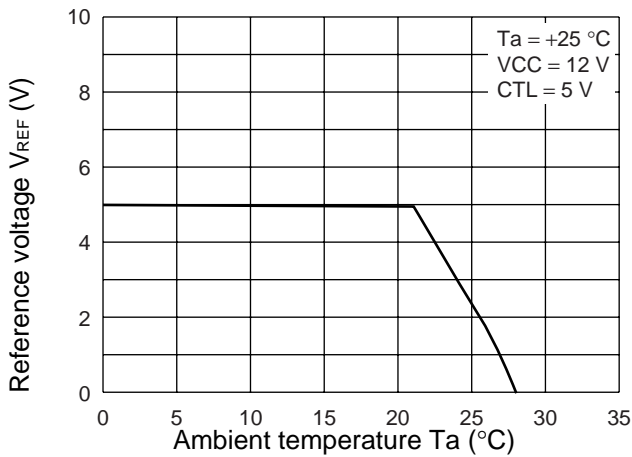
Power Supply Current vs. Power Supply Voltage



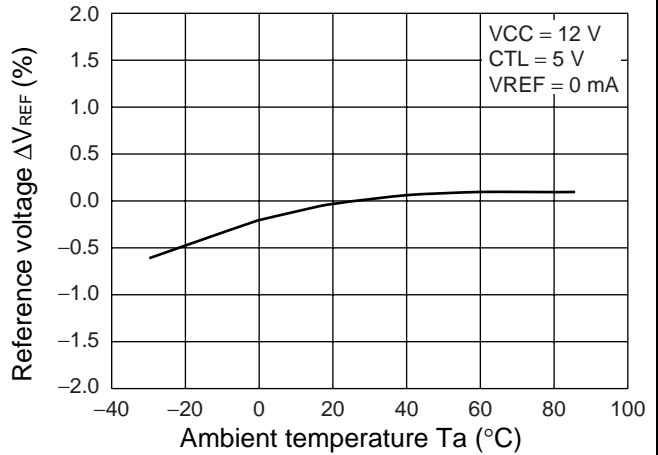
Reference Voltage vs. Power Supply Voltage



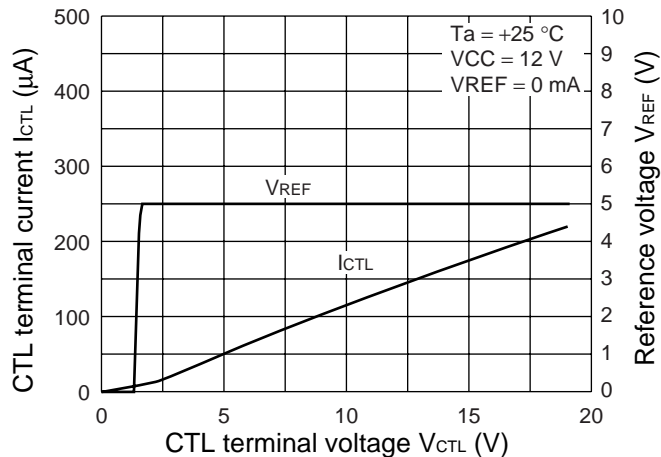
Reference Voltage vs. Ambient Temperature



Reference Voltage vs. Ambient Temperature

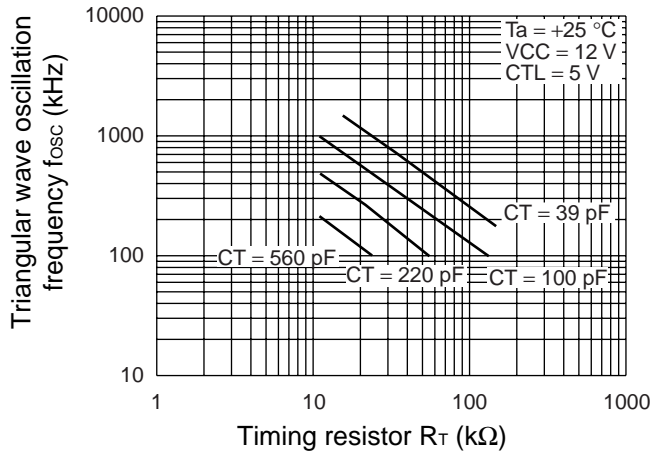


CTL terminal Current vs. CTL terminal Voltage

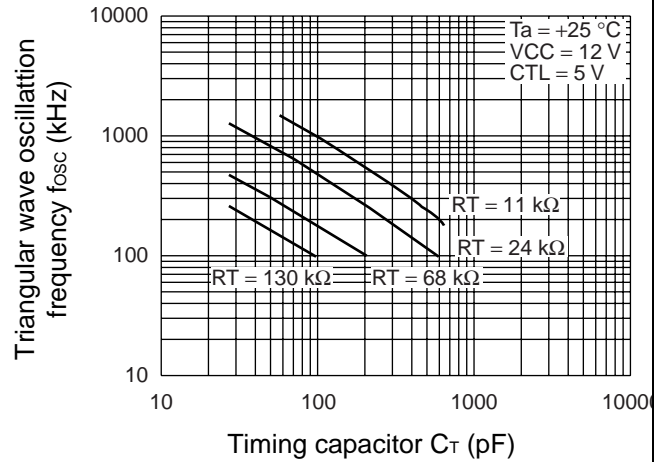


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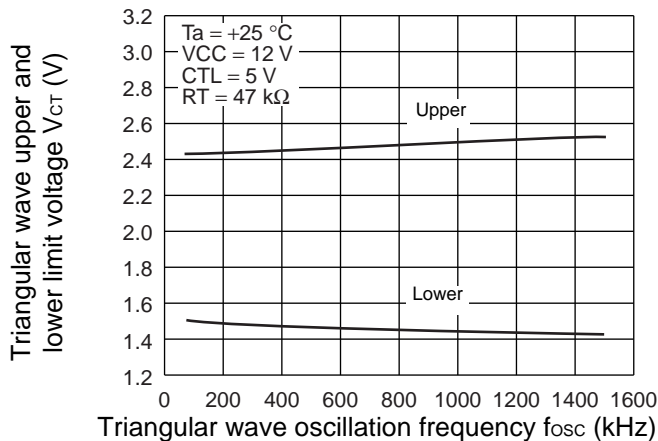
Triangular Wave Oscillation Frequency vs. Timing Resistor



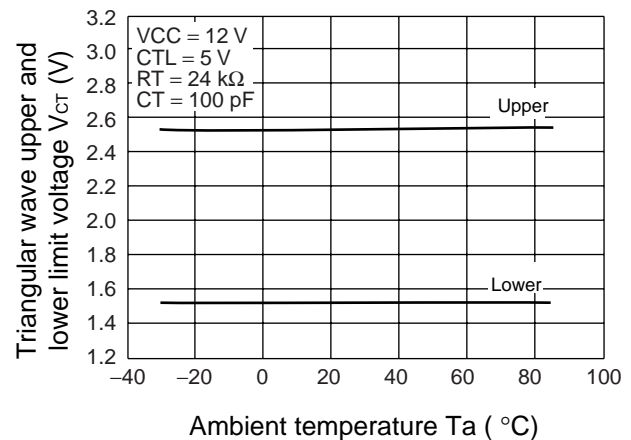
Triangular Wave Oscillation Frequency vs. Timing Capacitor



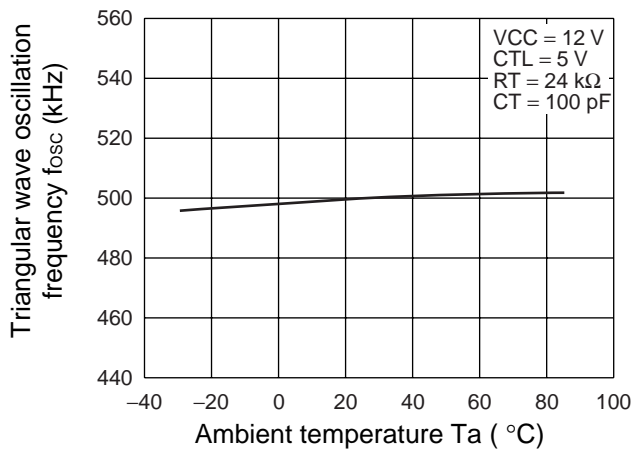
Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency



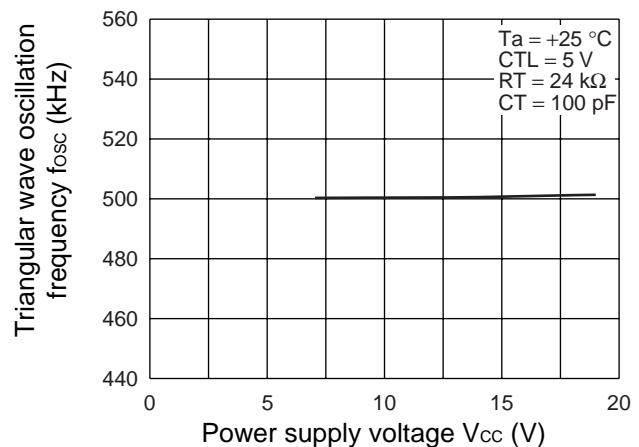
Triangular Wave Upper and Lower Limit Voltage vs. Ambient Temperature



Triangular Wave Oscillation Frequency vs. Ambient Temperature



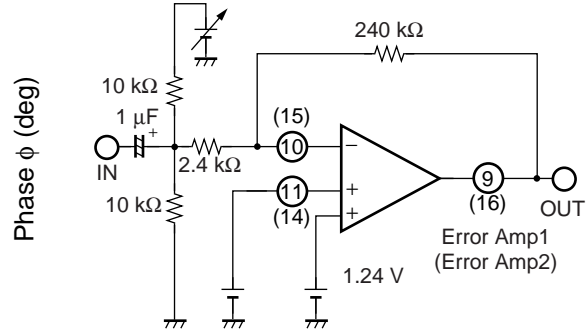
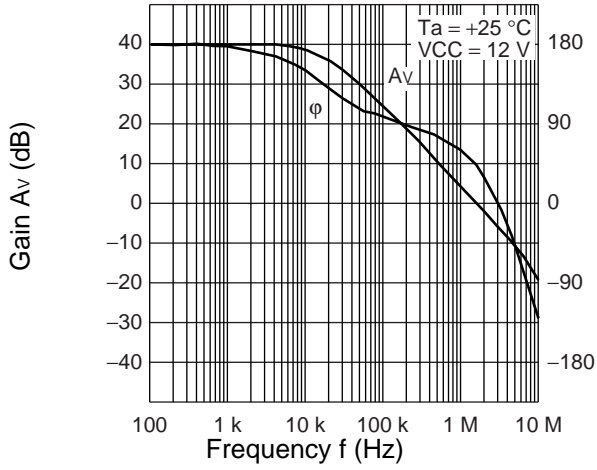
Triangular Wave Oscillation Frequency vs. Power supply voltage



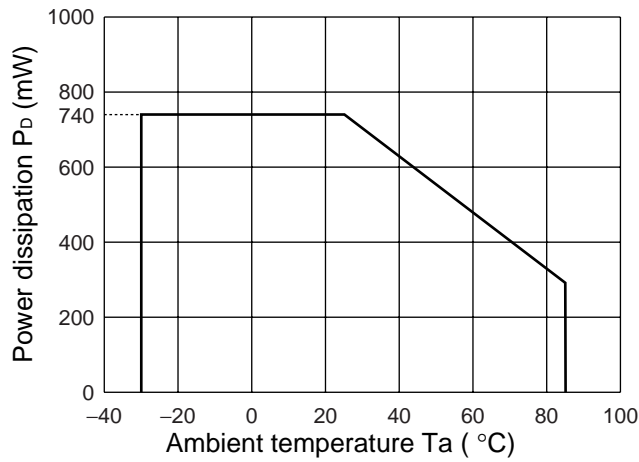
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Error Amplifier, Gain, Phase vs. Frequency



Power Dissipation vs. Ambient Temperature



■ FUNCTIONS

1. DC/DC Converter Functions

(1) Reference voltage block (REF)

The reference voltage circuit generates a temperature-compensated reference voltage (5.0 V Typ) from the voltage supplied from the power supply terminal (pin 7). The voltage is used as the reference voltage for the IC's internal circuitry.

The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 17).

(2) Triangular-wave oscillator block (OSC)

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 13) and RT terminal (pin 12) to generate triangular oscillation waveform amplitude of 1.5 V to 2.5 V.

The triangular waveforms are input to the PWM comparator in the IC.

(3) Error amplifier block (Error Amp1, Error Amp2)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS1 terminal (pin 11) and CS2 terminal (pin 14) which are the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/DC converter.

(4) PWM comparator block (PWM Comp.)

The PWM comparator is a voltage-to-pulse width modulator that controls the output duty depending on the input/output voltage.

The comparator keeps output transistor on while the error amplifier output voltage remain higher than the triangular wave voltage.

(5) Output block

The output block is in the totem pole configuration, capable of driving an external P-channel MOS FET.

(6) Bias voltage block (VH)

This bias voltage circuit outputs $V_{CC} - 5 \text{ V(Typ)}$ as minimum potential of the output circuit. In standby mode, this circuit outputs the potential equal to V_{CC} .

2. Control Function

When CTL terminal (pin 24) is "L" level, IC becomes the standby mode. The power supply current is 10 μ A (Max) at the standby mode.

On/Off Setting Conditions

| CTL | Power |
|-----|----------------|
| L | OFF (Standby) |
| H | ON (Operating) |

3. Protective Functions

(1) Timer-latch overcurrent protection circuit block (OCP)

The timer-latch overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the FET's drain and source using the external FET ON resistor, actuates the timer circuit, and starts charging the capacitor C_{SCP} connected to the CSCP terminal (pin 8). If the overcurrent remains flowing beyond the predetermined period of time, latch is set and OUT terminals (pin 3,22) of each channel are fixed at "H" level. And the circuit sets the latch to turn off the external FET. The detection current value can be set by resistor R_{LIM1} connected between the FET's drain and the ILIM1 terminal (pin 5) and resistor R_{LIM2} connected between the drain and the ILIM2 terminal (pin 20).

Changing connection enables to detect overcurrent at current sense resistor.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 17) voltage to 2.4 V (Min) or less. (See "1. Setting Timer-Latch Overcurrent Protection Detection Current" in "■ABOUT TIMER-LATCH PROTECTION CIRCUIT".)

(2) Timer-latch short-circuit protection circuit (SCP Logic, SCP Comp.)

The short-circuit detection comparator (SCP Comp.) detects the output voltage level of Error Amp, and if the error amp output voltage of any channel falls below the short-circuit detection voltage (3.1 V Typ), the timer circuits are actuated to start charging the external capacitor C_{SCP} connected to the CSCP terminal (pin 8).

When the capacitor voltage reaches about 0.73 V, the circuit is turned off the output transistor and sets the dead time to 100 %.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 24) to the "L" level to lower the VREF terminal (pin 17) voltage to 2.4 V (Min) or less. (See "2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit" in "■ABOUT TIMER-LATCH PROTECTION CIRCUIT".)

(3) Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 8) at the "L" level.

The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

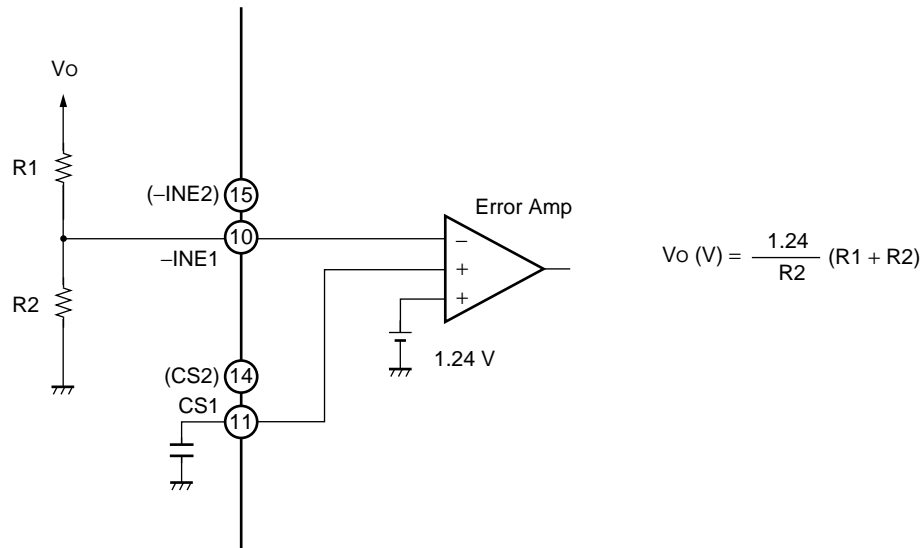
(4) Protection circuit operating function table

This table refers to output condition when protection circuit is operating.

| Operating circuit | CS1 | CS2 | OUT1 | OUT2 |
|----------------------------------|-----|-----|------|------|
| Overcurrent protection circuit | L | L | H | H |
| Short-circuit protection circuit | L | L | H | H |
| Under-voltage lockout | L | L | H | H |

■ SETTING THE OUTPUT VOLTAGE

• Output Voltage Setting Circuit



■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing capacitor (C_T) connected to the CT terminal (pin 13), and the timing resistor (R_T) connected to the RT terminal (pin 12).

Moreover, it shifts more greatly than the calculated values according to the constant of timing resistor (R_T) when the triangular wave oscillation frequency exceeds 1 MHz. Therefore, set it referring to “Triangular Wave Oscillation Frequency vs. Timing Resistor” and “Triangular Wave Oscillation Frequency vs. Timing Capacitor” in “■ TYPICAL CHARACTERISTICS”.

Triangular oscillation frequency : f_{osc}

$$f_{osc} \text{ (kHz)} \doteq \frac{1200000}{C_T \text{ (pF)} \bullet R_T \text{ (k}\Omega\text{)}}$$

■ SETTING THE SOFT-START AND DISCHARGE TIMES

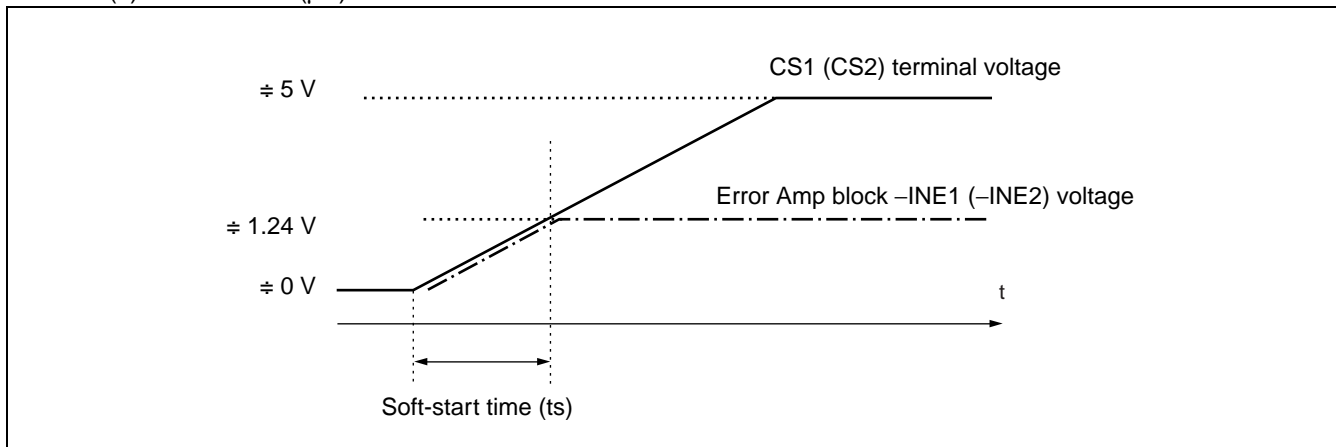
To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} and C_{S2}) to the CS1 terminal (pin 11) for channel 1 and the CS2 terminal (pin 14) for channel 2, respectively. When CTL terminal (pin 24) goes to "H" level and IC starts ($V_{CC} \geq UVLO$ threshold voltage), the external soft-start capacitors (C_{S1} and C_{S2}) connected to CS1 and CS2 terminals are charged at $10 \mu A$. The error amplifier output (FB1 (pin 9) , FB2 (pin 16)) is determined by comparison between the lower one of the potentials at two non-inverted input terminals (1.24 V, CS1 terminal voltages) and the inverted input terminal voltage ($-INE1$ (pin 10) voltage, $-INE2$ (pin 15) voltage).

The FB1 (FB2) terminal voltage is decided for the soft-start period by the comparison between 1.24 V in an internal reference voltage and the voltages of the CS1 (CS2) terminal. The DC/DC converter output voltage rises in proportion to the CS1 (CS2) terminal voltage as the soft-start capacitor connected to the CS1 (CS2) terminal is charged.

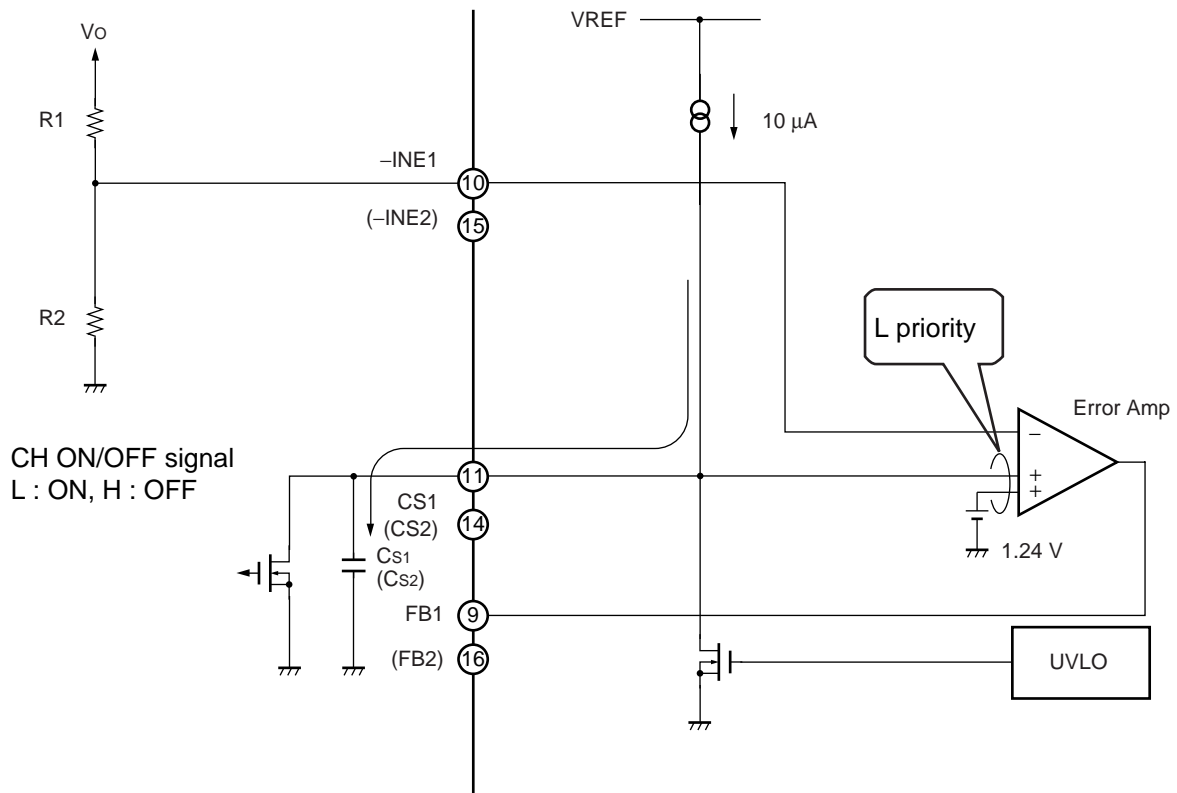
The soft-start time is obtained from the following formula:

Soft-start time: t_s (time to output 100%)

$$t_s (s) \approx 0.124 \times C_s (\mu F)$$



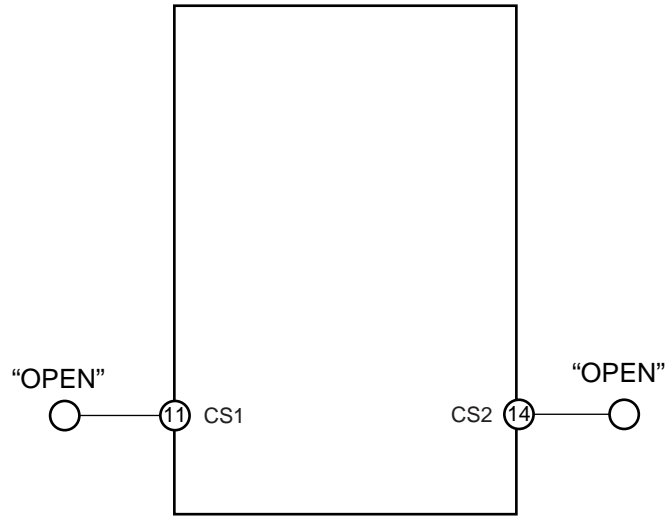
• Soft-Start Circuit



■ TREATMENT WITHOUT USING CS TERMINAL

When not using the soft-start function, open the CS1 terminal (pin 11) and the CS2 terminal (pin 14) .

- Without Setting Soft-Start Time



■ ABOUT TIMER-LATCH PROTECTION CIRCUIT

1. Setting Timer-Latch Overcurrent Protection Detection Current

The overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the FET's drain and source using the external FET ON resistor (R_{ON}), actuates the timer circuit, and starts charging the capacitor C_{SCP} connected to the CSCP terminal (pin 8). If the overcurrent remains flowing beyond the predetermined period of time, the circuit sets the latch to fix OUT terminals (pin 3, 22) at "H" level and turn off the external FET. The detection current value can be set by the resistors (R_{LIM1} and R_{LIM2}) connected between the FET's drain and the ILIM1 terminal (pin 5) and between the drain and the ILIM2 terminal (pin 20), respectively.

The internal current (I_{LIM}) can be set by the timing resistor (R_T) connected to the RT terminal (pin 12). Time until activating timer circuit and setting latch is equal to short-circuit detection time in "2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit".

Internal current value: I_{LIM}

$$I_{LIM} (\mu A) \cong \frac{2700}{R_T (k\Omega)}$$

Detection current value: I_{OCP}

$$I_{OCP} (A) \cong \frac{I_{LIM}(A) \times R_{LIM}(\Omega)}{R_{ON} (\Omega)} - \frac{(V_{IN}(V) - V_o(V)) \times V_o(V)}{2 \times V_{IN}(V) \times f_{osc}(Hz) \times L(H)}$$

R_{LIM} : Overcurrent detection resistor

R_{ON} : External FET ON resistor

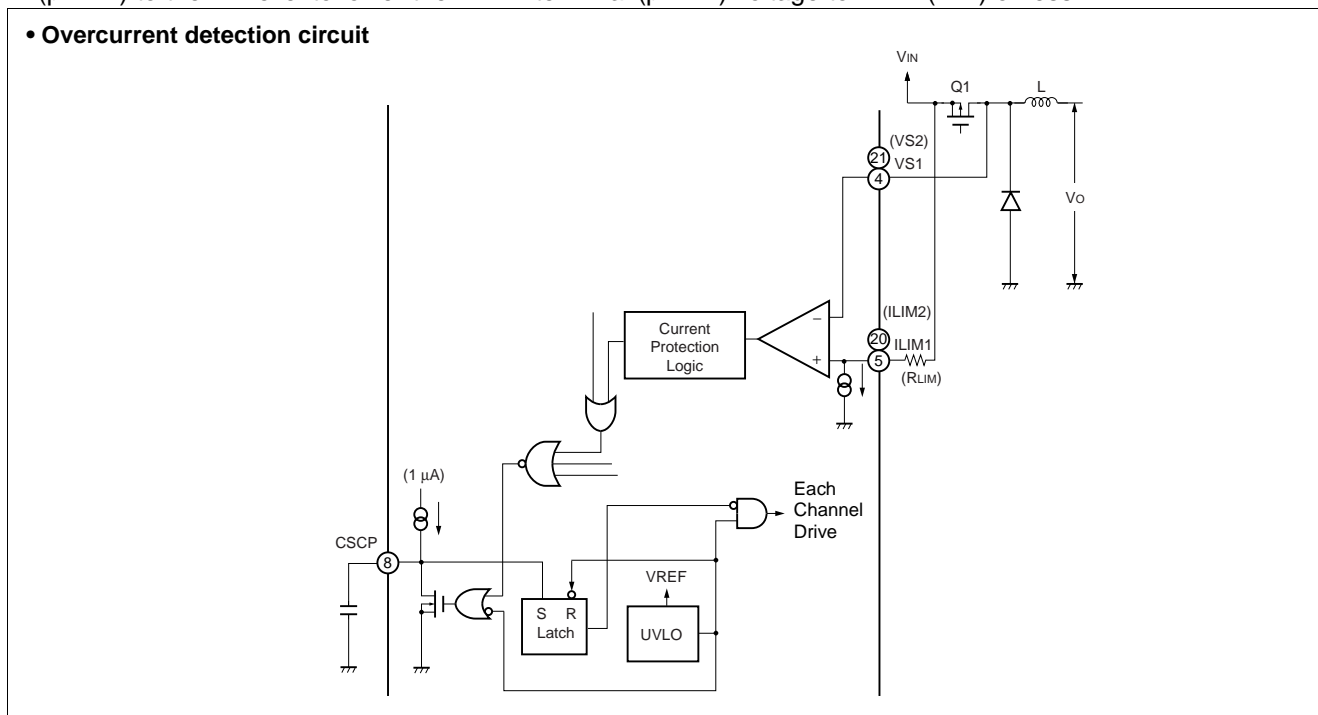
V_{IN} : Input voltage

V_o : DC/DC converter output voltage

f_{osc} : Oscillation frequency

L : Coil inductance

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 24) to the "L" level to lower the VREF terminal (pin 17) voltage to 2.4 V (Min) or less.



Overcurrent Protection Circuit: Range of Operation

When an overcurrent flow occurs, if the increased voltage between the drain and source of the FET is detected by means of the external FET (Q1) resistor, operational stability is lost when the external FET (Q1) ON interval determined by the oscillation frequency, input voltage, and output voltage falls below 450 ns.

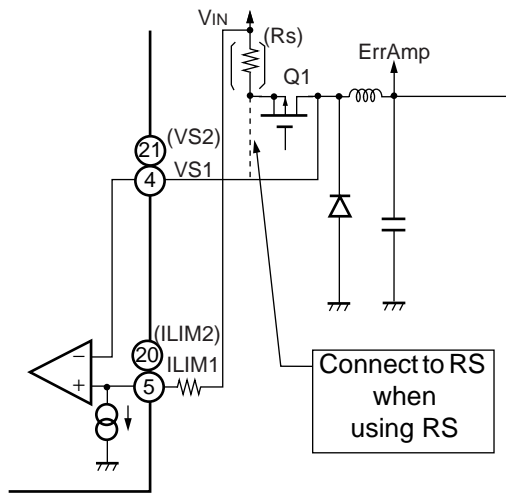
Therefore, the circuit should be used within a range that ensures that the ON interval does not fall below 450ns, according to the following formula.

$$\text{ON interval } 450 \text{ (ns)} \geq \frac{V_o \text{ (V)}}{V_{IN} \text{ (V)} \times f_{osc} \text{ (Hz)}}$$

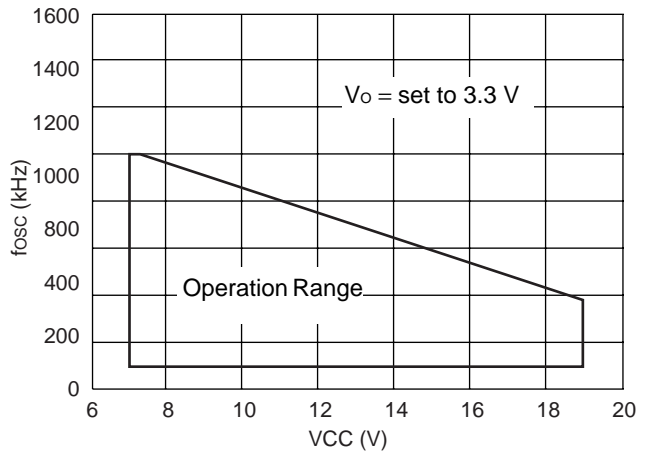
If the ON interval of the external FET (Q1) is below 450ns, we recommend the use of an overcurrent detection resistor RS to detect overcurrent, as shown below.

This example shows the range of operation of the overcurrent detection function with a setting of $V_o = 3.3\text{V}$.

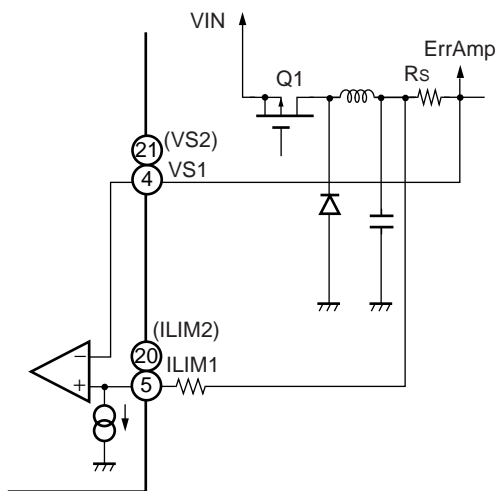
• Method to detect by current when external FET(Q1) is turned on



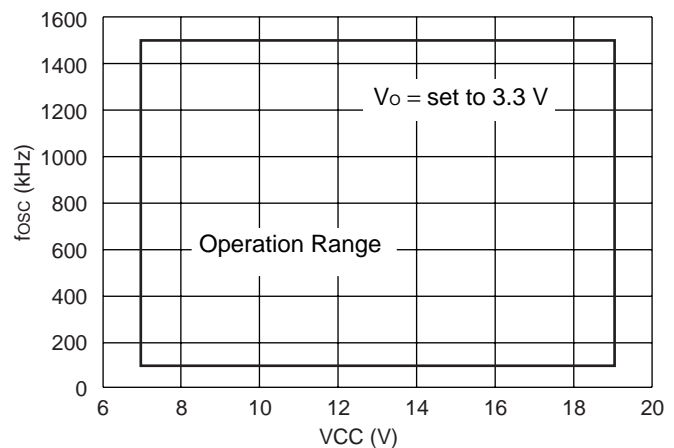
Overcurrent Detection Function Operating Range



• Method to detect by mean current



Overcurrent Detection Function Operating Range



2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage (3.1 V Typ).

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 8) is held at "L" level.

If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator goes to "H" level. This causes the external short-circuit protection capacitor C_{SCP} connected to the CSCP terminal to be charged at $1 \mu\text{A}$.

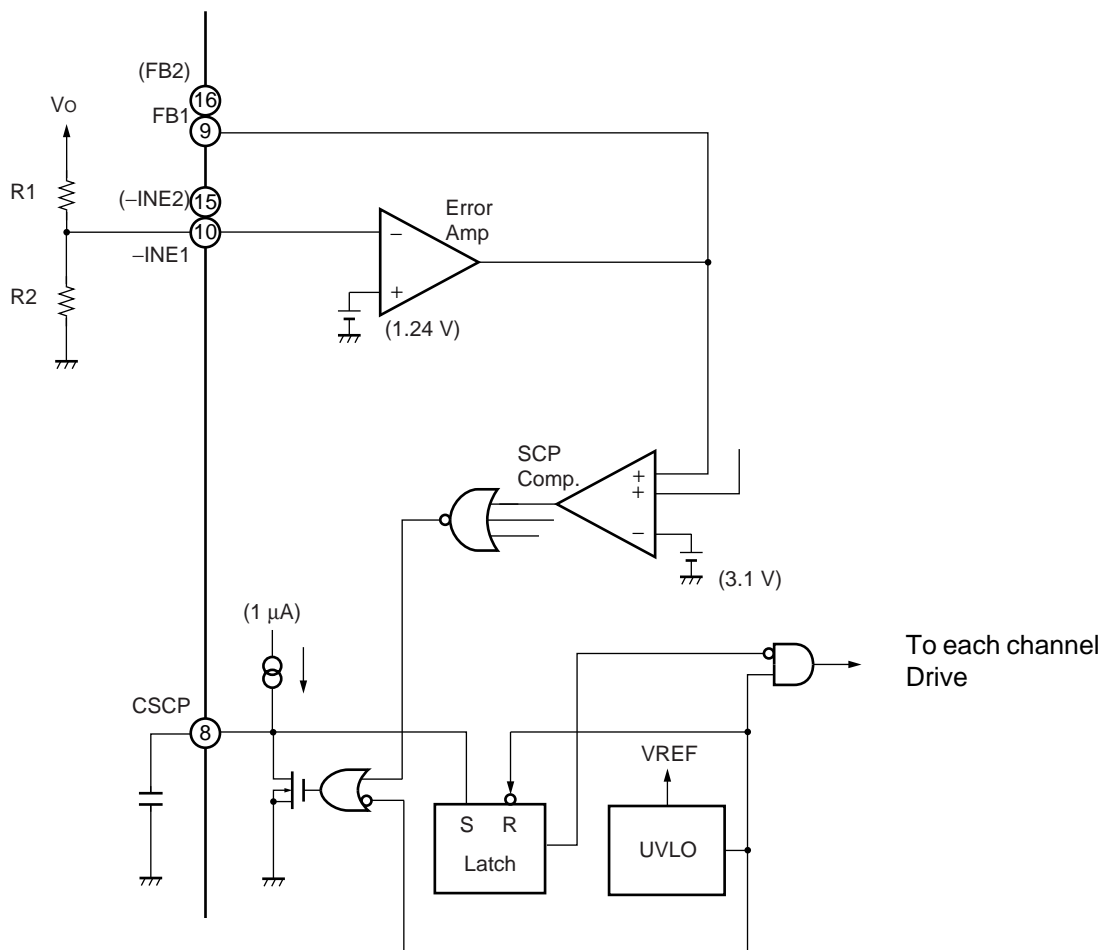
Short-circuit detection time (t_{SCP})

$$t_{SCP} \text{ (s)} \approx 0.73 \times C_{SCP} \text{ (\mu F)}$$

When the capacitor C_{SCP} is charged to the threshold voltage ($V_{TH} \approx 0.73 \text{ V}$), the latch is set and the external FET is turned off (dead time is set to 100%). At this time, the latch input is closed and the CSCP terminal is held at "L" level. If a short-circuit is detected on either of the two channels, both channels are shut off.

When the power supply is turned on back or VREF terminal (pin 17) voltage is less than 2.4 V (Min) by setting CTL terminal (pin 24) to "L" level, the latch is released.

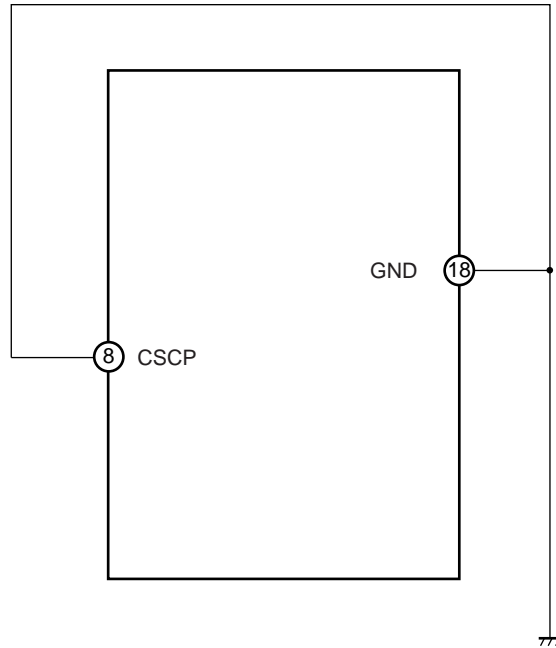
• Timer-latch short-circuit protection circuit



■ TREATMENT WITHOUT USING CSCP TERMINAL

When not using the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 8) to GND with the shortest distance.

• Treatment without using CSCP

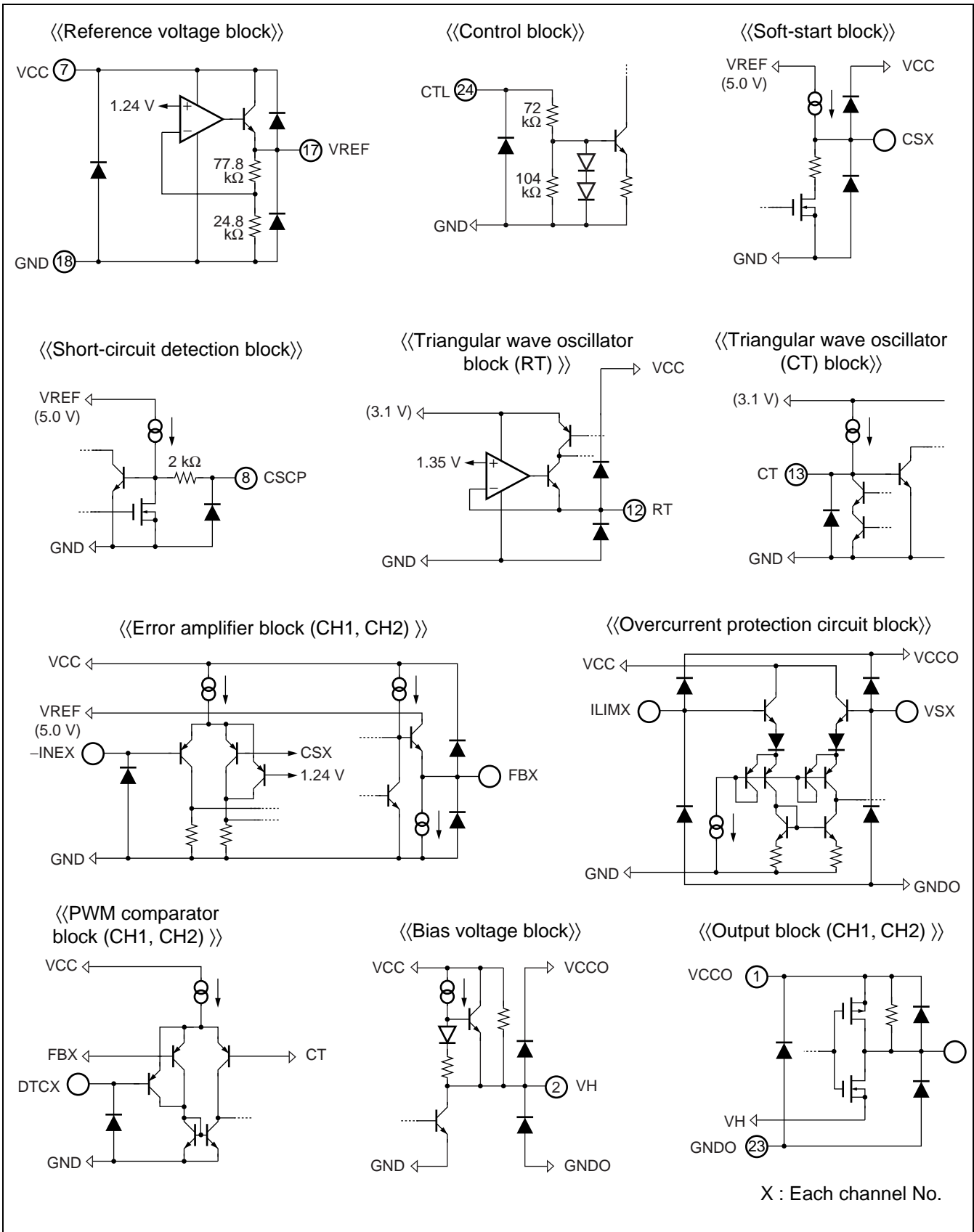


■ RESETTING THE LATCH OF EACH PROTECTION CIRCUIT

When the overcurrent, or short-circuit protection circuit detects each abnormality, it sets the latch to fix the output at the "L" level.

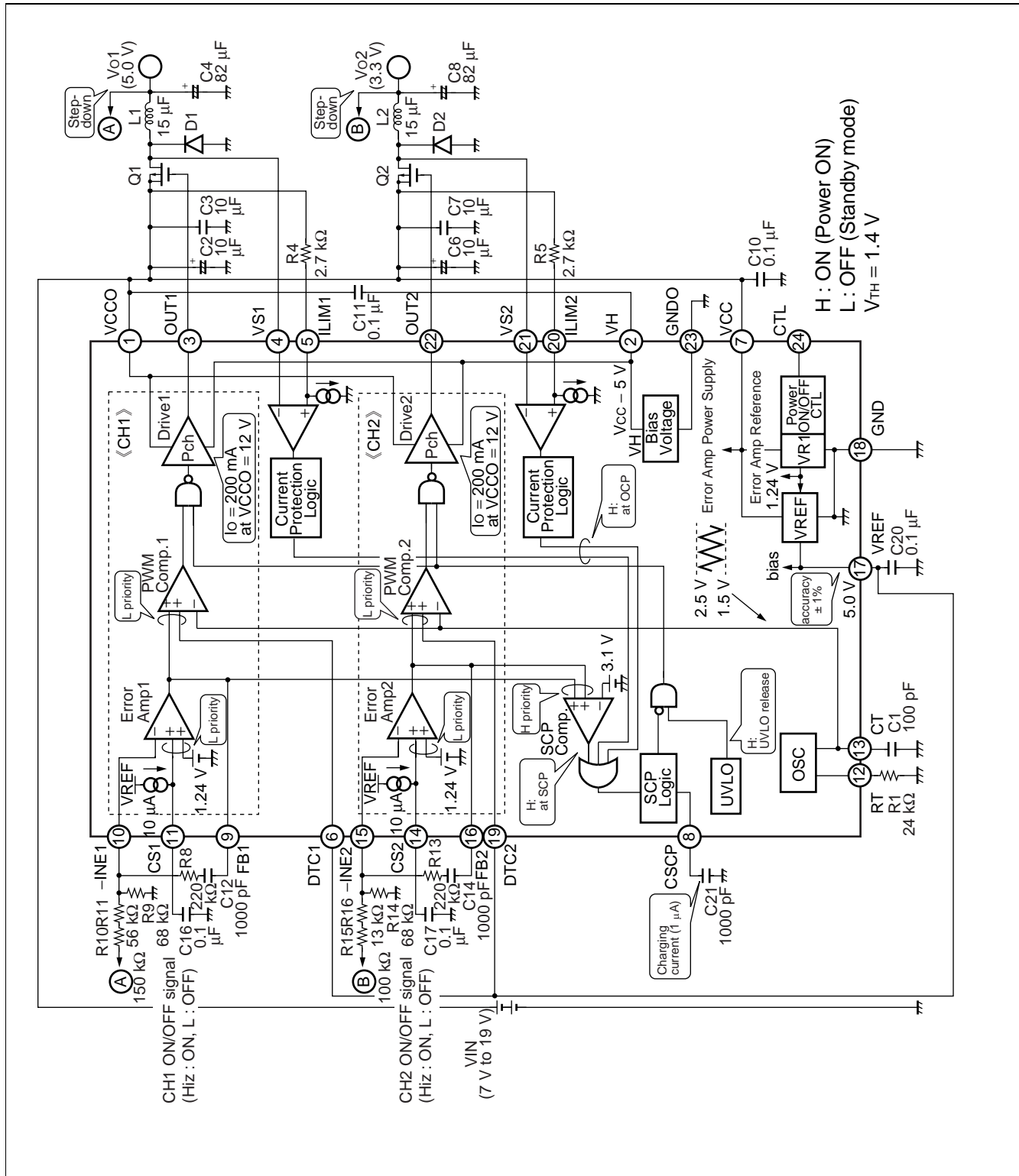
To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 24) to the "L" level to lower the VREF terminal (pin 17) voltage to 2.4 V (Min) or less.

I/O EQUIVALENT CIRCUIT



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APPLICATION EXAMPLE



■ PARTS LIST

| COMPONENT | ITEM | SPECIFICATION | | VENDOR | PARTS No. |
|---------------|--------------------|---------------------------------|----------------------|---------|---------------|
| Q1, Q2 | Pch FET | VDS = -30 V, ID = -6 A | | TOSHIBA | TPC8102 |
| D1, D2 | Diode | VF = 0.42 V (Max) , at IF = 3 A | | ROHM | RB0530L-30 |
| L1, L2 | Inductor | 15 μ H | 3.6 A, 50 m Ω | SUMIDA | CDRH104R-150 |
| C1 | Ceramics Condenser | 100 pF | 50 V | TDK | C1608CH1H101J |
| C2, C6 | OS-CON™ | 10 μ F | 20 V | SANYO | 20SVP10M |
| C3, C7 | Ceramics Condenser | 10 μ F | 25 V | TDK | C3225JF1E106Z |
| C4, C8 | OS-CON™ | 82 μ F | 6.3 V | SANYO | 6SVP82M |
| C10, C11, C20 | Ceramics Condenser | 0.1 μ F | 50 V | TDK | C1608JB1H104K |
| C12, C14, C21 | Ceramics Condenser | 1000 pF | 50 V | TDK | C1608JB1H102K |
| C16, C17 | Ceramics Condenser | 0.1 μ F | 50 V | TDK | C1608JB1H104K |
| R1 | Resistor | 24 k Ω | 0.5 % | ssm | RR0816P-243-D |
| R4, R5 | Resistor | 2.7 k Ω | 0.5 % | ssm | RR0816P-272-D |
| R8, R13 | Resistor | 220 k Ω | 0.5 % | ssm | RR0816P-224-D |
| R9, R14 | Resistor | 68 k Ω | 0.5 % | ssm | RR0816P-683-D |
| R10 | Resistor | 150 k Ω | 0.5 % | ssm | RR0816P-154-D |
| R11 | Resistor | 56 k Ω | 0.5 % | ssm | RR0816P-563-D |
| R15 | Resistor | 100 k Ω | 0.5 % | ssm | RR0816P-104-D |
| R16 | Resistor | 13 k Ω | 0.5 % | ssm | RR0816P-133-D |

Note : TOSHIBA : TOSHIBA Corporation
 ROHM : ROHM Co., Ltd
 SANYO : SANYO Electric Co., Ltd.
 TDK : TDK Corporation
 SUMIDA : SUMIDA Electric Co., Ltd.
 ssm : SUSUMU Co., Ltd.

■ SELECTION OF COMPONENTS

• Pch MOS FET

The P-ch MOSFET for switching use should be rated for at least 20% more than the maximum input voltage. To minimize continuity loss, use a FET with low $R_{DS(ON)}$ between the drain and source. For high input voltage and high frequency operation, on/off-cycle switching loss will be higher so that power dissipation must be considered. In this application, the Toshiba TPC8102 is used. Continuity loss, on/off switching loss, and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values, and also must be in accordance with overcurrent detection levels.

Continuity loss : P_C

$$P_C = I_D^2 \times R_{DS(ON)} \times \text{Duty}$$

On-cycle switching loss : $P_{S(ON)}$

$$P_{S(ON)} = \frac{V_{D(Max)} \times I_D \times t_r \times f_{OSC}}{6}$$

Off-cycle switching loss : $P_{S(OFF)}$

$$P_{S(OFF)} = \frac{V_{D(Max)} \times I_{D(Max)} \times t_f \times f_{OSC}}{6}$$

Total loss : P_T

$$P_T = P_C + P_{S(ON)} + P_{S(OFF)}$$

Example: Using the Toshiba TPC8102

CH1

Input voltage $V_{IN(Max)} = 19\text{ V}$, output voltage $V_O = 5\text{ V}$, drain current $I_D = 3\text{ A}$, Oscillation frequency $f_{OSC} = 500\text{ kHz}$, $L = 15\text{ }\mu\text{H}$, drain-source on resistance $R_{DS(ON)} \cong 50\text{ m}\Omega$, $t_r = t_f \cong 100\text{ ns}$.

Drain current (Max) : $I_{D(Max)}$

$$\begin{aligned} I_{D(Max)} &= I_O + \frac{V_{IN} - V_O}{2L} t_{on} \\ &= 3 + \frac{19 - 5}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.263 \\ &\cong \underline{3.25\text{ (A)}} \end{aligned}$$

Drain current (Min) : $I_{D(Min)}$

$$\begin{aligned} I_{D(Min)} &= I_O - \frac{V_{IN} - V_O}{2L} t_{on} \\ &= 3 - \frac{19 - 5}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.263 \\ &\cong \underline{2.75\text{ (A)}} \end{aligned}$$

$$\begin{aligned}
 P_C &= I_D^2 \times R_{DS(ON)} \times \text{Duty} \\
 &= 3^2 \times 0.05 \times 0.263 \\
 &\doteq \underline{0.118 \text{ W}}
 \end{aligned}$$

$$\begin{aligned}
 P_{S(ON)} &= \frac{V_{D(Max)} \times I_D \times t_r \times f_{OSC}}{6} \\
 &= \frac{19 \times 3 \times 100 \times 10^{-9} \times 500 \times 10^3}{6} \\
 &\doteq \underline{0.475 \text{ W}}
 \end{aligned}$$

$$\begin{aligned}
 P_{S(OFF)} &= \frac{V_{D(Max)} \times I_{D(Max)} \times t_f \times f_{OSC}}{6} \\
 &= \frac{19 \times 3.25 \times 100 \times 10^{-9} \times 500 \times 10^3}{6} \\
 &\doteq \underline{0.515 \text{ W}}
 \end{aligned}$$

$$\begin{aligned}
 P_T &= P_C + P_{S(ON)} + P_{S(OFF)} \\
 &\doteq 0.118 + 0.475 + 0.515 \\
 &\doteq \underline{1.108 \text{ W}}
 \end{aligned}$$

The above power dissipation figures for the TPC8102 are satisfied with ample margin at 2.4 W (Ta = +25 °C) .

CH2

Input voltage $V_{IN(Max)} = 19 \text{ V}$ output voltage $V_O = 3.3 \text{ V}$, drain current $I_D = 3 \text{ A}$, Oscillation frequency $f_{OSC} = 500 \text{ kHz}$, $L = 15 \mu\text{H}$, drain-source on resistance $R_{DS(ON)} \doteq 50 \text{ m}\Omega$, $t_r = t_f \doteq 100 \text{ ns}$.

Drain current (Max) : $I_{D(Max)}$

$$\begin{aligned}
 I_{D(Max)} &= I_O + \frac{V_{IN} - V_O}{2L} t_{on} \\
 &= 3 + \frac{19 - 3.3}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.174 \\
 &\doteq \underline{3.18 \text{ (A)}}
 \end{aligned}$$

Drain current (Min) : $I_{D(Min)}$

$$\begin{aligned}
 I_{D(Min)} &= I_O - \frac{V_{IN} - V_O}{2L} t_{on} \\
 &= 3 - \frac{19 - 3.3}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.174 \\
 &\doteq \underline{2.82 \text{ (A)}}
 \end{aligned}$$

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$$\begin{aligned} P_C &= I_D^2 \times R_{DS(ON)} \times \text{Duty} \\ &= 3^2 \times 0.05 \times 0.174 \\ &\approx \underline{0.078 \text{ W}} \end{aligned}$$

$$\begin{aligned} P_{S(ON)} &= \frac{V_{D(Max)} \times I_D \times tr \times f_{osc}}{6} \\ &= \frac{19 \times 3 \times 100 \times 10^{-9} \times 500 \times 10^3}{6} \\ &\approx \underline{0.475 \text{ W}} \end{aligned}$$

$$\begin{aligned} P_{S(OFF)} &= \frac{V_{D(Max)} \times I_{D(Max)} \times tf \times f_{osc}}{6} \\ &= \frac{19 \times 3.18 \times 100 \times 10^{-9} \times 500 \times 10^3}{6} \\ &\approx \underline{0.504 \text{ W}} \end{aligned}$$

$$\begin{aligned} P_T &= P_C + P_{S(ON)} + P_{S(OFF)} \\ &\approx 0.078 + 0.475 + 0.504 \\ &\approx \underline{1.057 \text{ W}} \end{aligned}$$

The above power dissipation figures for the TPC8102 are satisfied with ample margin at 2.4 W ($T_a = +25^\circ\text{C}$).

• Inductors

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light loads. Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.

Note also that the DC superimposition characteristics become worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency. The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current.

Inductance values are determined by the following formulas.

The L value for all load current conditions is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

$$\begin{aligned} &\text{Inductance value : L} \\ L &\geq \frac{2(V_{IN} - V_O)}{I_o} \text{ton} \end{aligned}$$

Example:

CH1

$$L \geq \frac{2(V_{IN} - V_o)}{I_o} t_{on}$$

$$\geq \frac{2 \times (19 - 5)}{I_o} \times \frac{1}{500 \times 10^3} \times 0.263$$

$$\geq \underline{4.91 \mu H}$$

CH2

$$L \geq \frac{2(V_{IN} - V_o)}{I_o} t_{on}$$

$$\geq \frac{2 \times (19 - 3.3)}{I_o} \times \frac{1}{500 \times 10^3} \times 0.174$$

$$\geq \underline{3.64 \mu H}$$

Inductance values derived from the above formulas are values that provide sufficient margin for continuous operation at maximum load current, but at which continuous operation is not possible at light loads. It is therefore necessary to determine the load level at which continuous operation becomes possible. In this application, the Sumida CDRH104R-150 is used. At 15 μH , the load current value under continuous operating conditions is determined by the following formula.

Load current value under continuous operating conditions : I_o

$$I_o \geq \frac{V_o}{2L} t_{off}$$

Example: Using the CDRH104R-150

15 μH (allowable tolerance $\pm 30\%$) , rated current = 3.6 A

CH1

$$I_o \geq \frac{V_o}{2L} t_{off}$$

$$\geq \frac{5}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.263)$$

$$\geq \underline{245.7 \text{ mA}}$$

CH2

$$I_o \geq \frac{V_o}{2L} t_{off}$$

$$\geq \frac{3.3}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.174)$$

$$\geq \underline{181.7 \text{ mA}}$$

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To determine whether the current through the inductor is within rated values, it is necessary to determine the peak value of the ripple current as well as the peak-to-peak values of the ripple current that affect the output ripple voltage. The peak value and peak-to-peak value of the ripple current can be determined by the following formulas.

Peak value : I_L

$$I_L \geq I_o + \frac{V_{IN} - V_o}{2L} \text{ton}$$

Peak-to-peak value : ΔI_L

$$\Delta I_L = \frac{V_{IN} - V_o}{L} \text{ton}$$

Example: Using the CDRH104R-150

15 μH (allowable tolerance $\pm 30\%$) , rated current = 3.6 A

Peak value:

CH1

$$\begin{aligned} I_L &\geq I_o + \frac{V_{IN} - V_o}{2L} \text{ton} \\ &\geq 3 + \frac{19 - 5}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.263 \\ &\geq \underline{3.25 \text{ A}} \end{aligned}$$

CH2

$$\begin{aligned} I_L &\geq I_o + \frac{V_{IN} - V_o}{2L} \text{ton} \\ &\geq 3 + \frac{19 - 3.3}{2 \times 15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.174 \\ &\geq \underline{3.18 \text{ A}} \end{aligned}$$

Peak-to-peak value:

CH1

$$\begin{aligned} \Delta I_L &= \frac{V_{IN} - V_o}{L} \text{ton} \\ &= \frac{19 - 5}{15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.263 \\ &= \underline{0.491 \text{ A}} \end{aligned}$$

CH2

$$\begin{aligned} \Delta I_L &= \frac{V_{IN} - V_o}{L} \text{ton} \\ &= \frac{19 - 3.3}{15 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.174 \\ &= \underline{0.364 \text{ A}} \end{aligned}$$

• Flyback diode

The flyback diode is generally used as a Schottky barrier diode (SBD) when the reverse voltage to the diode is less than 40V. The SBD has the characteristics of higher speed in terms of faster reverse recovery time, and lower forward voltage, and is ideal for achieving high efficiency. As long as the DC reverse voltage is sufficiently higher than the input voltage, the average current flowing through the diode is within the average output current level, and peak current is within peak surge current limits, there is no problem. In this application the Rohm RB053L-30 is used. The diode average current and diode peak current can be calculated by the following formulas.

Diode mean current : I_{Di}

$$I_{Di} \geq I_o \times \left(1 - \frac{V_o}{V_{IN}}\right)$$

Diode peak current : I_{Dip}

$$I_{Dip} \geq \left(I_o + \frac{V_o}{2L} \text{toff}\right)$$

Example: Using the Rohm RB053L-30

VR (DC reverse voltage) = 30 V, average output voltage = 3.0 A, peak surge current = 70 A,

VF (forward voltage) = 0.42 V, IF = 3.0 A

CH1

$$I_{Di} \geq I_o \times \left(1 - \frac{V_o}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.263)$$

$$\geq \underline{2.21 \text{ A}}$$

CH2

$$I_{Di} \geq I_o \times \left(1 - \frac{V_o}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.174)$$

$$\geq \underline{2.48 \text{ A}}$$

CH1

$$I_{Dip} \geq \left(I_o + \frac{V_o}{2L} \text{toff}\right)$$

$$\geq \underline{3.24 \text{ A}}$$

CH2

$$I_{Dip} \geq \left(I_o + \frac{V_o}{2L} \text{toff}\right)$$

$$\geq \underline{3.18 \text{ A}}$$

• Smoothing Capacitor

The smoothing capacitor is an indispensable element for reducing ripple voltage in output. In selecting a smoothing capacitor it is essential to consider equivalent series resistance (ESR) and allowable ripple current. Higher ESR means higher ripple voltage, so that to reduce ripple voltage it is necessary to select a capacitor with low ESR. However, the use of a capacitor with low ESR can have substantial effects on loop phase characteristics, and therefore requires attention to system stability. Care should also be taken to use a capacity with sufficient margin for allowable ripple current. This application uses the (OS-CON™) 6SVP82M made by Sanyo. The ESR, capacitance value, and ripple current can be calculated from the following formulas.

Equivalent Series Resistance : ESR

$$ESR \leq \frac{\Delta V_o}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

Capacitance value : C_L

$$C_L \geq \frac{\Delta I_L}{2\pi f (\Delta V_o - \Delta I_L \times ESR)}$$

Ripple current : I_{C_Lrms}

$$I_{C_Lrms} \geq \frac{(V_{IN} - V_o) \text{ ton}}{2\sqrt{3}L}$$

Example: Using the 6SVP82M

Rated voltage = 6.3 V, ESR = 50 mΩ, maximum allowable ripple current = 1570 mArms

Equivalent series resistance

CH1

$$\begin{aligned} ESR &\leq \frac{\Delta V_o}{\Delta I_L} - \frac{1}{2\pi f C_L} \\ &\leq \frac{0.050}{0.491} - \frac{1}{2\pi \times 500 \times 10^3 \times 82 \times 10^{-6}} \\ &\leq \underline{98.0 \text{ m}\Omega} \end{aligned}$$

CH2

$$\begin{aligned} \text{ESR} &\leq \frac{\Delta V_o}{\Delta I_L} - \frac{1}{2\pi f C_L} \\ &\leq \frac{0.033}{0.364} - \frac{1}{2\pi \times 500 \times 10^3 \times 82 \times 10^{-6}} \\ &\leq \underline{86.8 \text{ m}\Omega} \end{aligned}$$

Capacitance value

CH1

$$\begin{aligned} C_L &\geq \frac{\Delta I_L}{2\pi f (\Delta V_o - \Delta I_L \times \text{ESR})} \\ &\geq \frac{0.491}{2\pi \times 500 \times 10^3 \times (0.050 - 0.491 \times 0.05)} \\ &\geq \underline{6.14 \mu\text{F}} \end{aligned}$$

CH2

$$\begin{aligned} C_L &\geq \frac{\Delta I_L}{2\pi f (\Delta V_o - \Delta I_L \times \text{ESR})} \\ &\geq \frac{0.364}{2\pi \times 500 \times 10^3 \times (0.033 - 0.364 \times 0.05)} \\ &\geq \underline{7.83 \mu\text{F}} \end{aligned}$$

Ripple current

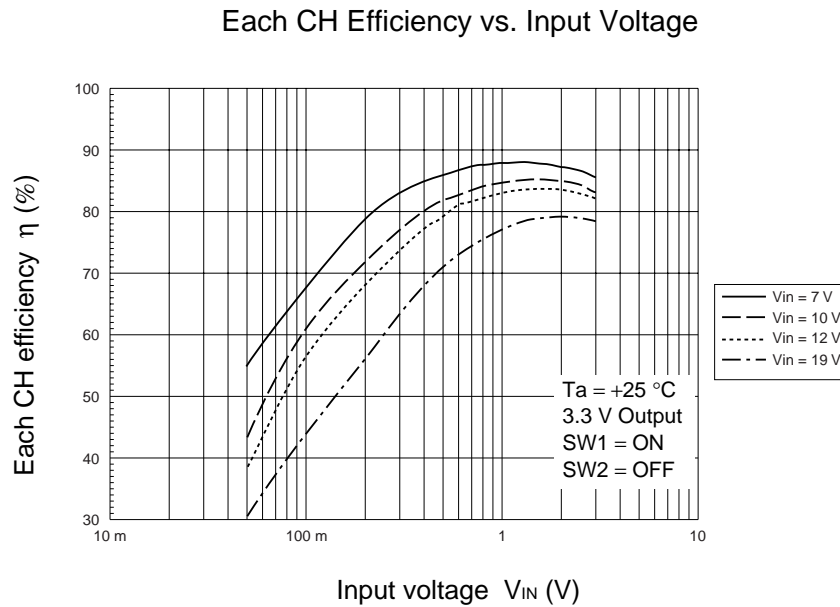
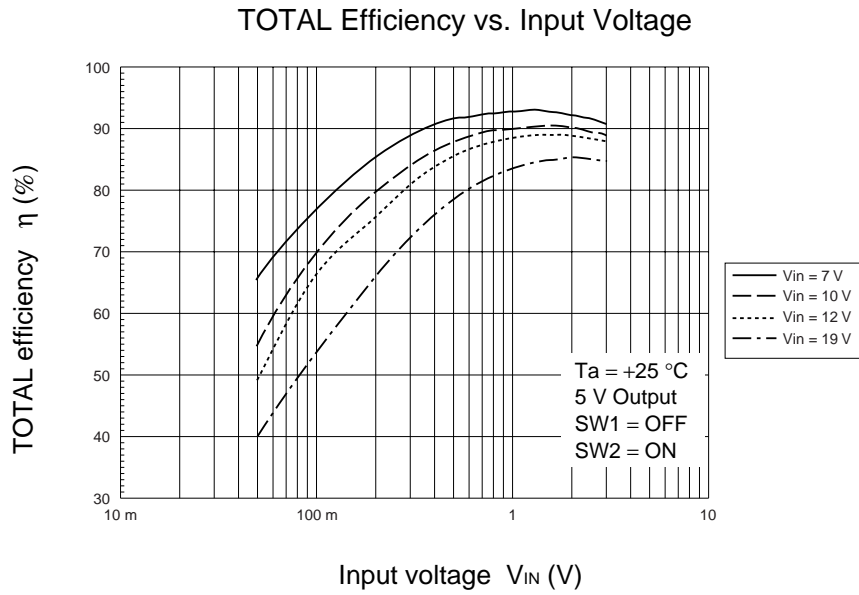
CH1

$$\begin{aligned} I_{C_L \text{rms}} &\geq \frac{(V_{IN} - V_o) \text{ton}}{2\sqrt{3}L} \\ &\geq \frac{(19 - 5) \times 0.263}{2\sqrt{3} \times 15 \times 10^{-6} \times 500 \times 10^3} \\ &\geq \underline{141.7 \text{ mArms}} \end{aligned}$$

CH2

$$\begin{aligned} I_{C_L \text{rms}} &\geq \frac{(V_{IN} - V_o) \text{ton}}{2\sqrt{3}L} \\ &\geq \frac{(19 - 3.3) \times 0.174}{2\sqrt{3} \times 15 \times 10^{-6} \times 500 \times 10^3} \\ &\geq \underline{105.1 \text{ mArms}} \end{aligned}$$

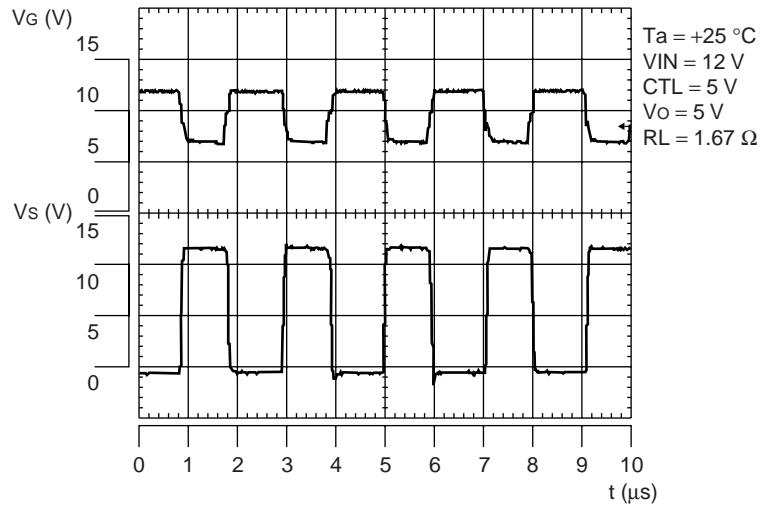
■ REFERENCE DATA



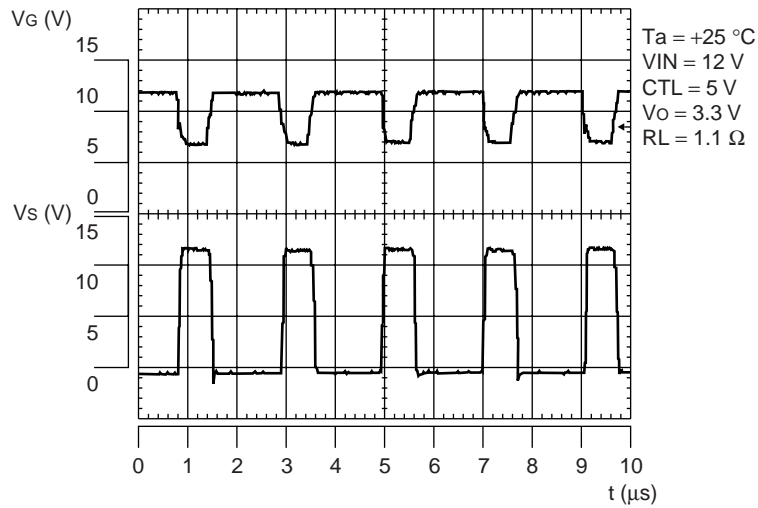
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Switching Wave Form (CH1)



Switching Wave Form (CH2)



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■ USAGE PRECAUTION

- Printed circuit board ground lines should be set up with consideration for common impedance.
- Take appropriate static electricity measures.
 - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
 - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
 - Work platforms, tools, and instruments should be properly grounded.
 - Working personnel should be grounded with resistance of 250 k Ω to 1 M Ω between body and ground.
- Do not apply negative voltages.

The use of negative voltages below -0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

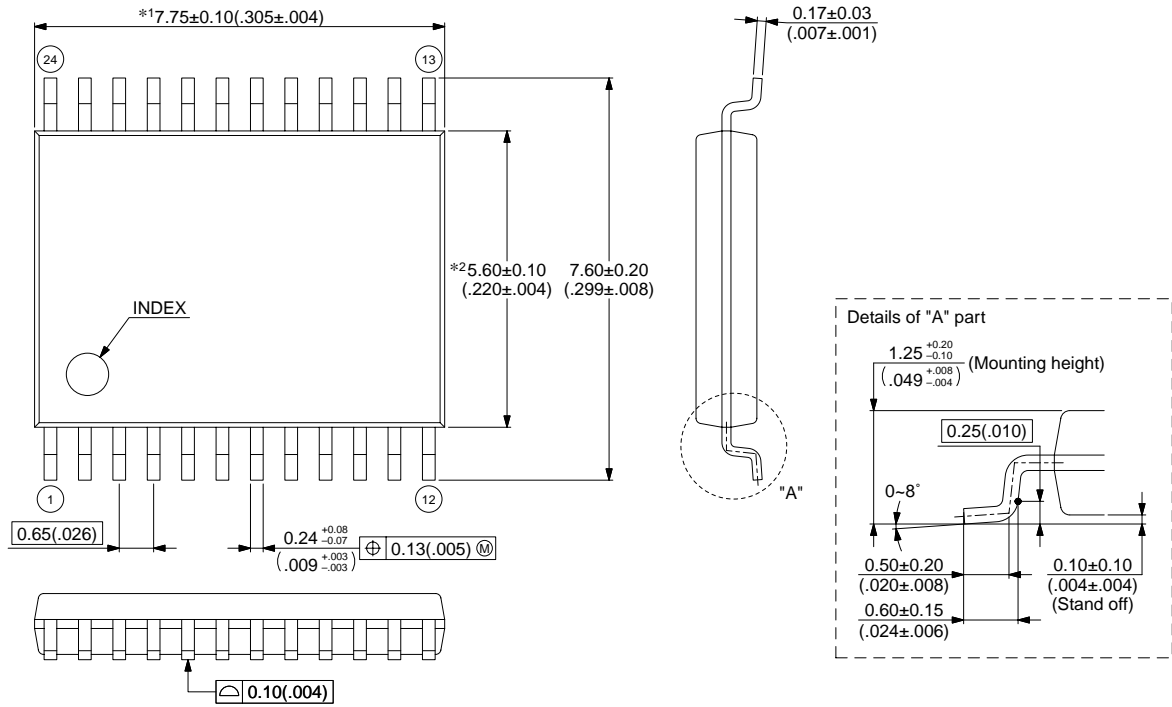
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|--------------------------------------|---------|
| MB39A104PFV | 24-pin plastic SSOP (FPT-24P-M03) | |

■ PACKAGE DIMENSIONS

24-pin plastic SSOP
(FPT-24P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) MAX) .
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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