FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27242-1E

ASSP For Power Supply Applications

5 ch DC/DC Converter IC with Synchronous Rectification

MB39A115

■ DESCRIPTION

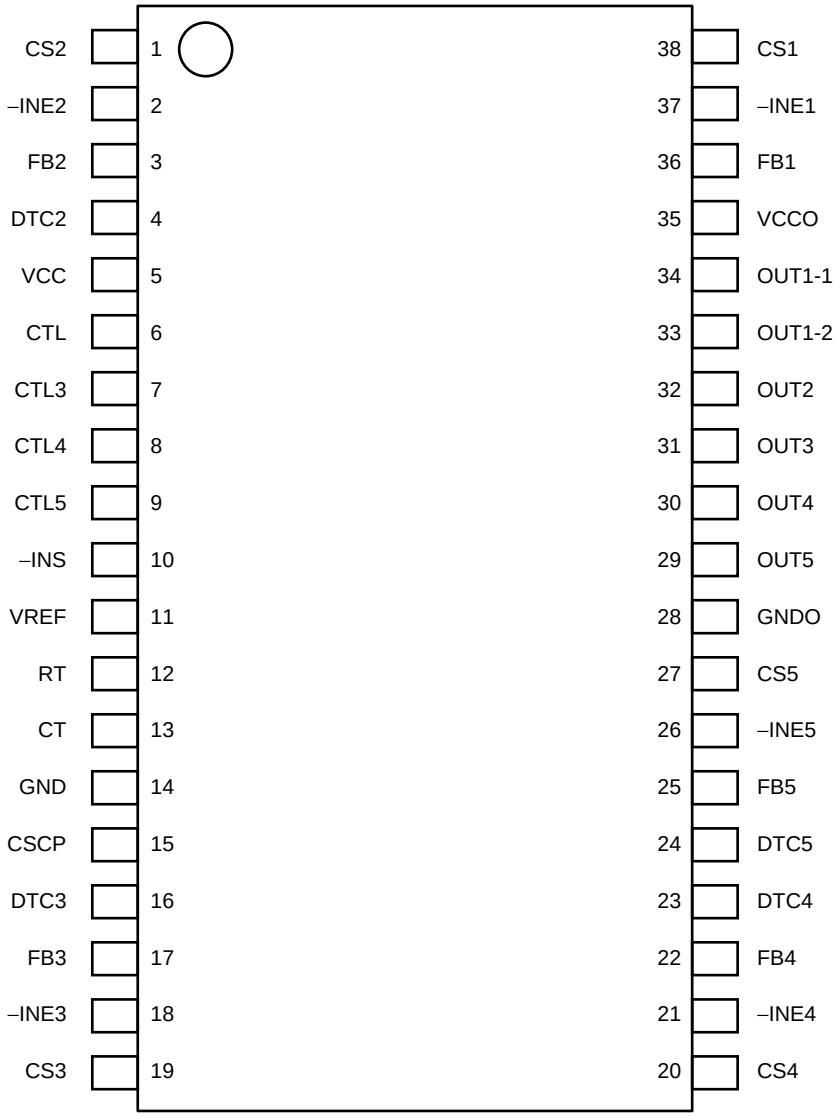
The MB39A115 is a 5-channel DC/DC converter IC using pulse width modulation (PWM) , and the MB39A115 is suitable for up conversion, down conversion, and up/down converstion. The MB39A115 is built in 5 channels into TSSOP-38P/BCC-40P package and operates at 2 MHz maximum and, this IC can control and soft-start at each channel. The MB39A115 is suitable for power supply of high performance potable instruments such as a digital still camera (DSC).

■ FEATURES

- Supports for down-conversion with synchronous rectification (ch.1)
- Supports for down-conversion and up/down Zeta conversion (ch.2 to ch.4)
- Supports for up-conversion and up/down Sepic conversion (ch.5)
- Low voltage start-up (ch.5) : 1.7 V
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V ± 1%
- Error amplifier threshold voltage : 1.0 V ± 1% (ch.1) , 1.23 V ± 1% (ch.2 to ch.5)
- Oscillation frequency range : 200 kHz to 2.0 MHz
- Standby current : 0 µA (Typ)
- Built-in soft-start circuit independent of loads
- Built-in totem-pole type output for MOS FET
- Short-circuit detection capability by external signal (–INS terminal)

■ PIN ASSIGNMENTS

TOP VIEW



(FPT-38P-M03)

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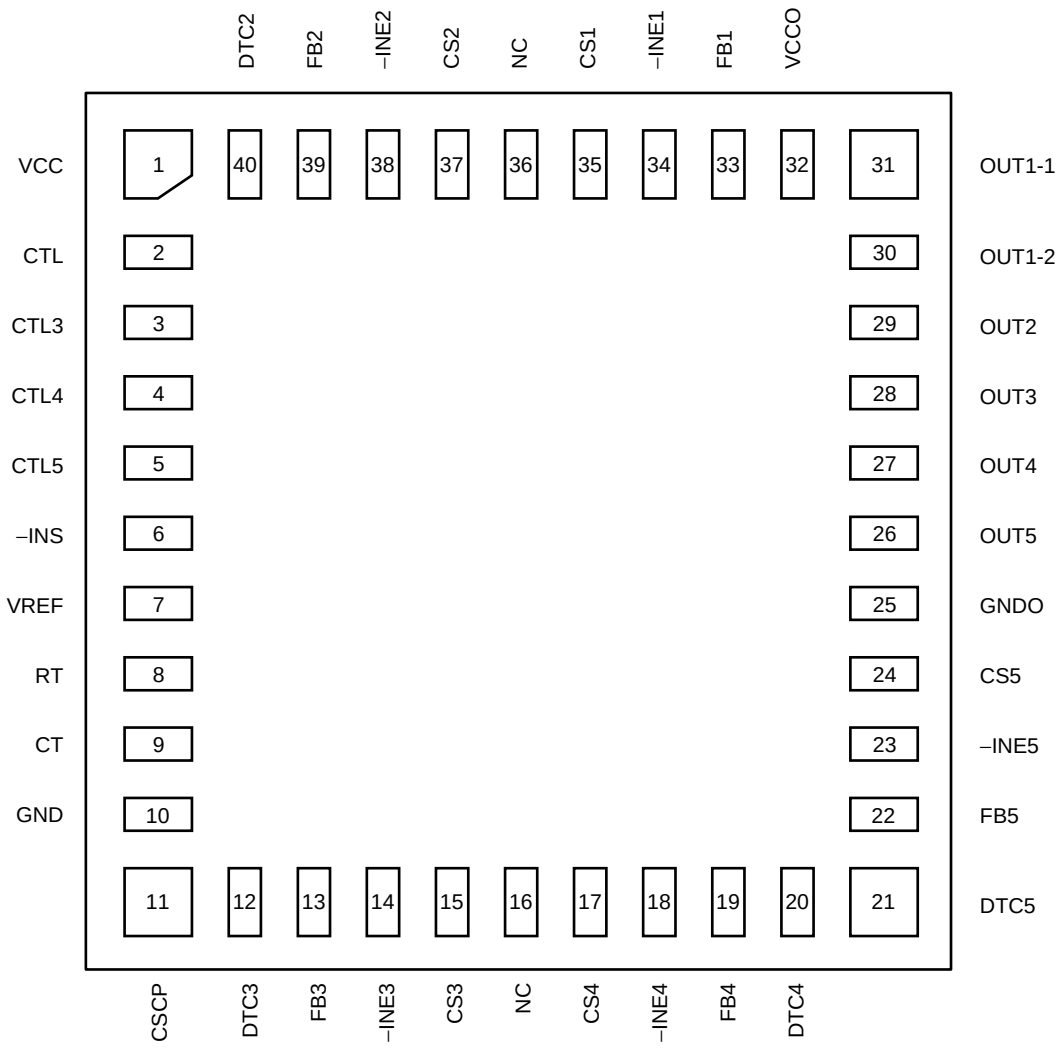
TOP VIEW (Penetration diagram from surface)



(LCC-40P-M07)

■ PIN DISCRIPTIONS

Block name	Pin No.		Pin name	I/O	Description
	TSSOP	BCC			
ch.1	36	33	FB1	O	Error amplifier output terminal.
	37	34	–INE1	I	Error amplifier inverted input terminal.
	38	35	CS1	—	Soft-start setting capacitor connection terminal.
	34	31	OUT1-1	O	P-ch drive output terminal. (External main side FET gate driving)
	33	30	OUT1-2	O	N-ch drive output terminal. (External synchronous rectification side FET gate driving) .
ch.2	4	40	DTC2	I	Dead time control terminal.
	3	39	FB2	O	Error amplifier output terminal.
	2	38	–INE2	I	Error amplifier inverted input terminal.
	1	37	CS2	—	Soft-start setting capacitor connection terminal.
	32	29	OUT2	O	P-ch drive output terminal.
ch.3	16	12	DTC3	I	Dead time control terminal.
	17	13	FB3	O	Error amplifier output terminal.
	18	14	–INE3	I	Error amplifier inverted input terminal.
	19	15	CS3	—	Soft-start setting capacitor connection terminal.
	31	28	OUT3	O	P-ch drive output terminal.
ch.4	23	20	DTC4	I	Dead time control terminal.
	22	19	FB4	O	Error amplifier output terminal.
	21	18	–INE4	I	Error amplifier inverted input terminal.
	20	17	CS4	—	Soft-start setting capacitor connection terminal.
	30	27	OUT4	O	P-ch drive output terminal.
ch.5	24	21	DTC5	I	Dead time control terminal.
	25	22	FB5	O	Error amplifier output terminal.
	26	23	–INE5	I	Error amplifier inverted input terminal.
	27	24	CS5	—	Soft-start setting capacitor connection terminal.
	29	26	OUT5	O	N-ch drive output terminal.
OSC	13	9	CT	—	Triangular wave frequency setting capacitor connection terminal.
	12	8	RT	—	Triangular wave frequency setting resistor connection terminal.

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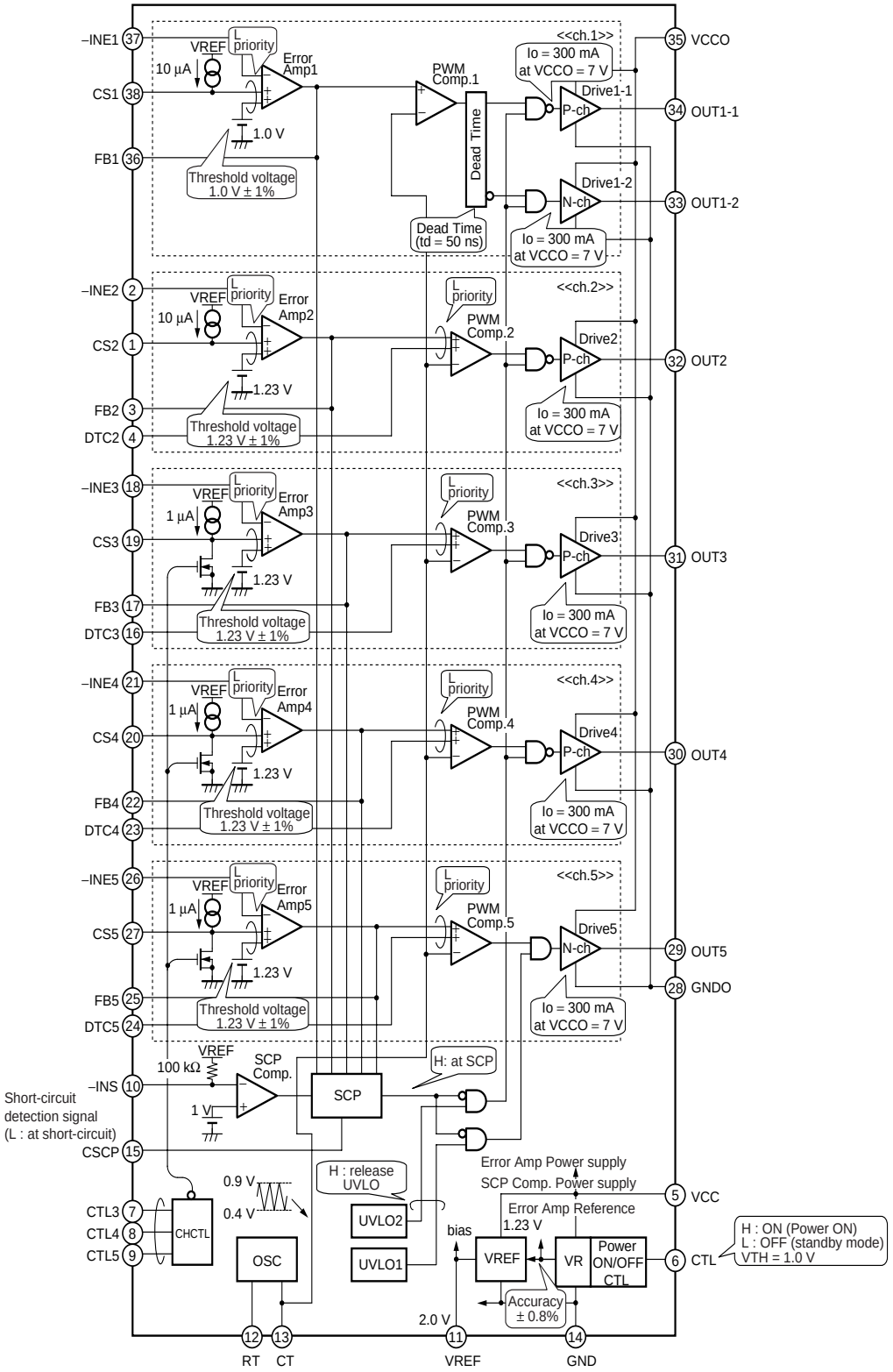
Block name	Pin No.		Pin name	I/O	Description
	TSSOP	BCC			
Control	6	2	CTL	I	Power supply control terminal.
	7	3	CTL3	I	ch.3 control terminal.
	8	4	CTL4	I	ch.4 control terminal.
	9	5	CTL5	I	ch.5 control terminal.
	15	11	CSCP	—	Short-circuit detection circuit capacitor connection terminal.
	10	6	–INS	I	Short-circuit detection comparator inverted input terminal.
Power	35	32	VCCO	—	Drive output block power supply terminal.
	5	1	VCC	—	Power supply terminal.
	11	7	VREF	O	Reference voltage output terminal.
	28	25	GNDO	—	Drive output block ground terminal.
	14	10	GND	—	Ground terminal.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, VCCO terminals	—	12	V
Output current	I_O	OUT1 to OUT5 terminals	—	20	mA
Peak output current	I_{OP}	OUT1 to OUT5 terminals Duty ≤ 5% (t = 1/f_{OSC} × Duty)	—	400	mA
Power dissipation	P_D	Ta ≤ +25 °C (TSSOP-38P)	—	1680*1	mW
		Ta ≤ +25 °C (BCC-40P)	—	1020*2	mW
Storage temperature	T_{STG}	—	–55	+125	°C

*1 : When mounted on a 76 × 76 × 1.6 mm FR-4 boards.

*2 : When mounted on a 117 × 84 × 0.8 mm FR-4 boards.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Start power supply voltage	V_{CC}	VCC, VCCO terminals (ch.5)	1.7	—	11	V
Power supply voltage	V_{CC}	VCC, VCCO terminals (ch.1 to ch.5)	2.5	7	11	V
Reference voltage output current	I_{REF}	VREF terminal	–1	—	0	mA
Input voltage	V_{INE}	–INE1 to –INE5 terminals	0	—	V_{CC} – 0.9	V
		–INS terminal	0	—	V_{REF}	V
	V_{DTC}	DTC2 to DTC5 terminals	0	—	V_{REF}	V
Control Input voltage	V_{CTL}	CTL, CTL3 to CTL5 terminals	0	—	11	V
Output current	I_O	OUT1 to OUT5 terminals	–15	—	+15	mA
Oscillation frequency	f_{OSC}	*	0.2	1.0	2.0	MHz
Timing capacitor	C_T	—	27	100	680	pF
Timing resistor	R_T	—	3.0	6.2	39	kΩ
Soft-start capacitor	C_S	CS1 to CS5 terminals	—	0.1	1.0	µF
Short-circuit detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

* : Refer to “■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY”.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 7 V, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [VREF]	Output voltage	V_{REF1}	11	VREF = 0 mA	1.98	2.00	2.02	V
		V_{REF2}	11	VCC = 2.5 V to 11 V	1.975	2.000	2.025	V
		V_{REF3}	11	VREF = 0 mA to –1 mA	1.975	2.000	2.025	V
	Input stability	Line	11	VCC = 2.5 V to 11 V	—	2*	—	mV
	Load stability	Load	11	VREF = 0 mA to –1 mA	—	2*	—	mV
	Temperature stability	$\Delta V_{REF}/V_{REF}$	11	Ta = 0 °C to +85 °C	—	0.20*	—	%
	Short-circuit output current	I_{OS}	11	VREF = 0 V	—	–300*	—	mA
Under voltage lockout protection circuit Block (ch.1 to ch.4) [UVLO2]	Threshold voltage	V_{TH}	34	VCC = ↑	1.7	1.8	1.9	V
	Hysteresis width	V_H	34	—	0.05	0.1	0.2	V
	Reset voltage	V_{RST}	34	VCC = ↓	1.55	1.7	1.85	V
Under voltage lockout protection circuit Block (ch.5) [UVLO1]	Threshold voltage	V_{TH}	30	VCC = ↑	1.35	1.5	1.65	V
	Hysteresis width	V_H	30	—	0.02	0.05	0.1	V
	Reset voltage	V_{RST}	30	VCC = ↓	1.27	1.45	1.63	V
Short-circuit detection Block [SCP]	Threshold voltage	V_{TH}	15	—	0.65	0.70	0.75	V
	Input source current	I_{CSCP}	15	—	–1.4	–1.0	–0.6	µA
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	$fosc_1$	29 to 34	CT = 100 pF, RT = 6.2 kΩ	0.95	1.0	1.05	MHz
		$fosc_2$	29 to 34	CT = 100 pF, RT = 6.2 kΩ VCC = 2.5 V to 11 V	0.945	1.00	1.055	MHz
	Frequency Input stability	$\Delta f_{OSC}/f_{OSC}$	29 to 34	CT = 100 pF, RT = 6.2 kΩ VCC = 2.5 V to 11 V	—	1.0*	—	%
	Frequency temperature stability	$\Delta f_{OSC}/f_{OSC}$	29 to 34	CT = 100 pF, RT = 6.2 kΩ Ta = 0 °C to +85 °C	—	1.0*	—	%
Soft-Start Block (ch.1, ch.2) [CS1, CS2]	Charge current	I_{CS}	1, 38	CS1, CS2 = 0 V	–13	–10	–7	µA
Soft-Start Block (ch.3 to ch.5) [CS3 to CS5]	Charge current	I_{CS}	19, 20, 27	CS3 to CS5 = 0 V	–1.3	–1.0	–0.7	µA

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(VCC = VCCO = 7 V, Ta = +25 °C)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Error Amp Block (ch.1) [Error Amp1]	Threshold voltage	V_{TH1}	37	VCC = 2.5 V to 11 V Ta = +25 °C	0.990	1.000	1.010	V
		V_{TH2}	37	VCC = 2.5 V to 11 V Ta = 0 °C to +85 °C	0.988	1.000	1.012	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	37	Ta = 0 °C to +85 °C	—	0.1*	—	%
	Input bias current	I_B	37	–INE1 = 0 V	–120	–30	—	nA
	Voltage gain	A_V	36	DC	—	100*	—	dB
	Frequency bandwidth	BW	36	A_V = 0 dB	—	1.4*	—	MHz
	Output voltage	V_{OH}	36	—	1.7	1.9	—	V
		V_{OL}	36	—	—	40	200	mV
	Output source current	I_{SOURCE}	36	FB1 = 0.65 V	—	–2	–1	mA
	Output sink current	I_{SINK}	36	FB1 = 0.65 V	150	200	—	µA
Error Amp Block (ch.2 to ch.5) [Error Amp2 to Error Amp5]	Threshold voltage	V_{TH1}	2, 18, 21, 26	VCC = 2.5 V to 11 V Ta = +25 °C	1.217	1.230	1.243	V
		V_{TH2}	2, 18, 21, 26	VCC = 2.5 V to 11 V Ta = 0 °C to +85 °C	1.215	1.230	1.245	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	2, 18, 21, 26	Ta = 0 °C to +85 °C	—	0.1*	—	%
	Input bias current	I_B	2, 18, 21, 26	–INE2 to –INE5 = 0 V	–120	–30	—	nA
	Voltage gain	A_V	3, 17, 22, 25	DC	—	100*	—	dB
	Frequency bandwidth	BW	3, 17, 22, 25	A_V = 0 dB	—	1.4*	—	MHz
	Output voltage	V_{OH}	3, 17, 22, 25	—	1.7	1.9	—	V
		V_{OL}	3, 17, 22, 25	—	—	40	200	mV
	Output source current	I_{SOURCE}	3, 17, 22, 25	FB2 to FB5 = 0.65 V	—	–2	–1	mA
	Output sink current	I_{SINK}	3, 17, 22, 25	FB2 to FB5 = 0.65 V	150	200	—	µA

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(VCC = VCCO = 7 V, Ta = +25 °C)

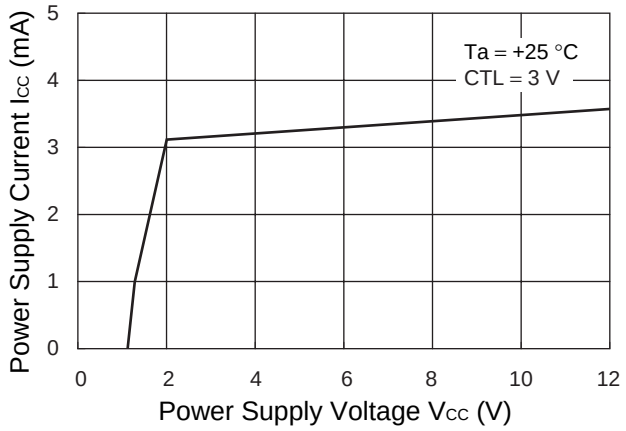
Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
PWM Comparator Block (ch.1 to ch.5) [PWM Comp.1 to PWM Comp.5]	Threshold voltage	V_{T0}	29 to 34	Duty cycle = 0%	0.35	0.4	0.45	V
		V_{T100}	29 to 34	Duty cycle = 100%	0.85	0.9	0.95	V
	Input current	I_{DTC}	4, 16, 23, 24	DTC = 0.4 V	–2.0	–0.6	—	µA
Output Block (ch.1 to ch.5) [Drive1 to Drive5]	Output source current	I_{SOURCE}	29 to 34	Duty ≤ 5% (t = 1/f_{OSC} × Duty) OUT = 0 V	—	–300*	—	mA
	Output sink current	I_{SINK}	29 to 34	Duty ≤ 5% (t = 1/f_{OSC} × Duty) OUT = 7 V	—	300*	—	mA
	Output on resistor	R_{OH}	29 to 34	OUT = – 15 mA	—	9	18	Ω
		R_{OL}	29 to 34	OUT = 15 mA	—	9	14	Ω
	Dead time	t_{D1}	33, 34	OUT2 ↓ – OUT1 ↓	—	50*	—	ns
		t_{D2}	33, 34	OUT1 ↑ – OUT2 ↑	—	50*	—	ns
Short-Circuit Detection Block [SCP Comp.]	Threshold voltage	V_{TH}	34	—	0.97	1.00	1.03	V
	Input bias current	I_B	10	–INS = 0 V	–25	–20	–17	µA
Control Block (CTL, CTL3 to CTL5) [CTL, CHCTL]	Output on condition	V_{IH}	6, 7 to 9	CTL, CTL3 to CTL5	1.5	—	11	V
	Output off condition	V_{IL}	6, 7 to 9	CTL, CTL3 to CTL5	0	—	0.5	V
	Input current	I_{CTLH}	6, 7 to 9	CTL, CTL3 to CTL5 = 3 V	5	30	60	µA
		I_{CTLL}	6, 7 to 9	CTL, CTL3 to CTL5 = 0 V	—	—	1	µA
General	Standby current	I_{CCS}	5	CTL, CTL3 to CTL5 = 0 V	—	0	2	µA
		I_{CCSO}	35	CTL = 0 V	—	0	1	µA
	Power supply current	I_{CC}	5	CTL = 3 V	—	4	6	mA

* : Standard design value

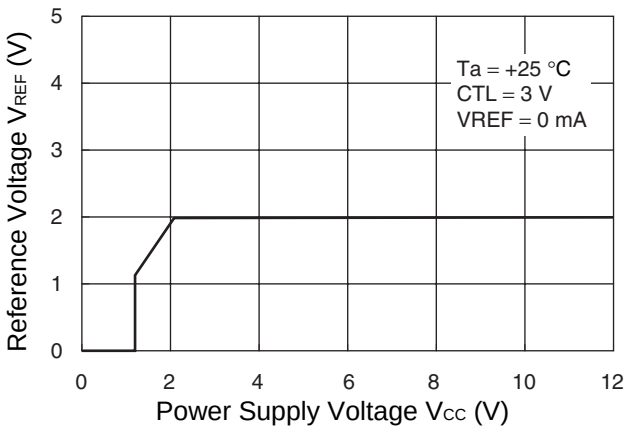
Note : The pin numbers referred are present on TSSOP-38P package.

■ TYPICAL CHARACTERISTICS

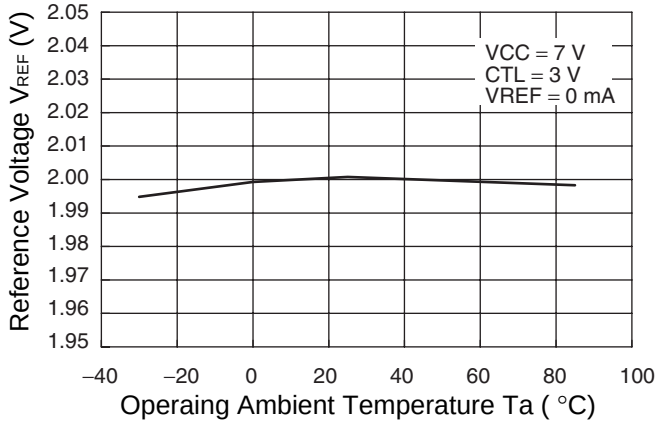
Power Supply Current vs.
Power Supply Voltage



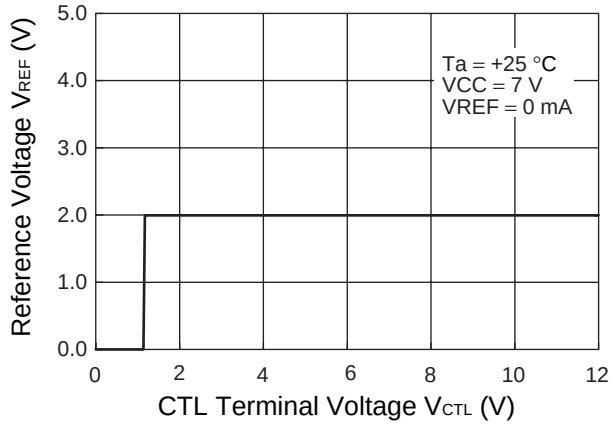
Reference Voltage vs.
Power Supply Voltage



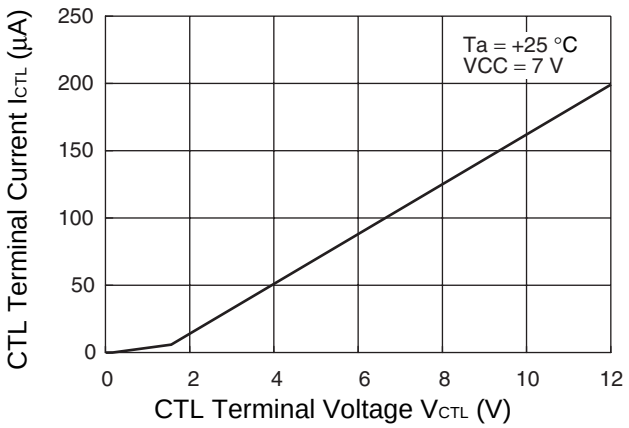
Reference Voltage vs.
Operating Ambient Temperature



Reference Voltage vs.
CTL Terminal Voltage



CTL Terminal Current vs.
CTL Terminal Voltage



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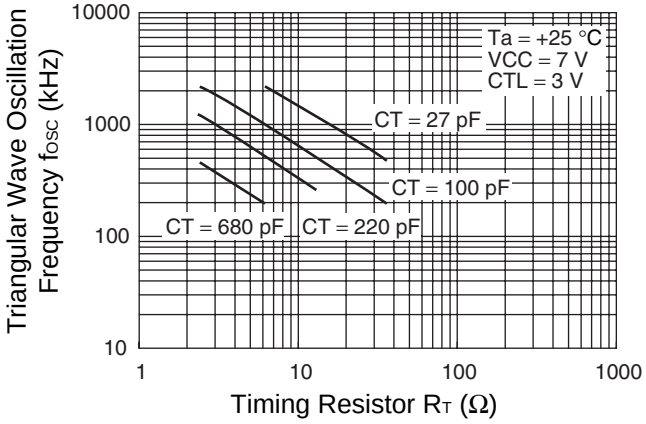
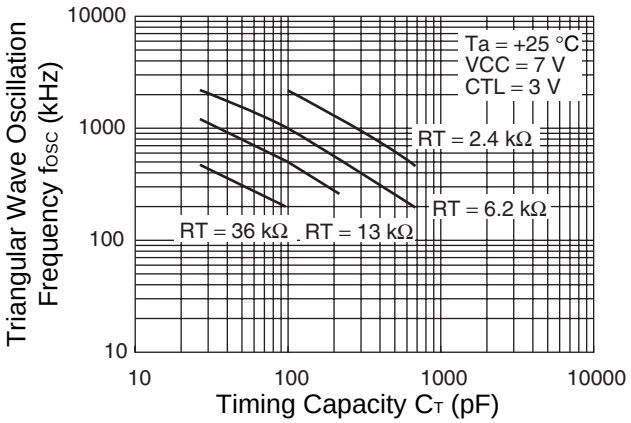
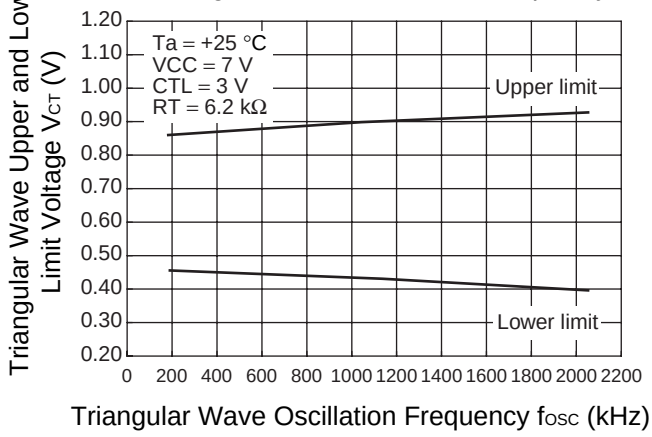
Triangular Wave Oscillation Frequency vs. Timing Resistor



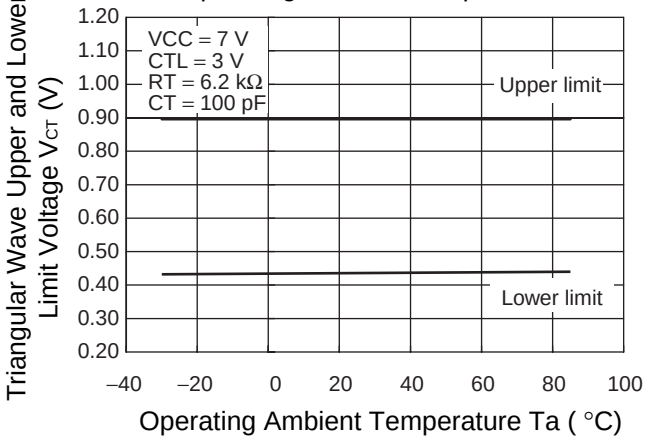
Triangular Wave Oscillation Frequency vs. Timing Capacity



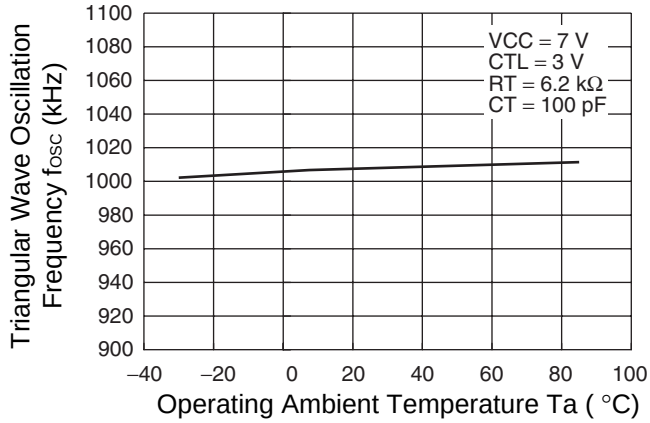
Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency



Triangular Wave Upper and Lower Limit Voltage vs. Operating Ambient Temperature



Triangular Wave Oscillation Frequency vs. Operating Ambient Temperature



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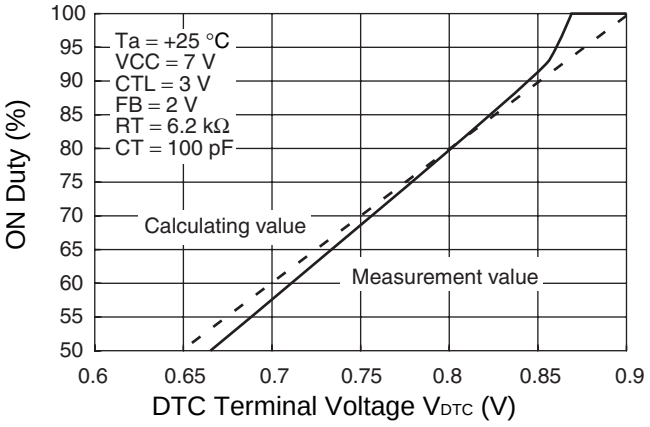
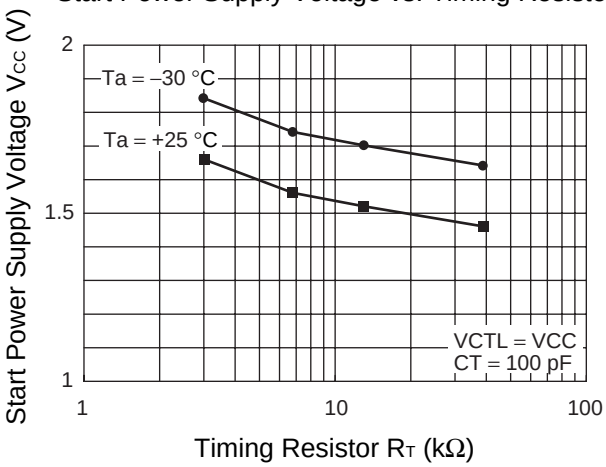
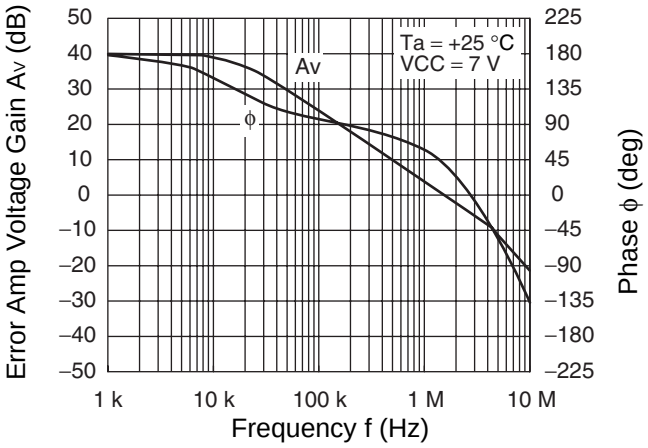
ON Duty vs. DTC Terminal Voltage

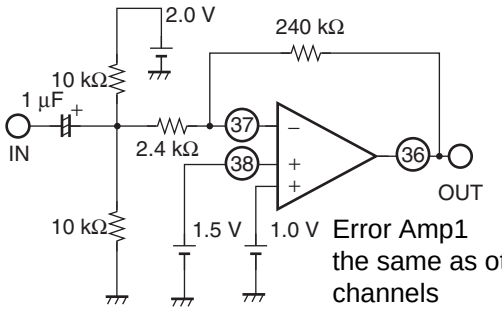


Start Power Supply Voltage vs. Timing Resistor



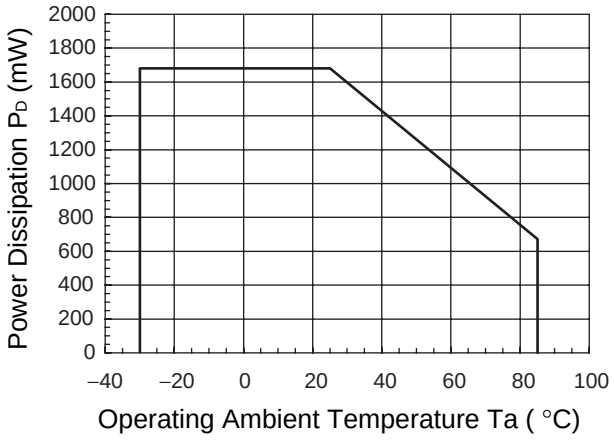
Error Amp Voltage Gain, Phase vs. Frequency



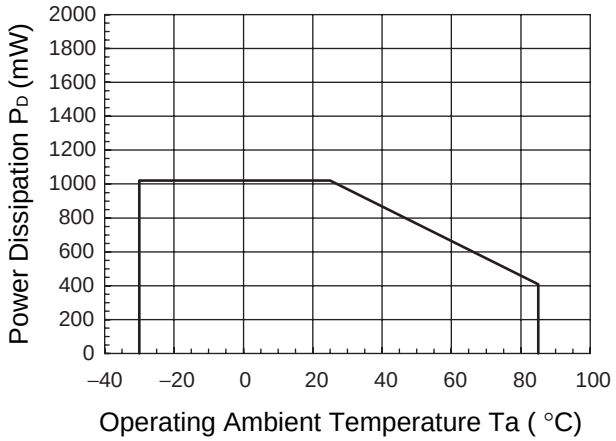


Error Amp1 the same as other channels

Power Dissipation vs. Operating Ambient Temperature (for TSSOP-38P)



Power Dissipation vs. Operating Ambient Temperature (for BCC-40P)



■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Function

(1) Reference voltage block (VREF)

The reference voltage circuit uses the voltage supplied from the VCC terminal (pin 5) to generate a temperature compensated stable voltage (2.0 V Typ) used as the reference voltage for the internal circuits of the IC. It is also possible to supply the load current of up to 1 mA to external circuits as a reference voltage through the VREF terminal (pin 11) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator block generates the triangular wave oscillation waveform width with 0.4 V to 0.9 V by the timing resistor (R_T) connected to the RT terminal (pin 12) , and the timing capacitor (C_T) connected to the CT terminal (pin 13) . The triangular wave is input to the PWM comparator circuits on the IC.

(3) Error amplifier block (Error Amp1 to Error Amp5)

The error amplifier detects output voltage of the DC/DC converter and outputs PWM control signals. An arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation for the system.

You can prevent surge currents when the IC is turned on by connecting soft-start capacitors to the CS1 terminal (pin 38) to CS5 terminal (pin 27) which are the noninverting input terminals of the error amplifier. The IC is started up at constant soft-start time intervals independent of the output load of the DC-DC converter.

(4) PWM comparator block (PWM Comp.1 to PWM Comp.5)

The PWM comparator block is a voltage-pulse width converter that controls the output duty depending on the input/output voltage.

An external output transistor is turned on, during intervals when the error amplifier output voltage and DTC voltage is higher than the triangular wave voltage.

(5) Output block (Drive1 to Drive5)

The output circuit uses a totem-pole configuration and is capable of driving an external P-ch MOS FET (main side of ch.1, ch.2, ch.3 and ch.4) and N-ch MOS FET (synchronous rectification side of ch.1 and ch.5).

2. Channel Control Function

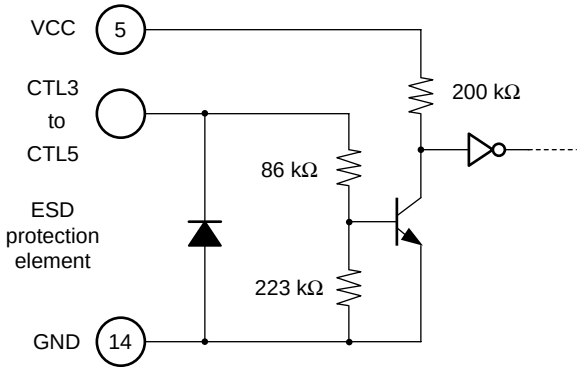
Use the CTL terminal (pin 6), CS1 terminal (pin 38), CS2 terminal (pin 1), CTL3 terminal (pin 7), CTL4 terminal (pin 8), and CTL5 terminal (pin 9) to set ON/OFF to the main and each channels.

On/off setting conditions for each channel

CTL	CS1	CS2	CTL3	CTL4	CTL5	Power	ch.1	ch.2	ch.3	ch.4	ch.5
L	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
H	GND	GND	L	L	L	ON	OFF	OFF	OFF	OFF	OFF
H	HiZ	GND	L	L	L	ON	ON	OFF	OFF	OFF	OFF
H	GND	HiZ	L	L	L	ON	OFF	ON	OFF	OFF	OFF
H	GND	GND	H	L	L	ON	OFF	OFF	ON	OFF	OFF
H	GND	GND	L	H	L	ON	OFF	OFF	OFF	ON	OFF
H	GND	GND	L	L	H	ON	OFF	OFF	OFF	OFF	ON
H	HiZ	HiZ	H	H	H	ON	ON	ON	ON	ON	ON

Note : Note that current which is over stand-by current flows into VCC terminal when the CTL terminal is in “L” level and one of the terminals between CTL3 to CTL5 terminals is set to “H” level.
(Refer to CTL3 to CTL5 terminals equivalent circuit)

- CTL3 to CTL5 terminals equivalent circuit



3. Protection Function

(1) Timer-latch short circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator (SCP) detects the output voltage level of each channel. If the output voltage of any channel is lower than the short-circuit detection voltage, the timer circuit is actuated to start charging to the capacitor (Cscp) externally connected to the CSCP terminal (pin 15).

When the capacitor (Cscp) voltage becomes about 0.7 V, the output transistor is turned off and the dead time is set to 100%.

The short-circuit detection from external input is capable by using –INS terminal (pin 10).

When the protection circuit is actuated, the power supply is recycled or the CTL terminal (pin 6) is set to "L" level, resetting the latch as the voltage at the VREF terminal (pin 11) becomes 1.27 V (Min) or less (Refer to "■SETTING THE TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT") .

(2) Under-voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in the power supply voltage, which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in the breakdown or degradation of the system. To prevent such malfunctions, under-voltage lockout protection circuit detects a decrease in internal reference voltage level with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 15) at the "L" level.

The system returns to the normal state when the power supply voltage reaches the threshold voltage of the under-voltage lockout protection circuit.

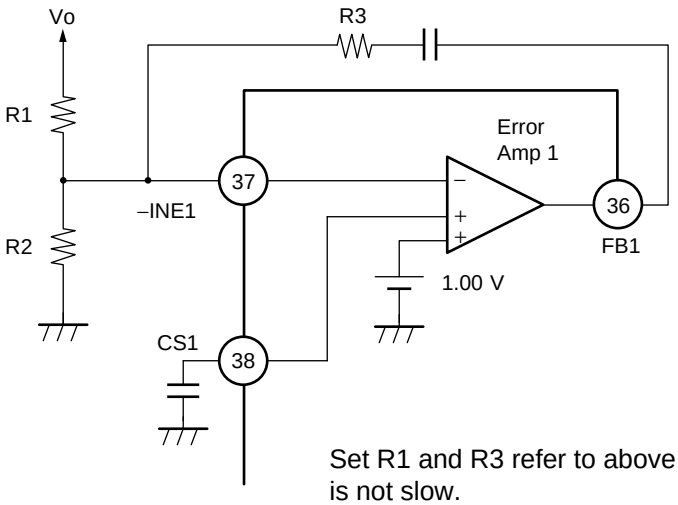
■ PROTECTION CIRCUIT OPERATING FUNCTION TABLE

The following table shows the state that the protection circuit is operating.

Operation circuit	OUT1-1	OUT1-2	OUT2	OUT3	OUT4	OUT5
Short-circuit protection circuit	H	L	H	H	H	L
Under voltage lockout protection circuit	H	L	H	H	H	L

■ SETTING THE OUTPUT VOLTAGE

• ch.1

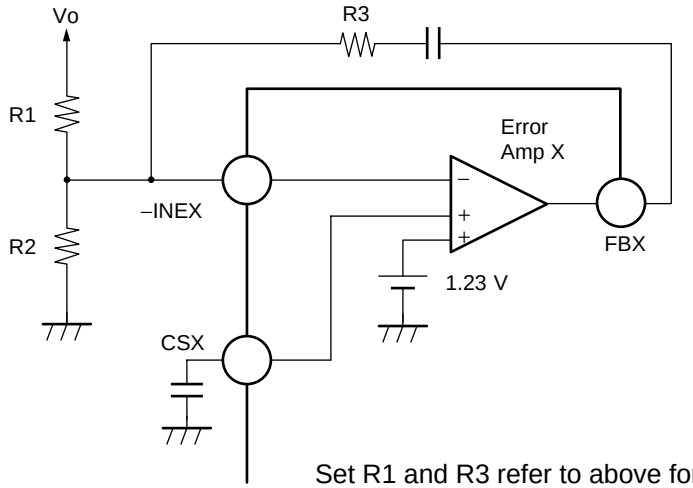


$$V_O = \frac{1.00\ V}{R2}\ (R1 + R2)$$

$$(R1 + R3) \geq \frac{V_O}{100\ \mu A}$$

Set R1 and R3 refer to above formula, then error amp's response is not slow.

• ch.2 to ch.5



$$V_O = \frac{1.23\ V}{R2}\ (R1 + R2)$$

$$(R1 + R3) \geq \frac{V_O}{100\ \mu A}$$

X : Each channel number

Set R1 and R3 refer to above formula, then error amp's response is not slow.

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by connecting a timing resistor (R_T) to the RT terminal (pin 12) and a timing capacitor (C_T) to the CT terminal (pin 13).

Triangular wave oscillation frequency : f_{OSC}

$$f_{OSC}\ (kHz) \fallingdotseq \frac{620000}{C_T\ (pF)\ \times R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START TIME

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} to C_{S5}) to the CS1 terminal (pin 38) to CS5 terminal (pin 27) respectively.

As illustrated below, when each $\overline{CTLX}$ is set to “L” from “H”, ch.1 and ch.2 charge the soft-start capacitors (C_{S1} and C_{S2}) externally connected to the CS1 and CS2 terminals at about 10 μA.

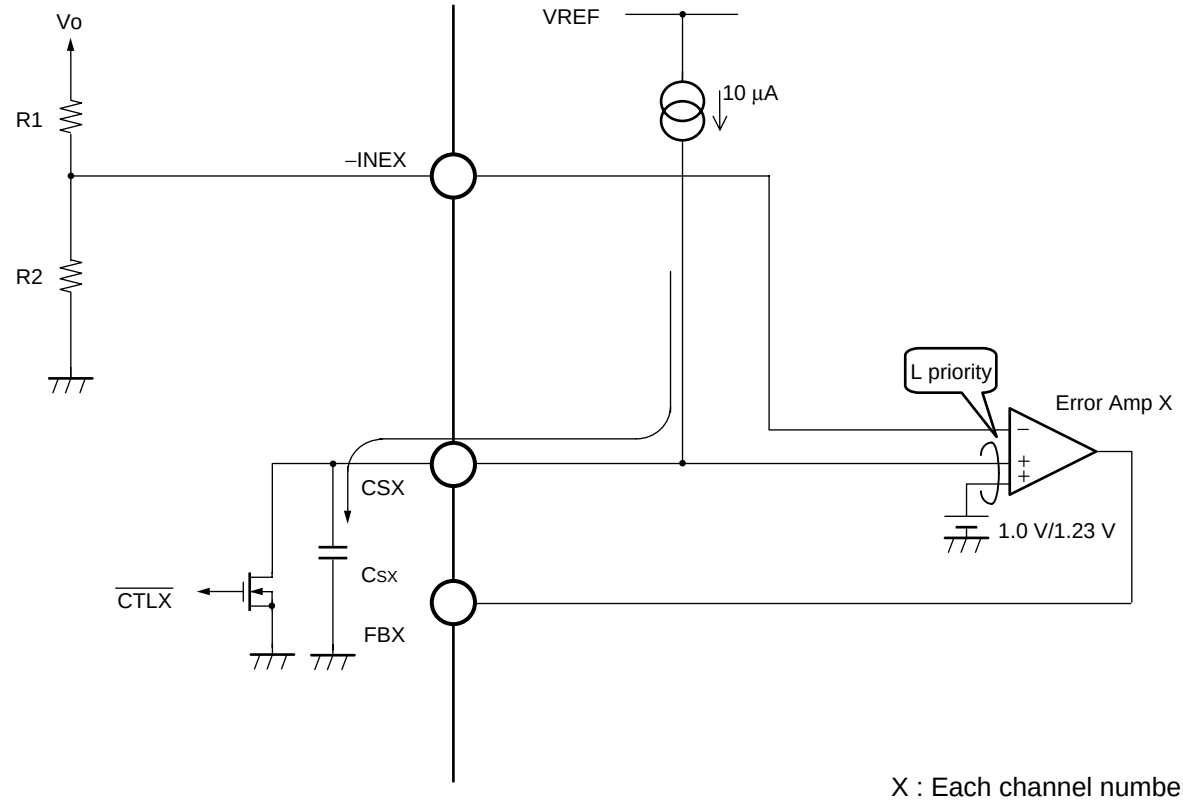
When each $\overline{CTLX}$ is set to “H” from “L”, ch.3 to ch.5 charge the soft-start capacitors (C_{S3} to C_{S5}) externally connected to the CS3 to CS5 terminals at about 1 μA.

The error amplifier output (FB1 to FB5 terminals) is determined by comparison between the lower voltage of the two non-inverted input terminal voltage (1.23 V (ch.1 : 1.0 V) , CS terminal voltage) and the inverted input terminal voltage (–INE1 to –INE5 terminal) . The FB terminal voltage is decided for the soft-start period (CS terminal voltage < 1.23 V (ch.1 : 1.0 V)) by the comparison between –INE terminal voltage and CS terminal voltage. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor externally connected to the CS terminal is charged. The soft-start time is obtained from the following formula :

Soft-start time : ts (time until output 100%)

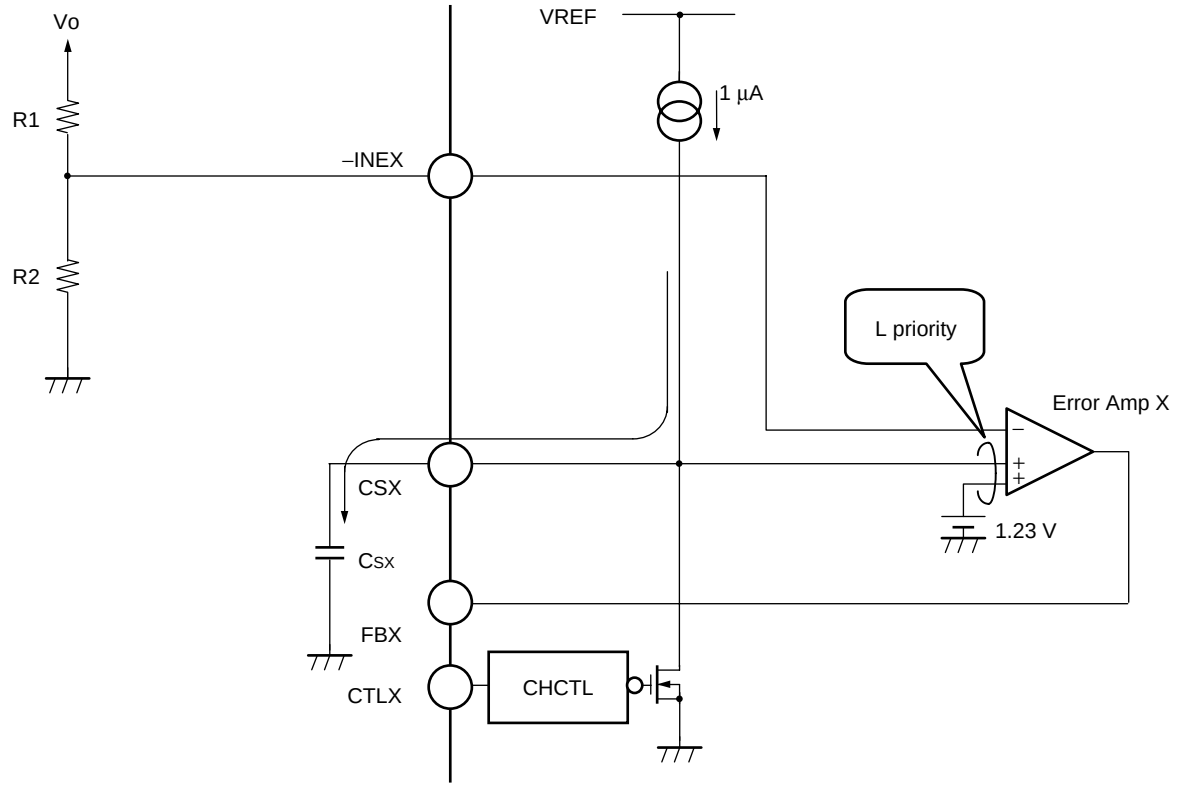
ch.1	:	ts (s) ≒ 0.100 × C_{SX} (μF)
ch.2	:	ts (s) ≒ 0.123 × C_{SX} (μF)
ch.3 to ch.5	:	ts (s) ≒ 1.23 × C_{SX} (μF)

• Soft-start circuit (ch.1, ch.2)



X : Each channel number

• Soft-start circuit (ch.3 to ch.5)

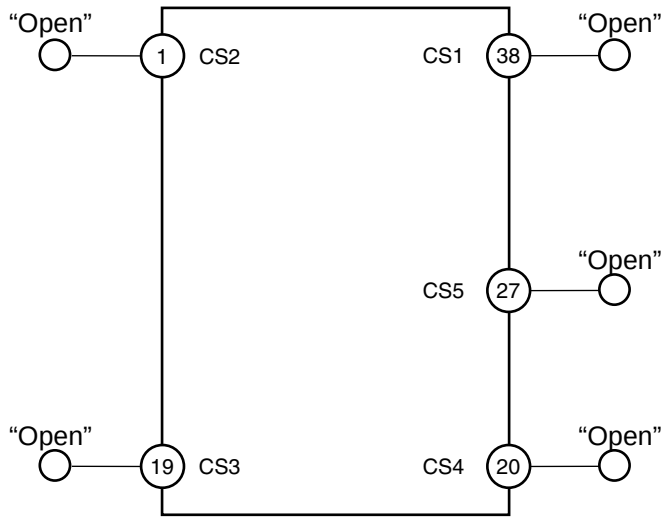


X : Each channel number

■ PROCESSING WHEN NOT USING CS TERMINAL

When soft-start function is not used, leave the CS1 terminal (pin 38), the CS2 terminal (pin 1), the CS3 terminal (pin 19), the CS4 terminal (pin 20) and the CS5 terminal (pin 27) open.

- When not setting soft-start time



■ SETTING THE TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage.

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 15) is held at "L" level.

If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level.

This causes the external short-circuit protection capacitor C_{SCP} connected to the CSCP terminal (pin 15) to be charged at 1 μA.

Short-circuit detection time : t_{CSCP}

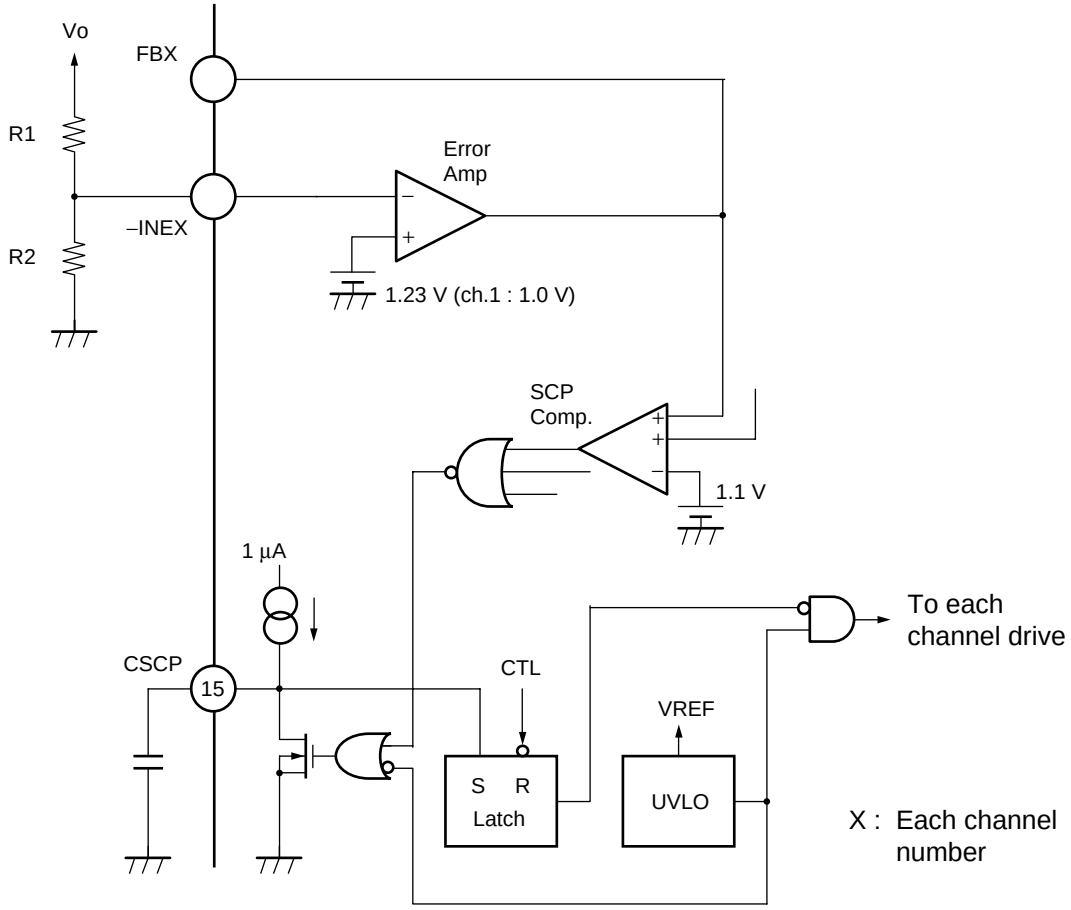
$$t_{CSCP}\ (s) \fallingdotseq 0.70 \times C_{SCP}\ (\mu F)$$

When the capacitor C_{SCP} is charged to the threshold voltage ($V_{TH} \fallingdotseq 0.70$ V) , the latch is set to and the external FET is turned off (dead time is set to 100%) . At this time, the latch input is closed and CSCP terminal (pin 15) is held at "L" level.

The short-circuit detection from external input is capable by using –INS terminal (pin 10) . In this case, the short-circuit detection operates when the –INS terminal voltage becomes the level of the threthold voltage ($V_{TH} \fallingdotseq$ IV) or less.

Note that the latch is reset as the voltage at the VREF terminal (pin 11) is decreased to 1.27 V (Min) or less by either recycling the power supply or setting the CTL terminal (pin 6) to “L” level.

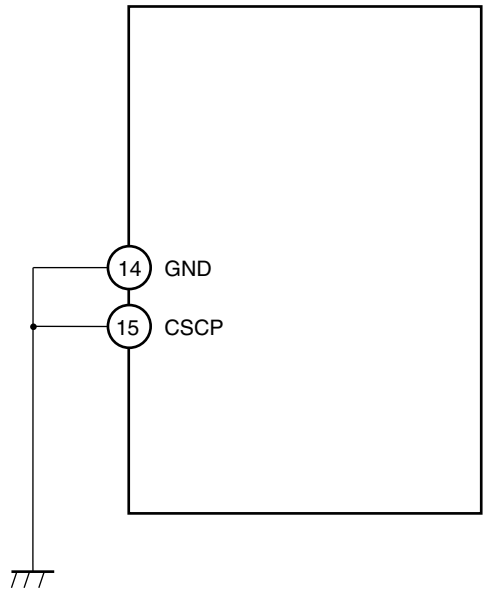
- Timer-latch short-circuit protection circuit



■ PROCESSING WHEN NOT USING CSCP TERMINAL

To disable the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 15) to GND in the shortest distance.

- Processing when not using the CSCP terminal



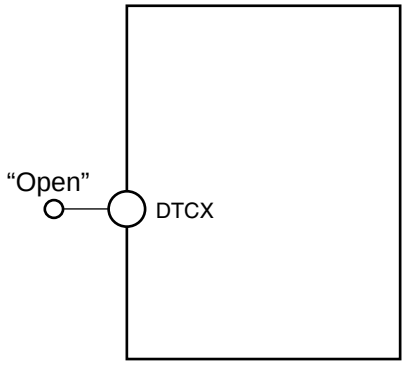
■ SETTING THE DEAD TIME

When the device is set for step-up or inverted output based on the step-up, step-up/down Zeta method, step up/down Sepic method, or flyback method, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100%). To prevent this, set the maximum duty of the output transistor.

When the DTC terminal is opened the maximum duty is 90% (Typ) because of this IC built-in resistor which sets the DTC terminal voltage.

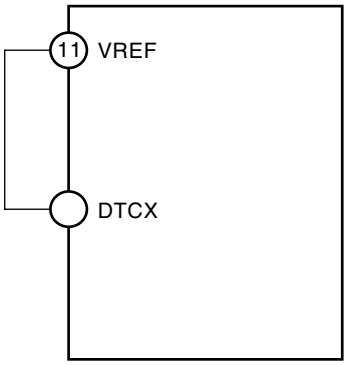
To disable the DTC terminal, connect it to the VREF terminal (pin 11) as illustrated below (when dead time is not set).

• When dead time is set:
(Setting with built-in resistor≒ 90%)



X : Each channel number

• When dead time is not set:



X : Each channel number

To change the maximum duty using external resistors, set the DTC terminal voltage by dividing resistance using the VREF voltage. Refer to "When dead time is set : (Setting by external resistors)."

It is possible to set without regard for the built-in resistance value (including tolerance) when setting the external resistance value to 1/10 of the built-in resistance or less.

Note that the VREF load current must be set such that the total current for all the channels does not exceed 1 mA.

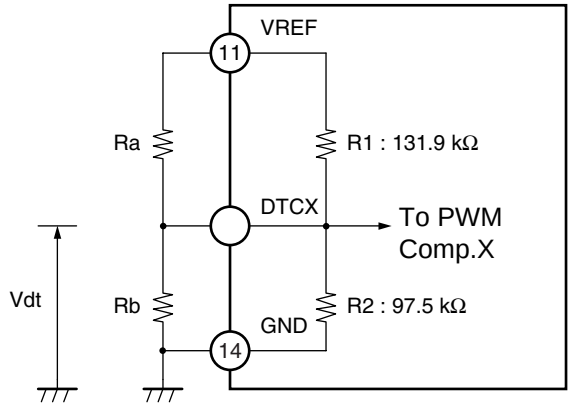
When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The formula for calculating the maximum duty is as follows, assuming that the triangular wave amplitude and triangular wave lower limit voltage are about 0.5 V and 0.4 V, respectively.

$$\text{DUTY (ON) Max} \fallingdotseq \frac{\text{Vdt} - 0.4\ \text{V}}{0.5\ \text{V}} \times 100\ (\%)$$

$$\text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF (condition : Ra} < \frac{\text{R1}}{10}\text{, Rb} < \frac{\text{R2}}{10}\text{)}$$

Note : DUTY obtained by the above-mentioned formula is a calculated value. For setting, refer to “ON Duty vs. DTC Terminal Voltage” in “■ TYPICAL CHARACTERISTICS”.

• When dead time is set :
(Setting by external resistors)



X : Each channel number

Setting example (for an aim maximum ON duty of 80% (Vdt = 0.8 V) with Ra = 13.7 kΩ and Rb = 9.1 kΩ)

• Calculation using external resistors Ra and Rb only

$$Vdt = \frac{Rb}{Ra + Rb} \times VREF \fallingdotseq 0.80\ V$$

$$DUTY\ (ON)\ Max \fallingdotseq \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \fallingdotseq 80\% \cdots\cdots (1)$$

• Calculation taking account of the built-in resistor (tolerance ± 20%) also

$$Vdt = \frac{(Rb, R2\ Combined\ resistance)}{(Ra, R1\ Combined\ resistance) + (Rb, R2\ Combined\ resistance)} \times VREF \fallingdotseq 0.80\ V \pm 0.13\%$$

$$DUTY\ (ON)\ Max \fallingdotseq \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \fallingdotseq 80\% \pm 0.2\% \bullet\bullet\bullet\bullet (2)$$

Based on (1) and (2) above, selecting external resistances of 1/10th or less of the built-in resistance enables the built-in resistance to be ignored.

As for the duty dispersion, please expect ± 5% at (fosc = 1 MHz) due to the dispersion of a triangular wave amplitude.

■ OPERATION EXPLANATION WHEN CTL TURNING ON AND OFF

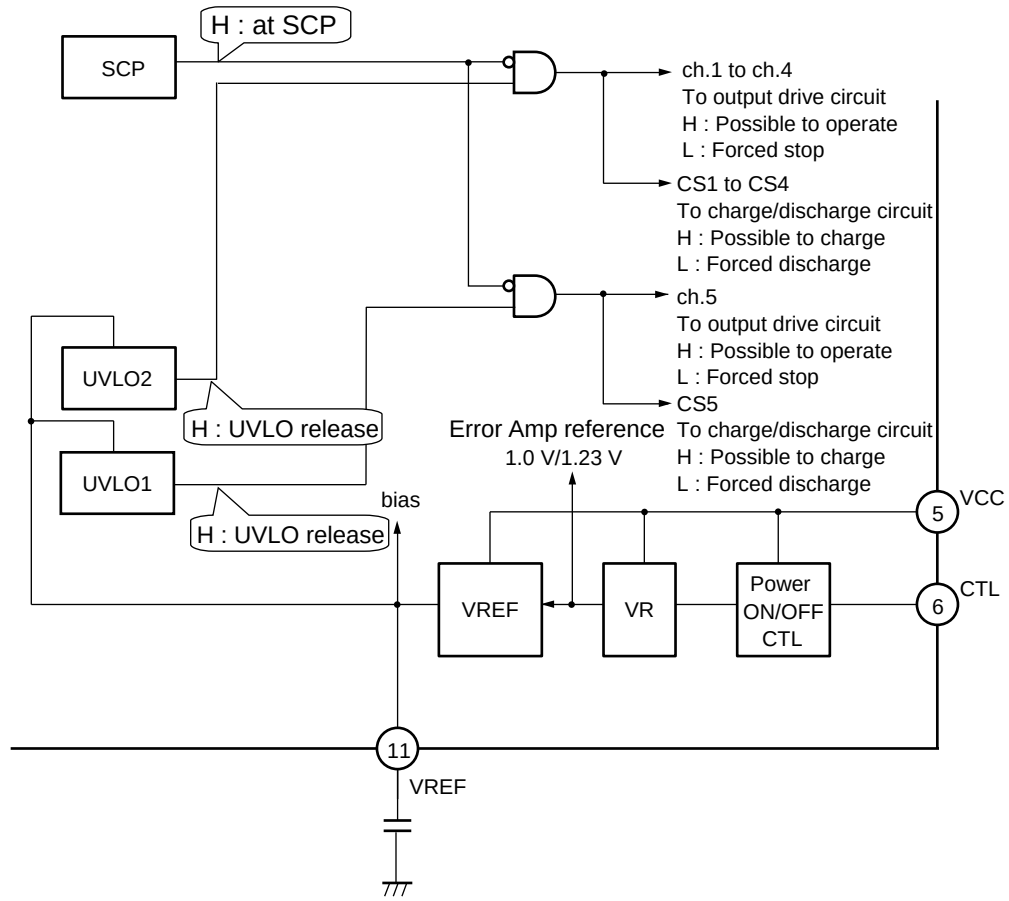
When CTL is turned on, internal reference voltage VR and VREF generate. When VREF exceeds each threshold voltage (VTH1, 2) of UVLO1 and UVLO2 (under voltage lockout protection circuit) , UVLO1 and UVLO2 are released, and the operation of output drive circuit of each channel becomes possible.

When CTL is off, VR and VREF fall. When VREF decreases and UVLO1 and UVLO2 fall below each reset voltage (VRST1, 2) , UVLO operates and output drive circuit of each channel is forcibly done the operation stop, and makes the output an off state.

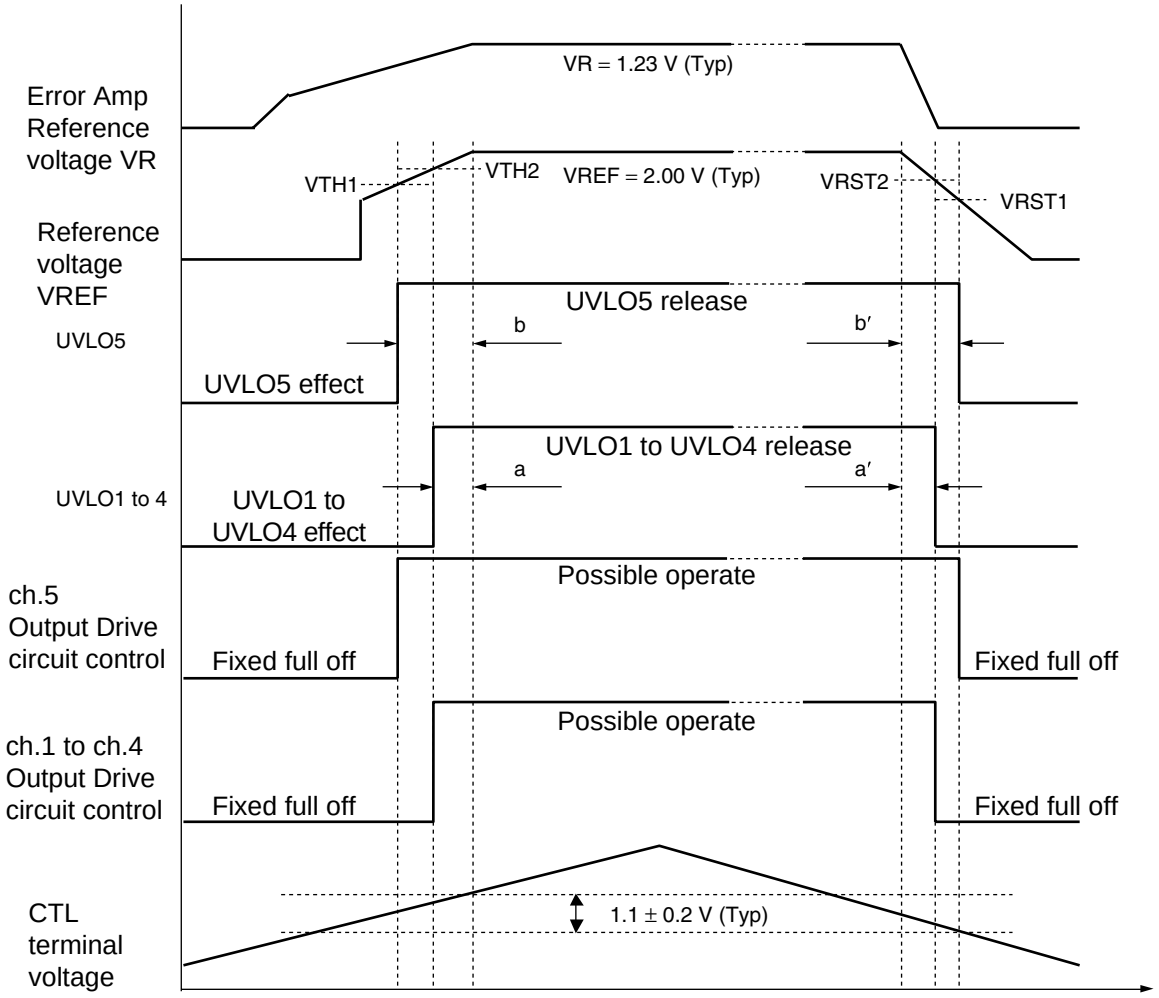
In the period until reaching to 2.0 V by VREF voltage after UVLO1 and UVLO2 are released by turning on CTL (refer to a and b in "• Timing chart") and the period until decreasing of VREF from 2.0 V after off CTL and operating of UVLO1 and UVLO2 (refer to a' and b' in "• Timing chart") , the bias voltage and the bias current in IC do not reach a prescribed value because VREF which is the reference voltage does not reach 2.0 V, and the speed of response of IC has decreased.

Moreover, when in this period IC does the input sudden charge or the load sudden charge or turning on and off of CTL3 to CTL5, IC cannot conform and the output might overshoot. Therefore, impress the voltage to CTL terminal by which the VREF voltage never stays in the above-mentioned period.

• CTL block equivalent circuit

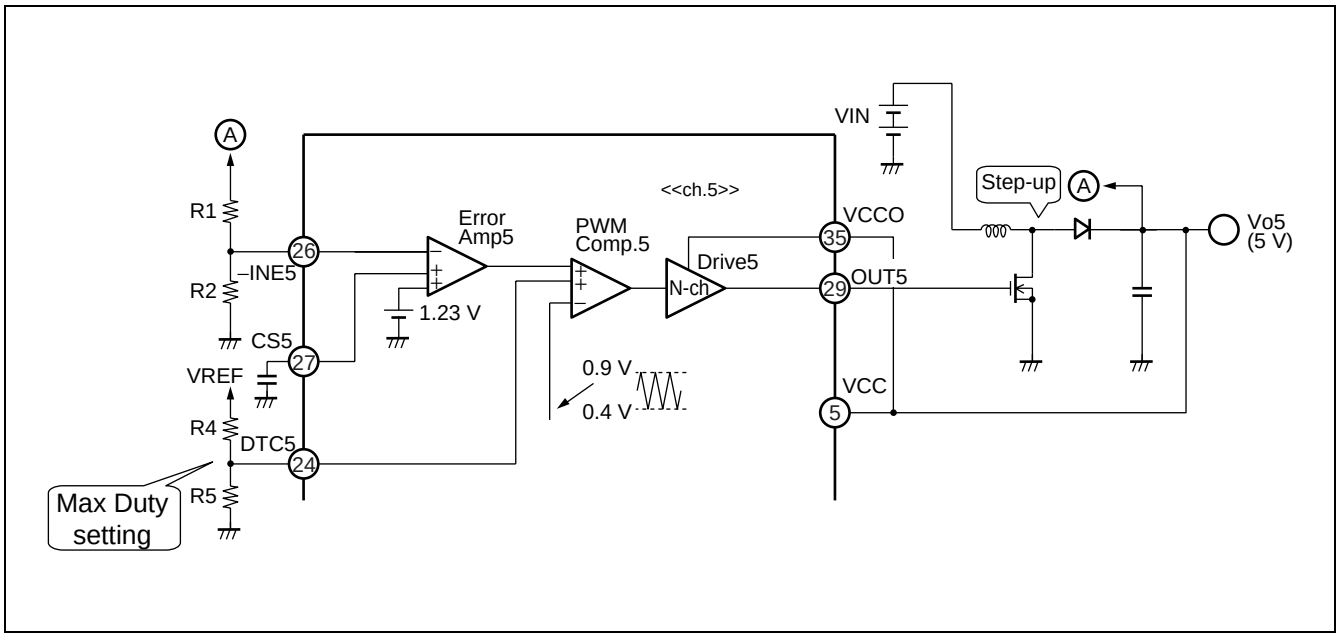


• Timing chart



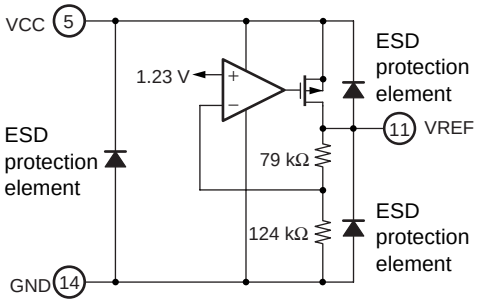
■ ABOUT THE LOW VOLTAGE OPERATION

1.7 V or more is necessary for the VCC terminal (pin 5) and the VCCO terminal (pin 35) for the self-power supply type to use the step-up circuit as the start voltage.
Even if thereafter VIN voltage decreases to 1.5 V, operation is possible if the VCC terminal voltage and the VCCO terminal voltage rise to 2.5 V or more after start-up. However, it is necessary not to exceed the maximum duty set value by the duty due to the VIN decrease. Including other channels, execute an enough operation margin confirmation when using it.

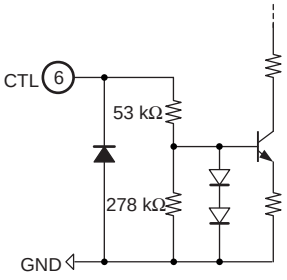


■ I/O EQUIVALENT CIRCUIT

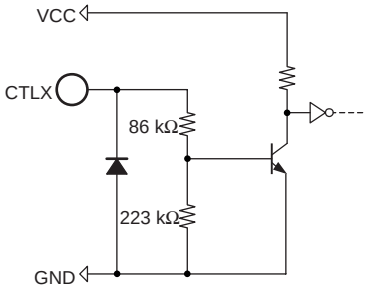
• Reference voltage block



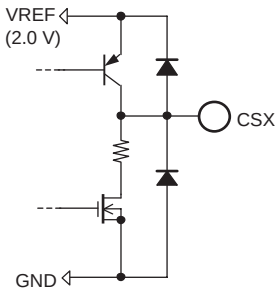
• Control block



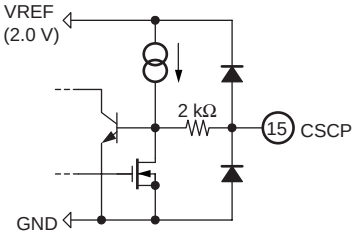
• Channel control block (ch.3 to ch.5)



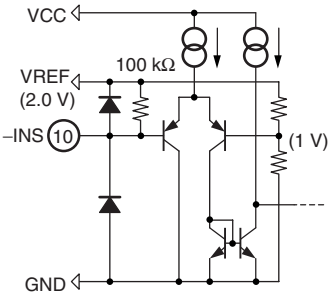
• Soft-start block



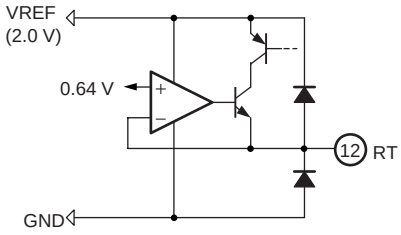
• Short-circuit detection block



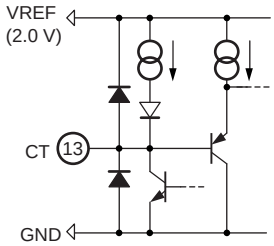
• Short-circuit detection comparator block



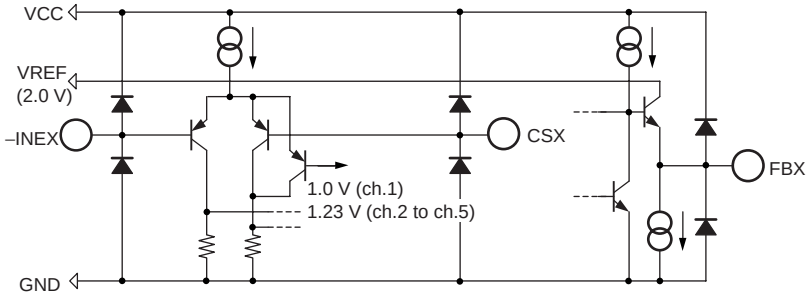
• Triangular wave oscillator block (RT)



• Triangular wave oscillator block (CT)



• Error amplifier block (ch.1 to ch.5)



X : Each cannel No.

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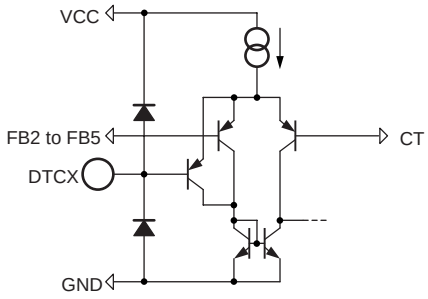
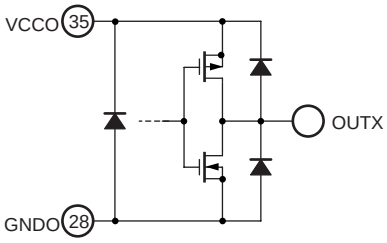
(Continued)

• PWM comparator block

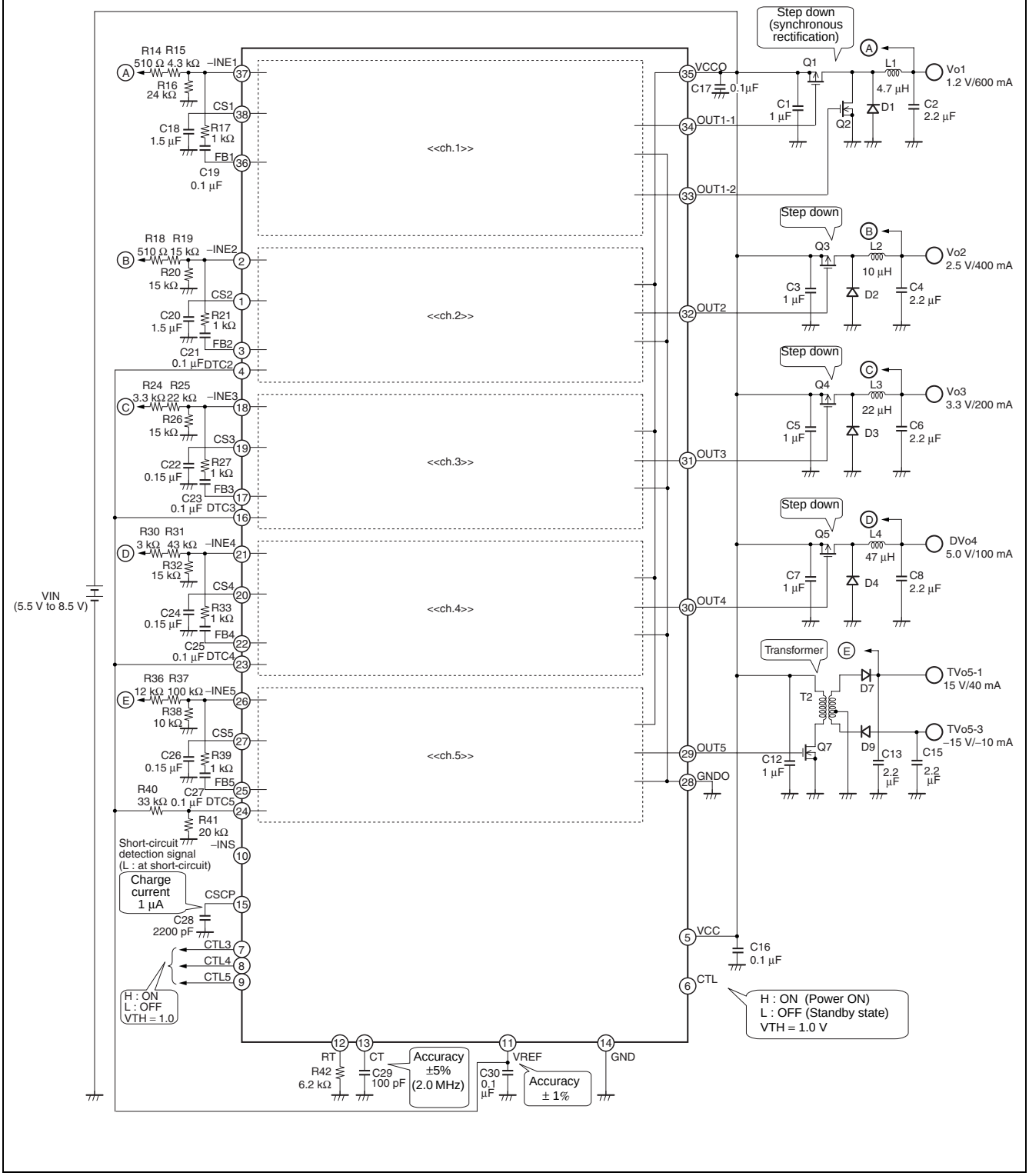


• Output block (ch.1 to ch.5))



X : Each cannel No.

■ APPLICATION EXAMPLE



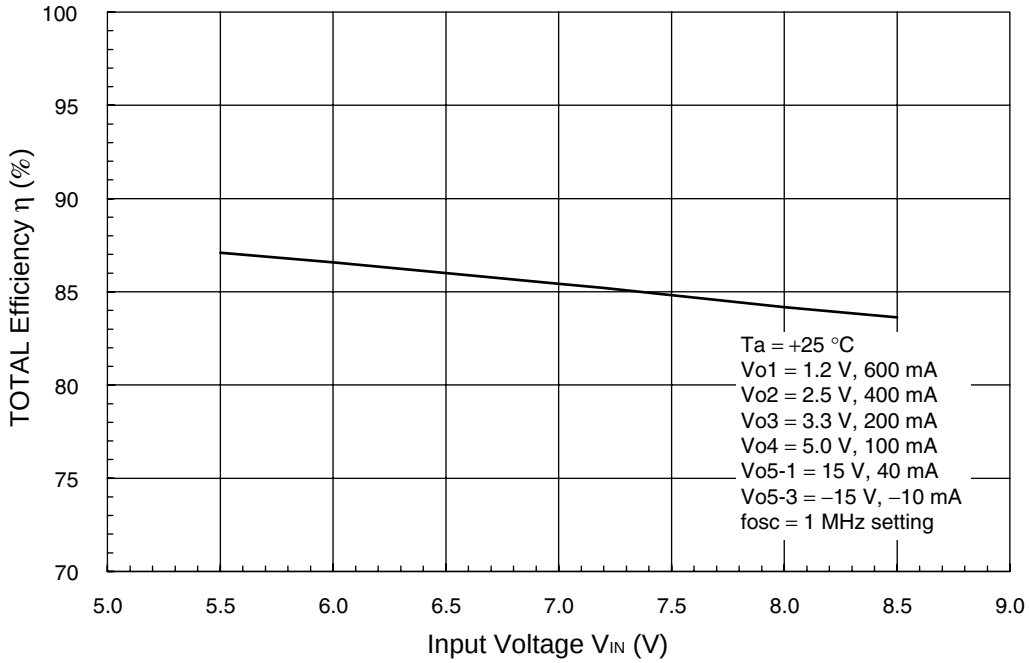
■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q3 to Q5	P-ch FET	VDS = –20 V, ID = –1.0 A		SANYO	MCH3307
Q2, Q7	N-ch FET	VDS = 30 V, ID = 1.4 A		SANYO	MCH3408
D1 to D4	Diode	VF = 0.4 V (Max) , at IF = 1 A		SANYO	SBS004
D7, D9	Diode	VF = 0.55 V (Max) , at IF = 0.5 A		SANYO	SB05-05CP
L1	Inductor	4.7 µH	1.4 A, 37 mΩ	TDK	RLF5018T-4R7M1R4
L2	Inductor	10 µH	0.94 A, 56 mΩ	TDK	RLF5018T-100MR94
L3	Inductor	22 µH	0.63 A, 130 mΩ	TDK	RLF5018T-220MR63
L4	Inductor	47 µH	0.59A, 210 mΩ	TDK	SLF6028T-470MR59
T2	Transformer	—	—	SUMIDA	CLQ52 5388-T139
C1, C3, C5, C7	Ceramics Condenser	1 µF	25V	TDK	C3216JB1E105K
C2, C4, C6, C8	Ceramics Condenser	2.2 µF	25V	TDK	C3216JB1E225K
C12	Ceramics Condenser	1 µF	25V	TDK	C3216JB1E105K
C13, C15	Ceramics Condenser	2.2 µF	25V	TDK	C3216JB1E225K
C16, C17, C19	Ceramics Condenser	0.1 µF	50V	TDK	C1608JB1H104K
C18, C20	Ceramics Condenser	1.5 µF	10V	TDK	C2012JB1A155K
C21, C23, C25	Ceramics Condenser	0.1 µF	50V	TDK	C1608JB1H104K
C22, C24, C26	Ceramics Condenser	0.15 µF	16V	TDK	C1608JB1C154K
C27, C30	Ceramics Condenser	0.1 µF	50V	TDK	C1608JB1H104K
C28	Ceramics Condenser	2200 pF	50V	TDK	C1608JB1H222K
C29	Ceramics Condenser	100 pF	50V	TDK	C1608CH1H101J
R14, R18	Resistor	510 Ω	0.5%	ssm	RR0816P-511-D
R15	Resistor	4.3 kΩ	0.5%	ssm	RR0816P-432-D
R16	Resistor	24 kΩ	0.5%	ssm	RR0816P-243-D
R17, R21, R27	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R19, R20, R26	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R24	Resistor	3.3 kΩ	0.5%	ssm	RR0816P-332-D
R25	Resistor	22 kΩ	0.5%	ssm	RR0816P-223-D
R30	Resistor	3 kΩ	0.5%	ssm	RR0816P-302-D
R31	Resistor	43 kΩ	0.5%	ssm	RR0816P-433-D
R32	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R33, R39	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R36	Resistor	12 kΩ	0.5%	ssm	RR0816P-123-D
R37	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R38	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R40	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R41	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R42	Resistor	6.2 kΩ	0.5%	ssm	RR0816P-622-D

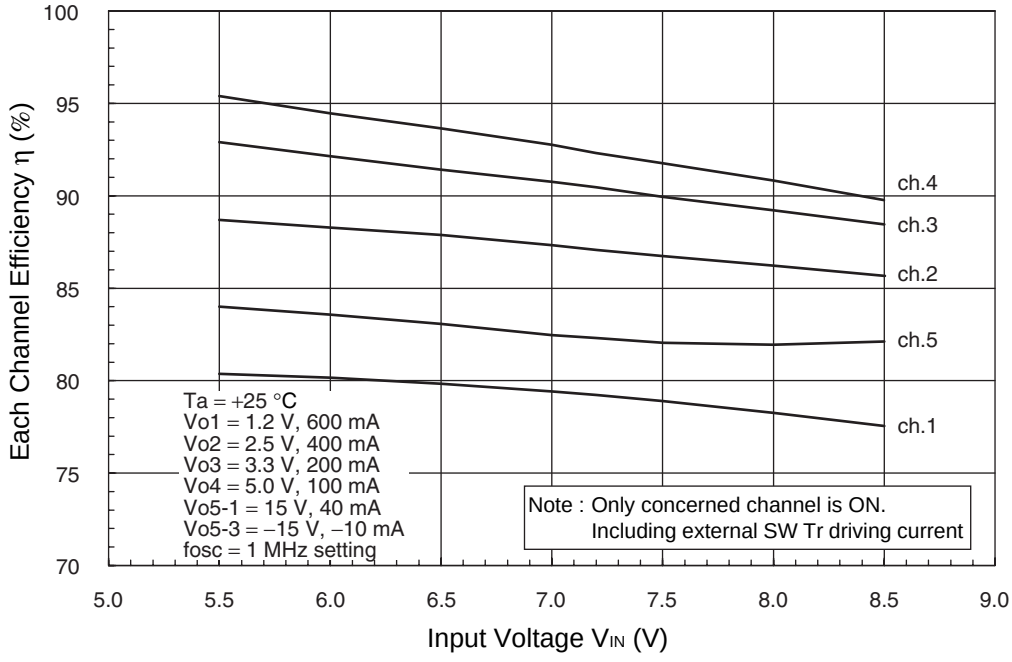
Notes : SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SUMIDA : Sumida Corporation
ssm : SUSUMU CO., LTD.

■ REFERENCE DATA

TOTAL Efficiency vs. Input Voltage

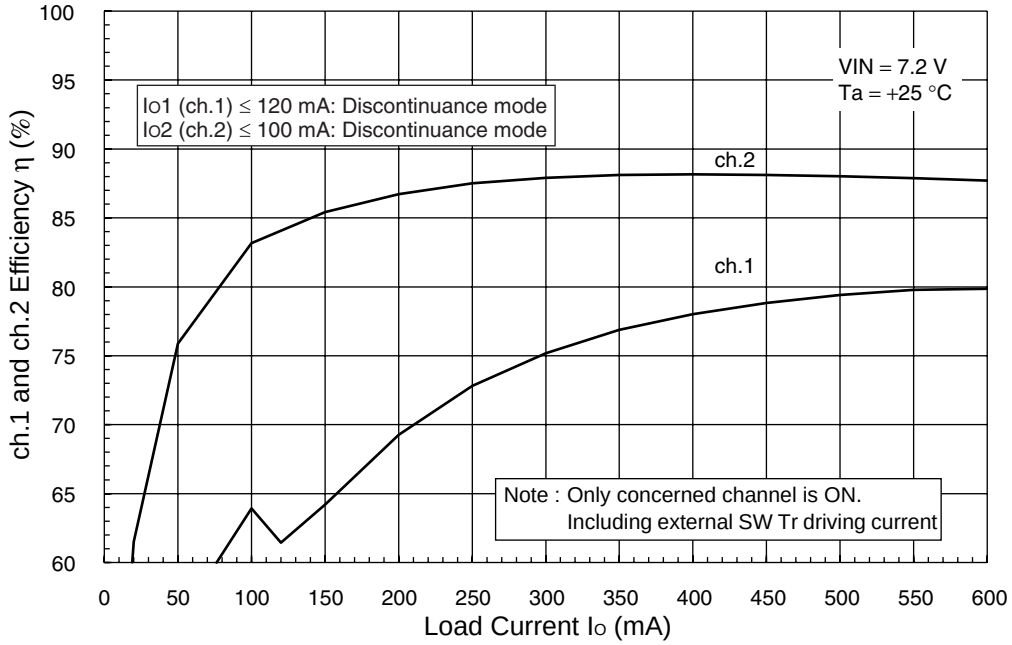


Each Channel Efficiency vs. Input Voltage

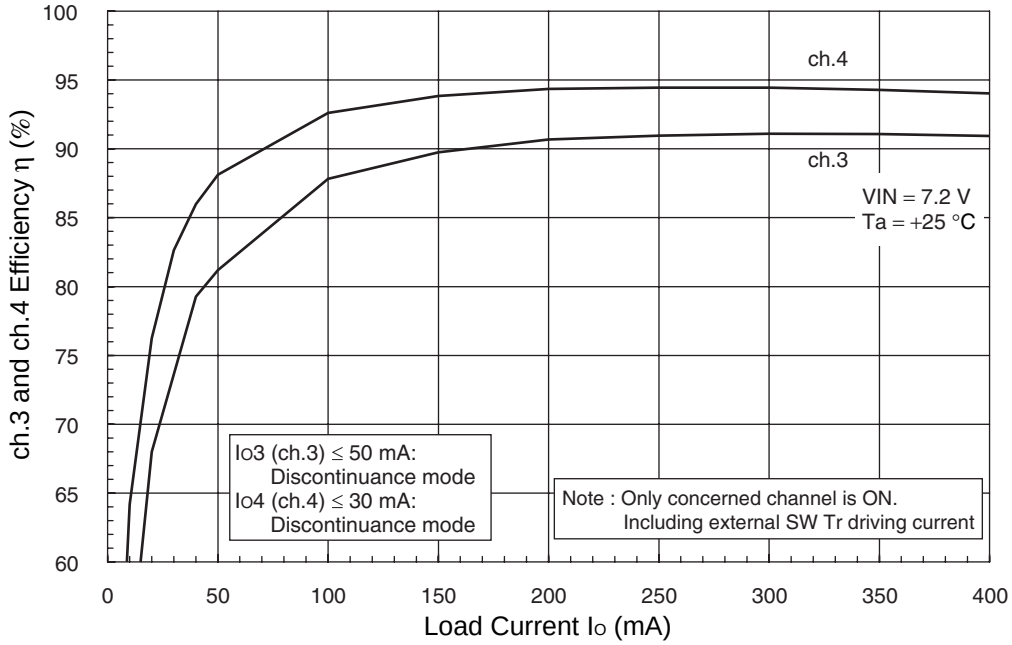


(Continued)

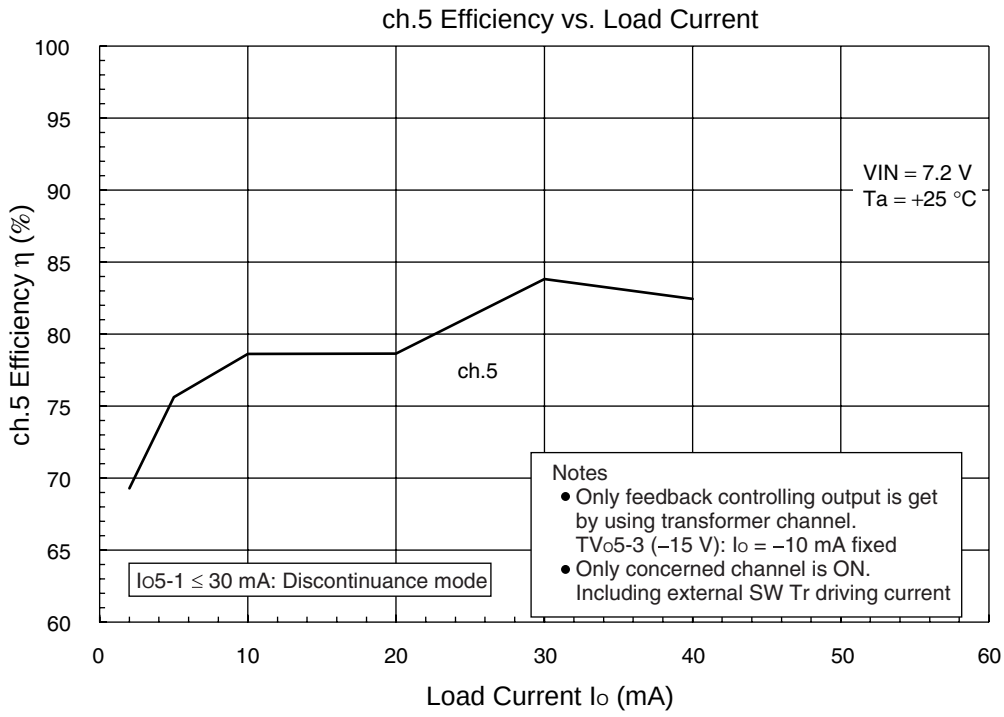
ch.1 and ch.2 Efficiency vs. Load Current



ch.3 and ch.4 Efficiency vs. Load Current

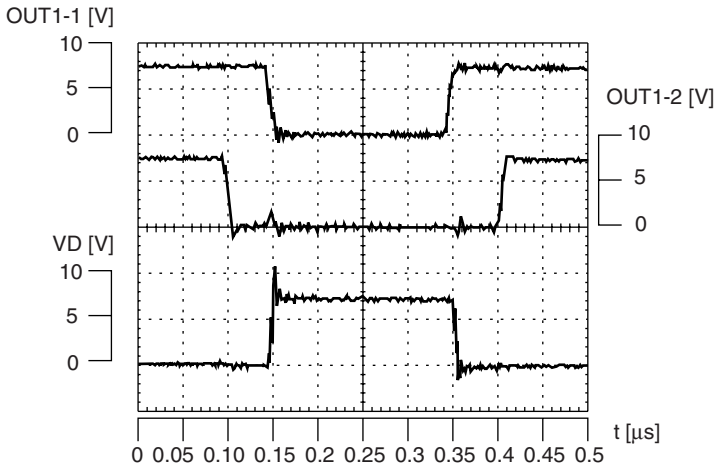


(Continued)

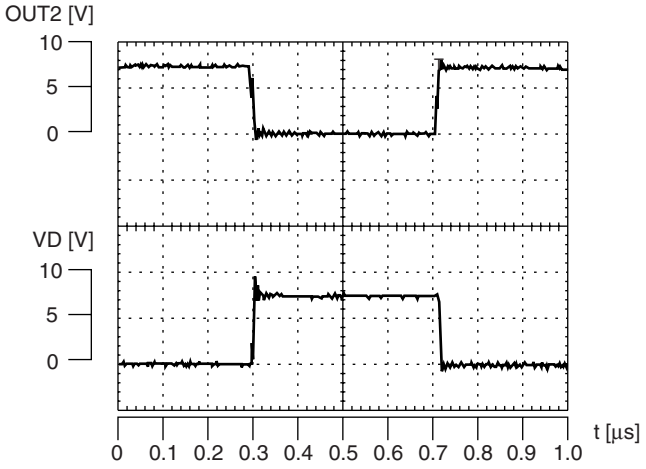


(Continued)

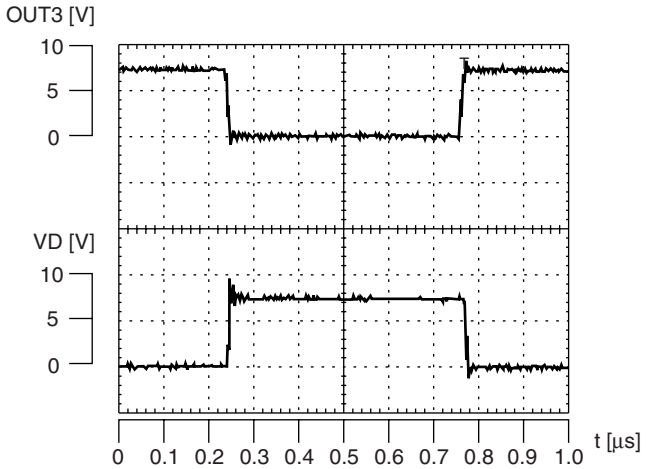
Switching waveform



ch.1
VIN = 7.2 V
Vo1 = 1.2 V
Io1 = 600 mA



ch.2
VIN = 7.2 V
Vo2 = 2.5 V
Io2 = 400 mA



ch.3
VIN = 7.2 V
Vo3 = 3.3 V
Io3 = 200 mA

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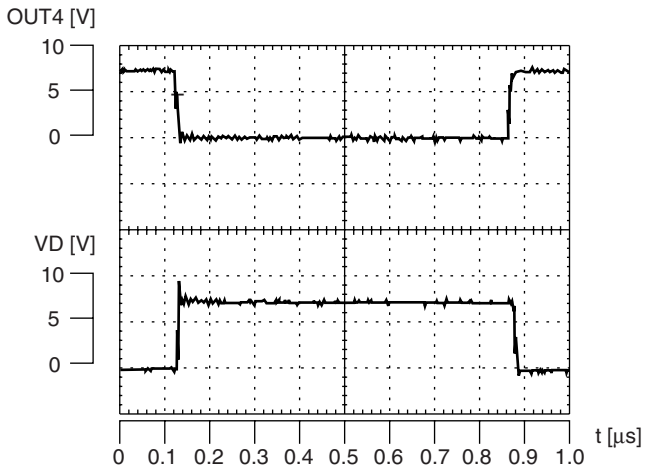
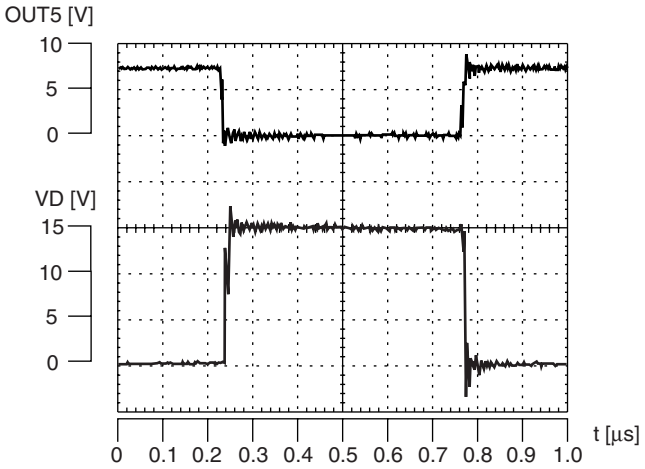


ch.4
VIN = 7.2 V
Vo4 = 5 V
Io4 = 100 mA



ch.5
VIN = 7.2 V
Vo5-1 = 15 V
Vo5-3 = –15 V
Io5-1 = 40 mA
Io5-3 = –10 mA

■ USAGE PRECAUTIONS

• Printed circuit board ground lines should be set up with consideration for common impedance.

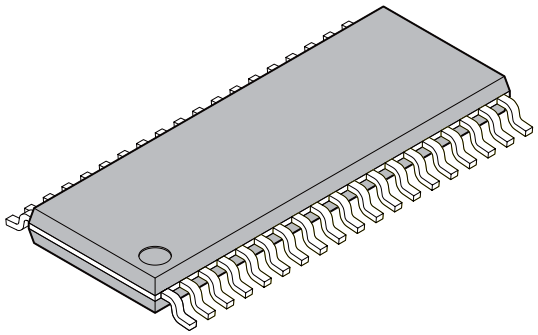
• Take appropriate static electricity measures.
  • Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  • After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  • Work platforms, tools, and instruments should be properly grounded.
  • Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

• Do not apply a negative voltages.
  • The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

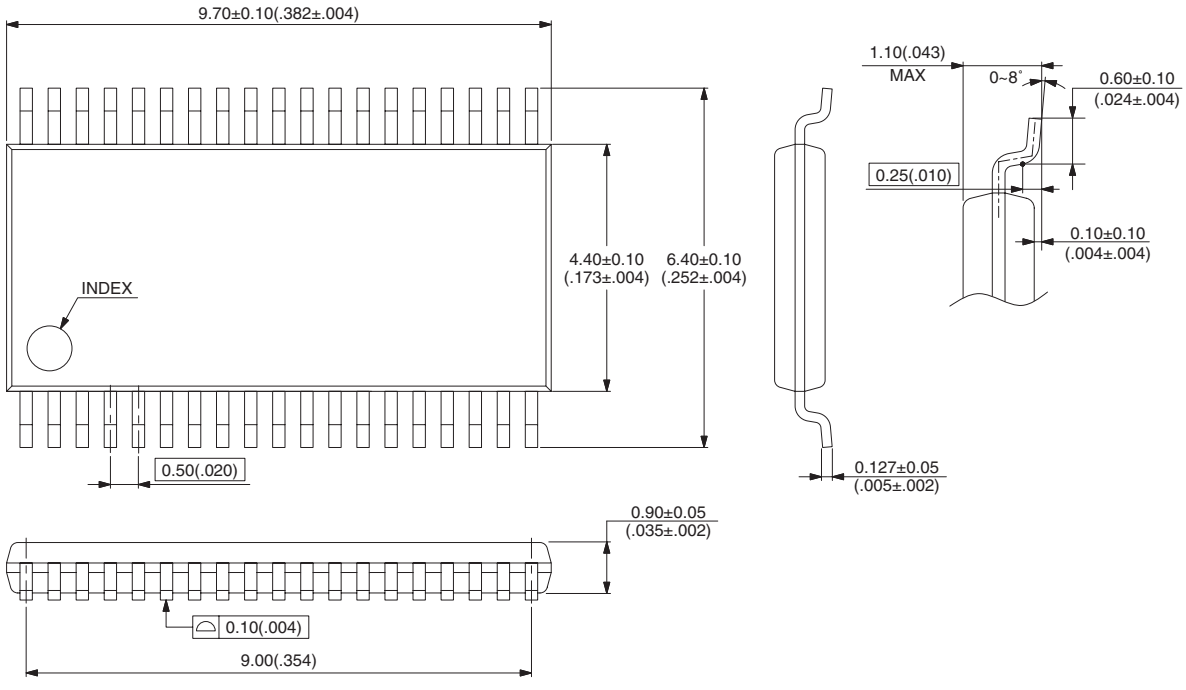
■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A115PFT	38-pin plastic TSSOP (FPT-38P- M03)	
MB39A115PV2	40-pin plastic BCC (LCC-40P-M07)	

■ PACKAGE DIMENSIONS

38-pin plastic TSSOP		
	Lead pitch	0.50 mm
	Package width × package length	4.40 × 9.70 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.10 mm MAX
(FPT-38P-M03)		

38-pin plastic TSSOP
(FPT-38P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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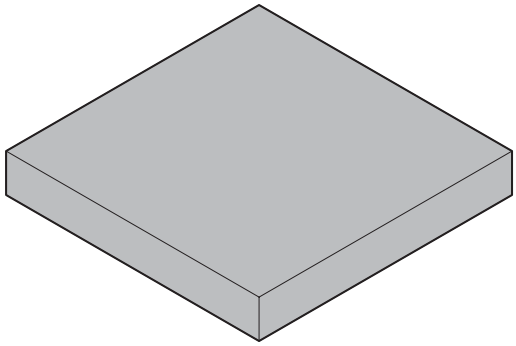
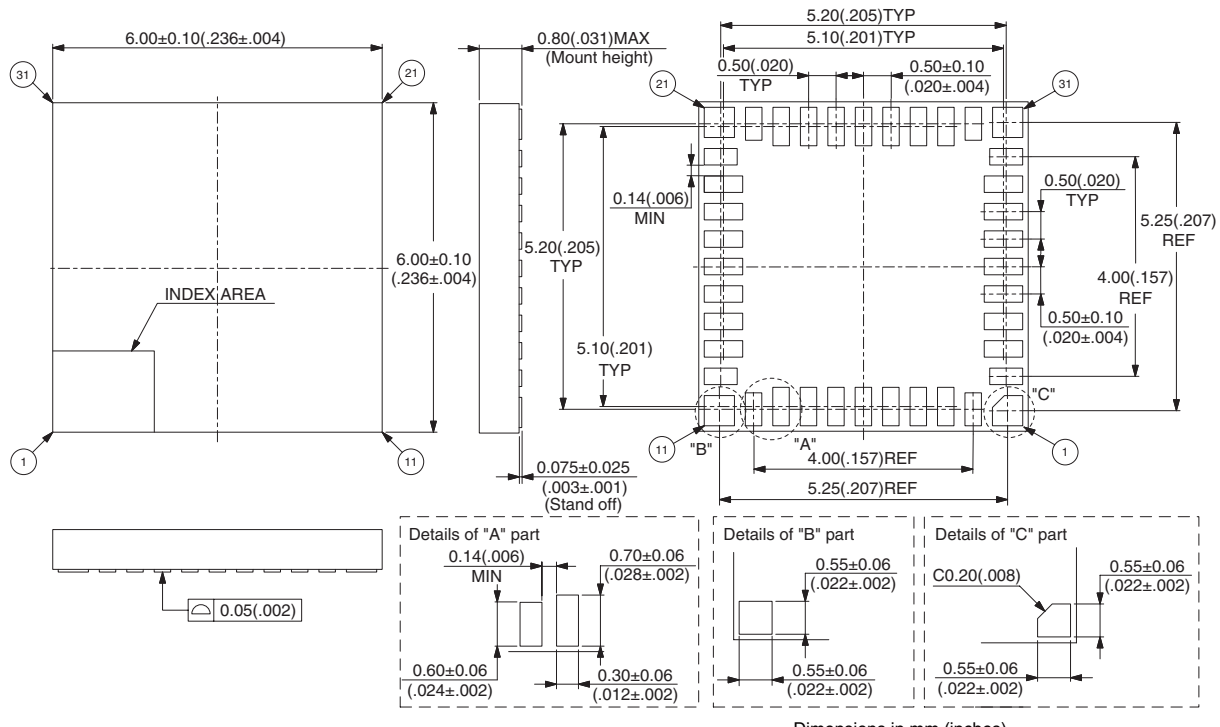
40-pin plastic BCC		
 (LCC-40P-M07)	Lead pitch	0.50 mm
	Package width × package length	6.00 mm × 6.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.05 g

40-pin plastic BCC
(LCC-40P-M07)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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