FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–27265–6E

*ASSP For Power Management Applications (Rechargeable Battery)*

# Synchronous Rectification DC/DC Converter IC for Charging Li-ion Battery

# MB39A132

## ■ DESCRIPTION

MB39A132, which is used for charging Li-ion battery, is a synchronous rectification DC/DC converter IC adopting pulse width modification (PWM). It can control charge voltage and charge current separately and supports the N-ch MOS driver. In addition, MB39A132 is suitable for down-conversion.
MB39A132 has an AC adapter detection comparator, which is independent of the DC/DC converter control block, and can control the source supplying voltage to the system.
MB39A132 supports a wide input voltage range, enables low current consumption in standby mode, and can control the charge voltage and charge current with high precision, which is perfect for the built-in Li-ion battery charger used in devices such as notebook PC.

## ■ FEATURES

- Supports 2/3/4-Cell battery pack
- Two built-in constant current control loops
- Built-in AC adapter detection function (ACOK pin)
- Charge voltage setting accuracy: ±0.5% (Ta = + 25 °C to + 85 °C)
- Charge voltage control setting can be selected without using any external resistor. (4.00 V/Cell, 4.20 V/Cell, 4.35 V/Cell)
  Output voltage can also be freely set by using the external resistor.
- Two built-in high-precision current detection amplifiers
  :Input offset voltage:+3 mV
  :Detection accuracy: ±1 mV (+INC1, +INC2 = 3 V to VCC)
- Charge current control setting can be selected without using any external resistor. ($R_S$ = 20 mΩ: 2.85 A)
  Charge current can also be freely set by using the external resistor.
- Switching frequency can be set by using the external resistor
  (MB39A132 has a built-in frequency setting capacitor.):100 kHz to 2 MHz
- Built-in off time control function
- In standby mode (Icc = 6 µA Typ), only the AC adapter detection function is in operation.

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**Power Supply online Design Simulation**
**Easy DesignSim**

This product supports the web-based design simulation tool.
It can easily select external components and can display useful information.
Please access from the following URL.

http://edevice.fujitsu.com/pmic/en-easy/?m=ds


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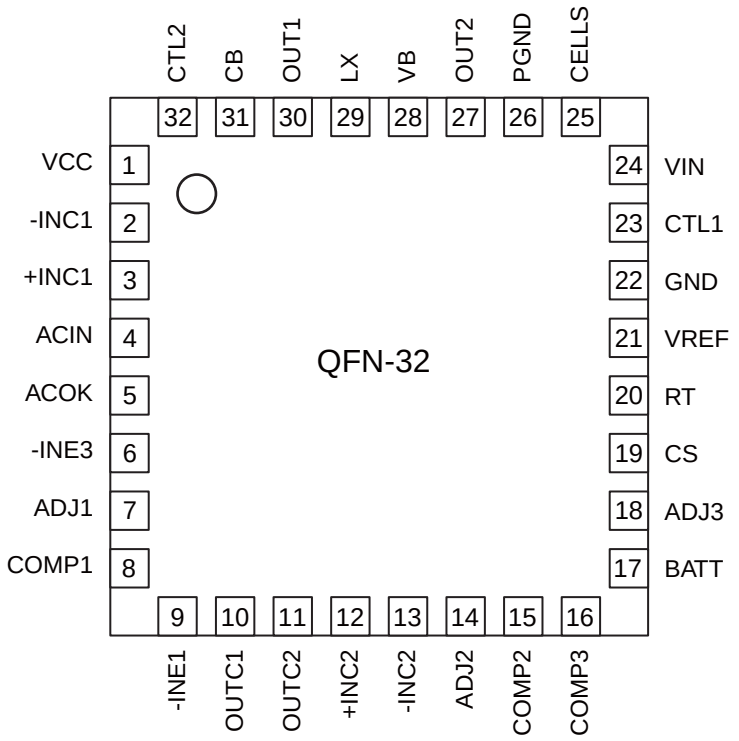
- Built-in output stage for N-ch MOS FET synchronous rectification
- Built-in charge stop function at low VCC pin voltage
- Built-in soft-start function whose setting time can be adjusted
- Equipped with the function enabling the independent operation of the AC adapter current detection amplifier
- Package: QFN-32

## ■ APPLICATIONS

- Internal charger used in notebook PC
- Handy terminal device etc.

## ■ PIN ASSIGNMENT

(TOP VIEW)




(LCC-32P-M19)

## ■ PIN DESCRIPTIONS

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | VCC | — | Power supply pin for reference power and control circuit (Battery side). |
| 2 | -INC1 | I | Current detection amplifier (Current Amp1) inverted input pin. |
| 3 | +INC1 | I | Current detection amplifier (Current Amp1) non-inverted input pin. |
| 4 | ACIN | I | AC adapter voltage detection block (AC Comp.) input pin. |
| 5 | ACOK | O | AC adapter voltage detection block (AC Comp.) output pin.<br>ACOK = Lo-Z when ACIN = H, ACOK = Hi-Z when ACIN = L |
| 6 | -INE3 | I | Error amplifier (Error Amp3) inverted input pin. |
| 7 | ADJ1 | I | Error amplifier (Error Amp1) non-inverted input pin. |
| 8 | COMP1 | O | Error amplifier (Error Amp1) output pin. |
| 9 | -INE1 | I | Error amplifier (Error Amp1) inverted input pin. |
| 10 | OUTC1 | O | Current detection amplifier (Current Amp1) output pin. |
| 11 | OUTC2 | O | Current detection amplifier (Current Amp2) output pin. |
| 12 | +INC2 | I | Current detection amplifier (Current Amp2) non-inverted input pin. |
| 13 | -INC2 | I | Current detection amplifier (Current Amp2) inverted input pin. |
| 14 | ADJ2 | I | Input pin for the charge current control block.<br>ADJ2 pin “GND to 4.4 V” :Charge current control block output = ADJ2 pin voltage<br>ADJ2 pin “4.6 V to VREF” :Charge current control block output = 1.5 V |
| 15 | COMP2 | O | Error amplifier (Error Amp2) output pin. |
| 16 | COMP3 | O | Error amplifier (Error Amp3) output pin. |
| 17 | BATT | I | Charge voltage control block battery voltage input pin. |
| 18 | ADJ3 | I | Charge voltage control block setting input pin.<br>ADJ3 pin “GND” :Charge voltage 4.00 V/Cell<br>ADJ3 pin “1.1 V to 2.2 V” :Charge voltage 2 × ADJ3 pin voltage/Cell<br>ADJ3 pin “2.4 V to 3.9 V” :Charge voltage 4.35 V/Cell<br>ADJ3 pin “4.1 V to VREF” :Charge voltage 4.20 V/Cell |
| 19 | CS | — | Soft-start capacitor connection pin. |
| 20 | RT | — | Triangular wave oscillation frequency setting resistor connection pin. |
| 21 | VREF | O | Reference voltage output pin. |
| 22 | GND | — | Ground pin. |
| 23 | CTL1 | I | Power supply control pin.<br>When the CTL1 pin is set to “H” level, the DC/DC converter becomes operable.<br>When the CTL1 pin is set to “L” level, the DC/DC converter becomes stand-by. |
| 24 | VIN | — | Power supply pin for ACOK function and Current Amp1(AC adapter side). |
| 25 | CELLS | I | Charge voltage setting switch pin (2/3/4-Cell).<br>CELLS = VREF: 4 Cells, CELLS = OPEN: 3 Cells, CELLS = GND: 2 Cells |
| 26 | PGND | — | Ground pin. |
| 27 | OUT2 | O | External low-side FET gate drive pin. |
| 28 | VB | O | FET drive circuit power supply pin. |
| 29 | LX | — | External high-side FET source connection pin. |
| 30 | OUT1 | O | External high-side FET gate drive pin. |

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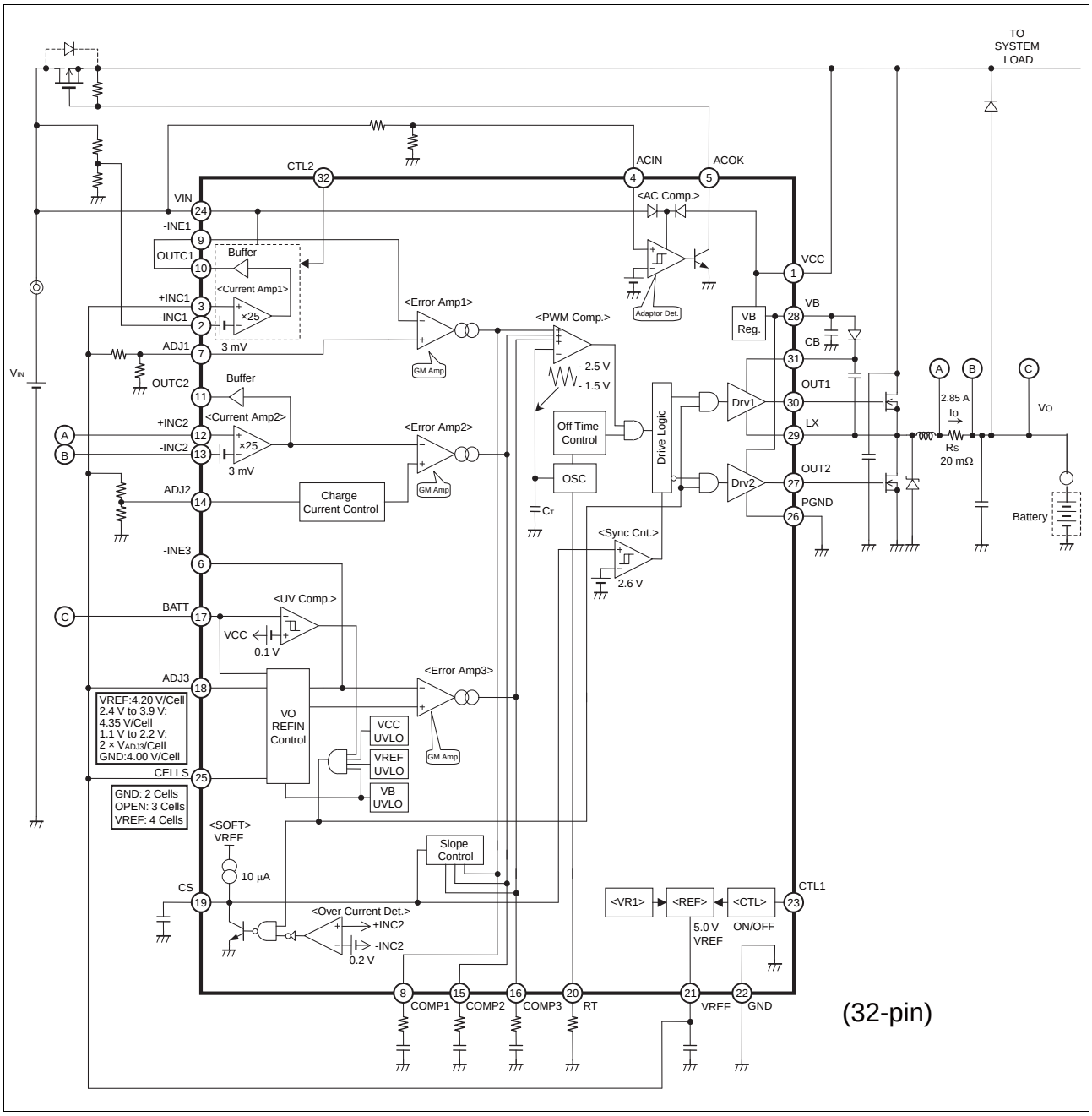
| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 31 | CB | — | Boot strap capacitor connection pin. The capacitor is connected between the CB pin and the LX pin. |
| 32 | CTL2 | I | Power supply control pin for Current Amp1.<br>When the CTL1 pin is set to “H” level, the DC/DC converter becomes operable.<br>When the CTL1 pin is set to “L” level, the DC/DC converter becomes stand-by. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power supply voltage | $V_{VCC}$ | VCC pin | − 0.3 | + 27 | V |
| | $V_{VIN}$ | VIN pin | − 0.3 | + 27 | V |
| CB pin input voltage | $V_{CB}$ | CB pin | − 0.3 | + 32 | V |
| CTL1, CTL2 pin input voltage | $V_{CTL}$ | CTL1, CTL2 pins | − 0.3 | + 27 | V |
| Input voltage | $V_{INC}$ | -INC1, +INC1 pins | − 0.3 | + 27 | V |
| | | -INC2, +INC2, BATT pins | − 0.3 | + 20 | V |
| | $V_{ADJ}$ | ADJ1, ADJ2, ADJ3, CELLS pins | − 0.3 | $V_{VREF}$ + 0.3 | V |
| | $V_{INE}$ | -INE1, -INE3 pins | − 0.3 | $V_{VREF}$ + 0.3 | V |
| ACIN input voltage | $V_{ACIN}$ | ACIN pin | − 0.3 | $V_{VIN}$ | V |
| ACOK pin output voltage | $V_{ACOK}$ | ACOK pin | − 0.3 | + 27 | V |
| Output current | $I_{OUT}$ | OUT1, OUT2 pins | − 60 | + 60 | mA |
| Power dissipation | $P_D$ | Ta ≤ + 25 °C | — | 4400*1,*2,*3 | mW |
| | | | — | 1900*1,*2,*4 | mW |
| | | Ta = + 85 °C | — | 1760*1,*2,*3 | mW |
| | | | — | 760*1,*2,*4 | mW |
| Storage temperature | $T_{STG}$ | — | − 55 | + 125 | °C |

*1 : See the diagram of "■ TYPICAL CHARACTERISTICS • Power Dissipation vs. Operating Ambient Temperature", for the package power dissipation of Ta from + 25 °C to + 85 °C.

*2 : When the IC is mounted on a 10x10 cm two-layer square epoxy board.

*3 : IC is mounted on a two-layer epoxy board, which has thermal vias, and the IC's thermal pad is connected to the epoxy board.

*4 : IC is mounted on a two-layer epoxy board, which has no thermal vias, and the IC's thermal pad is connected to the epoxy board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power supply voltage | $V_{VCC}$ | VCC pin | 8 | — | 25 | V |
| | $V_{VIN}$ | VIN pin | 8 | — | 25 | V |
| CB pin input voltage | $V_{CB}$ | CB pin | — | — | 30 | V |
| Reference voltage output current | $I_{VREF}$ | — | − 1 | — | 0 | mA |
| Bias output current | $I_{VB}$ | — | − 1 | — | 0 | mA |
| Input voltage | $V_{INC}$ | -INC1, +INC1 pins | 0 | — | $V_{VCC}$ | V |
| | | -INC2, +INC2, BATT pins | 0 | — | 19 | V |
| | $V_{ADJ}$ | ADJ1 pin | 0 | — | $V_{VREF}$ − 1.5 | V |
| | | ADJ2 pin (when using the internal reference voltage) | 4.6 | — | $V_{VREF}$ | V |
| | | ADJ2 pin (external voltage setting) | 0 | — | 4.4 | V |
| | | ADJ3 pin (when using the internal reference voltage) | 4.1 | — | $V_{VREF}$ | V |
| | | | 2.4 | — | 3.9 | V |
| | | | 0 | — | 0.9 | V |
| | | ADJ3 pin (external voltage setting) | 1.1 | — | 2.2 | V |
| | | CELLS pin | 0 | — | $V_{VREF}$ | V |
| | $V_{INE}$ | -INE1, -INE3 pins | 0 | — | $V_{VREF}$ | V |
| ACIN pin input voltage | $V_{ACIN}$ | — | 0 | — | $V_{VREF}$ | V |
| ACOK pin output voltage | $V_{ACOK}$ | — | 0 | — | 25 | V |
| ACOK pin output current | $I_{ACOK}$ | — | 0 | — | 1 | mA |
| CTL1, CTL2 pin input voltage | $V_{CTL}$ | — | 0 | — | 25 | V |
| Output current | $I_{OUT}$ | OUT1, OUT2 pins | − 45 | — | + 45 | mA |
| | | OUT1, OUT2 pins Duty ≤ 5% (t = 1/fosc × Duty) | − 1200 | — | + 1200 | mA |
| Switching frequency | $f_{OSC}$ | — | 100 | 500 | 2000 | kHz |
| Timing resistor | $R_{RT}$ | RT pin | 8.2 | 33 | 180 | kΩ |
| Soft-start capacitor | $C_{CS}$ | CS pin | — | 0.22 | — | µF |
| CB pin capacitor | $C_{CB}$ | — | — | 0.1 | — | µF |
| Bias output capacitor | $C_{VB}$ | VB pin | — | 1.0 | — | µF |
| Reference voltage output capacitor | $C_{REF}$ | VREF pin | — | 0.1 | 1.0 | µF |

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| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Operating ambient temperature | Ta | — | − 30 | + 25 | + 85 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, VCC pin = 19 V, VB pin = 0 mA, VREF pin = 0 mA)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Reference Voltage Block [REF] | Threshold voltage | $V_{VREF1}$ | 21 | — | 4.963 | 5.000 | 5.037 | V |
| | | $V_{VREF2}$ | 21 | Ta = − 10 °C to + 85 °C | 4.950 | 5.000 | 5.050 | V |
| | Input stability | VREF | 21 | VCC pin = 8 V to 25 V | — | 1 | 10 | mV |
| | Load stability | VREF | 21 | VREF pin = 0 mA to − 1mA | — | 1 | 10 | mV |
| | Short-circuit output current | Ios | 21 | VREF pin = 1 V | − 70 | − 35 | − 17 | mA |
| Triangular Wave Oscillator Block [OSC] | Oscillation frequency | $f_{OSC}$ | 30 | RT pin = 33 kΩ | 450 | 500 | 550 | kHz |
| | Frequency temperature variation | df/fdT | 30 | Ta = − 30 °C to + 85 °C | — | 1* | — | % |
| Error Amplifier Block [Error Amp1] | Input offset voltage | $V_{IO}$ | 7 | COMP1 pin = 2 V | — | 1* | 5 | mV |
| | Input bias current | $I_{ADJ1}$ | 7 | ADJ1 pin = 0 V | − 100 | — | — | nA |
| | Transconduc-tance | Gm | 8 | — | — | 20* | — | µA/V |
| Error Amplifier Block [Error Amp2] | Threshold voltage | $V_{TH1}$ | 14 | ADJ2 pin = VREF pin | — | 1.5* | — | V |
| | Transconduc-tance | Gm | 15 | — | — | 20* | — | µA/V |

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(Ta = + 25 °C, VCC pin = 19 V, VB pin = 0 mA, VREF pin = 0 mA)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Error Amplifier Block [Error Amp3] | Threshold voltage | $V_{TH1}$ | 17 | COMP3 pin = 2 V, Ta = + 25 °C to + 85 °C ADJ3 pin = CELLS pin = VREF pin | − 0.5 | 0 | + 0.5 | % |
| | | $V_{TH2}$ | 17 | COMP3 = 2 V, Ta = − 10 °C to + 85 °C ADJ3 pin = CELLS pin = VREF pin | − 0.7 | 0 | + 0.5 | % |
| | | $V_{TH3}$ | 17 | COMP3 = 2 V, Ta = + 25 °C to + 85 °C 2.4 V ≤ ADJ3 pin ≤ 3.9 V CELLS pin = VREF pin | − 0.5 | 0 | + 0.5 | % |
| | | $V_{TH4}$ | 17 | COMP3 pin = 2 V, Ta = − 10 °C to + 85 °C 2.4 V ≤ ADJ3 pin ≤ 3.9 V CELLS pin = VREF pin | − 0.7 | 0 | + 0.5 | % |
| | | $V_{TH5}$ | 17 | COMP3 pin = 2 V, Ta = + 25 °C to + 85 °C ADJ3 = GND pin, CELLS pin = VREF pin | − 0.5 | 0 | + 0.5 | % |
| | | $V_{TH6}$ | 17 | COMP3 pin = 2 V, Ta = − 10 °C to + 85 °C ADJ3 pin = GND pin, CELLS pin = VREF pin | − 0.7 | 0 | + 0.5 | % |
| | Input current | $I_{BATTH}$ | 17 | 2.4 V ≤ ADJ3 ≤ 3.9 V CELLS pin = VREF pin, BATT pin = 16.8 V | — | 34 | 60 | µA |
| | | $I_{BATTL}$ | 17 | VCC pin = 0 V, BATT pin = 16.8 V | — | 0 | 1 | µA |
| | Transcon-ductance | Gm | 16 | — | — | 280* | — | µA/V |

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(Ta = + 25 °C, VCC pin = 19 V, VB pin = 0 mA, VREF pin = 0 mA)

| Parameter | | Sym-bol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Current Detection Amplifier Block [Current Amp1, Current Amp2] | Input current | $I+_{INCH1}$ | 3 | +INC1 pin = 3 V to VCC pin, ΔVin = − 100 mV | — | 20 | 30 | µA |
| | | $I+_{INCH2}$ | 12 | +INC2 pin = 3 V to VCC pin, ΔVin = − 100 mV | — | 30 | 45 | µA |
| | | $I-_{INCH}$ | 2,13 | − INC1 pin = − INC2 pin = 3 V to VCC pin, ΔVin = − 100 mV | — | 0.1 | 0.2 | µA |
| | | $I+_{INCL}$ | 3,12 | +INC1 pin = +INC2 pin = 0.1 V, ΔVin = − 100 mV | − 240 | − 160 | — | µA |
| | | $I-_{INCL}$ | 2,13 | − INC1 pin = − INC2 pin = 0.1 V, ΔVin = − 100 mV | − 270 | − 180 | — | µA |
| | Input offset voltage | $V_{OFF1}$ | 10,11 | +INC1 pin = +INC2 pin = 3 V to VCC pin | 2 | 3 | 4 | mV |
| | | $V_{OFF2}$ | 10,11 | +INC1 pin = +INC2 pin = 0 V to 3 V | 1 | 3 | 5 | mV |
| | Common mode input voltage range | $V_{CM}$ | 10,11 | — | 0 | — | $V_{VCC}$ | V |
| | Voltage gain | Av | 10,11 | +INC1 pin = +INC2 pin = 3 V to VCC pin, ΔVin = − 100 mV | 24.5 | 25.0 | 25.5 | V/V |
| | Frequency bandwidth | BW | 10,11 | $A_V$ = 0 dB | — | 2* | — | MHz |
| | Output voltage | $V_{OUTCH}$ | 10,11 | — | 4.7 | 4.9 | — | V |
| | | $V_{OUTCL}$ | 10,11 | +INC1 pin = +INC2 pin = 3 V to VCC pin | 50 | 75 | 100 | mV |
| | Output source current | $I_{SOURCE}$ | 10,11 | OUTC1 pin = OUTC2 pin = 2 V | — | − 2 | − 1 | mA |
| | Output sink current | $I_{SINK}$ | 10,11 | OUTC1 pin = OUTC2 pin = 2 V | 25 | 50 | — | µA |
| | OUTC1 pin Output voltage | $V_{OUTC1}$ | 10 | VIN pin = 0 V | — | 0 | — | V |
| PWM Comparator Block [PWM Comp.] | Threshold voltage | $V_{TL}$ | 30 | Duty cycle = 0 % | 1.4 | 1.5 | — | V |
| | | $V_{TH}$ | 30 | Duty cycle = 100 % | — | 2.5 | 2.6 | V |
| Output Block [OUT] | Output ON resistance | $R_{OH}$ | 27,30 | OUT1,OUT2 pin = − 45 mA | — | 4 | 7 | Ω |
| | | $R_{OL}$ | 27,30 | OUT1,OUT2 pin = + 45 mA | — | 1 | 3.5 | Ω |

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(Ta = + 25 °C, VCC pin = 19 V, VB pin = 0 mA, VREF pin = 0 mA)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Control Block [CTL1,CTL2] | ON condition | VON | 23,32 | IC operation mode | 2 | — | 25 | V |
| | OFF condition | VOFF | 23,32 | IC standby mode | 0 | — | 0.8 | V |
| | Input current | $I_{CTLH}$ | 23,32 | CTL1, CTL2 pin = 5 V | — | 25 | 40 | µA |
| | | $I_{CTLL}$ | 23,32 | CTL1, CTL2 pin = 0 V | — | 0 | 1 | µA |
| Bias Voltage Block [VB] | Output voltage | VB | 28 | — | 4.9 | 5.0 | 5.1 | V |
| | Load stability | Load | 28 | VB pin = 0 mA to − 10 mA | — | 10 | 50 | mV |
| Synchronous Rectification Control Block [Synchronous Cnt.] | CS threshold voltage | $V_{TLH}$ | 19 | — | 2.55 | 2.60 | 2.65 | V |
| | | $V_{THL}$ | 19 | — | 2.5 | 2.55 | 2.60 | V |
| | Hysteresis width | $V_H$ | 19 | — | — | 0.05* | — | V |
| Under Voltage Lockout Protection Circuit Block [UVLO] | Threshold voltage | $V_{TLH}$ | 1 | VCC pin | — | 7.5 | 7.9 | V |
| | | $V_{THL}$ | 1 | VCC pin | 7.0 | 7.4 | — | V |
| | Hysteresis width | $V_H$ | 1 | VCC pin | — | 0.1 | — | V |
| | Threshold voltage | $V_{TLH}$ | 28 | VB pin | 3.8 | 4.0 | 4.2 | V |
| | | $V_{THL}$ | 28 | VB pin | 3.1 | 3.3 | 3.5 | V |
| | Hysteresis width | $V_H$ | 28 | VB pin | — | 0.7 | — | V |
| | Threshold voltage | $V_{TLH}$ | 21 | VREF pin | 2.6 | 2.8 | 3.0 | V |
| | | $V_{THL}$ | 21 | VREF pin | 2.4 | 2.6 | 2.8 | V |
| | Hysteresis width | $V_H$ | 21 | VREF pin | — | 0.2 | — | V |
| Over Current Detection Block [Over Current Det.] | Output voltage | $V_H$ | 12 | -INC2 pin = 12.6 V | 12.75 | 12.80 | 12.85 | V |
| Under Input Voltage Detection Block [UV Comp.] | Threshold voltage | $V_{TLH}$ | 1 | BATT pin = 12.6 V | 12.6 | 12.8 | 13.0 | V |
| | | $V_{THL}$ | 1 | BATT pin = 12.6 V | 12.5 | 12.7 | 12.9 | V |
| | Hysteresis width | $V_H$ | 1 | BATT pin = 12.6 V | — | 0.1 | — | V |
| AC Adapter Voltage Detection Block [AC Comp.] | Threshold voltage | $V_{TLH}$ | 4 | — | 1.237 | 1.250 | 1.263 | V |
| | | $V_{THL}$ | 4 | — | 1.227 | 1.240 | 1.253 | V |
| | Hysteresis width | $V_H$ | 4 | — | — | 10 | — | mV |
| | Input current | $I_{-INCL}$ | 4 | — | — | — | 200 | nA |
| | ACOK pin output leak current | $I_{LEAK}$ | 5 | ACOK pin = 25 V | — | 0 | 1 | µA |
| | ACOK pin output “L” Level voltage | $V_{ACOKL}$ | 5 | ACOK pin = 1 mA | — | 0.9 | 1.1 | V |

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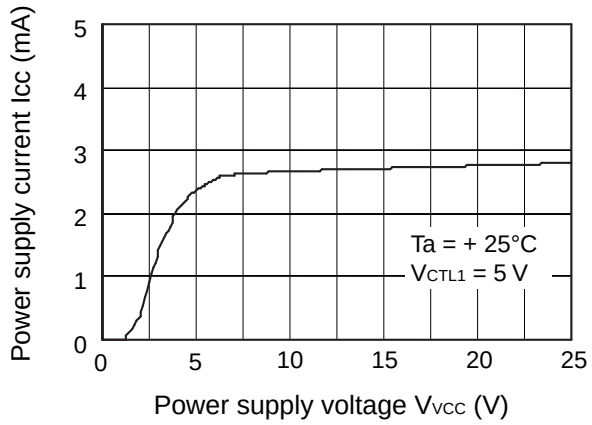
(Ta = + 25 °C, VCC pin = 19 V, VB pin = 0 mA, VREF pin = 0 mA)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Charge Voltage Control Block [VO REFIN Control] | Threshold voltage | $V_{THH}$ | 18 | At 4.2 V/Cell | 3.91 | 4.00 | 4.09 | V |
| | | $V_{THM}$ | 18 | At 4.35 V/Cell | 2.21 | 2.30 | 2.39 | V |
| | | $V_{THL}$ | 18 | At 4.0 V/Cell | 0.91 | 1.00 | 1.09 | V |
| | Input current | $I_{IN}$ | 18 | ADJ3 pin | — | 0 | 1 | µA |
| | Input voltage | $V_H$ | 25 | At 4Cells | $V_{VREF}$ – 0.4 | — | $V_{VREF}$ | V |
| | | $V_M$ | 25 | At 3Cells | 2.4 | — | 2.6 | V |
| | | $V_L$ | 25 | At 2Cells | 0 | — | 0.3 | V |
| | Input current | $I_{INL}$ | 25 | CELLS pin = 0 V | – 8.3 | – 5 | — | µA |
| | | $I_{INH}$ | 25 | CELLS pin = VREF pin | — | 5 | 8.3 | µA |
| Charge Current Control Block [Charge Current Control] | Threshold voltage | $V_{TH}$ | 14 | — | 4.41 | 4.5 | 4.59 | V |
| | Input current | $I_{IN}$ | 14 | ADJ2 pin | — | 0 | 1 | µA |
| Soft-start Block [SOFT] | Charge current | $I_{CS}$ | 19 | — | – 14 | – 10 | – 6 | µA |
| General | Standby current | $I_{VINL}$ | 24 | VIN pin = 19 V, ACIN pin = 0 V | — | 0 | 1 | µA |
| | | $I_{INS}$ | 24 | VCC pin = 0 V, CTL1, CTL2 pin = 0 V, ACIN pin = 5 V, VIN pin = 19 V | — | 6 | 10 | µA |
| | | $I_{CCS}$ | 1 | VIN pin = 0 V, CTL1, CTL2 pin = 0 V, ACIN pin = 0 V, VCC pin = 19 V | — | 0 | 1 | µA |
| | Power supply current | $I_{IN}$ | 24 | VIN pin = 19 V, VCC pin = 0 V, ACIN pin = 5 V, CTL1 pin = 0 V, CTL2 pin = 5 V | — | 300 | 450 | µA |
| | | $I_{CC}$ | 1 | VIN pin = 0 V, VCC pin = 19 V, ACIN pin = 0 V, CTL1 pin = 5 V, CTL2 pin = 0 V | — | 2.4 | 3.6 | mA |
| | | $I_{INCC}$ | 1,24 | VIN pin = 19 V, VCC pin = 19 V, ACIN pin = 5 V, CTL1 pin = 5 V, CTL2 pin = 5 V | — | 2.7 | 4.1 | mA |

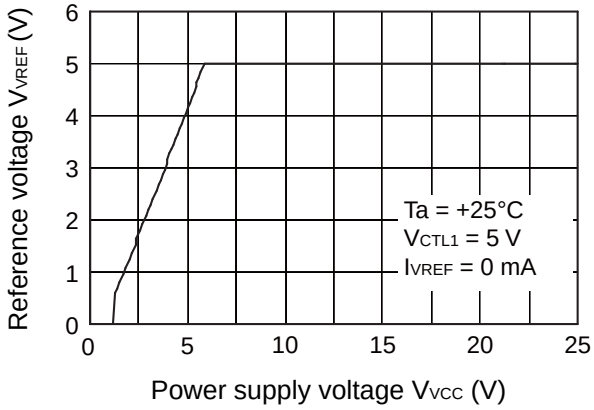
*: This value is not be specified. This should be used as a reference to support designing the circuits.

## ■ TYPICAL CHARACTERISTICS

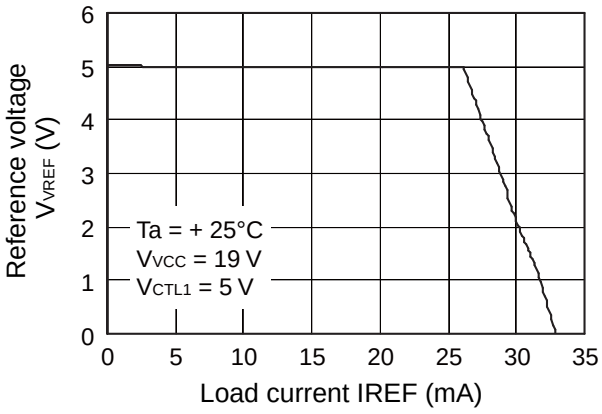
Power supply current vs.
Power supply voltage



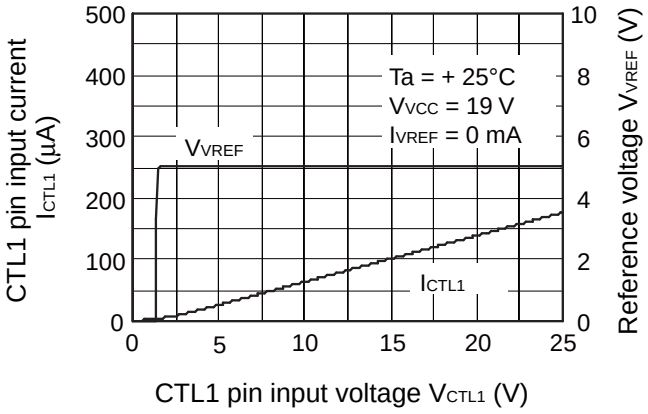

Reference voltage vs. Power supply voltage



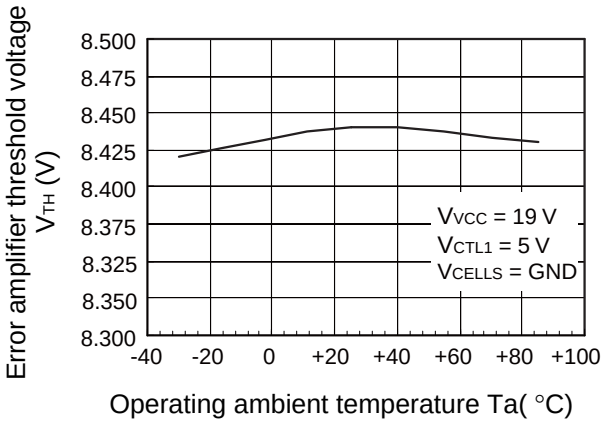

Reference voltage vs. Load current



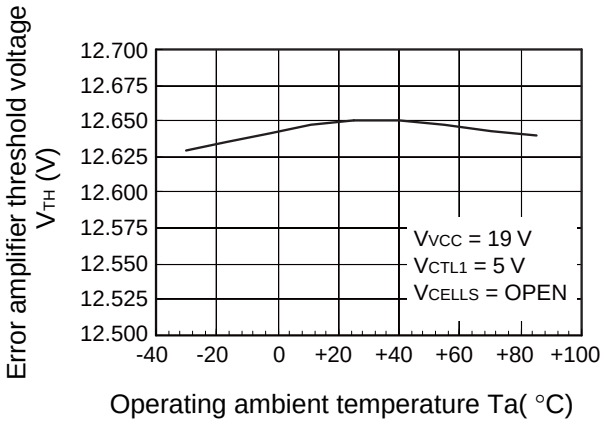

CTL1 pin input current,
Reference voltage vs.
CTL1 pin input voltage




Error amplifier threshold voltage vs.
Operating ambient temperature




Error amplifier threshold voltage vs.
Operating ambient temperature

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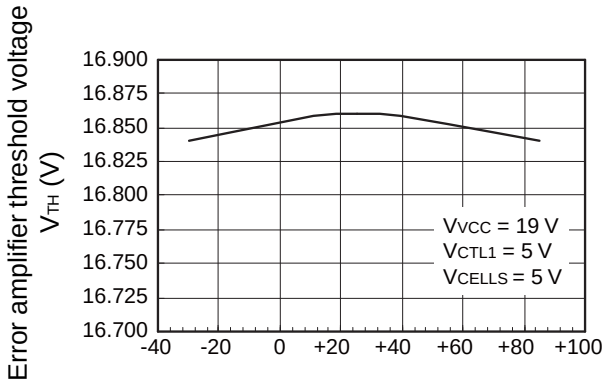
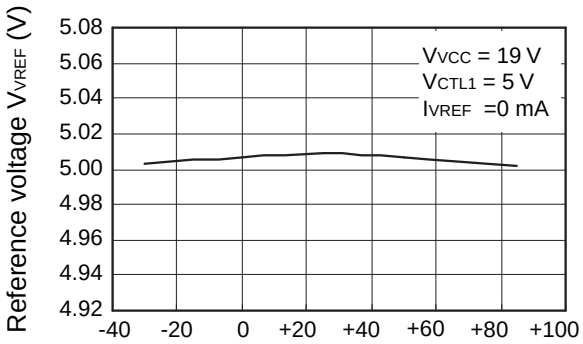
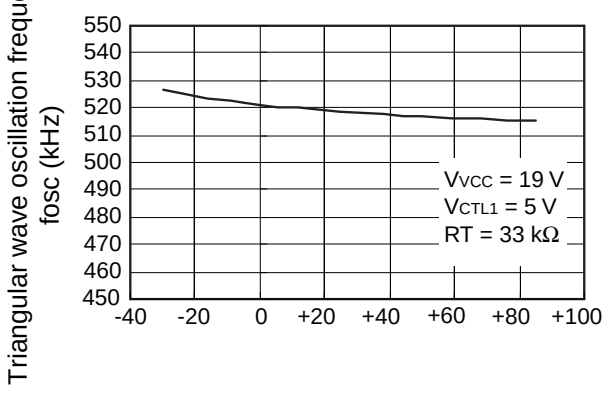
Error amplifier threshold voltage vs.
Operating ambient temperature



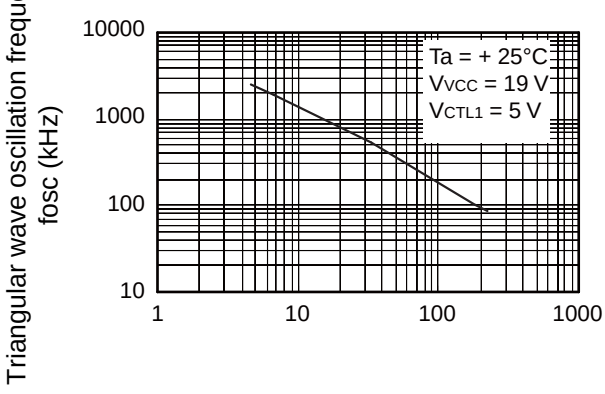

Reference voltage vs.
Operating ambient temperature



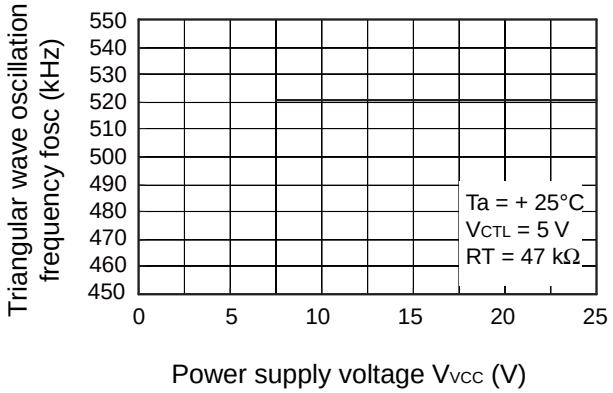

Triangular wave oscillation frequency vs.
Operating ambient temperature



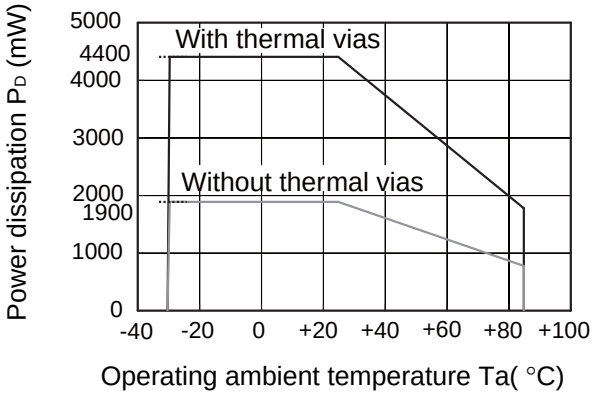

Triangular wave oscillation frequency vs.
Timing resistor




Triangular wave oscillation frequency vs.
Power supply voltage




Power dissipation vs.
Operating ambient temperature



## ■ FUNCTIONAL DESCRIPTION

MB39A132 is an N-ch MOS driver-supported DC/DC converter which uses pulse width modulation (PWM) for charging Li-ion battery and controls the charge voltage and current when charging the battery. To stabilize the power supplied from a battery or an adapter to a system, this DC/DC converter has a battery charging control function and an AC adapter voltage detection function.

When MB39A132 controls charge voltage (constant voltage mode), it can freely set the charge voltage with the voltage input to the ADJ3 pin (pin 18) and the CELLS pin (pin 25). It compares the BATT pin (pin 17) voltage and the internal reference voltage with the error amplifier (Error Amp3), outputs PWM control signals and then outputs the charge voltage freely set by the IC.

When MB39A132 controls charge current (constant current mode), it amplifies the voltage drop occurring on both ends of the charge current sense resistor (Rs) by 25 times with the current detection amplifier (Current Amp2), and then outputs the amplified voltage to the OUTC2 pin (pin 11). It compares the output voltage of the current detection amplifier (Current Amp2) and the voltage set in the ADJ2 pin (pin 14) with the error amplifier (Error Amp2), and then outputs PWM control signals for executing constant-current charge.

When MB95A132 controls AC adapter power, in the case of an output voltage drop in the AC adapter, the converter amplifies the voltage difference between the voltage applied to the -INC1 pin (pin 2) that has dropped and the +INC1 pin (pin 3) voltage ($V_{VREF}$) by 25 times with the current detection amplifier (Error Amp1), and then outputs the amplified voltage value to the OUTC1 pin (pin 10). It compares the output voltage of the current detection amplifier (Current Amp1) to the ADJ1 pin (pin 7) voltage using the error amplifier (Error Amp1) to output PWM control signals for controlling the charge current so that the AC adapter power can be kept constant.

The triangular wave voltage generated by the triangular wave oscillator is compared with the output voltage of one of the three error amplifiers (Error Amp1, Error Amp2 and Error Amp3) that has the lowest potential. The main FET is turned on during the period when the triangular wave voltage is lower than the error amplifier output voltage.

In addition, the AC Comp. detects installation/removal of the AC adapter and its information is output through the ACOK pin (pin 5).

## 1. Blocks of DC/DC Converter

### (1) Reference voltage block (REF)

The reference voltage circuit uses the voltage supplied from the VCC pin (pin 1) to generate stable voltage (Typ. 5.0 V) that has undergone temperature compensation. The generated voltage is used as the reference power supply for the internal circuitry of the IC.
This block can output load current of up to 1 mA from the reference voltage VREF pin (pin 21).

### (2) Triangular wave oscillator block (OSC)

The triangular wave oscillator builds the capacitor for frequency setting into, and generates the triangular wave oscillation waveform by connecting the frequency setting resistor with the RT pin (pin 20).
The triangular wave is input to the PWM comparator on the IC.

Triangular wave oscillation frequency: fosc

fosc (kHz) ≒ 17000/RT (kΩ)

### (3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current Amp1) and outputs a PWM control signal.
In addition, a stable phase compensation can be made available to the system by connecting the resistor and the capacitor to the COMP1 pin (pin 8).

### (4) Error amplifier block (Error Amp2)

This amplifier detects the output signal from the current detection amplifier (Current Amp2), compares this to the output signal from the charge current control circuit, and outputs a PWM control signal to be used in controlling the charge current.
In addition, a stable phase compensation can be made available to the system by connecting the resistor and the capacitor to the COMP2 pin (pin 15).

### (5) Error amplifier block (Error Amp3)

This error amplifier (Error Amp3) detects the output voltage from the DC/DC converter, compares this to the output signal from the VO REFIN controller circuit, and outputs the PWM control signal. Arbitrary output voltage from 2 Cell to 4 Cell can be set by connecting an external resistor of charging voltage to ADJ3 pin (pin 18).
In addition, a stable phase compensation can be made available to the system by connecting the resistor and the capacitor to the COMP3 pin (pin 16).

### (6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) amplifies the voltage difference between the +INC1 pin (pin 3) and the -INC1 pin (pin 2) by 25 times and outputs the amplified signal to the OUTC1 pin (pin 10).

### (7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) detects a voltage drop occurring at both ends of the charge current sense resistor (Rs) with the +INC2 pin (pin 12) and the -INC2 pin (pin 13). It outputs the signal amplified by 25 times to the inverted input pin of the following error amplifier (Error Amp2) and to the OUTC2 pin (pin 11).

### (8) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty according to the output voltage of the error amplifiers (Error Amp1 to Error Amp3).
The triangular wave voltage generated by the triangular wave oscillator is compared with the output voltage of one of the three error amplifiers (Error Amp1, Error Amp2 and Error Amp3) that has the lowest potential. The main FET is turned on during the period when the triangular wave voltage is lower than the error amplifier output voltage.

### (9) Output block (OUT)

The output block uses a CMOS configuration on both the high-side and the low-side, and can drive the external N-ch MOS FET.

**(10) Power supply control block (CTL1)**

The power supply control block controls the DC/DC converter operation. When the CTL1 pin (pin 23) is set to "L" level, the DC/DC converter enters standby mode. In the standby mode, only the AC adapter detection function is operable. (The typical supply current value is 6 μA in the standby mode.)

CTL1 function table

| CTL1 | DC/DC converter control | AC adapter detection |
|---|---|---|
| L | OFF (Standby) | ON (Active) |
| H | ON (Active) | ON (Active) |

**(11) Current Amp1 control block (CTL2)**

The Current Amp1 controller controls the Current Amp1 operation. When the CTL2 pin is set to "H" level, the Current Amp1 becomes operable.
When the CTL1 pin (pin 23) is set to the "L" level and the CTL2 pin (pin32) is set to the "H" level after full-charge, only Current Amp1 and the AC adapter detection function becomes operable.

CTL2 function table

| CTL2 | Current Amp1 | AC adapter detection |
|---|---|---|
| L | OFF (Standby) | ON (Active) |
| H | ON (Active) | ON (Active) |

**(12) Bias voltage block (VB)**

The bias voltage block outputs 5 V (Typ) for the power supply of the output circuit and for setting the bootstrap voltage.

**(13) Off time control block (Off Time Control)**

When this IC operates by high on-duty, voltage of both ends of bootstrap capacitor CB is decreasing gradually. In such the case, off time control block charges with CB by compulsorily generating off time (0.3 μs Typ).

## 2. Protection Functions

### (1) Under voltage lockout protection circuit (VREF-UVLO)

A momentary decrease in internal reference voltage (VREF) may cause malfunctions in the control IC, resulting in breakdown or degradation of the system. To prevent such malfunction, the under voltage lockout protection circuit detects internal reference voltage drop and fixes the OUT1 pin (pin 30) and the OUT2 pin (pin 27) at the “L” level. UVLO will be released when the internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VREF-UVLO) operation function table

When UVLO is operating (VREF voltage is lower than UVLO threshold voltage.), the logic value of the following pin is fixed.

| OUT1 | OUT2 | CS | VB |
|---|---|---|---|
| L | L | L | L |

### (2) Under voltage lockout protection circuit (VCC-UVLO, VB-UVLO)

The transient state or the momentary decrease in power supply voltage, which occurs when the bias voltage (VB) for output circuit is turned on, may cause malfunctions in the control IC, resulting in breakdown or degradation of the system. To prevent such malfunction, the under voltage lockout protection circuit detects a bias voltage drop and fixes the OUT1 pin (pin 30) and the OUT2 pin (pin 27) at the “L” level. UVLO will be released when the power supply voltage or internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VCC-UVLO, VB-UVLO) operation function table

When UVLO is operating (VCC voltage or VB voltage is lower than UVLO threshold voltage.), the logical value of the following pin is fixed.

| OUT1 | OUT2 | CS |
|---|---|---|
| L | L | L |

### (3) Under input voltage detection block (UV Comp.)

It compares the VCC pin (pin 1) voltage with the BATT pin (pin 17) voltage. If the VCC voltage is lower than the BATT pin voltage plus 0.1 V (Typ), the comparator fixes the OUT1 pin (pin 30) and the OUT2 pin (pin 27) at "L" level.
The system resumes operation when the input voltage is higher than the threshold voltage of the under input voltage detection comparator.

Protection circuit (UV Comp.) operation function table

When under input voltage is detected (Input voltage is lower than UV Comp. threshold voltage), the logical value of the following pin is fixed.

| OUT1 | OUT2 | CS |
|---|---|---|
| L | L | L |

**(4) Overcurrent detection block (Over Current Det.)**

When this block detects that the potential difference between the +INC2 pin (pin 12) and the -INC2 pin (pin 13) exceeds 0.2 V (Typ), and excessive current flows in the charging direction due to a sudden change of load, this block will determine that overcurrent occurs, and sets the CS pin (pin 19) to "L" level and the ON duty to 0%. Afterward, when the overcurrent ceases to exist, the soft-start operation is started.

$$\text{Overcurrent detection value : } Ioc\,det(A) = \frac{0.2(V)}{R_S(\Omega)}$$

Charge current and overcurrent detection value by $R_S$ value (example)

| $R_S$ | ADJ2 | Io | OCDet |
|---|---|---|---|
| 20 mΩ | 0.5 V to 4.4 V | 0.85 A to 8.65 A | 10 A |
| 15 mΩ | 0.5 V to 4.4 V | 1.13 A to 11.5 A | 13 A |

**(5) Overtemperature detection**

The circuit protects an IC from heat destruction. If the temperature at the joint reaches +150 °C, the circuit set OUT1 (pin 30) and OUT2 (pin 27) pins to "L", and stops voltage output.

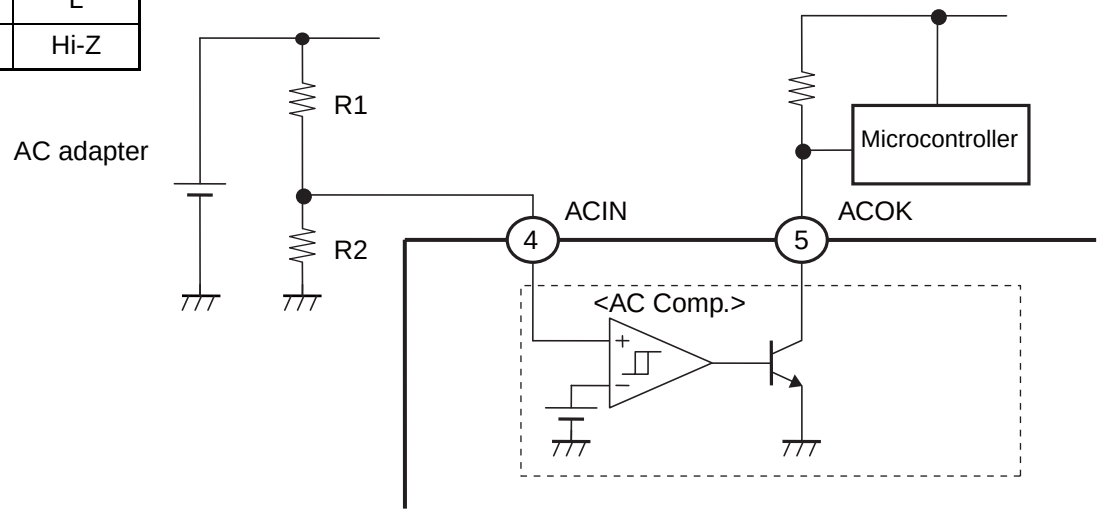
In addition, if the temperature at the joint drops to +125 °C, the voltage output restarts again.
When designing a DC/DC power supply system, do not exceed the absolute maximum ratings of this IC in order to prevent overtemperature protection from being activated.

## 3. Detection Function

### AC adapter voltage detection block (AC Comp.)

When the AC adapter voltage detection block (AC Comp.) detects that ACIN pin (pin 4) voltage is below 1.25 V (Typ), it and sets ACOK pin (pin 5) in the AC adapter voltage detection block to Hi-Z. In addition, power is supplied from the VCC pin (pin 1) or the VIN pin (pin 24), whichever has higher voltage.
This function operates regardless of the input level of the CTL1 pin (pin 23) and CTL2 pin (pin 32).

| ACIN | ACOK |
|---|---|
| H | L |
| L | Hi-Z |




AC adapter detection voltage setting

$V_{IN}$ = Low to High

Vth = (R1 + R2) / R2 × 1.25 V

$V_{IN}$ = High to Low

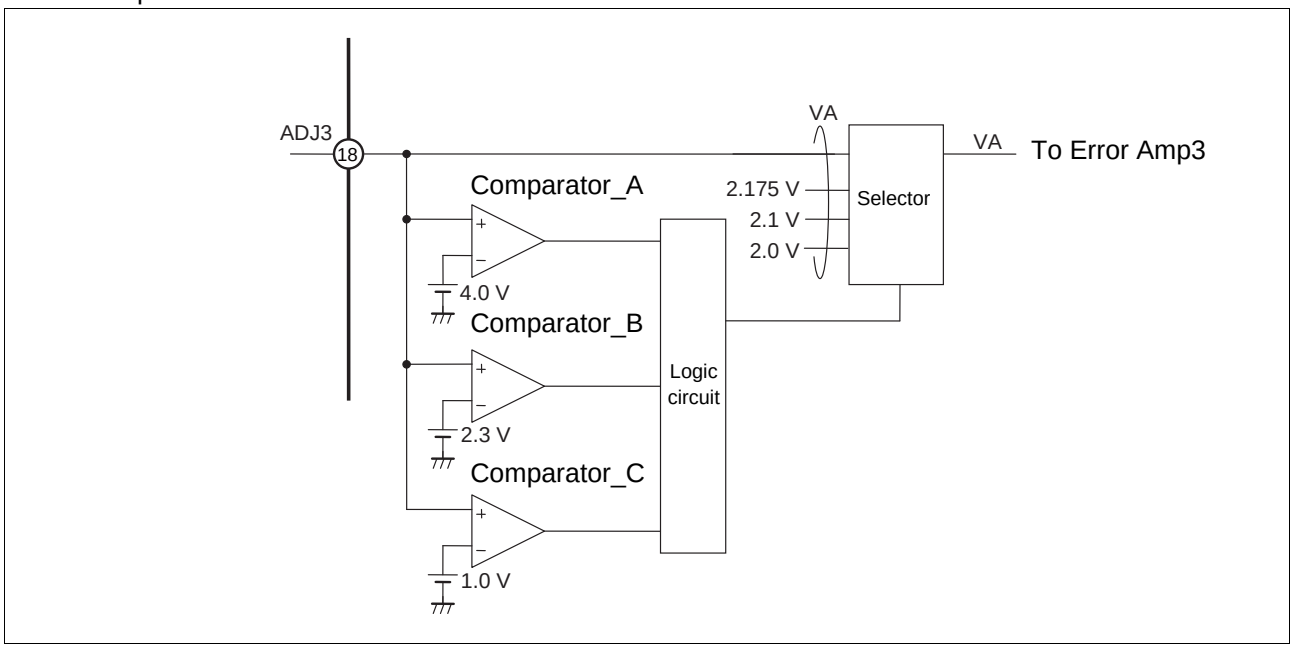
Vth = (R1 + R2) / R2 × 1.24 V

## ■ SETTING THE CHARGE VOLTAGE

The charge voltage (DC/DC converter output voltage) can be set by the input voltage to ADJ3 pin (pin 18) and CELLS pin (pin 25). The ADJ3 pin can set charge voltage per cell. The value of charge voltage can be freely set when the ADJ3 pin is connected to an external resistor. When the VREF level voltage or the GND level voltage is input to the ADJ3 pin, the internal high-precision reference voltage set in advance can be used. When the VREF level voltage or the GND level voltage is input to the CELLS pin, or the CELLS pin is left unconnected, the number of series batteries can be set.
The correspondence between the ADJ3 pin, the CELLS pin and charge voltage (DC/DC converter output voltage) is shown below.

| ADJ3 pin Input Voltage | CELLS pin | Charge Voltage | Remarks |
|---|---|---|---|
| VREF pin (ADJ3 ≥ 4.1V) | GND | 8.4 V | 2 Cells × 4.20 V/Cell |
| | OPEN | 12.6 V | 3 Cells × 4.20 V/Cell |
| | VREF | 16.8 V | 4 Cells × 4.20 V/Cell |
| 2.4 V ≤ ADJ3 pin ≤ 3.9 V | GND | 8.7 V | 2 Cells × 4.35 V/Cell |
| | OPEN | 13.05 V | 3 Cells × 4.35 V/Cell |
| | VREF | 17.4 V | 4 Cells × 4.35 V/Cell |
| GND pin (0 V ≤ ADJ3 pin ≤ 0.9 V) | GND | 8.0 V | 2 Cells × 4.00 V/Cell |
| | OPEN | 12.0 V | 3 Cells × 4.00 V/Cell |
| | VREF | 16.0 V | 4 Cells × 4.00 V/Cell |
| External voltage setting (1.1 V ≤ ADJ3 pin ≤ 2.2 V) | GND | 4 × ADJ3 pin voltage | 2 Cells × 2 × ADJ3 pin voltage/Cell |
| | OPEN | 6 × ADJ3 pin voltage | 3 Cells × 2 × ADJ3 pin voltage/Cell |
| | VREF | 8 × ADJ3 pin voltage | 4 Cells × 2 × ADJ3 pin voltage/Cell |

• ADJ3 pin internal circuit



## ■ SETTING THE CHARGE CURRENT

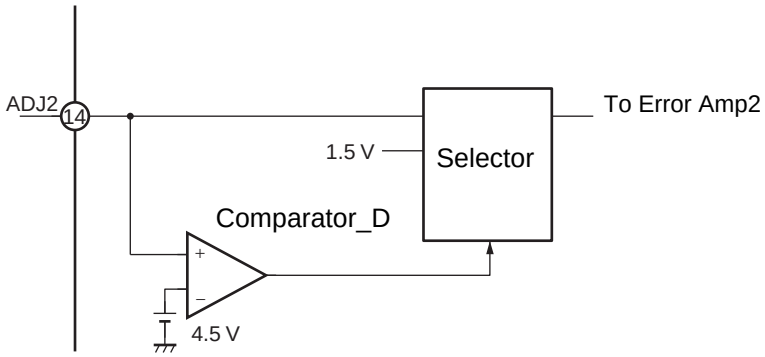
The error amplifier (Error Amp2) compares the output voltage of charge current control block set by the ADJ2 pin (pin 14) with the output signal from the charge current detection amplifier (Current Amp2), and outputs a the PWM control signal. The maximum charge current for battery can be set according to the ADJ2 pin voltage. When a current exceeding the setting current value is going to flow, constant current charge will be executed at that setting current value, and the charge voltage will drop.

Battery charge current setting voltage: ADJ2

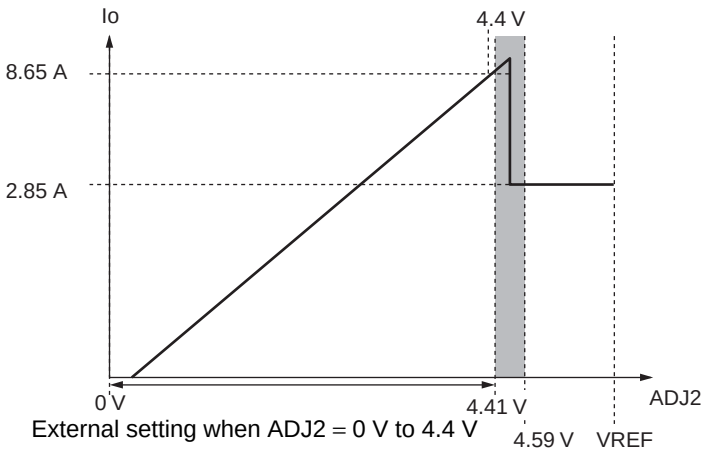
$$\text{Charge current upper limit } I_O = \frac{\text{Output voltage in the charge current control block} - 0.075}{\text{Current detection amplifier gain (25 V/V Typ)} \times \text{sense resistor } R_S(\Omega)}$$

| ADJ2 pin input voltage | Charge current control block output voltage | Charge current | |
|---|---|---|---|
| | | $R_S$ = 20 mΩ | $R_S$ = 15 mΩ |
| VREF pin (ADJ2 pin ≥ 4.6 V) | 1.5 V | 2.85 A | 3.8 A |
| External Voltage Setting (ADJ2 pin = GND pin to 4.4 V) | $V_{ADJ2}$(V) | 2 × (ADJ2 pin – 0.075)(A) | 2.66 × (ADJ2 pin – 0.075) (A) |

- ADJ2 pin internal circuit

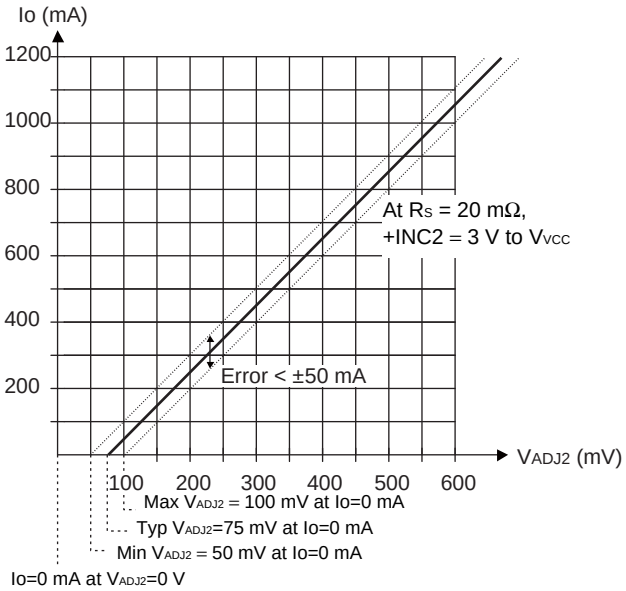



- Example of the charge current setting (at $R_S$ = 20 mΩ)




External setting when ADJ2 = 0 V to 4.4 V

Internal reference voltage setting when ADJ2 = 4.6 V to VREF


Io (mA)
1200
1000
800
600
400
200
At Rs = 20 mΩ,
+INC2 = 3 V to VVCC
Error < ±50 mA
VADJ2 (mV)
100
200
300
400
500
600
Max VADJ2 = 100 mV at Io=0 mA
Typ VADJ2=75 mV at Io=0 mA
Min VADJ2 = 50 mV at Io=0 mA
Io=0 mA at VADJ2=0 V

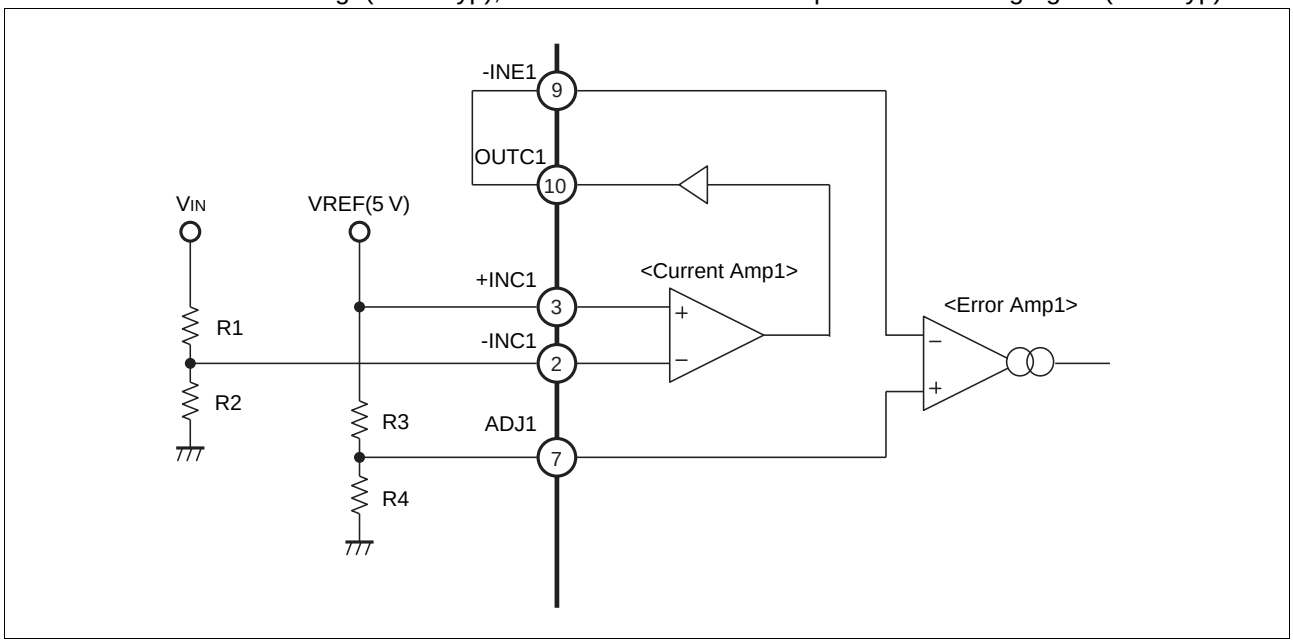
## ■ SETTING DYNAMICALLY-CONTROLLED CHARGING

With the connection shown below, when the voltage of the AC adapter ($V_{IN}$) drops and reaches Vth, the result of the equation shown below, the converter becomes dynamically-controlled charging mode and then controls charge current to maintain a constant power level of the AC adapter.

AC adapter voltage in dynamically-controlled-charging mode: Vth

$$Vth = [(1 - \frac{1}{Av} \times \frac{R4}{R3 + R4})VREF + 3\ mV] \times \frac{R1 + R2}{R2}$$

VREF = Reference voltage(5.0 V Typ), $A_V$ = Current detection amplifier block voltage gain (25.0 Typ)



## ■ SETTING THE SOFT-START TIME

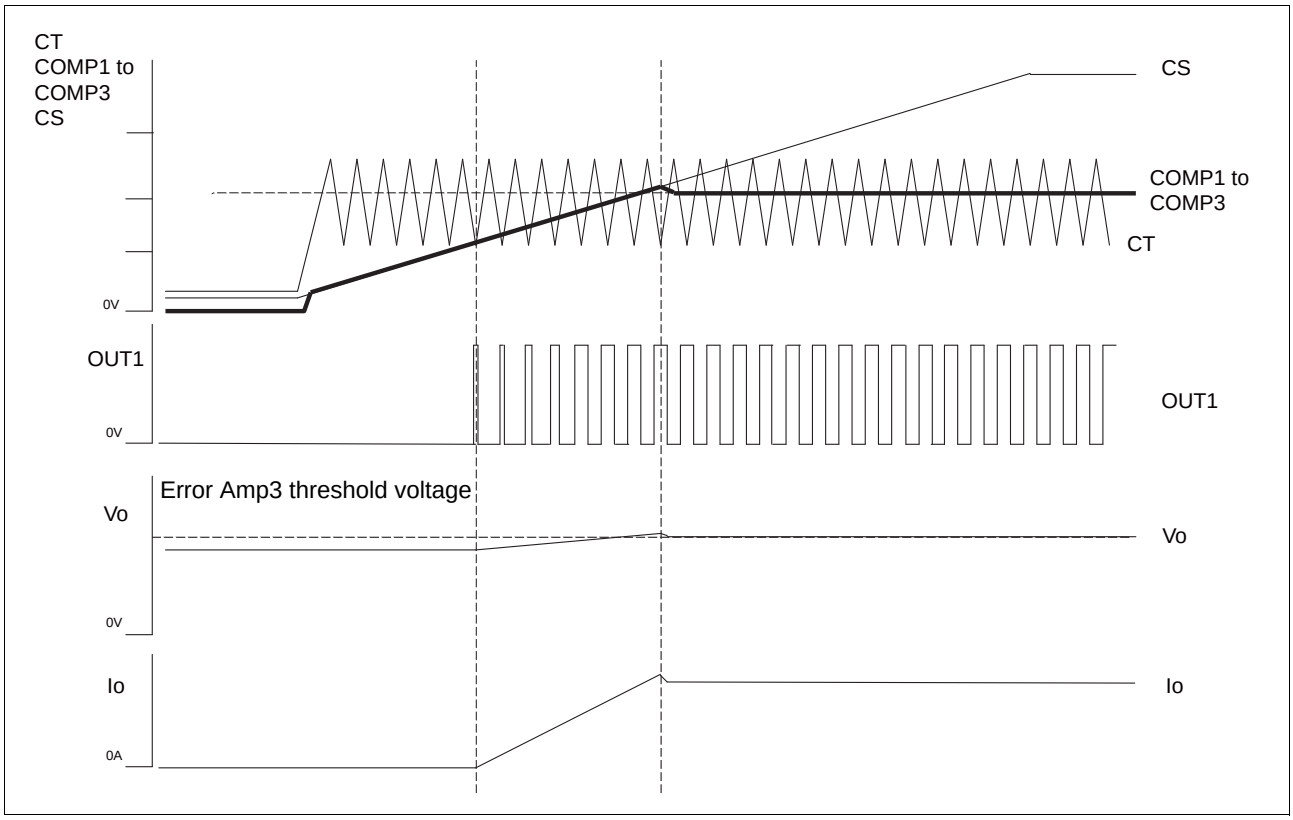
To prevent rush current at start-up of IC, the soft-start time can be set by connecting a soft-start capacitor ($C_S$) to the CS pin (pin 19). When the CTL1 pin (pin 23) and the CTL2 pin (pin 32) are set to “H” level and the IC is started (Vcc 3 ≥ UVLO threshold voltage), the external capacitor (Cs) for soft-start ($C_S$) connected to the CS pin is charged at 10 μA.

The output ON duty depends on the result of comparison done by the PWM comparator among the COMP1 pin (pin 8) voltage, the COMP2 pin (pin15) voltage, the COMP3 pin (pin16) voltage and the triangular wave oscillator output voltage (CT). During soft-start, the COMP1 pin, the COMP2 pin, and the COMP3 pin voltages are clamped so that the voltages of those three pins will not exceed the CS pin voltage. Therefore, the output voltage of the DC/DC converter and current increase can be set by the output ON duty in proportion to rise of the CS pin voltage.

The ON duty is affected by the ramp voltage of the COMP1 pin, the COMP2 pin, and the COMP3 pin until the output voltage of one of the three Error Amp reaches the DC/DC converter loop control voltage.

Soft-start time is obtained from the following formula.

Soft-start time (time for the output ON duty to reach 80%): $ts(s) \fallingdotseq 0.23 \times Cs\ (\mu F)$



## ■ TRANSIT RESPONSE AT STEP LOAD CHANGE

The constant voltage control loop and the constant current control loop are independent of each other . When a load changes suddenly, a control loop is replaced by the other.

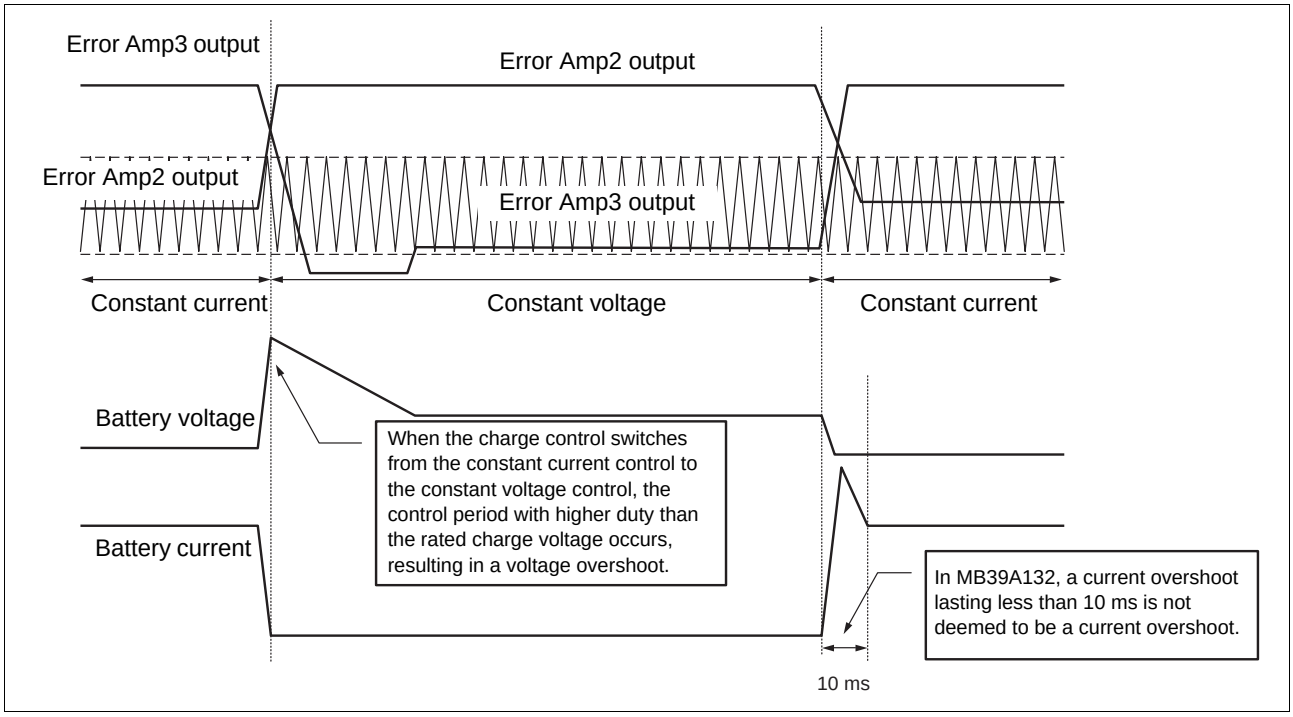
Overshoot of the battery voltage and current is generated by the delay occurring in a control loop at a mode change.

The delay time is determined by the phase compensation components values.

When the constant current control changes to the constant voltage control after the battery is removed, the control period with higher duty than the setting charge voltage occurs, resulting in a voltage overshoot. However, since the battery is removed, no excessive voltage is to be applied to the battery.

When the constant voltage control changes to the constant current control after the battery is inserted, the control period with higher duty than the rated charge current occurs, resulting in current overshoot.

In MB39A132, a current overshoot lasting less than 10 ms is not deemed to be a current overshoot.

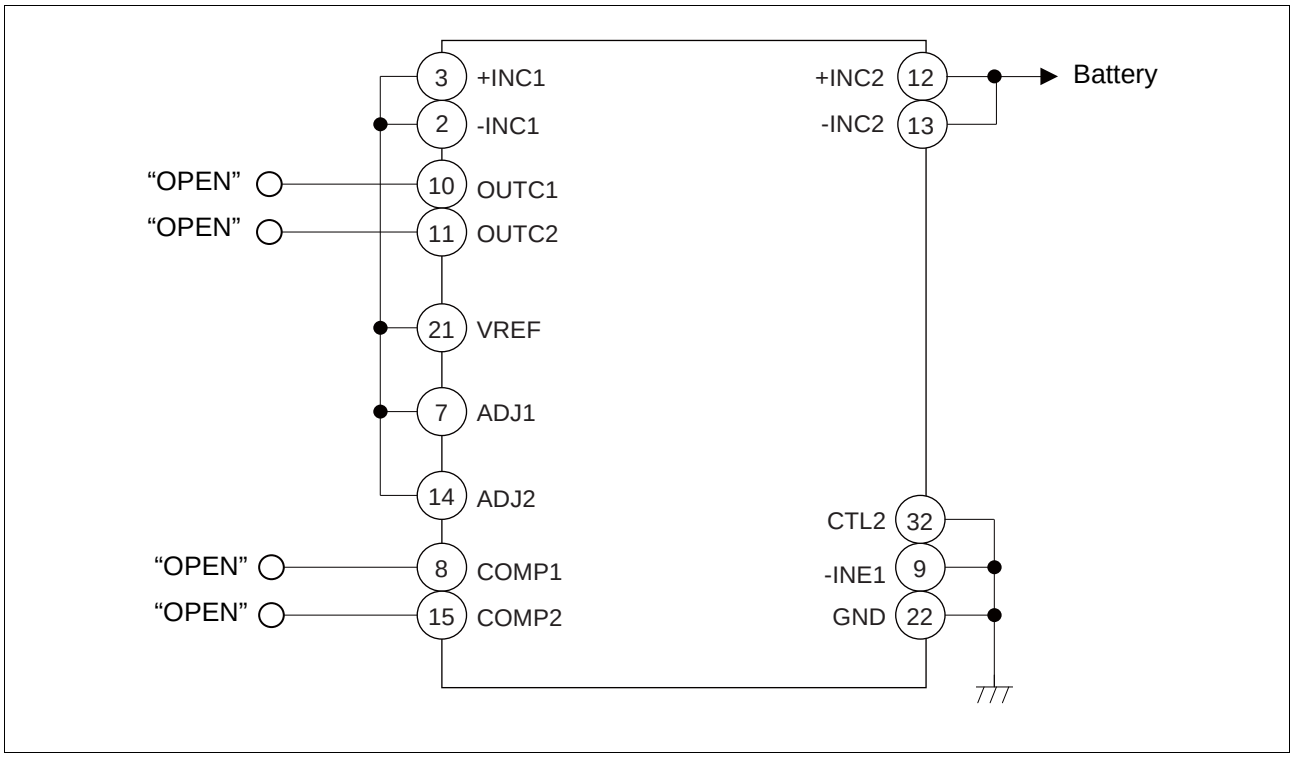


## ■ CONNECTION WITHOUT USING THE CURRENT AMP1,CURRENT AMP2 AND THE ERROR AMP1, ERROR AMP2

When Current Amp1, Current Amp2 and Error Amp1, Error Amp2 are no used,

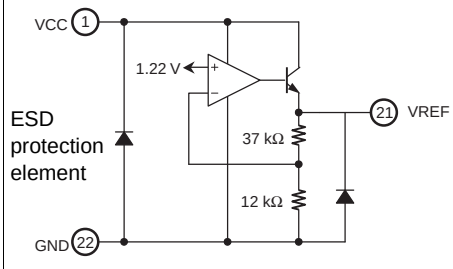
- Connect the +INC1 pin (pin 3) and the -INC1 pin (pin 2) to the VREF pin (pin 21)
- Connect the +INC2 pin (pin 12) and the -INC2 pin (pin 13) to the battery
- Leave the OUTC1 pin (pin 10), the OUTC2 pin (pin 11), the COMP1 pin (pin 8) and the COMP2 pin (pin 15) open
- Connect the ADJ1 pin (pin 7) and the ADJ2 pin (pin 14) to the VREF pin
- Connect the -INE1 pin (pin 9) to the GND pin (pin 22)

Moreover, when Current Amp1 is not used, connect the CTL2 pin (pin 32) to the GND pin (pin 22).

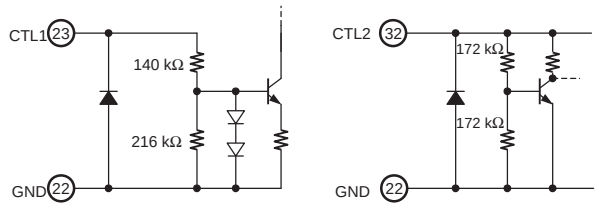


## ■ I/O EQUIVALENT CIRCUIT

<Reference voltage block>




<Control block>

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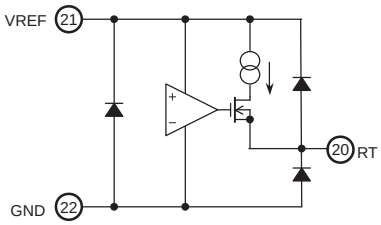


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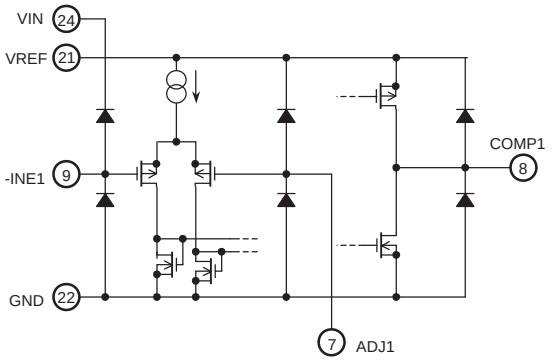


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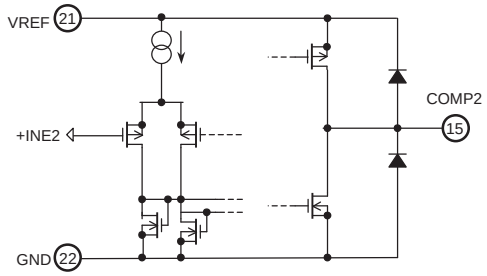


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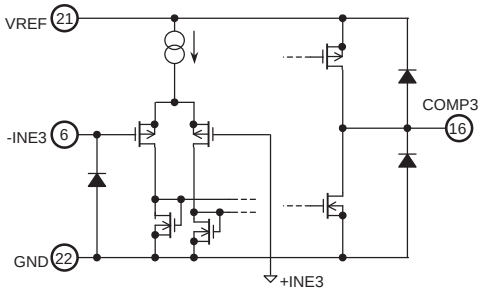


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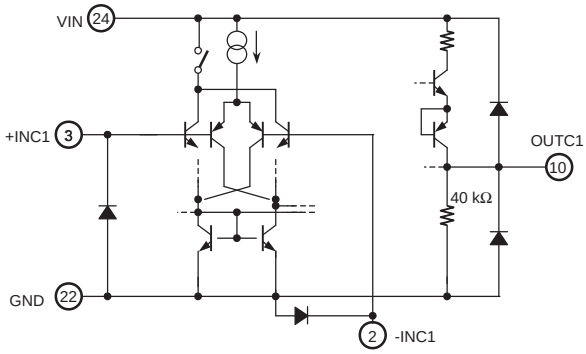


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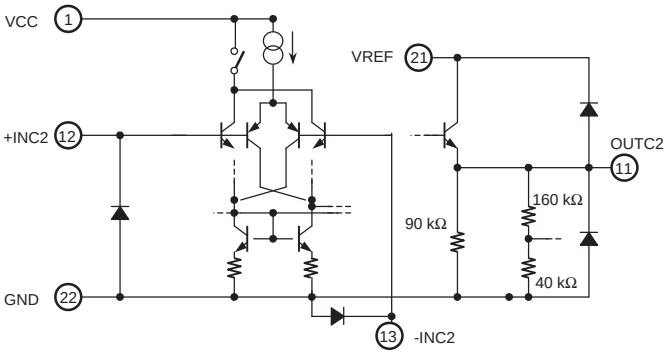


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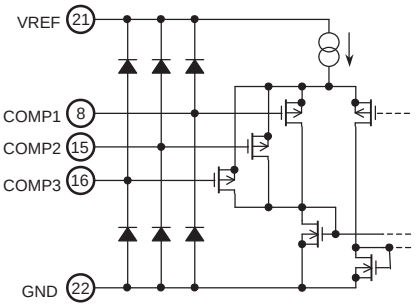
<PWM comparator block >

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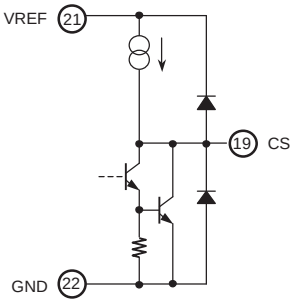


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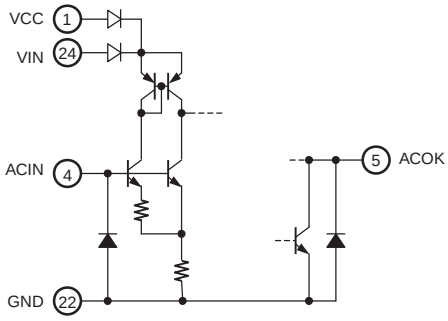


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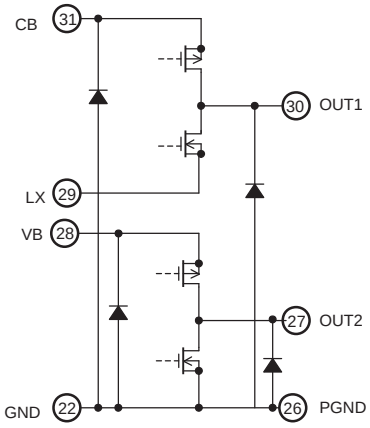
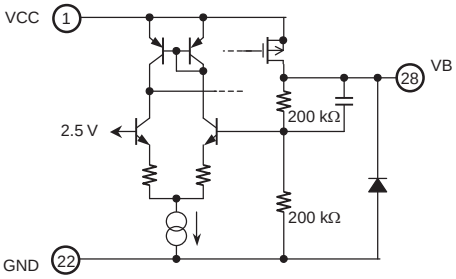



<Bias voltage block >

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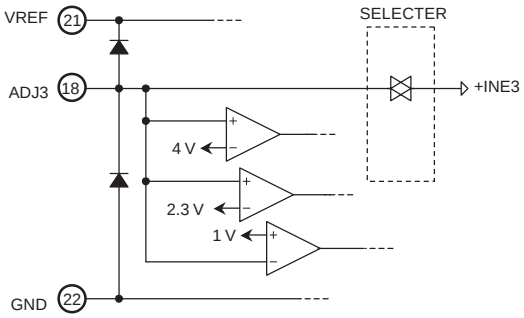


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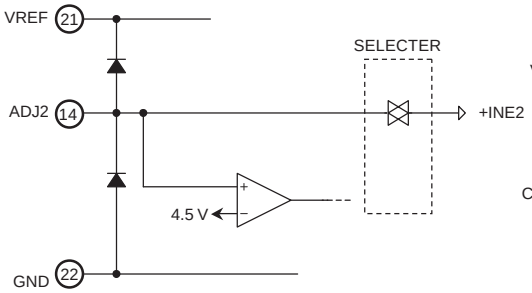
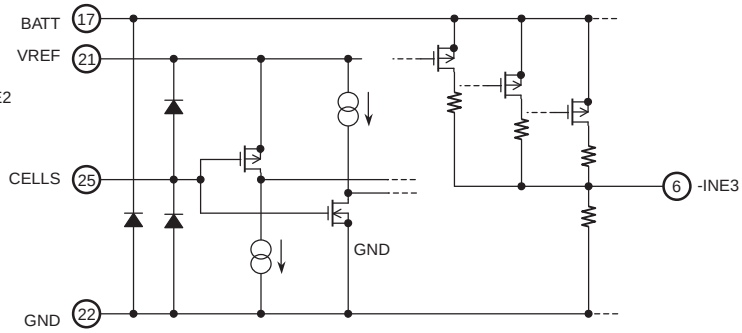
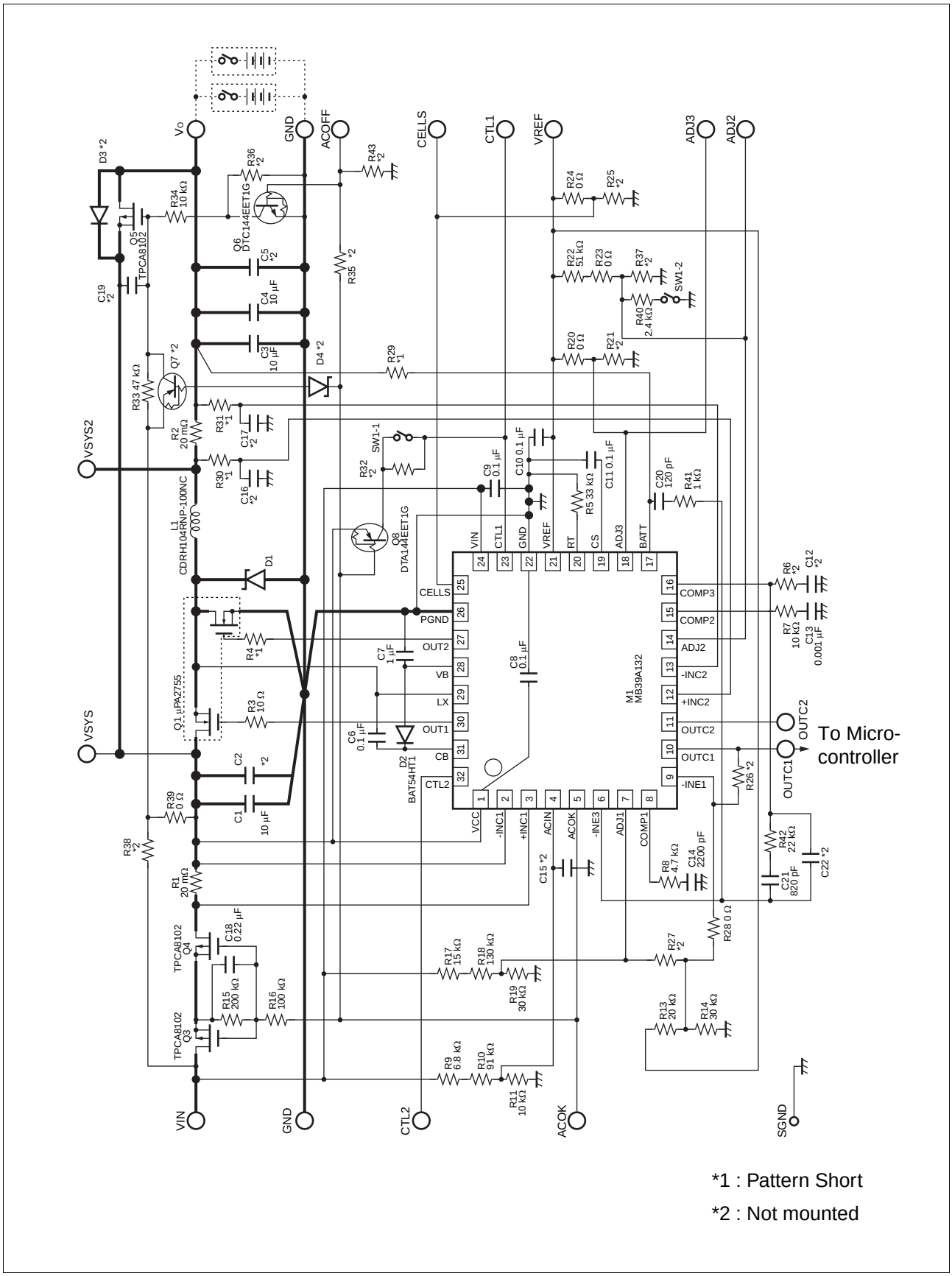



<Cell switch block >



## ■ TYPICAL APPLICATION CIRCUIT



• Parts list

| Com-ponent | Item | Specification | Vendor | Package | Part Number | Remarks |
|---|---|---|---|---|---|---|
| M1 | IC | — | FSL | QFN-32 | MB39A132 | |
| Q1 | Dual N-ch FET | VDS = − 30 V, ID = 8 A (Max) | RENESAS | SOP-8 | μPA2755 | |
| Q3 | P-ch FET | VDS = − 30 V, ID = 40 A (Max) | TOSHIBA | SOP Advance | TPCA8102 | |
| Q4 | P-ch FET | VDS = − 30 V, ID = 40 A (Max) | TOSHIBA | SOP Advance | TPCA8102 | |
| Q5 | P-ch FET | VDS = − 30 V, ID = 40 A (Max) | TOSHIBA | SOP Advance | TPCA8102 | |
| Q6 | Transistor | VCEO = 50 V | ON Semi | SC-75 | DTC144EET1G | |
| Q7 | Transistor | | | | | Not mounted |
| Q8 | Transistor | VCEO = 50 V | ON Semi | SC-75 | DTA144EET1G | |
| D1 | Diode | VF = 0.5 V at IF = 2.0 A | Fairchild | SMB | SS23 | |
| D2 | Diode | VF = 0.4 V (Max) at IF = 10 mA | ON Semi | SOD-323 | BAT54HT1 | |
| D3 | Diode | | | | | Not mounted |
| D4 | Diode | | | | | Not mounted |
| L1 | Inductor | 10 μH 35 mΩ Max Irms = 4.4 A | SUMIDA | SMD | CDRH104RNP-100NC | |
| C1 | Ceramic capacitor | 10 μF(25 V) | TDK | 3216 | C3216JB1E106K | |
| C2 | Ceramic capacitor | | | | | Not mounted |
| C3 | Ceramic capacitor | 10 μF(25 V) | TDK | 3216 | C3216JB1E106K | |
| C4 | Ceramic capacitor | 10 μF(25 V) | TDK | 3216 | C3216JB1E106K | |
| C5 | Ceramic capacitor | | | | | Not mounted |
| C6 | Ceramic capacitor | 0.1 μF(50 V) | TDK | 1608 | C1608JB1H104K | |
| C7 | Ceramic capacitor | 1 μF(16 V) | TDK | 1608 | C1608JB1C105K | |
| C9 | Ceramic capacitor | 0.1 μF(50 V) | TDK | 1608 | C1608JB1H104K | |
| C10 | Ceramic capacitor | 0.1 μF(50 V) | TDK | 1608 | C1608JB1H104K | |
| C11 | Ceramic capacitor | 0.1 μF(50 V) | TDK | 1608 | C1608JB1H104K | |
| C12 | Ceramic capacitor | | | | | Not mounted |
| C13 | Ceramic capacitor | 0.001 μF(50 V) | TDK | 1608 | C1608JB1H102K | |
| C14 | Ceramic capacitor | 2200 pF(50 V) | TDK | 1608 | C1608CH1H222J | |
| C15 | Ceramic capacitor | | | | | Not mounted |
| C16 | Ceramic capacitor | | | | | Not mounted |
| C17 | Ceramic capacitor | | | | | Not mounted |
| C18 | Ceramic capacitor | 0.22 μF(25 V) | TDK | 1608 | C1608JB1E224K | |
| C19 | Ceramic capacitor | | | | | Not mounted |
| C20 | Ceramic capacitor | 120 pF(50 V) | TDK | 1608 | C1608CH1H121J | |
| C21 | Ceramic capacitor | 820 pF(50 V) | TDK | 1608 | C1608CH1H821J | |

*(Continued)*

| Com-ponent | Item | Specification | Vendor | Package | Parts No. | Remarks |
|---|---|---|---|---|---|---|
| C22 | Ceramic capacitor | | | | | Not mounted |
| R1 | Resistor | 20 mΩ | KOA | SL1 | SL1TTE20L0D | |
| R2 | Resistor | 20 mΩ | KOA | SL1 | SL1TTE20L0D | |
| R3 | Resistor | 10 Ω | SSM | 1608 | RR0816Q-100-D | Pattern cut |
| R4 | Resistor | | | 1608 | | Pattern short |
| R5 | Resistor | 33 kΩ | SSM | 1608 | RR0816P333D | |
| R6 | Resistor | | | | | Not mounted |
| R7 | Resistor | 10 kΩ | SSM | 1608 | RR0816P103D | |
| R8 | Resistor | 4.7 kΩ | SSM | 1608 | RR0816P472D | |
| R9 | Resistor | 6.8 kΩ | SSM | 1608 | RR0816P682D | |
| R10 | Resistor | 91 kΩ | SSM | 1608 | RR0816P913D | |
| R11 | Resistor | 10 kΩ | SSM | 1608 | RR0816P103D | |
| R13 | Resistor | 20 kΩ | SSM | 1608 | RR0816P203D | |
| R14 | Resistor | 30 kΩ | SSM | 1608 | RR0816P303D | |
| R15 | Resistor | 200 kΩ | SSM | 1608 | RR0816P204D | |
| R16 | Resistor | 100 kΩ | SSM | 1608 | RR0816P104D | |
| R17 | Resistor | 15 kΩ | SSM | 1608 | RR0816P153D | |
| R18 | Resistor | 130 kΩ | SSM | 1608 | RR0816P134D | |
| R19 | Resistor | 30 kΩ | SSM | 1608 | RR0816P303D | |
| R20 | Resistor | 0 Ω | KOA | 1608 | RK73Z1J | |
| R21 | Resistor | | | | | Not mounted |
| R22 | Resistor | 51 kΩ | SSM | 1608 | RR0816P513D | |
| R23 | Resistor | 0 Ω | KOA | 1608 | RK73Z1J | |
| R24 | Resistor | 0 Ω | KOA | 1608 | RK73Z1J | |
| R25 | Resistor | | | | | Not mounted |
| R26 | Resistor | | | | | Not mounted |
| R27 | Resistor | | | | | Not mounted |
| R28 | Resistor | 0 Ω | KOA | 1608 | RK73Z1J | |
| R29 | Resistor | | | 1608 | | Pattern short |
| R30 | Resistor | | | 1608 | | Pattern short |
| R31 | Resistor | | | 1608 | | Pattern short |
| R32 | Resistor | | | | | Not mounted |
| R33 | Resistor | 47 kΩ | SSM | 1608 | RR0816P473D | |
| R34 | Resistor | 10 kΩ | SSM | 1608 | RR0816P103D | |
| R35 | Resistor | | | | | Not mounted |
| R36 | Resistor | | | | | Not mounted |
| R37 | Resistor | | | | | Not mounted |

*(Continued)*

*(Continued)*

| Com-ponent | Item | Specification | Vendor | Package | Parts No. | Remarks |
|---|---|---|---|---|---|---|
| R38 | Resistor | | | | | Not mounted |
| R39 | Resistor | 0 Ω | KOA | 1608 | RK73Z1J | |
| R40 | Resistor | 2.4 kΩ | SSM | 1608 | RR0816P242D | |
| R41 | Resistor | 1 kΩ | SSM | 1608 | RR0816P102D | |
| R42 | Resistor | 22 kΩ | SSM | 1608 | RR0816P223D | |
| R43 | Resistor | | | | | Not mounted |

FSL : Fujitsu Semiconductor Limited
RENESAS : Renesas Electronics Corporation
TOSHIBA : TOSHIBA Corporation
ON Semi : ON Semiconductor
SUMIDA : SUMIDA Corporation
TDK : TDK Corporation
KOA : KOA Corporation
SSM : SUSUMU Co.,Ltd.
Fairchild : Fairchild Semiconductor International, Inc.

## ■ APPLICATION NOTE

- Inductor selection

As a rough guide, the inductance of an inductor should keep the peak-to-peak value of inductor ripple current below 50% of the maximum charge current. The inductance fulfilling the above condition can be found by the following formula.

$$L \geq \frac{V_{IN} - V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

L : Inductance [H]
$I_{OMAX}$ : Maximum charge current [A]
LOR : Inductor ripple current peak to peak value - Maximum charge current ratio (0.5)
$V_{IN}$ : Switching power-supply voltage [V]
$V_O$ : Charge voltage [V]
$f_{OSC}$ : Switching frequency [Hz]

The minimum charge current (critical current) in the condition that inductor current does not flow in reverse can be found by the following formula.

$$I_{OC} = \frac{V_O}{2 \times L} \times \frac{V_{IN} - V_O}{V_{IN} \times f_{OSC}}$$

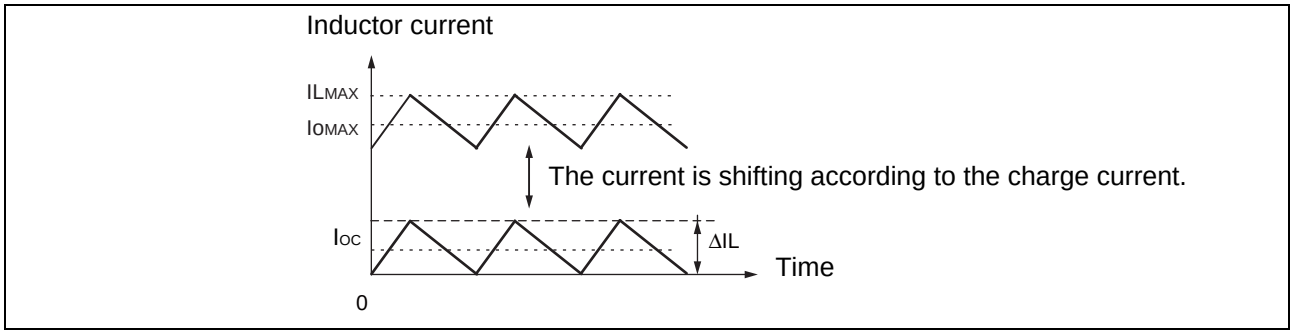
$I_{OC}$ : Critical current [A]
L : Inductance [H]
$V_{IN}$ : Switching power-supply voltage [V]
$V_O$ : Charge voltage [V]
$f_{OSC}$ : Switching frequency [Hz]

The maximum value of the current flowing through the inductor needs to be found in order to determine whether the current flowing through the inductor is within the rated value. The maximum current flowing through the inductor can be found by the following formula.

$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$I_{LMAX}$ : Maximum inductor current [A]
$I_{OMAX}$ : Maximum charge current [A]
$\Delta IL$ : Inductor ripple current peak to peak value [A]

$$\Delta IL \geq \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$



• SWFET selection

If MB39A132 is used for the charger for a notebook PC, since the output voltage of an AC adapter, which is the input voltage of an SWFET, is 25 V or less, in general, a 30 V class MOS FET can be used as the SWFET. Obtain the maximum value of the current flowing through the SWFET in order to determine whether the current flowing through the SWFET is within the rated value. The maximum current flowing through the SWFET can be found by the following formula.

$$I_{DMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$I_{DMAX}$ : Maximum SWFET drain current [A]

$I_{OMAX}$ : Maximum charge current [A]

$\Delta IL$ : Inductor ripple current peak to peak value [A]

In addition, find the loss of the SWFET in order to determine whether the allowable loss of the SWFET is within the rated value. The allowable loss of the high-side of FET can be found by the following formula.

$$P_{HisideFET} = P_{RON\_Hiside} + P_{SW\_Hiside}$$

$P_{HisideFET}$ : FET loss of high-side [W]

$P_{RON\_Hiside}$: FET continuity loss of high-side [W]

$P_{SW\_Hiside}$ : FET switching loss of high-side [W]

FET continuity loss of high-side

$$P_{RON\_Hiside} = I_{OMAX}^2 \times \frac{V_O}{V_{IN}} \times R_{ON\_Hiside}$$

$P_{RON\_Hiside}$: FET continuity loss of high-side [W]

$I_{OMAX}$ : Maximum charge current [A]

$V_{IN}$ : Switching power supply voltage [V]

$V_O$ : Output voltage [V]

$R_{ON\_Hiside}$ : FET ON resistance of high-side [Ω]

FET switching loss of high-side

$$P_{SW\_Hiside} = \frac{V_{IN} \times f_{OSC} \times (Ibtm \times Tr + Itop \times Tf)}{2}$$

$P_{SW\_Hiside}$ : FET switching loss of high-side [W]

$V_{IN}$ : Switching power supply voltage [V]

$f_{OSC}$ : Switching frequency (Hz)

Ibtm : Bottom value of ripple current of inductor [A]

$$Ibtm = I_{OMAX} - \frac{\Delta IL}{2}$$

Itop : Top value of ripple current of inductor [A]

$$Itop = I_{OMAX} - \frac{\Delta IL}{2}$$

ΔIL : Inductor ripple current peak to peak value [A]
Tr : FET turn-on time of high-side [s]
Tf : FET turn-off time of high-side [s]

Tr and Tf can be easily found by the following formula.

$$Tr = \frac{Qgd \times 4}{5 - Vgs(on)} \qquad Tf = \frac{Qgd \times 1}{Vgs(on)}$$

Qgd : Gate-Drain charge of high-side FET [C]
Vgs(on) : Gate-Source voltage of high-side FET with Qgd [V]

The FET loss of the low-side can be found by the following formula.

$$P_{LosideFET} = P_{RON\_Loside} = I_{OMAX}^2 \times (1 - \frac{V_O}{V_{IN}}) \times R_{on\_Loside}$$

$P_{LosideFET}$ : FET loss of low-side [W]
$P_{RON\_Loside}$ : FET continuity loss of low-side [W]
$I_{OMAX}$ : Maximum charge current [A]
$V_{IN}$ : Switching power supply voltage [V]
$V_O$ : Output voltage [V]
$R_{on\_Loside}$ : FET ON resistance of synchronous rectification [Ω]

The FET voltage transiting between drain-source of the low-side is generally small. The SWFET loss is omitted in this document as it is negligible.

Since the power for driving gate of SWFET is supplied by LDO in IC, the SWFET allowable maximum total gate charge (QgTotalMax) is determined by the following formula.

$$QgTotalMax \leq \frac{0.03}{f_{OSC}}$$

QgTotalMax : High-side FET allowable maximum total charge [C]
$f_{OSC}$ : Oscillation frequency [Hz]

• Fly-back diode selection

The DC/DC converter control IC needs a fly-back diode.

Select a Schottky barrier diode (SBD) that has a small forward voltage drop.

The current rating value for the fly-back diode can be calculated by the following formula.

$$I_F \geq I_{OMAX} \times (1 - \frac{Vo}{V_{IN}})$$

$I_F$ : Current rating value of fly-back diode [A]

$I_{OMAX}$ : Maximum charge current [A]

$V_{IN}$ : Switching power supply voltage [V]

Vo : Charge voltage [V]

The rating of a fly-back diode can be found by the following formula.

$V_{R\_Fly} > V_{IN}$

$V_{R\_Fly}$ : DC reverse voltage of fly-back diode [V]

$V_{IN}$ : Switching power supply voltage [V]

- Output capacitor selection

Since a high ESR causes the output ripple voltage to increase, a low-ESR capacitor is needs to be used in order to reduce the output ripple voltage. Use a capacitor that has sufficient ratings to surge current generated when the battery is inserted or removed. Generally, the ceramic capacitor is used as the output capacitor.

With the switching ripple voltage taken into consideration, the minimum capacitance required can be found by the following formula.

$$Co \geq \frac{1}{2\pi \times fosc \times (\Delta V_O/\Delta IL - ESR)}$$

Co : Output capacitance [F]

ESR : Series resistance element of output capacitance [Ω]

$\Delta V_O$ : Switching ripple voltage [V]

$\Delta IL$ : Inductor ripple current peak to peak value [A]

fosc : Switching frequency [Hz]

Since an overshoot occurs in the DC/DC converter output voltage when a battery being charged is removed, use a capacitor having sufficient withstand voltage. Generally, the capacitor having a rated withstand voltage higher than the maximum input voltage is sued.

Moreover, use a capacitor having sufficient tolerance for allowable ripple current. The allowable ripple current required can be found by the following formula.

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

Irms : Allowable ripple current (Root-mean-square value) [A]

$\Delta IL$ : Inductor ripple current peak-to-peak value [A]

• Input capacitor selection

Select an input capacitor that has an ESR as small as possible. A ceramic capacitor is ideal. If a high-capacitance capacitor is needed for which there is no suitable ceramic capacitor use a polymer capacitor or a tantalum capacitor having a low ESR.
The ripple voltage by the switching operation of the DC/DC converter is generated in the power supply voltage. Please consider the lower limit value of the input capacitor according to the allowable ripple voltage. The ripple voltage of the power supply can be easily found by the following formula.

$$\Delta V_{IN} = \frac{I_{OMAX}}{C_{IN}} \times \frac{V_O}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OMAX} + \frac{\Delta IL}{2}\right)$$

$\Delta V_{IN}$ : Switching power supply ripple voltage peak-to-peak value [V]

$I_{OMAX}$ : Maximum charge current [A]

$C_{IN}$ : Input capacitance [F]

$V_{IN}$ : Switching power supply voltage [V]

$V_O$ : Charge voltage [V]

$f_{OSC}$ : Switching frequency [Hz]

ESR : Series resistance element of input capacitance [Ω]

$\Delta IL$ : Inductor ripple current peak-to-peak value [A]

The ripple voltage of the power supply can be decreased by raising the switching frequency besides using the capacitor.
The capacitor has its own frequency, temperature and bias voltage, therefore its effective capacitance can be extremely small depending on the application conditions.

Select a capacitor whose rating has a sufficient margin against input voltage.
In addition, when using a capacitor having an allowable ripple current rating, select a capacitor that has a sufficient margin against ripple current.

The allowable ripple current can be found by the following formula.

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}}$$

Irms : Allowable ripple current (Root-mean-square value) [A]

$I_{OMAX}$ : Maximum charge current [A]

$V_{IN}$ : Switching power supply voltage [V]

$V_O$ : Charge voltage [V]

• Bootstrap diode selection

Select a Schottky barrier diode (SBD) that has a small forward voltage drop.
The current to drive the gate of High-side FET flows to the SBD of the bootstrap circuit. The average current can be found by the following formula. Select a bootstrap diode that keep the average current below the current rating.

$I_D \geq Qg \times f_{OSC}$

$I_D$ : Forward current [A]

Qg : FET total gate electric charge of high-side [C]

$f_{OSC}$ : Oscillation frequency [Hz]

The rating of the bootstrap diode can be found by the following formula.

$V_{R\_BOOT} > V_{IN}$

$V_{R\_BOOT}$ : Bootstrap diode DC reverse voltage [V]

$V_{IN}$ : Switching power supply voltage [V]

• Bootstrap capacitor selection

The bootstrap capacitor needs to be sufficiently charged to drive the gate of the high-side FET. Therefore, select a capacitor that can store charge at least 10 times Qg of the high-side FET as the bootstrap capacitor.

$$C_{BOOT} \geq 10 \times \frac{Qg}{V_B}$$

$C_{BOOT}$: Bootstrap capacitance [F]

Qg : Withstand voltage FET gate charge [C]

$V_B$ : VB voltage [V]

The rating of bootstrap capacitor can be found by the following formula.

$V_{CBOOT} > V_{IN}$

$V_{CBOOT}$ : Rating of bootstrap capacitor [V]

$V_{IN}$ : Switching power supply voltage [V]

• VB capacitor

Although the typical capacitance value for a VB capacitor is 1 μF, it has to be adjusted if the switching FET used has a large Qg. The bootstrap capacitor needs to be sufficiently charged to drive the gate of the high-side FET. Therefore, select a capacitor that can store charge at least 100 times the total of Qg of the high-side FET and Qg of the low-side switching FET as the VB capacitor.

$$C_{VB} \geq 100 \times \frac{Qg}{V_B}$$

$C_{VB}$ : VB pin capacitance [F]

Qg : Total gate charge of high-side FET and low-side switching FET [C]

VB : VB voltage [V]

The rating of VB capacitor can be found by the formula.

$V_{CVB} > V_B$

$V_{CVB}$ : Withstand voltage of VB capacitor [V]

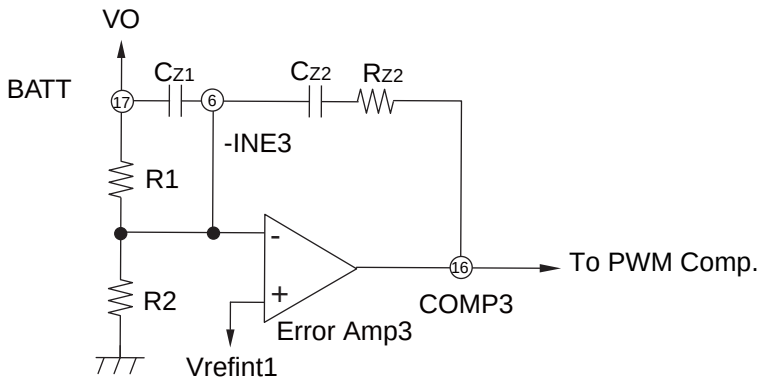
$V_B$ :VB voltage [V]

• Design of phase compensation circuit

(1) Constant voltage (CV) mode phase compensation circuit

When a low-ESR capacitor, such as a ceramic capacitor, is used as the output capacitor, it is easier for the DC/DC converter to oscillate as the phase delay approaches 180 degrees due to the resonance frequency of LC. In this situation, perform phase compensation by connecting a RC phase lead compensator between the -INE3 pin (pin 6) and the COMP3 pin (pin 16), and between the -INE3 pin (pin 6) and the BATT pin (pin 17) .

2pole-2zero phase compensation circuit




The constant for the phase lead compensation circuit can be found by the following formula.

$$C_{Z1} \fallingdotseq \frac{5.1 \times 10^{-6}}{(2 \times CELLS - 1)\, f_{LC}}$$

$$R_{Z2} \fallingdotseq 8.9 \times 10^{4} \times \frac{f_{CO}}{V_{IN} \times f_{LC}} + 3600$$

$$C_{Z2} \fallingdotseq \frac{1}{2\pi \times R_{Z2} \times f_{LC}}$$

CELLS : Number of battery series cells

$f_{LC}$ : Resonance frequency of inductor and output capacitor [Hz]

$V_{IN}$ : Switching power supply voltage [V]

$f_{CO}$ : Crossover frequency [Hz]

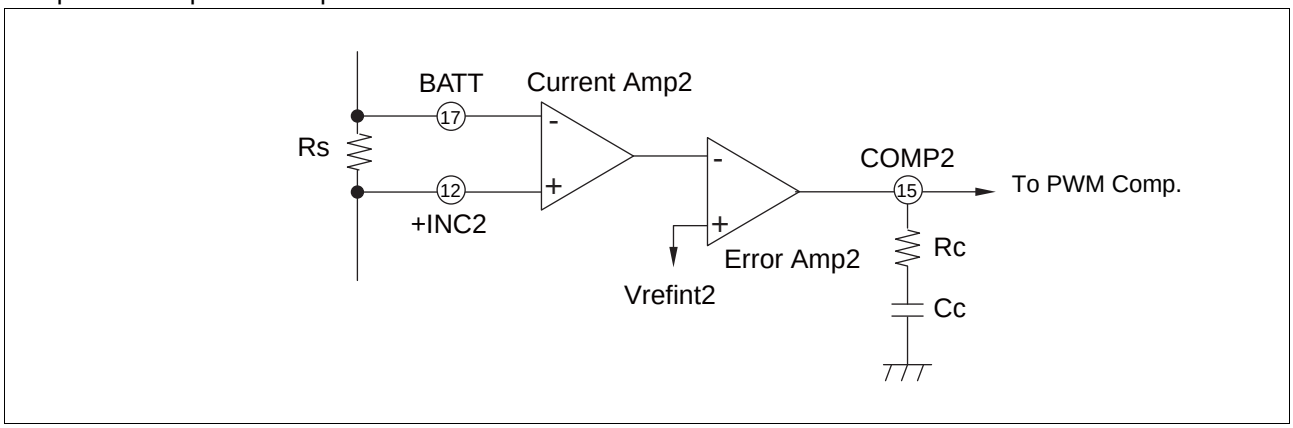
As for the crossover frequency (fco) indicating the bandwidth of the control loop of the DC/DC converter, while a high crossover frequency is good for quick response, it increases the risk of oscillation due to an insufficient phase margin.

Though this crossover frequency can be freely set, keep the frequency in the range of 1/10-1/5 of the switching frequency (fosc) whenever possible.

(2) Constant current (CC) mode phase compensation circuit

In constant current mode, since the output capacitor impedance has little effects on the loop response characteristic, connect the 1pole-1zero phase compensation circuit with the output pin (COMP2) of the error amplifier 2 (gm amplifier).

1pole-1zero phase compensation circuit




RC and Cc of the phase lead circuit can be found by the following formula.

$$Rc \fallingdotseq 1.2 \times 10^4 \times \frac{f_{CO} \times L}{Rs \times V_{IN}}$$

$$Cc \fallingdotseq \frac{\sqrt{L \times Co}}{Rc}$$

Rs : Charge current detection resistance [Ω]

$V_{IN}$ : Switching power supply voltage [V]

L : Inductor value [H]

Co : Output capacitance [F]

$f_{CO}$ : Crossover frequency [Hz]

- Allowable loss, and thermal design

In general, the allowable loss and thermal design of this IC can be ignored because this IC is highly effective. However, when this IC is used with high power supply voltage, high switching frequency, high load, or high temperature, it is necessary to take account of the allowable loss and thermal design while using this IC.

The IC internal loss (PIC) can be found by the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Qg \times f_{OSC})$$

$P_{IC}$ : IC internal loss [W]

$V_{CC}$ : Power supply voltage ($V_{IN}$) [V]

$I_{CC}$ : Power supply current [A] (3.6 mA Max)

$Qg$ : Total charge of all switching FET [C] (Total charge at Vgs = 5 V)

$f_{OSC}$ : Switching frequency [Hz]

The junction temperature (Tj) can be found by the following formula.

$$Tj = Ta + \theta ja \times P_{IC}$$

$Tj$ : Junction temperature [ °C]

$Ta$ : Ambient temperature [ °C]

$\theta ja$ : QFN-32 package heat resistance (22.7 °C/W)

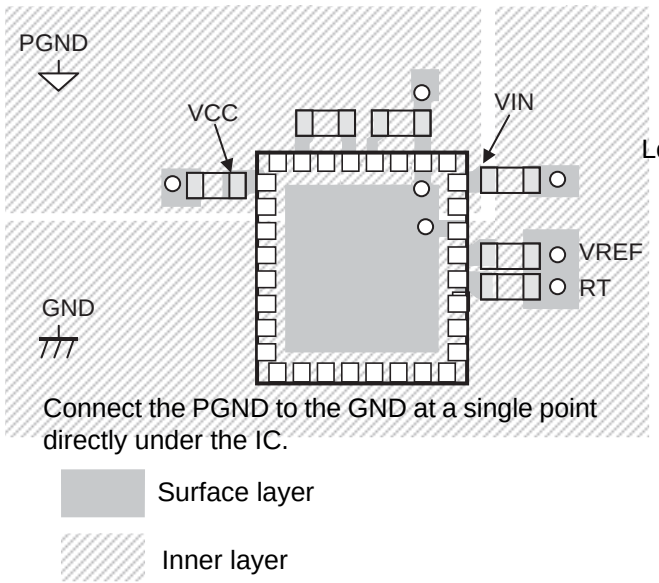
$P_{IC}$ : IC internal loss [W]

• Board layout

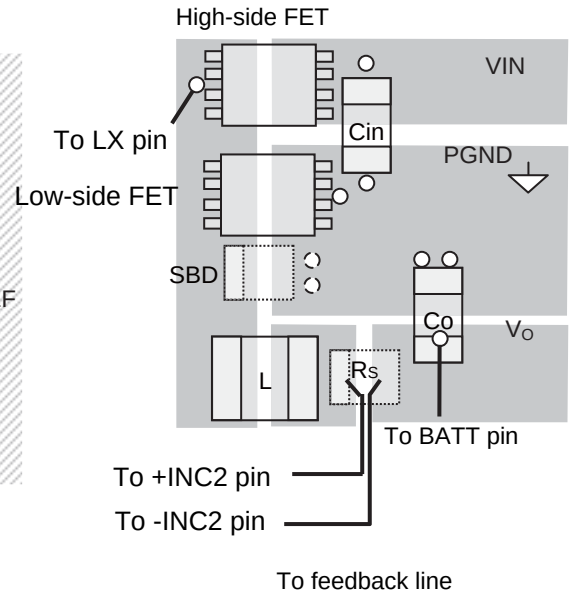
When designing the layout, consider the points listed below. Take account of the following points when designing the board layout.

- Place a GND plane on the IC mounting surface whenever possible. Connect bypass capacitors connected to switching components to the switching GND (PGND pin), and controller components to GND (GND pin). Separate different GND so that no large current path passes through the controller GND (GND pins). When designing the connection of the controller GND and the switching GND, make their connection underneath the IC. Connect PGND to the controller GND at only one point to prevent large current from flowing to the controller GND. Connect the controller GND to PGND only at one point of PGND in order to prevent a large current path from passing the controller GND.
- Connect to the input capacitor ($C_{IN}$), SWFET, SBD, inductor (L), sense resistor (Rs), output capacitor (Co) on the surface layer. Do not connect to them via any through-hole.
- For a loop composed of input capacitors (CIN), switching FET and SBD, minimize its current loop. When minimizing routing and loops, give priority to this loop over others.
- Create through-holes directly next to the GND pins of the input capacitor (CIN), SBD, output capacitor (Co), and connect these pins to the GND of the inner layer.
- Place the boot strap capacitor (CBOOT) as close to the CB, LX pins as possible.
- Place the input capacitor ($C_{IN}$) and high-side FET as close together as possible. Bring out the net of the LX pin from a point close to the source pin of the high-side FET. Large currents momentarily flow through the net of the LX pin. Use a wiring width of about 0.8 mm, and minimize the length of routing.
- Large currents momentarily flow through the nets of the OUT1, OUT2 pins, which are connected to the switching FET gate. Use a wiring width of about 0.8 mm and minimize the length of routing.
- Place the bypass capacitor connected to VCC, VIN, VREF, and VB pins, and the resistance connected to the RT pin as close to the respective pins as possible. Moreover, connect the bypass capacitor and the GND pin of the $f_{OSC}$:setting resistance in close proximity to the GND pin of the IC.
  (Strengthen the connection to the internal layer GND by making through-holes in close proximity to each of the GND pin of the IC, terminals of bypass capacitors, terminals of the fosc setting resistors.)
- -INCx,+INCx, BATT,COMPx,RT pins is sensitive to noise. Therefore, minimize the routing of these pins and keep them as far away from switching components as possible.
- The remote sensing (Kelvin connection) of the routing of the -INC2 and +INC2 pins are very sensitive to noise. Therefore, make their routing close to each other and keep the routing as far away from switching components as possible.

GND routing example



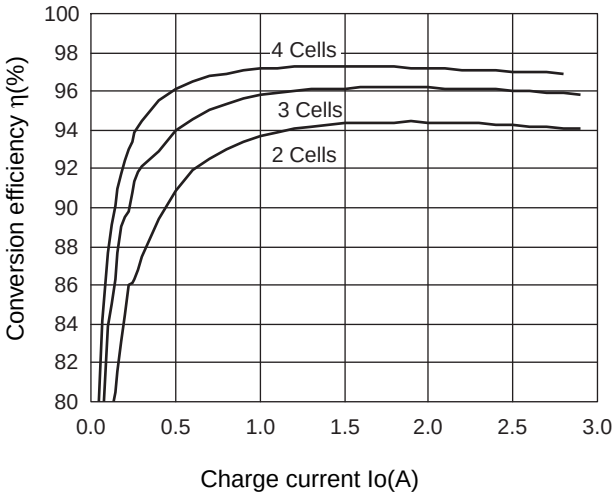

Example of switching components



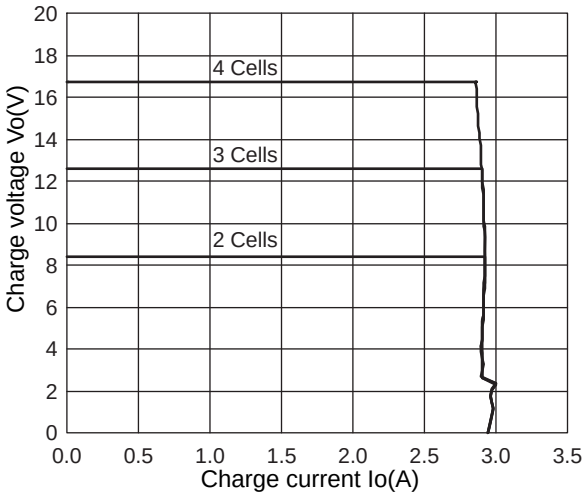
## ■ REFERENCE DATA

Unless otherwise specified, the measurement conditions are $V_{IN}$ = 19 V, Io = 2.85 A, Li+ battery 4 Cells, and Ta = + 25 °C.

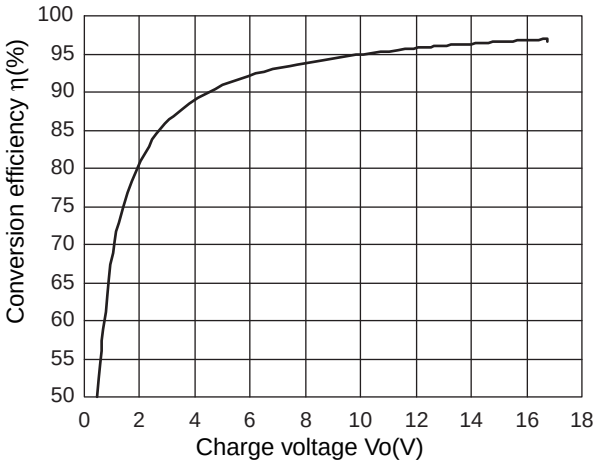
Conversion efficiency - Charge current
(Constant voltage mode)



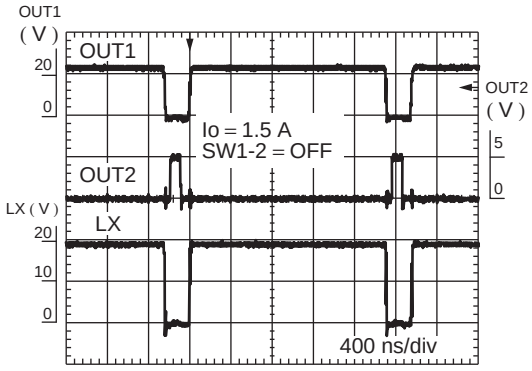

Charge voltage - Charge current



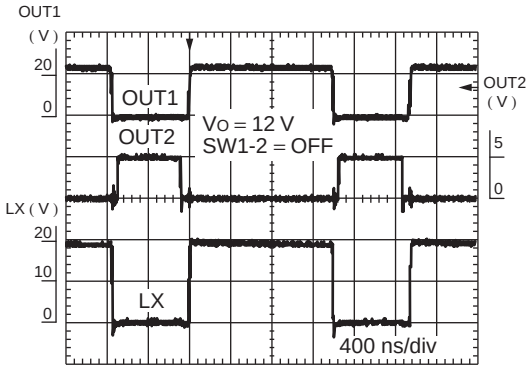

Conversion efficiency - Charge voltage
(Constant current mode)




Switching waveform
(Constant voltage mode)

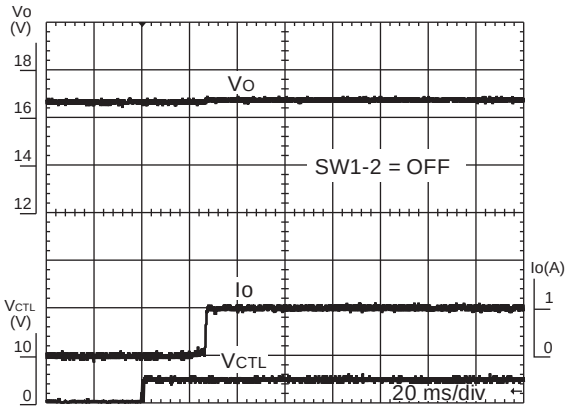



Switching waveform
(Constant current mode)

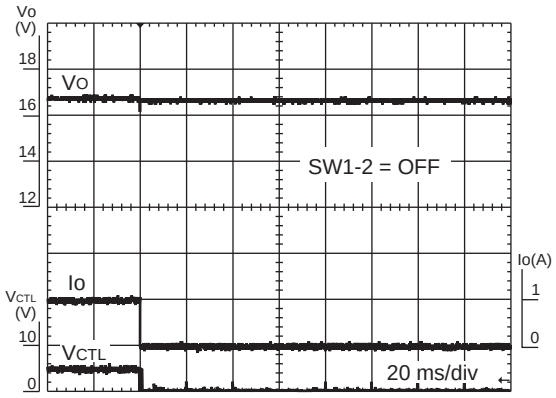



*(Continued)*

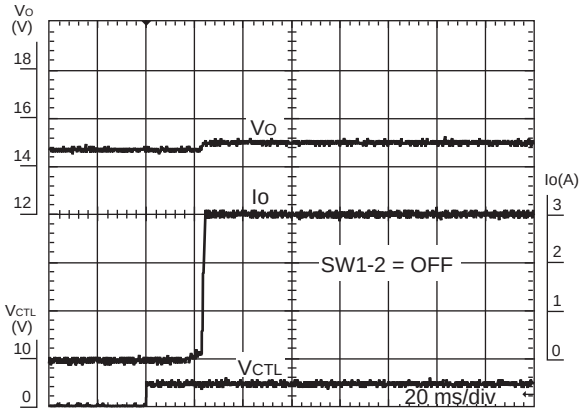
Start and stop
(Constant voltage mode)



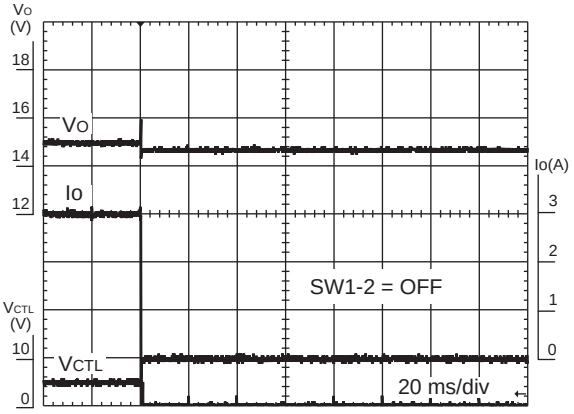

Start and stop
(Constant voltage mode)




Start and stop
(Constant current mode)




Start and stop
(Constant current mode)

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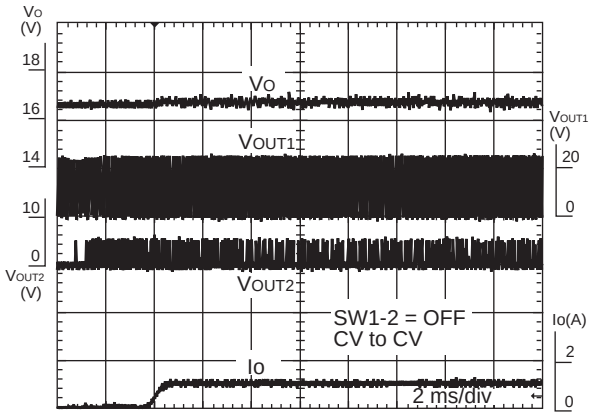
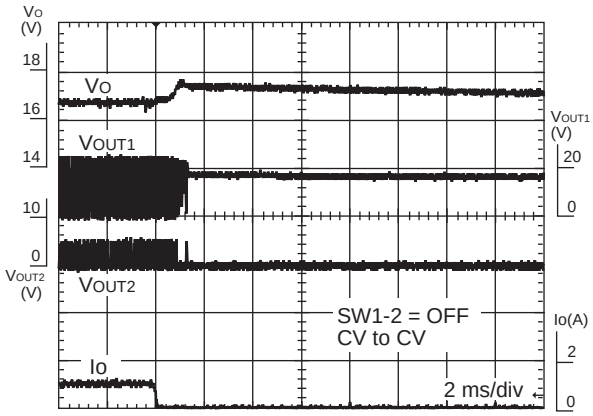
*(Continued)*

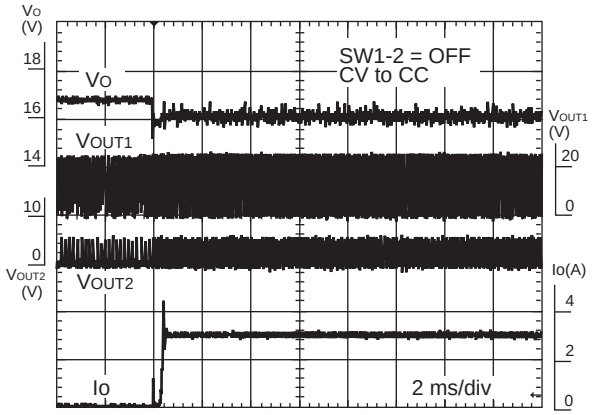
Load-step response
(Constant voltage mode)
Battery insertion



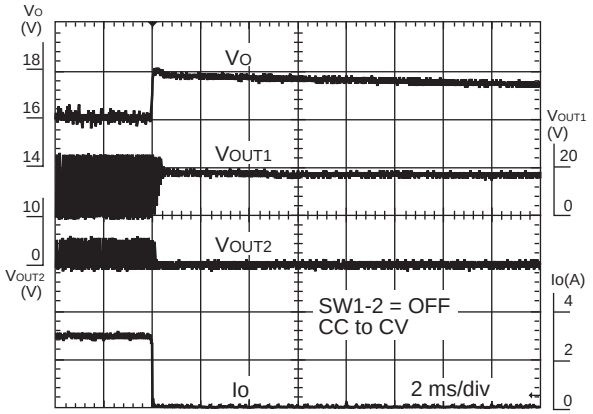

Load-step response
(Constant voltage mode)
Battery removal




Load-step response
(Constant current mode)
Battery insertion




Load-step response
(Constant current mode)
Battery removal



## ■ USAGE PRECAUTION

### 1. Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to be normally operated within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

### 2. Use the devices within recommended operating conditions

The recommended operating conditions are the recommended values that guarantee the normal operations of LSI.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

### 3. Printed circuit board ground lines should be set up with consideration for common impedance

### 4. Take appropriate measures against static electricity

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in series between body and ground.

### 5. Do not apply negative voltages

The use of negative voltages below –0.3 V may cause the parasitic transistor to be activated on LSI lines, which can cause malfunctions.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB39A132WQN | 32-pin plastic QFN<br>(LCC-32P-M19) | |

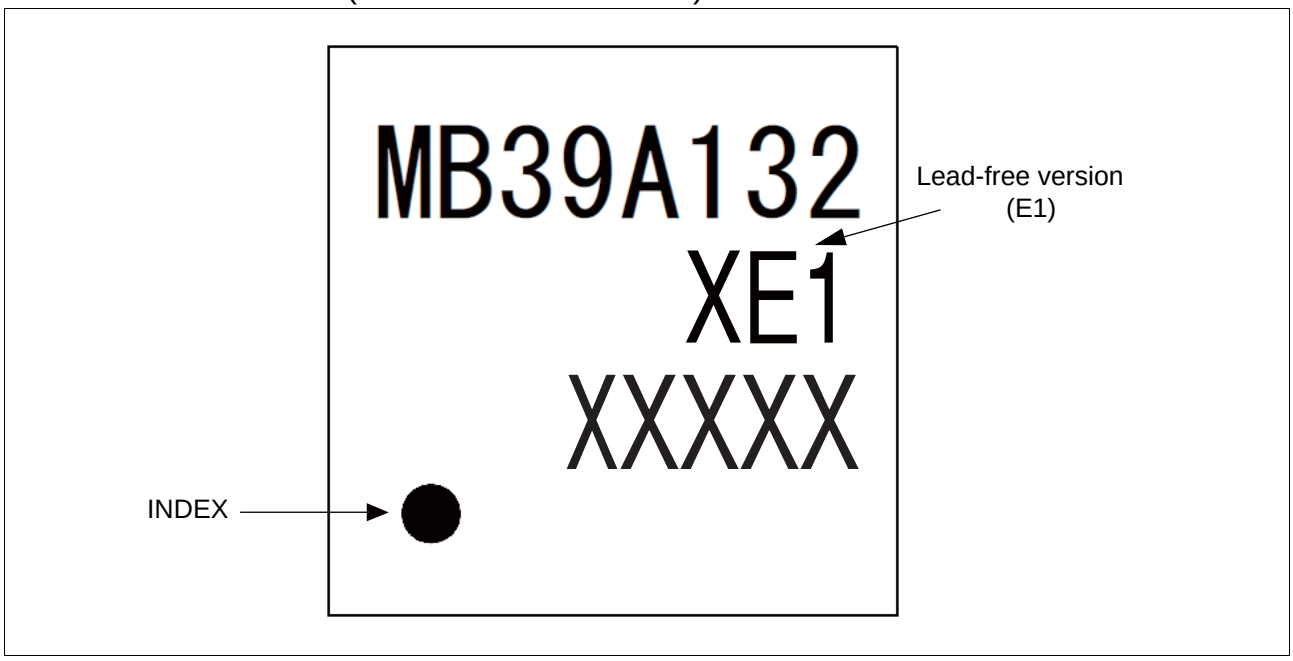
## ■ EV BOARD ORDERING INFORMATION

| EV board part No. | EV board version No. | Remarks |
|---|---|---|
| MB39A132EVB-02 | Board rev.2.0 | QFN-32 |

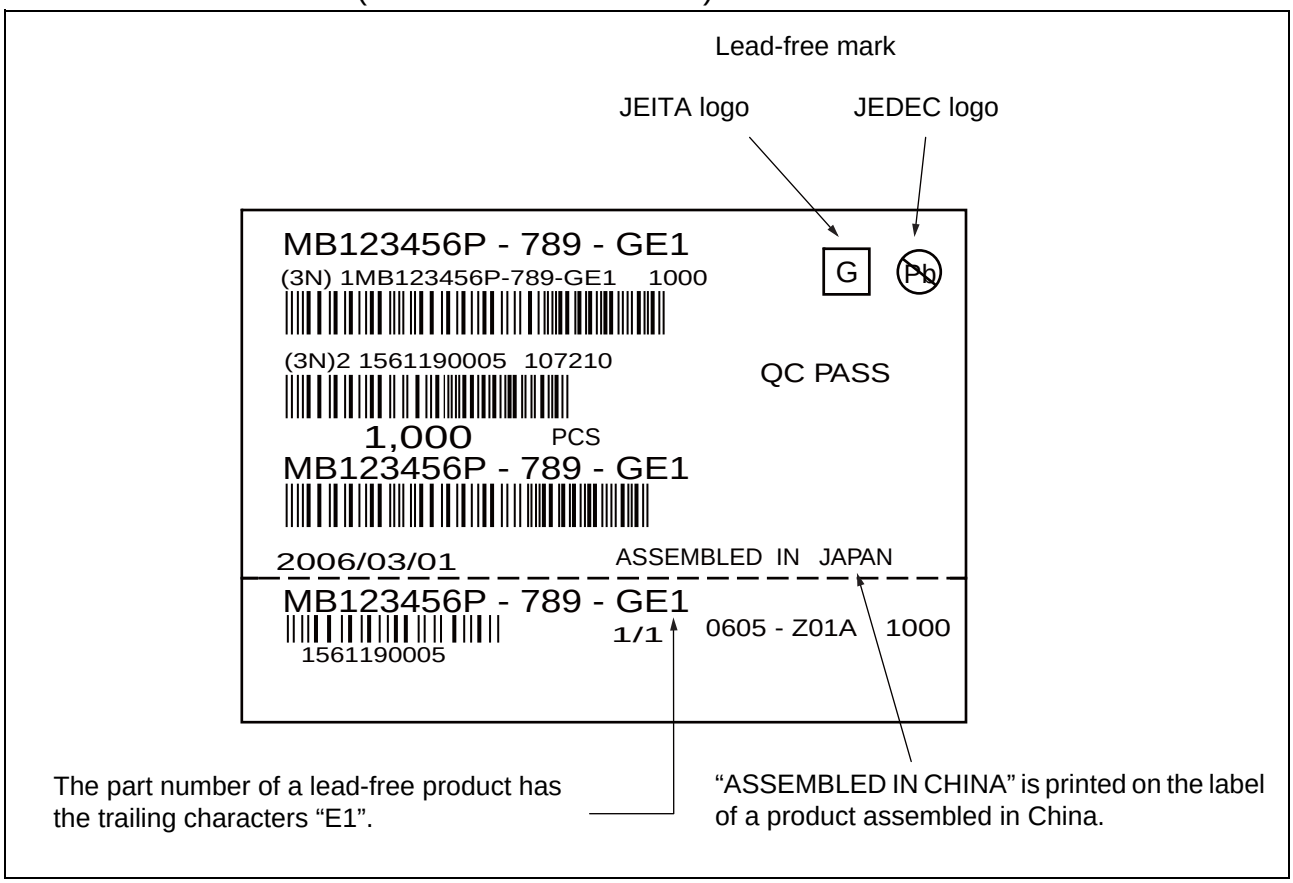
## ■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of FUJITSU SEMICONDUCTOR with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .
A products whose part number has trailing characters “E1” is RoHS compliant.

## ■ MARKING FORMAT (LEAD-FREE VERSION)




## ■ LABELING SAMPLE (LEAD-FREE VERSION)



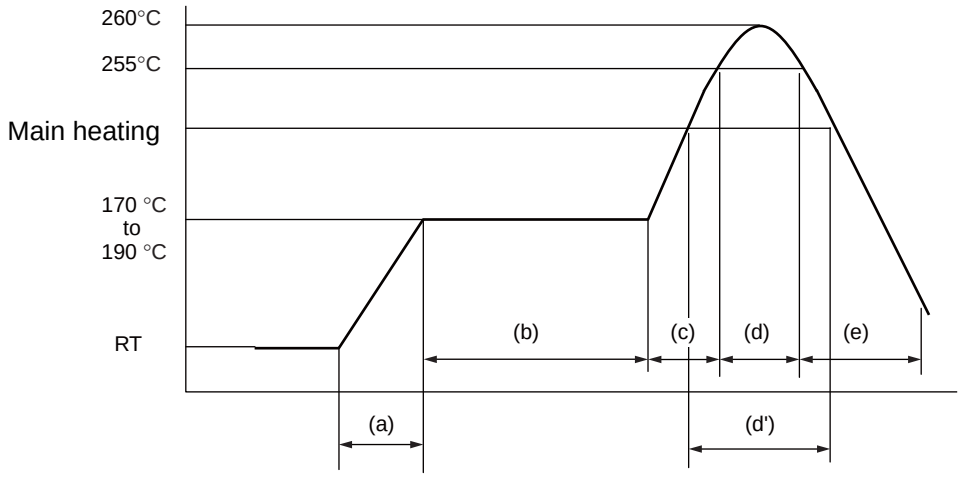
## ■ MB39A132WQN RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

**[Fujitsu Semiconductor Recommended Mounting Conditions]**

| Item | Condition | |
|---|---|---|
| Mounting Method | IR (infrared reflow) , Manual soldering (partial heating method) | |
| Mounting times | 2 times | |
| Storage period | Before opening | Please use it within two years after Manufacture. |
| | From opening to the 2nd reflow | Less than 8 days |
| | When the storage period after opening was exceeded | Please process within 8 days after baking (125 °C, 24H) |
| Storage conditions | 5 °C to 30 °C, 70%RH or less (the lowest possible humidity) | |

**[Mounting Conditions]**

**(1) IR (infrared reflow)**




"H" level : 260 °C Max
(a) Temperature increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature increase gradient : Average 1 °C/s to 4 °C/s
(d) Peak temperature : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') Main heating : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

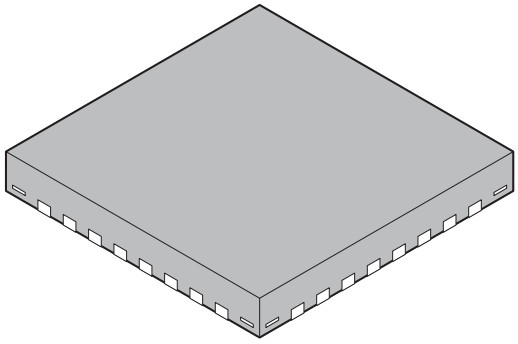
(Note)Temperature : on the top of the package body

**(2) Manual soldering (partial heating method)**

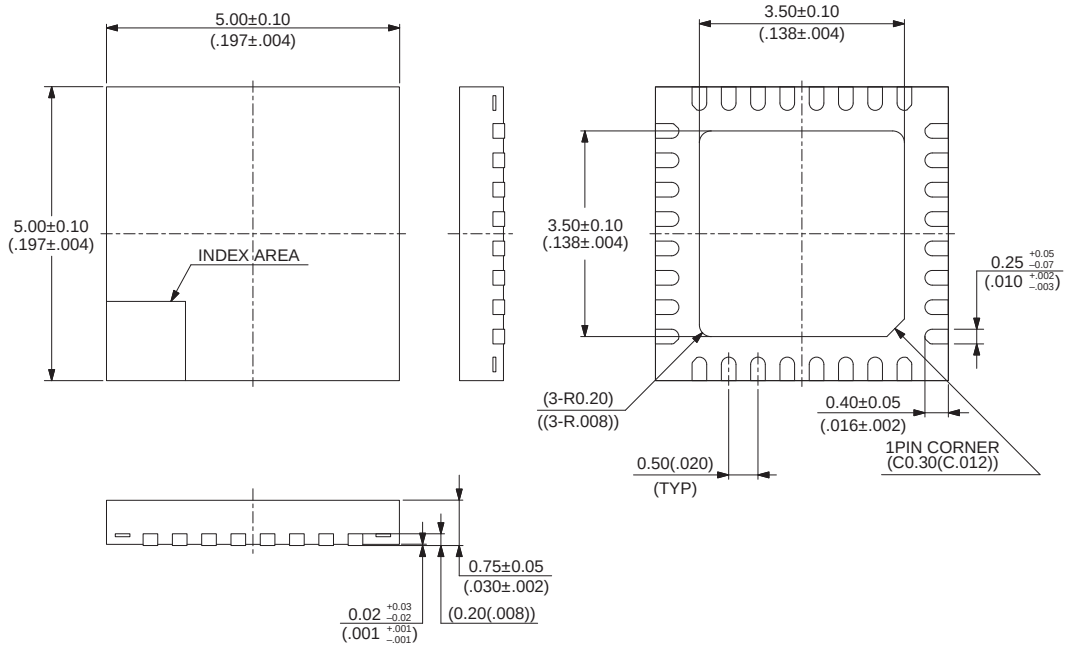
Temperature at the tip of an soldering iron: 400 °C max

Time: Five seconds or below per pin

## ■ PACKAGE DIMENSIONS

| 32-pin plastic QFN | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 5.00 mm × 5.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.80 mm MAX |
| | Weight | 0.06 g |
| | | |
| (LCC-32P-M19) | | |

32-pin plastic QFN
(LCC-32P-M19)






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| 31 | ■ TYPICAL APPLICATION CIRCUIT | Deleted annotation symbol. |
| 32 | • Parts list | Revised symbol “D1”. |
| 38 | ■ APPLICATION NOTE<br>• Fly-back diode selection | Revised the description. |

## ■ CONTENTS

# MEMO

# MEMO

# MEMO

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Edited: Sales Promotion Department