FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27713-1E

ASSP For Power Supply Applications (Secondary Battery)

Sensor IC For Li-Ion Battery Pack Control

MB39F101

■ DESCRIPTION

The MB39F101 is a Li-ion battery pack control IC for 3/4-cell series Li-ion battery packs in notebook PCs. The MB39F101 is composed of 10-bit A/D converter where battery information received from protection IC is processed digitally, 1280-bit flash memory which stores battery initial information and control information, and I^2C controlling circuit which communicates with main body of PC.

Deleting the microprocessor in the battery pack becomes possible by setting using MB3838A (protection IC made by Fujitsu) . Similar data to SBS can be outputted, and the battery remainder amount monitoring system of high performance and a low cost can be composed.

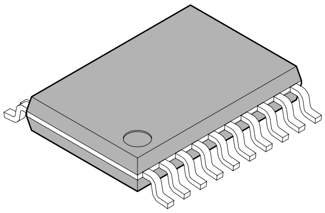
■ FEATURES

- Low cost flash memory technology adoption
- For 3/4-cell series Li-ion battery pack
- For I^2C BUS*
- The A/D conversion is simultaneously possible of voltage drop by the voltage measurement and the current sense resistor.

* : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ PACKAGE

20-pin plastic SSOP



(FPT-20P-M03)

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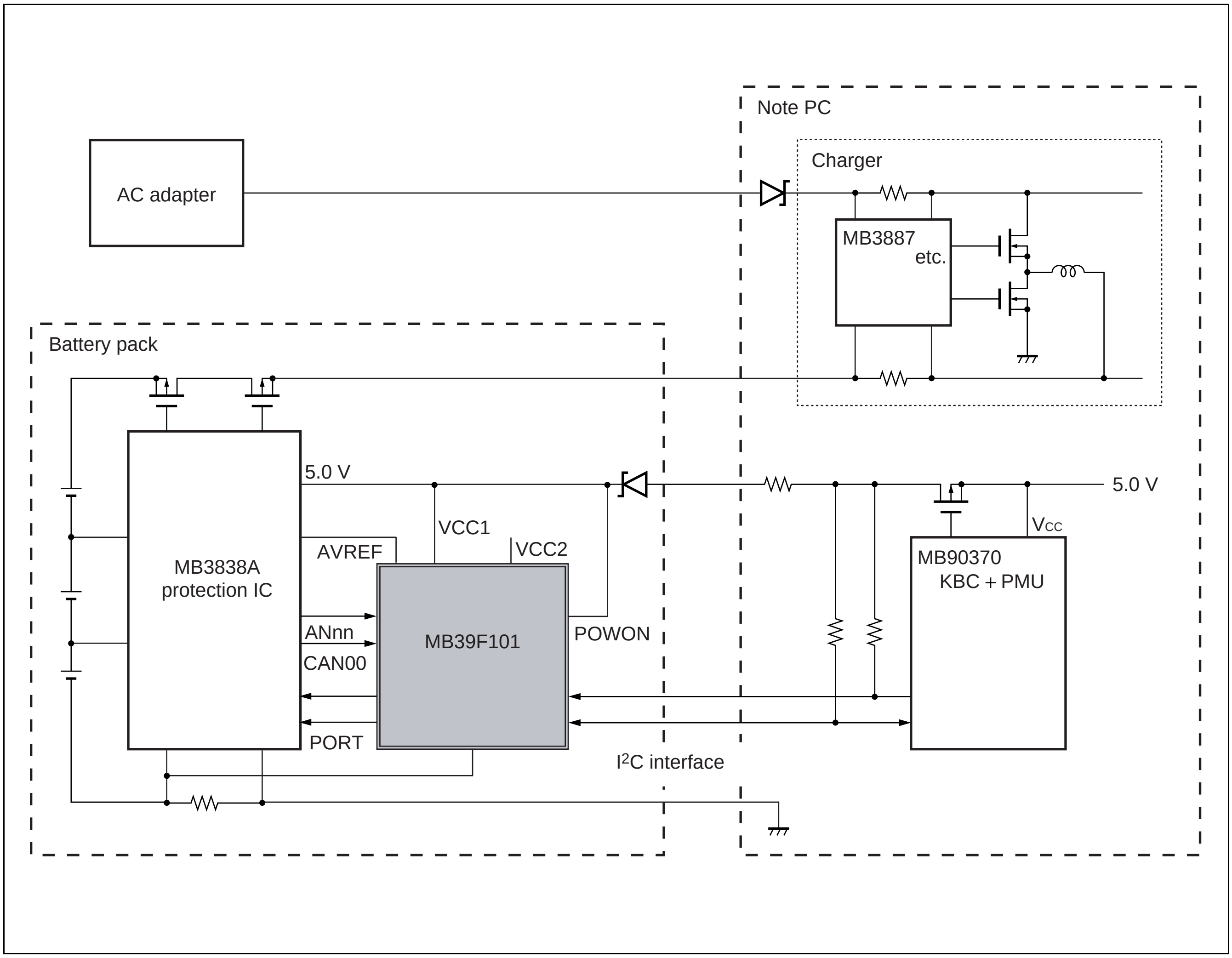
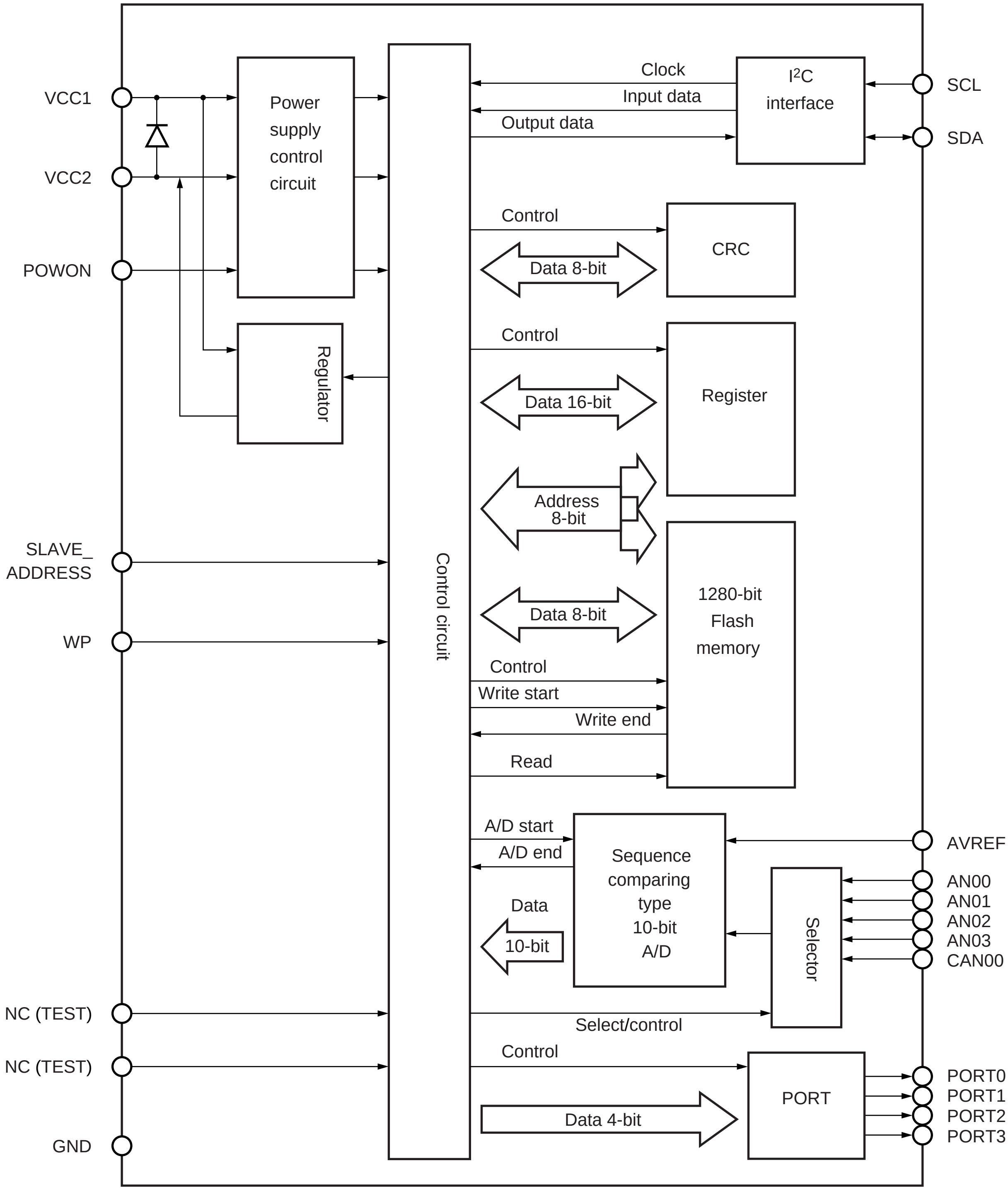
■ EXAMPLE OF SYSTEM CONFIGURATION

This IC has the following function in the battery pack of note PC.

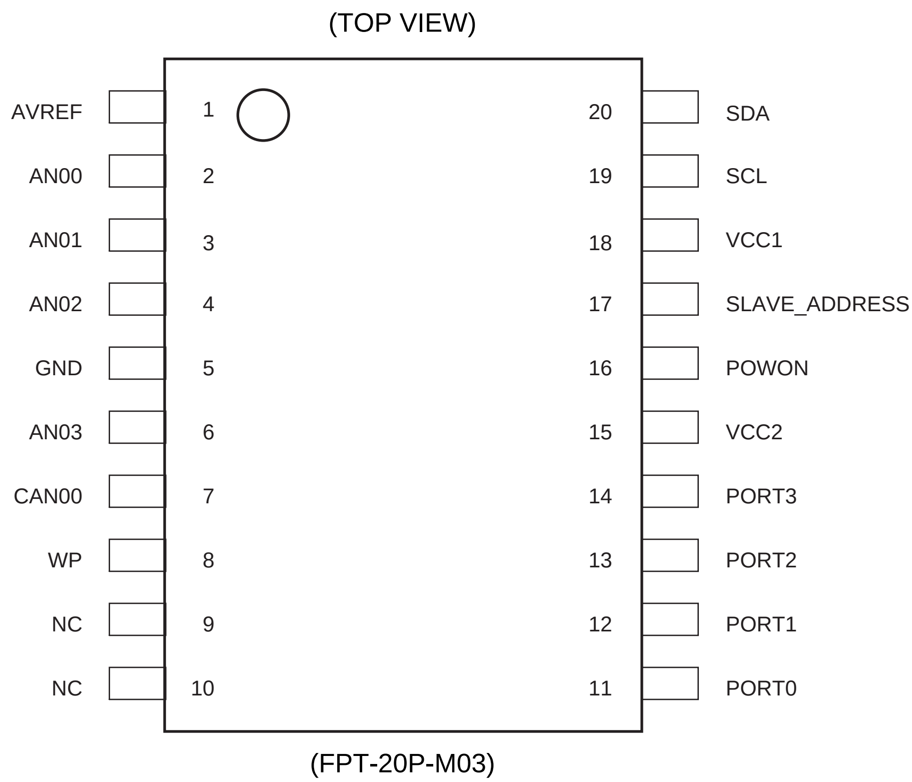
- Flash memory to memorize type and charge and discharge characteristic of battery
- A/D converter for measurement of voltage and current of battery
- I²C interface to communicate data and A/D conversion result of Flash memory with PC side microprocessor



■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Symbol	I/O	Descriptions
1	AVREF	I	Reference voltage input terminal for A/D converter.
2	AN00	I	A/D converter input terminal (0) .
3	AN01	I	A/D converter input terminal (1) .
4	AN02	I	A/D converter input terminal (2) .
5	GND	—	GND terminal (The substrate of IC) .
6	AN03	I	A/D converter input terminal (3) .
7	CAN00	I	A/D converter input terminal (For current sense) .
8	WP	I	Write protection terminal. 80_H-FF_H becomes read-only at “H”.
9, 10	NC	—	No connection terminal (For test) . Make it to open or GND.
11	PORT0	O	Port output terminal (0) .
12	PORT1	O	Port output terminal (1) .
13	PORT2	O	Port output terminal (2) .
14	PORT3	O	Port output terminal (3) .
15	VCC2	O	Internal voltage monitor terminal. Ground capacity usually.
16	POWON	I	Operation and stop control terminal of IC.
17	SLAVE_ ADDRESS	I	Slave address setting terminal.
18	VCC1	—	Power supply terminal. (VCC1 = 5.0 V)
19	SCL	I	I^2C interface and a clock signal input terminal.
20	SDA	I/O	I^2C interface and a data signal I/O terminal.

1. NOTE ON USING PINS

- **VCC1**

VCC1 is an input terminal for the power supply. Impress 5.0 V power supply from the power supply.

When an external power supply is input to this terminal, insert the diode so that the terminal VCC1 side may become a cathode side between an external power supply and the terminal VCC1, because the current does not flow to an external power supply.

When 5.0 V is not impressed to VCC1, writing to the Flash memory and the A/D conversion cannot be executed.

At the normal operation, do occurrence of the voltage in which step down is done for VCC2 from VCC1 because of built-in regulator.

The power supply must be impressed during the operation of writing the Flash memory.

When the power supply is not impressed, data is not guaranteed.

- **VCC2**

VCC2 is the generated voltage monitor terminal of built-in regulator.

Ground capacity when using it usually.

- **AVREF**

AVREF is the reference voltage input terminal for A/D conversion.

1/1024 of the reference voltages input to AVREF is a minimum resolution voltage from which do the measurement by A/D conversion.

Give the voltage impressed to AVREF below the VCC1 voltage.

When the A/D conversion is waited, it is cut off from an internal circuit by analog SW.

Do not impress the voltage to the AVREF terminal with the power supply not impressed to VCC1.

Because the current flows through the ESD element, IC might be destroyed.

- **POWON**

POWON is operation and stop control terminal of IC.

POWON terminal “H” level : Do the operation of IC.

Power On Reset is done when POWON changes from “L” level into “H” level, and IC is initialized.

POWON terminal “L” level : IC is stopped, and the consumption of the power supply current is minimized.

Do not make it to “L” level during the operation of writing the Flash memory.

Data is not guaranteed when becoming “L” level.

Make it to “L” level when you turn on the power supply.

It is a Schmitt trigger input.

- **SDA, SCL**

SDA is a data line for the I^2C interface, and SCL is a clock line.

It is a Schmitt trigger input.

• SLAVE_ADDRESS

SLAVE_ADDRESS is slave address setting terminal when communicating by the I²C interface.

Upper 7-bit becomes slave address among the data of 8-bit forwarded first, and least significant 1bit specifies the direction where data is forwarded.

SLAVE_ADDRESS terminal "H" level : slave address $A8_H$ (write) $A9_H$ (read)

"L" level : slave address $A0_H$ (write) $A1_H$ (read)

Bit 0 and 2 of slave address are "1" fixation, and bit 1, 3, 5, and 6 are "0" fixation.

Do not change the input level while communicating I²C.

Because the I²C communication is not normally done when the input level changes, IC should be likely to be initialized (Make the POWON terminal "L" level) .

It is a Schmitt trigger input.

slave address

bit No.	0	1	2	3	4	5	6	7
	1	0	1	0	SA	0	0	R/W

When R/W is "0", it writes in MB39F101 (Write) .
When R/W is "1", it reads from MB39F101 (Read) .

• WP

WP is read-only (Write Protection) setting terminal of built-in Flash memory.

WP terminal "H" level : Read-only of Flash memory

"L" level : Writing permission of Flash memory

Area where writing protection with WP terminal can be set

System memory area (80_H to FF_H) : Possible to set it.

User memory area (60_H to $7F_H$) : Not possible to set it. (Write enable always)

Reading has been permitted regardless of the state of the WP terminal.

Do not change the input level while communicating I²C.

Because the I²C communication is not normally done when the input level changes, IC should be likely to be initialized (Make the POWON terminal "L" level) .

It is a Schmitt trigger input.

• PORT0 to 3

PORT0 to 3 are a general-purpose Port output.

Information on the register written through the I²C interface is outputted as it is.

The content of the register is cleared when do the occurrence of Power On Reset, and the Port output becomes "L" level.

It is CMOS output.

- **AN00 to AN03**

  AN00 to AN03 are a input signal for A/D conversion.

  The A/D conversion circuit chooses any from among analog signals input to AN00 to AN03 and does A/D conversion.

  When A/D conversion is waited, it is cut off from an internal circuit by analog SW.

  Do not impress the voltage to the AN00 to AN03 terminals with the power supply not impressed to VCC1.

  Because the current flows through the ESD element, IC might be destroyed.

- **CAN00**

  CAN00 is a input signal for A/D conversion.

  Voltage drop by the current sense resistor is done and A/D conversion is done.

  The A/D conversion operation executes one of AN00 to AN03 and A/D conversion of the CAN00 terminal at the same time.

  When A/D conversion is waited, it is cut off from an internal circuit by analog SW.

  Do not impress the voltage to the CAN00 terminal with the power supply not impressed to VCC1.

  Because the current flows through the ESD element, IC might be destroyed.

- **NC**

  NC is a terminal only for the shipment examination of IC.

  Make it to open or GND when mounting.

* : When mounting, it is recommended to assume GND.

  When the voltage is impressed in the following cases :
  - It becomes a test mode and no normal operation.
  - The current flows.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC1}	–0.5	6.0	V	VCC1 terminal
Input voltage	V_{i1}	–0.5	V_{CC1} + 0.5 (< 6.0)	V	AVREF, AN00, AN01, AN02, AN03, CAN00 terminals
	V_{i2}	–0.5	6.0	V	SCL, SDA, SLAVE, ADDRESS, WP, POWON, NC terminals
Output voltage	V_{O1}	–0.5	4.0	V	VCC2 terminal
	V_{O2}	–0.5	VCC2 + 0.5 (< 4.0)	V	PORT0, PORT1, PORT2, PORT3 terminals
Storage temperature	T_{STG}	–55	+125	°C	—

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC1}	4.5	5.0	5.5	V	—
Input voltage	V_i	GND	—	V_{CC1}	V	—
Data transfer rate	f_{SCL}	—	100	300	kHz	I^2C data transfer rate (SCL terminal)
Flash memory rewriting-number of times	—	—	—	2000	Times	—
Operating ambient temperature	Ta	–30	+ 25	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• Power supply current

(Ta = +25 °C)

Parameter	Symbol	Mesurement	Value			Unit	Remarks
			Min	Typ	Max		
Normal operation mode power supply current	I_{CC1}	*1	—	135	—	µA	At VCC2 open/ normal operation mode/ I^2C data waiting
Sleep mode power supply current	I_{CC1}	*2	—	10	—	µA	At VCC2 open/ sleep mode/ I^2C data waiting
Stop mode power supply current	I_{CC1}	*3	—	0.1	10	µA	VCC2 open/stop mode
Power supply current at Flash memory write	I_{CC1}	*4	—	(2)	—	mA	At VCC2 open/ normal operation mode/ Design reference value (average)
Power supply current at Flash memory read	I_{CC1}	*5	—	(150)	—	µA	At VCC2 open/ normal operation mode/ Design reference value (average)
Power supply current at A/D conversion	I_{CC1}	*6	—	(1.5)	—	mA	At VCC2 open/ normal operation mode/ Design reference value (average)

*1 : VCC1 = 5.0 V/VCC2 = open /POWON = 5.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V/another open
*2 : VCC1 = 5.0 V/VCC2 = open /POWON = 5.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V/another open
*3 : VCC1 = 5.0 V/VCC2 = open /POWON = 0.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V/another open
*4 : VCC1 = 5.0 V/VCC2 = open /POWON = 5.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V/another open
*5 : VCC1 = 5.0 V/VCC2 = open /POWON = 5.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V/another open
*6 : VCC1 = 5.0 V/VCC2 = open /POWON = 5.0 V/SDA•SDL = 5.0 V/SLAVE_ADDRESS•WP = 0.0 V /AVREF = 5.0 V/AN00 to AN03•CAN00 = 2.5 V

• **Digital Block**

Under the recommended operation condition

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Input voltage	V_{IH}	$V_{CC1} \times 0.7 + 0.4$	—	—	V	POWON terminal When VCC1 = 4.5 V to 5.5 V is impressed
	V_{IL}	—	—	$V_{CC1} \times 0.3 - 0.4$	V	
	V_{IH}	$(V_{CC2}) \times 0.7 + 0.4$	—	—	V	SDA, SCL, SLAVE_ADDRESS, WP terminals Standard as for the regulator output voltage. Possible to impress it to V_{IH} = 5.5 V
	V_{IL}	—	—	$(V_{CC2}) \times 0.3 - 0.4$	V	
Input current	I_{IH}	—	—	1.0	µA	POWON, SDA, SCL, SLAVE_ADDRESS, WP terminals V_{IH} = 5.5 V
	I_{IL}	–1.0	—	—	µA	POWON, SDA, SCL, SLAVE_ADDRESS, WP terminals V_{IH} = 0.0 V
Output voltage	V_{OL}	—	—	0.4	V	SDA terminal VCC2 = 3.3 V, I_{OL} = 3.0 mA
	V_{OH}	$(V_{CC2}) - 0.4$	—	—	V	PORT0 to 3 terminals VCC2 = 3.3 V, I_{OH} = –100 µA
	V_{OL}	—	—	0.4	V	PORT0 to 3 terminals VCC2 = 3.3 V, I_{OL} = 100 µA
Output current	I_{OL}	3.0	—	—	mA	SDA terminal VCC2 = 3.3 V
	I_{OH}	—	—	–100	µA	PORT0 to 3 terminals VCC2 = 3.3 V *1
	I_{OL}	100	—	—	µA	PORT0 to 3 terminals VCC2 = 3.3 V
Output delay time	Delay time	—	1.0	—	µs	PORT0 to 3 terminals At no-load *2

*1 : The output current to the PORT0 to 3 terminals shall not be excess of 100 µA with total.

*2 : The content written in the PORT register is time until being reflected in the PORT terminal.
Stop condition ->Period until being reflected PORT terminal by I^2C interface input

- **Flash Memory Block**

(VCC1 = 5 V, Ta = +25 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Write time	Write time	—	53.0 *1	63.8	ms	VCC1 = 5.0 V, VCC2 = open Data write in 8 bytes (erase, program)
Read time	Read time	—	(17.6)	*2	µs	Under the recommended operation condition

*1 : Stop condition → Time to return of “ACK” by slave_address input by I^2C interface input.

*2 : Be in time for the data transfer by the I^2C interface.

- **A/D Block**

(VCC1 = 5 V, AVREF ≥ 33.0 V, Ta = +25 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	—
Total error	—	–3	—	3	LSB	—
Conversion time	—	—	80 *	—	ms	One of AN00 to AN03 and CAN00 terminal conversion
Input cut-off current	I_{IZH}	—	—	1.0	µA	AVREF, AN00 to AN03, CAN00 terminals At waiting for A/D conversion V_{IH} = 5.0 V
	I_{IZL}	–1.0	—	—	µA	AVREF, AN00 to AN03, CAN00 terminals At waiting for A/D conversion V_{IL} = 0.0 V
Input current	Iref	—	(140)	—	µA	AVREF terminal At A/D conversion ( )=Design reference value VAVREF = 5.0 V
Input impedance	Rin	—	(2.6)	—	kΩ	AN00 to AN03, CAN00 terminals At A/D conversion ( )=Design reference value
	Cin	—	(28)	—	pF	
Sampling time	—	—	(13)	—	µs	( )=Design reference value

* : Stop condition → Period until conversion end is set in A/D Command and Status Register by I^2C interface input.

- **Regulator and others**

(VCC1 = 5 V, Ta = +25 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Output voltage	V_O	—	3.24	—	V	Normal operation mode/ I^2C data waiting VCC2 output voltage
	V_O	—	2.59	—	V	Sleep mode/ I^2C data waiting VCC2 output voltage
Output current	I_O	—	—	10 *1	mA	Normal operation mode/ VCC2 output current
	I_O	—	—	100 *2	µA	Sleep mode/ VCC2 output current
Sleep mode shift time	—	12 *3	—	—	µs	Time necessary for shifting mode
Voltage detection	V_{IH}	4.5 *4	—	—	V	Under the recommended operation condition
Power supply turning on and Power On Reset time	—	20 *5	—	—	µs	

*1 : A built-in regulator corresponds only to the drive of this IC.
Do not drive the current from this IC via VCC2.

*2 : The output current to the PORT0 to 3 terminals shall not be excess of 100 µA with total.

*3 : Time necessary for return to sleep mode → normal operation mode and shift to normal operation mode → sleep mode
Do neither write to Flash memory nor the A/D conversion for this period.

*4 : Detect the power-supply voltage of 4.5 V or more not being impressed to the VCC1 terminal when the battery is discharged, and set the stop of the write prohibition of the Flash memory, the A/D conversion, and the regulator (Power Status Register) .

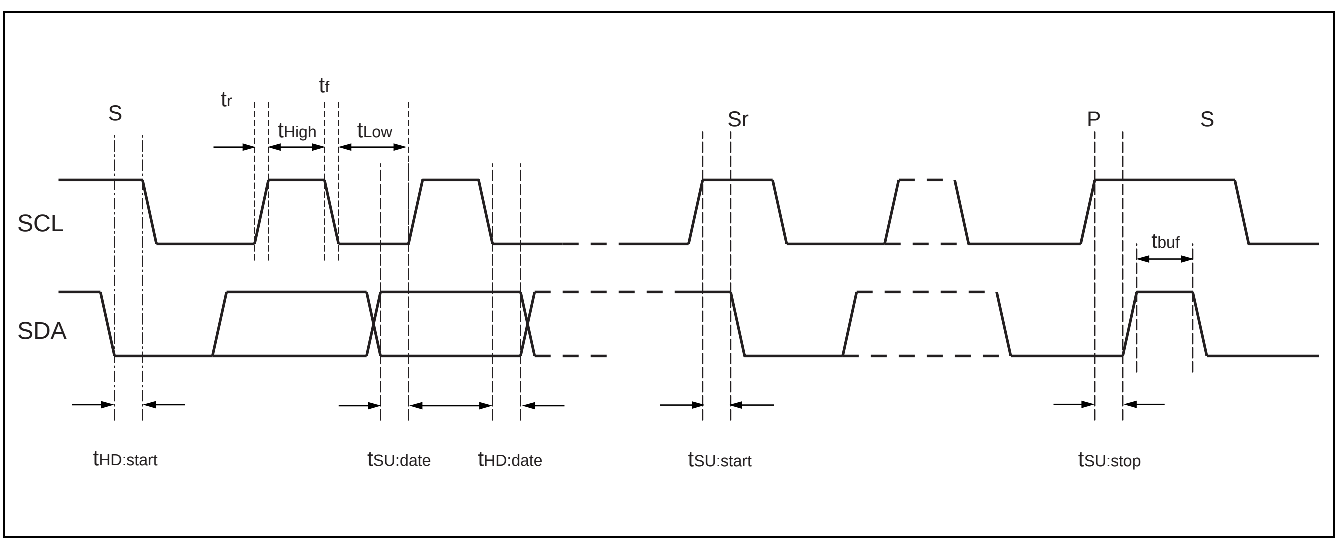
*5 : It is necessary time in power supply turning on to VCC1 terminal or Power On Reset by the shift to “L” → “H” of the POWON terminal.
Do not communicate for this period by the I^2C interface.

■ I²C INTERFACE INPUT TIMING

Under the recommended operation condition

Parameter	Symbol	Value				Unit	Remarks
		SCL = 100 kHz		SCL = 300 kHz			
		Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	—	100	—	300	kHz	—
Start condition hold time	$t_{HD\ :\ start}$	4.0	—	0.6	—	µs	—
Restart condition setup time	$t_{SU\ :\ start}$	4.7	—	0.6	—	µs	—
Stop condition setup time	$t_{SU\ :\ stop}$	4.0	—	0.6	—	µs	—
Stop to Start bus release time	tbuf	4.7	—	1.3	—	µs	—
SCL "L" time	t_{Low}	4.7	—	1.3	—	µs	—
SCL "H" time	t_{High}	4.0	—	0.6	—	µs	—
SCL/SDA rise time	tr	—	1.0	—	0.3	µs	—
SCL/SDA fall time	tf	—	0.3	—	0.3	µs	—
Data hold time	$t_{HD\ :\ datat}$	0.0	—	0.0	—	µs	—
Data setup time	$t_{SU\ :\ datat}$	0.25	—	0.1	—	µs	—
SCL/SDA capacitive load	Cb	—	400	—	400	pF	—

Note : V_{IH}/V_{IL} level standard



■ FUNCTIONS

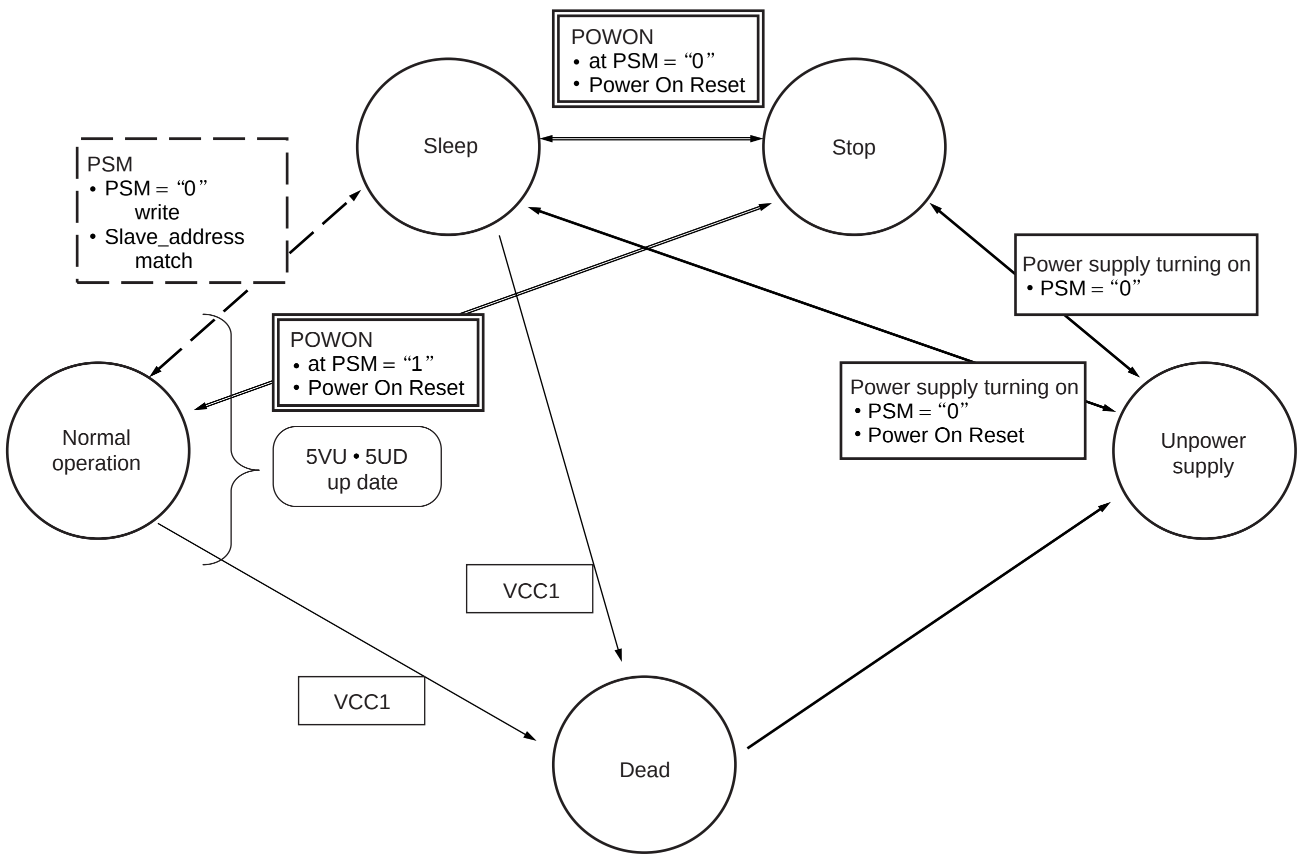
1. ABOUT THE OPERATION MODE

• About the kind of the operation mode

5 kinds of state are set as follows.

	Mode	Normal operation	Sleep	Dead	Stop	Unpower supply
Condition	VCC1	5.0 V impressing	5.0 V impressing	4.5 V or less detection	5.0 V impressing	Not impress
	POWON	"H"	"H"	—	"L"	"L"
	Power Status Register Bit0 (Power Save Mode)	"1"	"0"	—	—	Undefined
State	Regulator	Normal operation	L Power	Stop	Stop	Stop
	Flash memory write	Possible	Stop	Stop	Stop	Stop
	Flash memory read	Possible	Stop	Stop	Stop	Stop
	A/D conversion	Possible	Stop	Stop	Stop	Stop
	PORT setting and output	Possible	State holding before	Undefined	"L"	Don't care
	Power supply current (At waiting for I^2C data)	typ135 µA	typ10 µA	—	Leak current	—

• **About the operation mode transition**



Notes : • PSM : Power Status Register Bit0 (Power Save Mode)
• 5VU : Power Status Register Bit10 (5 V up)
• 5VD : Power Status Register Bit11 (5 V down)

• **About Power On Reset**

In the following cases, Power On Reset operates.

- Case to use POWON terminal as single control terminal
  Case which became POWON = "L".
- Case to connect (short) POWON terminal and VCC1.
  When turning on the power to the power supply terminal (VCC1 or VCC2) and POWON terminal simultaneously from the state that the power supply is not impressed neither VCC1 or VCC2.

About the content of Power On Reset

- The logic state of the controlling circuit, the Flash memory, and A/D is cleared, and it initializes it.
- PORT output "L"
- PORT register "0" clearness
- A/D conversion result register "0" clearness
- CRC initialization
- Power Status Register Bit9 (Power On reset) "1" set
- Address register "00_H"

2. ABOUT THE COMPOSITION OF THE I²C INTERFACE AND DATA

• About the bit composition of data

The bit composition in data like the Flash memory and the register, etc. is Big endian.

Most significant bit (MSB) is assumed to be bit 0 about bit No. and least significant bit (LSB) is assumed to be bit 7 or bit 15.

Flash memory (1 byte composition)

0	1	2	3	4	5	6	7	bit No.
MSB							LSB	

Register (2 byte composition)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	bit No.
MSB															LSB	

• About the address composition of the register

The address composition of the register which is 2 byte composition is Little endian.

Therefore, note that the LSB side becomes subordinate address, and the MSB side becomes precede address. (Address 00_H side : Low byte address/address FF_H side : High byte address)

Register (2 byte composition)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	bit No.
a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	
MSB															LSB	

High byte address (nnh + 1)

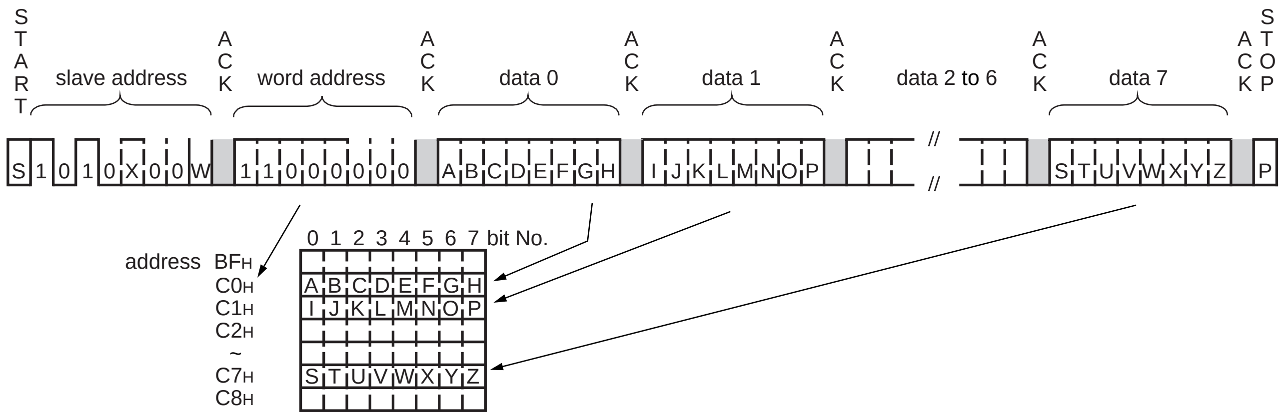
Low byte address (nnh)

Address	0	1	2	3	4	5	6	7	bit No.
$nn_H - 1$ (Address)									
nn_H (Address)	i	j	k	l	m	n	o	p	
$nn_H + 1$ (Address)	a	b	c	d	e	f	g	h	
$nn_H + 2$ (Address)									

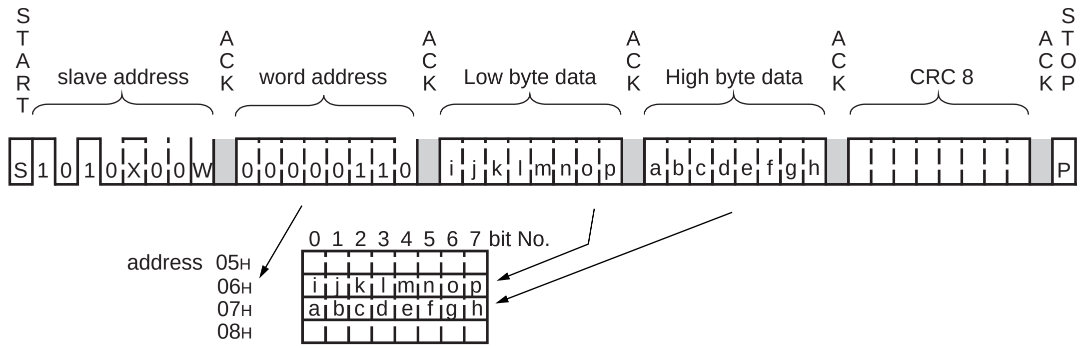
- **About the data bit composition on the I²C interface**

The data bit row is sent and received from MSB in order of LSB.

- Case with Flash memory (example)



- Case with register (example)



3. I²C INTERFACE

• Composition of I²C interface

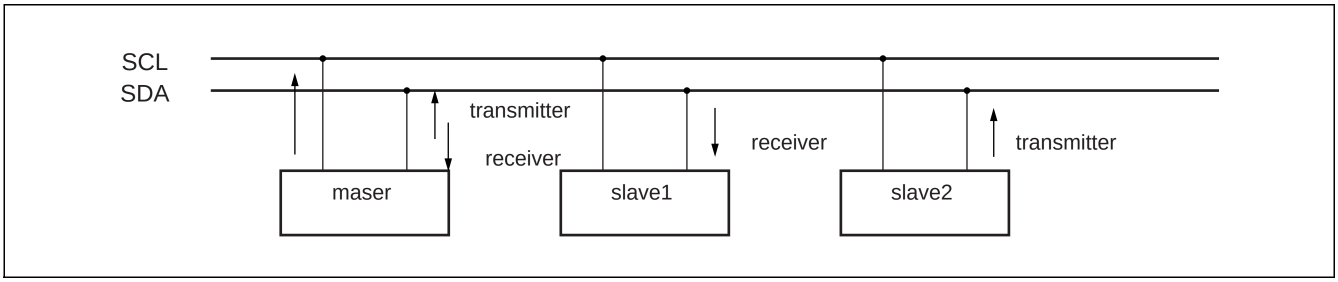
The I²C interface does the data communication of each 1 byte (8-bit) with two signal lines (bus) of SCL (serial clock line) and SDA (serial data line) .

Multiple device are connected with this bus.
- master : Device which occurs clock signal and controls data transfer (CPU etc.)
- slave : Device for which address is specified from master

This IC is set as slave, and the function which becomes master is not provided.

Each device is defined as follows by the direction of the communication.
- transmitter : Device which transmits data to bus
- receiver : Device which receives data from bus

This IC has both transmitter and receiver functions



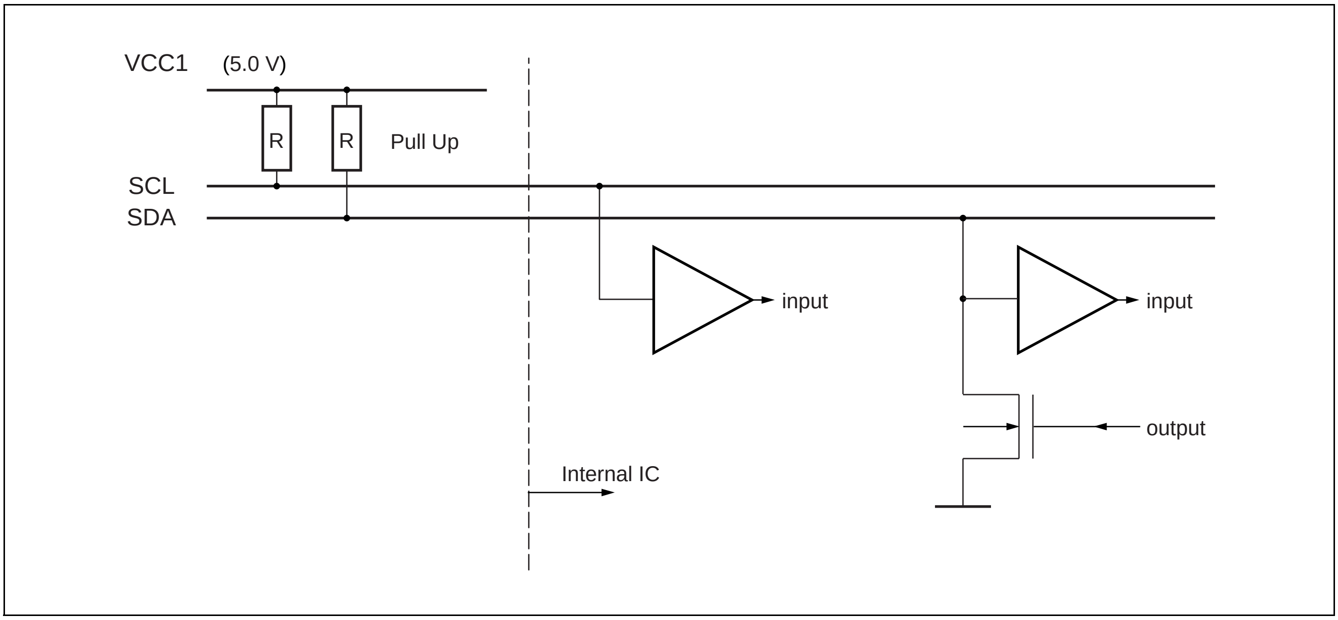
In this IC, it defines as follows
- write : Data is transmitted from master, and this IC receives data.
- read : This IC transmits data, and master receives data.

• Definition of signal line

SCL and SDA are connected with the power supply by the Pull-up resistor.

The output circuit is open Drain output.

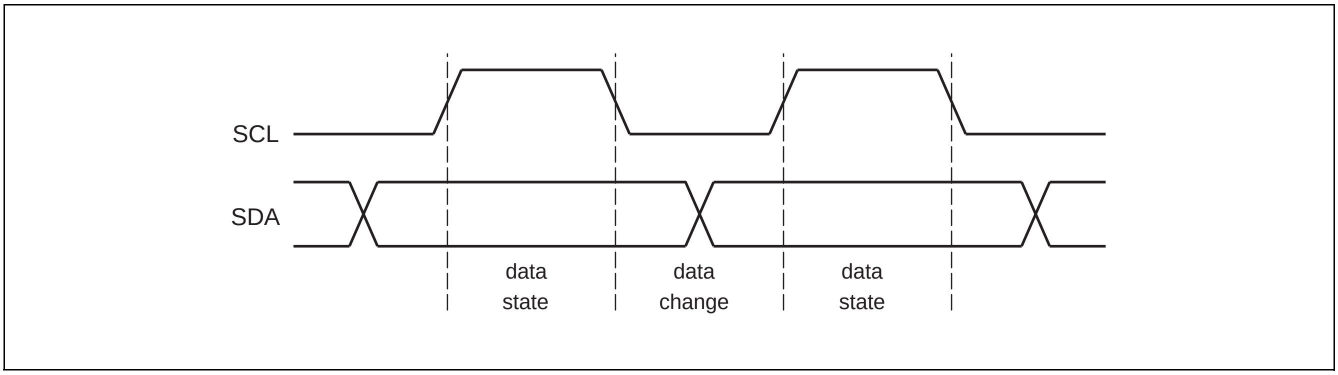
When the bus is not used (state of waiting) , open Drain is turned off, and it becomes open “H”.



• Effectiveness of data

In the following cases, data is effective.
- It changes when SCL is “L” level.
- SCL holds the state between the “H” levels.

The incorporation of data is done by the fall of SCL



The SCL signal change when SDA is “H” level means start or the stop condition.

• Definition of start and stop condition

Start and stop conditions are outputted from master, and direct slave the beginning and end of the communication.

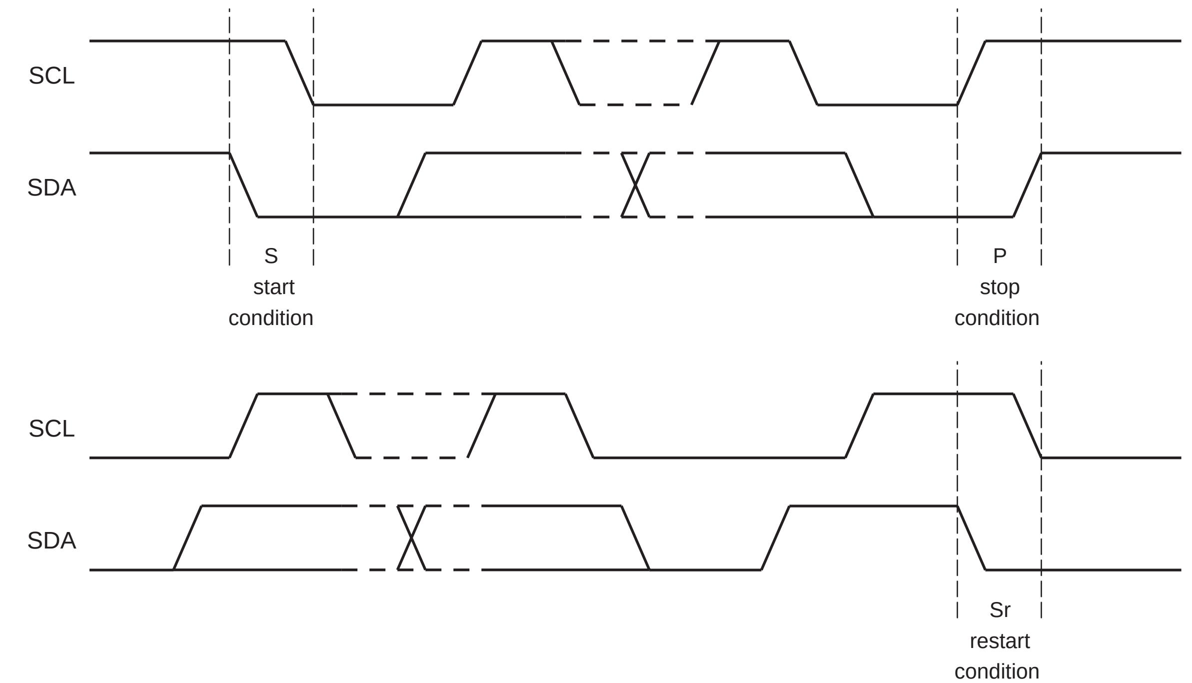
- start : When SCL is “H”, SDA is changed into “H” -> “L”.
- stop : When SCL is “H”, SDA is changed into “L” -> “H”.

“Restart” can be output instead of outputting 2 conditions of “stop”-“start” when continuously communicating.

However, make it to the “stop” condition after transmitting write data to the Flash memory or register when it is write.

Reception data is disregarded when the “restart” condition is outputted, and write is not executed.

After fixing the stop condition, this IC executes write.



- **ACK signal**

The ACK signal is a signal which confirms the data reception when communicating.

Receiver returns the ACK signal which shows that data was able to be received to transmitter whenever data is received in 1 byte (8-bit) .

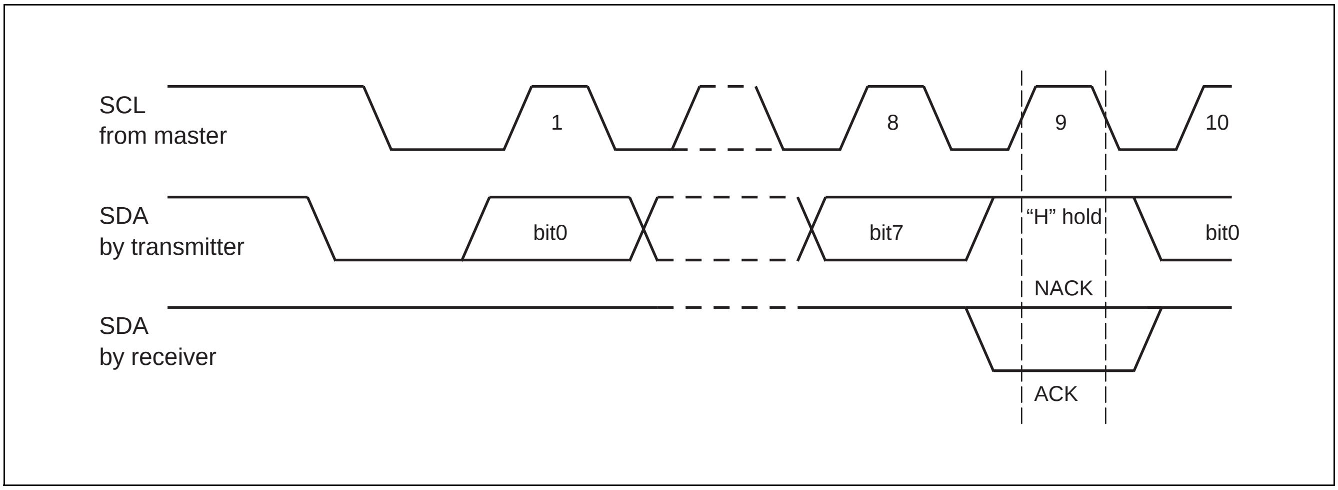
The ACK signal is transmitted with the 9 th clock after data 8-bit is transmitted according to the SCL signal where do the occurrence of master.

Transmitter maintains SDA output open H with the SCL 9 th clock.

Receiver outputs the following to SCL 9 th clock and informs transmitter of the data reception situation.
- Case where data was able to be received : SDA output “L” (ACK)
- Case where data was not able to be received : SDA output open “H” (NACK)

However, when master is receiver, do not return ACK to end the data transmission and to open the bus after receiving the last data.

In this case, slave transmitter is opened the bus (open H) , and enters stop from master or the state of the restart condition reception waiting.



- **About the operation executing writing in the Flash memory**

After the stop condition is fixed after data is received, write to the Flash memory is executed.

Even if all conditions and datas are disregarded, and it is necessary to receive slave address from master while executing write, SDA maintains “open H” and does not return ACK.

■ MEMORY MAP

	Address	Content	Address	Content		Remarks
Register area	00$_H$	A/D conversion result CAN00 Lbyte	01$_H$	A/D conversion result CAN00 Hbyte		
	02$_H$	A/D conversion result ANnn Lbyte	03$_H$	A/D conversion result ANnn Hbyte		
	04$_H$	A/D command/status Lbyte	05$_H$	A/D command/status Hbyte		
	06$_H$	PORT Lbyte	07$_H$	PORT Hbyte		
	08$_H$	Power status Lbyte	09$_H$	Power status Hbyte		
	0A$_H$ to 4F$_H$	Unmounting				
	50$_H$	For TEST	51$_H$	For TEST		Normal write/read wrong
	52$_H$ to 57$_H$	Unmounting				
Flash memory area	58$_H$ to 5F$_H$	Flash memory area for control				Normal write/read wrong
	60$_H$ to 67$_H$	User memory area 8 bytes × 4				Write protection nothing
	68$_H$ to 6F$_H$					
	70$_H$ to 77$_H$					
	78$_H$ to 7F$_H$					
	80$_H$ to 87$_H$	System memory area 8 byte × 16				Write protection object area with WP terminal
	88$_H$ to 8F$_H$					
	90$_H$ to 97$_H$					
	98$_H$ to 9F$_H$					
	A0$_H$ to A7$_H$					
	A8$_H$ to AF$_H$					
	B0$_H$ to B7$_H$					
	B8$_H$ to BF$_H$					
	C0$_H$ to C7$_H$					
	C8$_H$ to CF$_H$					
	D0$_H$ to D7$_H$					
	D8$_H$ to DF$_H$					
	E0$_H$ to E7$_H$					
	E8$_H$ to EF$_H$					
	F0$_H$ to F7$_H$					
	F8$_H$ to FF$_H$					

Register area :

- 2 bytes + each CRC8 (3 bytes in total) and read/Write
- Data is disregarded though write in the unmounting area ends normally on I²C.
- Reading data of read in the unmounting area is not fixed.

Flash memory area :

- Write by every 8 bytes (erase/program)

1. DEFINITION OF MEMORY MAP

- The space shown in the memory map divides into the Register area and the Flash memory area.
- The Register area is a space allocated for the control register to control the operation of each circuit.
  00_H to 57_H is allocated as address.
- The Flash memory area is a space of Flash memory which can be rewritten.
  58_H to FF_H is allocated as address.

2. FLASH MEMORY AREA

(1) User Memory Area

- Address 60_H to $7F_H$ is allocated.
- The writing protection is not set.
- Read is always possible.

(2) System Memory Area

- Address 80_H to FF_H is allocated.
- The writing protection can be set.
  Write is possible only that Write Protection is not set with the WP terminal (At “L”) .
  It informs that it is Write Protection to the HOST side by not returning “ACK” after data in the 1st byte is received if 80_H to FF_H is specified for write address when Write Protection is set, and write is not executed.
- Read is always possible.

(3) Area For Flash Memory Control

- Address 58_H to $5F_H$ is allocated.
- Neither read nor write can be done excluding the TEST mode.
  Case where 58_H to $5F_H$ is specified for address in state usually
  At write :
  It informs that it is a region for the Flash memory control to the HOST side by not returning “ACK” after data in the 1st byte is received, and write is not executed.
  At read :
  Data that read is done is not fixed (FF_H fixation) .

3. WRITE/READ TO FLASH MEMORY AREA

- It becomes write by every all 8 bytes.
  Erase (write of data “1”) and program (write of data “0”) are done according to reception data in bulk at write.
- Write is executed only at 8 bytes in the length of data when write is done.
  Do not disregard reception data when the length of data is shorter than that of 8 bytes, and do not execute write.
  It informs that it is the HOST side of the length’s of data length by not returning “ACK” after data in the 9th byte is received when the length of data is longer than that of 8 bytes, and write is not executed.
- Specify 8 byte boundary address for address when write is done.
  It informs that it is not 8 byte boundary address to the HOST side by not returning “ACK” after data in the 1st byte is received when 8 byte boundary address is not specified, and write is not executed.

- Write is possible that only power supply voltage (5.0 V) is impressed to VCC1, and the usual do operation of the regulator.
  It informs that it is Write Protection to the HOST side by not returning “ACK” after data in the 1st byte is received when power supply voltage (5.0 V) is not impressed to $V_{CC}1$, and write is not executed.
  Data is not guaranteed when entering the following states while executing write.
  - Power supply voltage (5.0 V) was not impressed to VCC1.
  - The POWON terminal was made “L”.
- Output “Stop” condition after transmitting write data.
  Reception data is disregarded for “Restart” condition, and write is not executed.
- It informs that write is being executed by not returning “ACK” on the HOST side while executing write even if correct slave address is received by the I^2C interface input.
- Specify 8 byte boundary address for address when read is done.
  When 8 byte boundary address is not specified, data that read is done is not fixed (FF_H fixation) .
- Read is done by arbitrary length of byte.
  Even if the content of the address counter is not 8 byte boundary address when read is done arbitrary byte as length continues in read (When read address is not specified) , read is possible.
- After read, only the length of byte which does read is added as for the content of the address counter.
- When the content of the address counter exceeds FF_H, it is set to 60_H.

4. WRITE/READ TO REGISTER AREA

- Everything becomes read and write for the unit of data 2byte + CRC8 (Cyclic Redundancy Check − 8) .
- The generation polynomial formula of CRC8 is “$X^8 + X^2 + X + 1$”.
- The CRC8 generation of each data 2byte is cleared. (Do not calculate continuously.)
- Write is executed only at 3 bytes in (data 2 byte + CRC8 1 byte) total in the length of data when write is done.
  Reception data is disregarded when the length of data is shorter than that of 3 bytes, and write is not executed.
  It informs that it is the HOST side of the length’s of data length by not returning “ACK” after data in the 4th byte is received when the length of data is longer than that of 3 bytes, and write is not executed.
- Specify 2 byte boundary address for address when write is done.
  It informs that it is not 2 byte boundary address to the HOST side by not returning “ACK” after data in the 1st byte is received when 2 byte boundary address is not specified, and write is not executed.
- When CRC8 is not corresponding, write is not executed.
  It informs that it is a code disagreement to the HOST side by not returning “ACK” immediately after the reception of the CRC8 code when the received CRC8 code the CRC8 code by the calculation and in IC are not corresponding at write, and write is not executed.
- Output “Stop” condition after transmitting write data and CRC8.
  Reception data is disregarded for “Restart” condition, and write is not executed.
- Specify 2 byte boundary address for address when read is done.
  When 2 byte boundary address is not specified, data that read is done is not fixed (FF_H fixation) .
- After read, only the length of byte which does read is added as for the content of the address counter.

5. ABOUT THE A/D CONVERSION OPERATION

- Address 00_H to 05_H is allocated as a register for A/D conversion.
- A/D conversion is executed by doing data to address 04_H, 05_H (A/D command/status register) in write.
- The A/D conversion operation executes one of AN00 to AN03 terminals and the CAN00 terminal at the same time. The result is stored in address 00_H, 01_H (A/D conversion result CAN00 register) and address 02_H, 03_H (A/D conversion result ANnn register) .
- The AN00 to AN03 terminal is selected with address 04_H, 05_H (A/D command/status register) .
- The end of A/D conversion is stored in address 04_H, 05_H (A/D command/status register) .

- The A/D conversion is possible that only power-supply voltage (5.0 V) is impressed to VCC1, and the usual do operation of the regulator.
- When not understanding the state that the A/D conversion is possible, it is checked in address 08_H, 09_H (Power status register) .
- A/D conversion is converted into data of 10-bit based on the voltage of AVREF terminal (A/D reference voltage input) .
  1 LSB = V (AVREF) /2^{10}

6. REGISTER FOR A/D CONVERSION

(1) A/D Conversion Result CAN00 Register

- Address 00_H, 01_H is allocated.
- The result of A/D conversion of the CAN00 terminal (for current sense) is stored.
- Only read is possible.
  Case to do write
  - The reception of data ends normally.
  - Reception data is disregarded.

MSB / LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	D_{00}	D_{01}	D_{02}	D_{03}	D_{04}	D_{05}	D_{06}	D_{07}	D_{08}	D_{09}

Bit 0 to 5 : It is unused. “0” is always read.
Bit 6 to 15 : The result of the A/D conversion is stored.

(2) A/D Conversion Result ANnn Register

- Address 02_H, 03_H is allocated.
- The result of the A/D conversion for one terminal of AN00 to AN03 terminals is stored.
- The AN00 to AN03 terminals are selected with address 04_H, 05_H (A/D command/status register) .
- Only read is possible.
  Case to do write
  - The reception of data ends normally.
  - Reception data is disregarded.

MSB / LSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	D_{00}	D_{01}	D_{02}	D_{03}	D_{04}	D_{05}	D_{06}	D_{07}	D_{08}	D_{09}

Bit 0 to 5 : It is unused. “0” is always read.
Bit 6 to 15 : The result of the A/D conversion is stored.

(3) A/D Command/Status Register

- Address 04_H, 05_H is allocated.
- The instruction of start and the situation of the end for A/D conversion is stored.
- The AN00 to AN03 terminals which do A/D conversion are selected.
- Read/Write is possible.

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
S	0	0	0	0	0	0	0	0	0	0	0	0	0	ANnn	

Bit 0 : It is Start signal which specifies beginning A/D conversion.
When “1” is done in write, A/D conversion is begun.
It is reset that A/D conversion is completed in “0”.

Bit 1 to 13 : It is unused. “0” is always read.
When write is done, data is disregarded.

Bit 14, 15 : The AN00 to AN03 terminals which do A/D conversion are selected.
Set terminal No. by the binary number.

(4) PORT Register

- Address 06_H, 07_H is allocated.
- The output of the PORT terminal corresponding to bit is set.
- Correspondence of write data and PORT terminal output
  “1” : Output “H”
  “0” : Output “L”
- Read/Write is possible.

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
P_0	P_1	P_2	P_3	0	0	0	0	0	0	0	0	0	0	0	0

Bit 0 : It corresponds to PORT0.
Bit 1 : It corresponds to PORT1.
Bit 2 : It corresponds to PORT2.
Bit 3 : It corresponds to PORT3.
Bit 4 to 15 : It is unused. “0” is always read.
When write is done, data is disregarded.

(5) Power Status Register

- Address 08_H, 09_H is allocated.
- The shift instruction to sleep mode (low-power consumption) and the state of the power supply are stored.
- Read/Write is possible.

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PS	0	0	0	0	0	0	0	BTS	RST	5VU	5VD	BWT	0	0	0

Bit 0 : It is Power Save Mode.

- In the state of the normal operation, it shifts to sleep mode (low-power consumption) by doing "0" in write.
- It wakes up automatically when slave address is corresponding because of the I^2C interface input, and IC is selected, and it is set in "1".

When the power supply is turned on from the state that the power supply is not impressed to both VCC1/VCC2, it is automatically set in sleep mode (low-power consumption) and it is set in "0".

Bit 8 : It is Battery Status.
The state of a present VCC1 terminal voltage (battery state) and the regulator operation is stored.
When this bit is "0", neither the write operation to the Flash memory nor the A/D conversion operation can be done.

- "0" : The battery is discharged, the VCC1 terminal becomes less than 4.5 V, and the regulator has stopped.
- "1" : The battery is normal, the VCC1 terminal becomes 4.5 V or more, and do the operation of the regulator usually.

Bit 9 : It is Power On Reset.
It is shown that did the occurrence of Power On Reset in the past.
After read is done, this bit is cleared to "0".

- "0" : After read the register, no do occurrence of Power On Reset.
- "1" : Did the occurrence of Power On Reset in the past.

Bit 10 : It is 5 V Up.
It is shown to have shifted from other states to the state of the normal operation in the past.

- 4.5 V or more was impressed to the VCC1 terminal again, and it shifted in the state of the normal operation.
- It woke up from sleep mode (low-power consumption) , and it shifted in the state of the normal operation.
- The POWON terminal became "L" to "H", and it shifted in the state of the normal operation.
- Turning on the power supply was done from the state that the power supply was not impressed to both VCC1 and VCC2.
  After read is done, this bit is cleared to "0".
- "0" : After read the register, no do occurrence of the shift to the state of the normal operation.
- "1" : Did the occurrence of the shift to the state of the normal operation in the past.

Bit 11 : It is 5 V Down.
It is shown to have shifted from the state of the normal operation to other states in the past.

- The VCC1 terminal became less than 4.5 V.
- It shifted to sleep mode (low-power consumption) .
- The POWON terminal became "L".
- It entered the state not being impressed for a power supply both VCC1 and VCC2.
  After read is done, this bit is cleared to "0".

- “0” : After read the register, no do occurrence of the shift excluding the state of the normal operation.
- “1” : Did the occurrence of the shift excluding the state of the normal operation in the past.

Bit 12 : It is Flash memory Bad write.
It is shown that did the occurrence of Flash memory write failure in the past.

- The VCC1 terminal became less than 4.5 V while executing write.
  After read is done, this bit is cleared to “0”.
- “0” : After read the register, no do occurrence of Flash memory write failure.
- “1” : Did the occurrence of Flash memory write failure in the past.
  When this bit is “1”, Flash memory is damaged. There is a possibility that write/read cannot be normally done.

Bit 1 to 7/Bit 13 to 15 : It is unused. “0” is always read.
When write is done, data is disregarded.

(6) Register For Test

- Address 50_H, 51_H is allocated.
- Write cannot be done excluding the TEST mode.
  Case where 50_H, 51_H is specified for address in state usually
  At write :
  It informs that it is a register for the test to the HOST side by not returning “ACK” after data in the 1st byte is received, and write is not executed.
- Read cannot be done.
  Data that read is done is not fixed.

(7) Unmounting Area

- Address $0A_H$ to $4F_H$/52_H to 57_H is a unmounting area.
- Write/Read cannot be done.
  At write :
  Reception data is disregarded.
  At read :
  Data that read is done is not fixed.

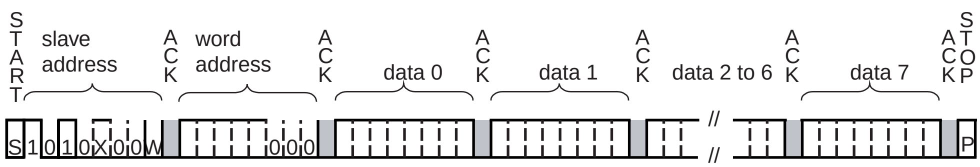
■ I²C INTERFACE DATA FORMAT

: Signal that master transmits

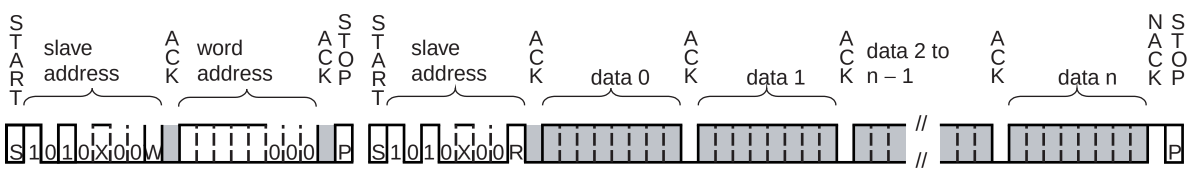
: Signal that this IC transmits

1. WRITE/READ FORMAT TO FLASH MEMORY AREA

(1) At Flash Memory Write



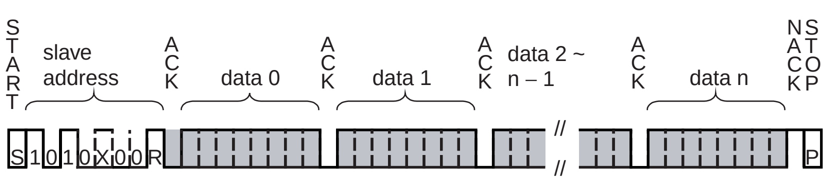
(2) At Flash Memory Read (case to specify word address)



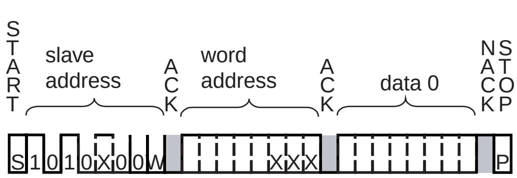
(3) At Flash Memory Read (case where word address is not specified)

When read is continuously done, read can do data from the following address of address which does read immediately before.

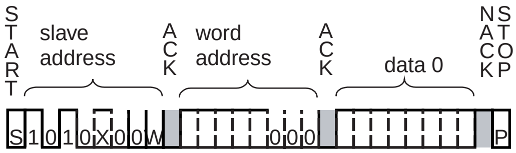
However, when Power On Reset and write are executed before at the time of doing read, read data is not fixed.



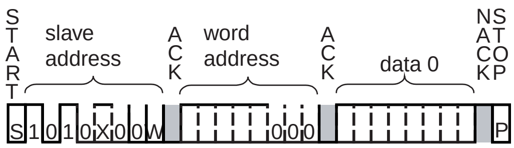
(4) Report Of Error (case where word address is not 8 byte boundary.)



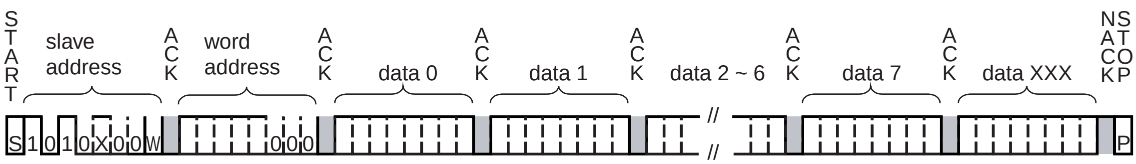
(5) Report Of Error (case where voltage is not impressed to VCC1 at write)



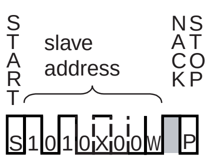
(6) Report Of Error (case where writing protection is set to system memory area at write)



(7) Report Of Error (case where data is long at write)

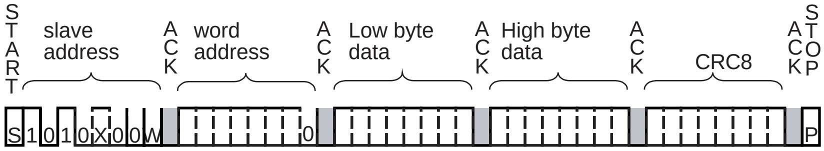


(8) Report Of Error (case with transmission from master while executing write)

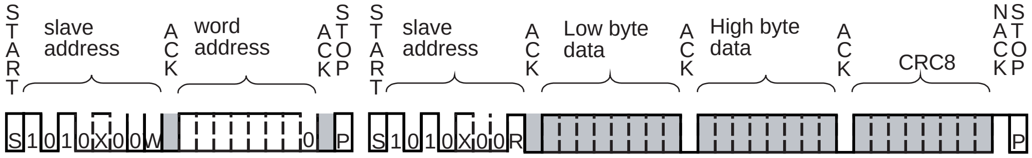


2. WRITE/READ FORMAT TO REGISTER AREA

(1) At Register Write



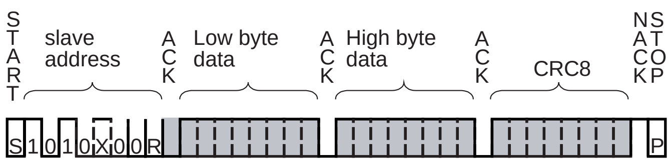
(2) At Register Read (case to specify word address)



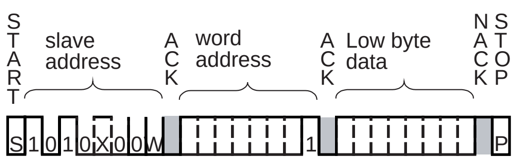
(3) At Register Read (case to specify word address)

When read is continuously done, read can do data from the following address of address which does read immediately before.

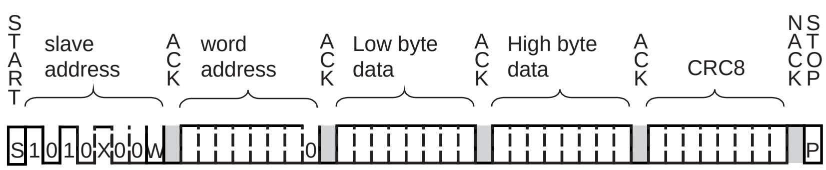
However, when Power On Reset and write are executed before at the time of doing read, read data is not fixed.



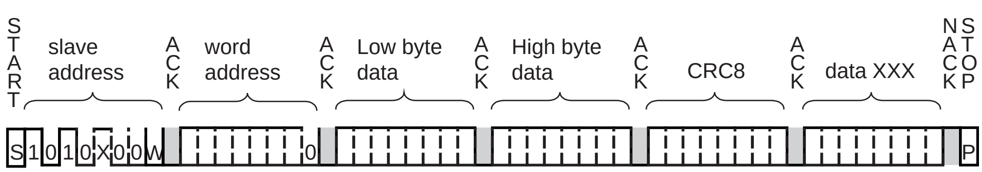
(4) Report Of Error (Case where word address is not 2 byte boundary.)



(5) Report Of Error (case to which CRC8 are not corresponding at write)

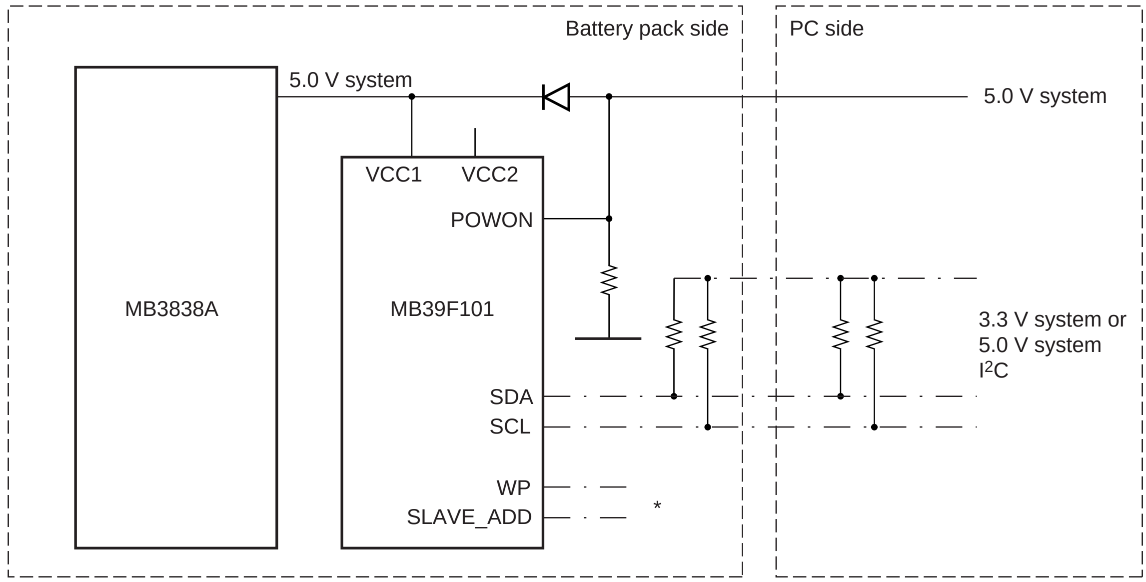


(6) Report Of Error (case where data is long at write)



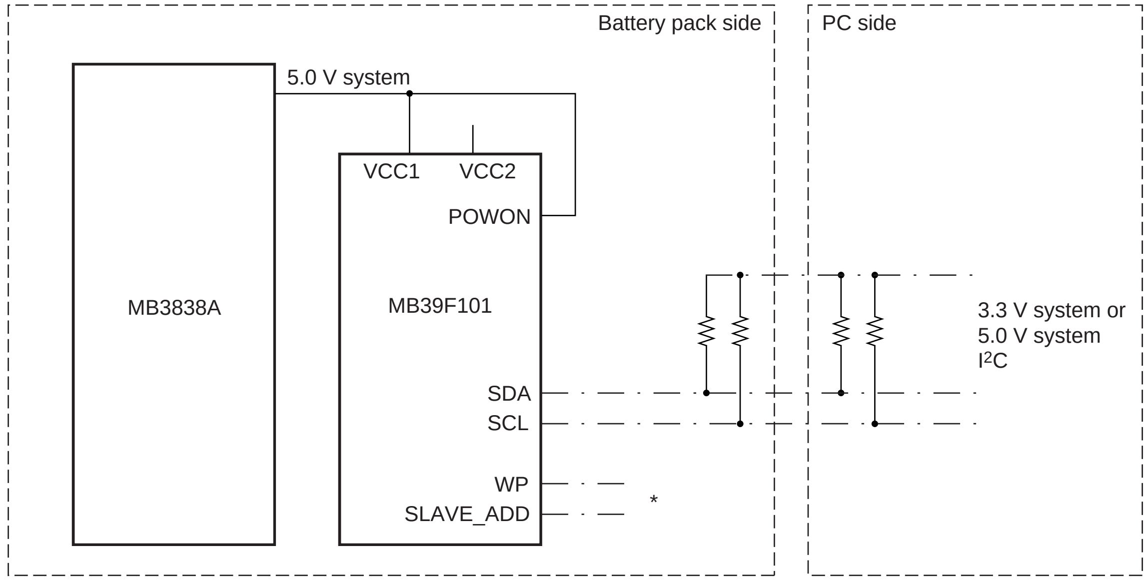
■ CONNECTION WITH EXTERNAL CIRCUIT

1. Connection example 1
(The individual control of each control terminal and VCC1 are impressed from the outside.)



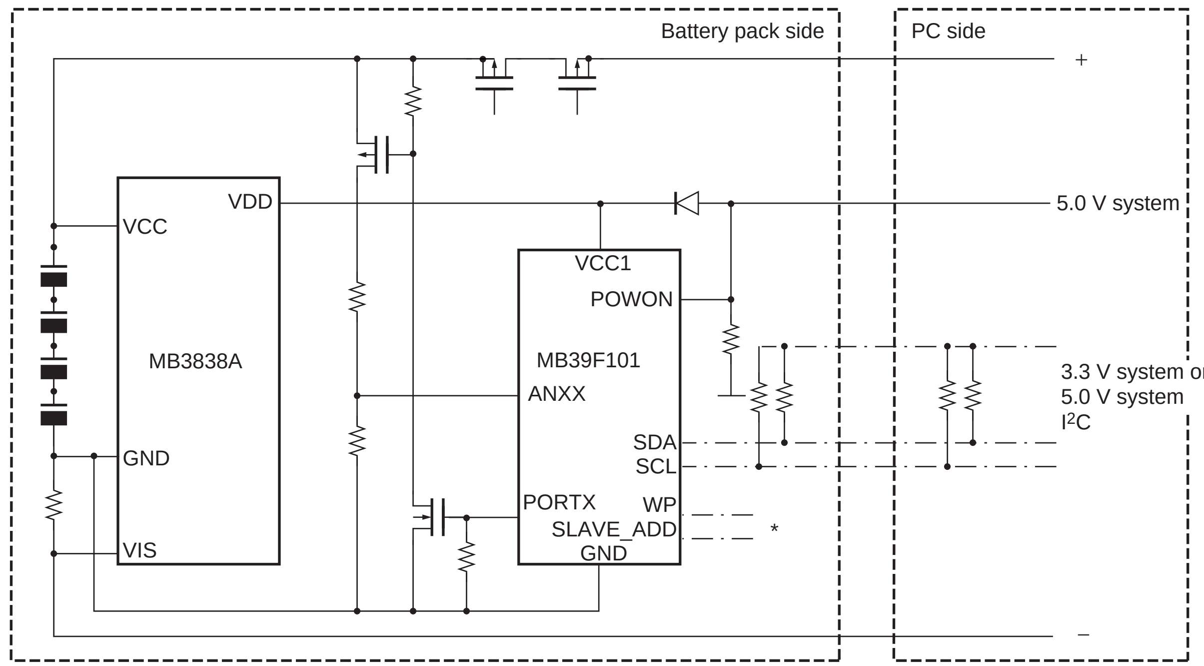
* : WP/SLAVE_ADDRESS is Pull-up or GND to 5.0 V system or 3.3 V system.

2. Connection example 2
(Each control terminal is not individually controlled.)



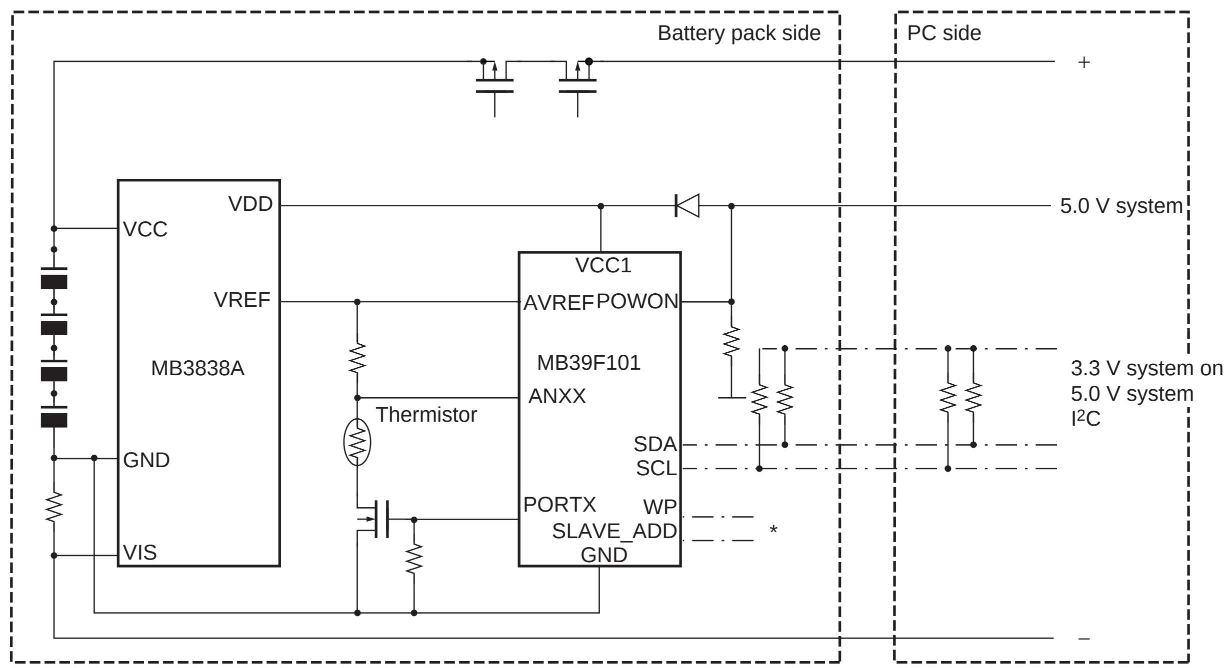
* : WP/SLAVE_ADDRESS is Pull-up or GND to 5.0 V system or 3.3 V system.

3. Connection example 3 (case for measurement of total battery voltage in state of overdischarge)



* : WP/SLAVE_ADDRESS is Pull-up or GND to 5.0 V system or 3.3 V system.

4. Connection example 4 (case to do thermometry)



* : WP/SLAVE_ADDRESS is Pull-up or GND to 5.0 V system or 3.3 V system.

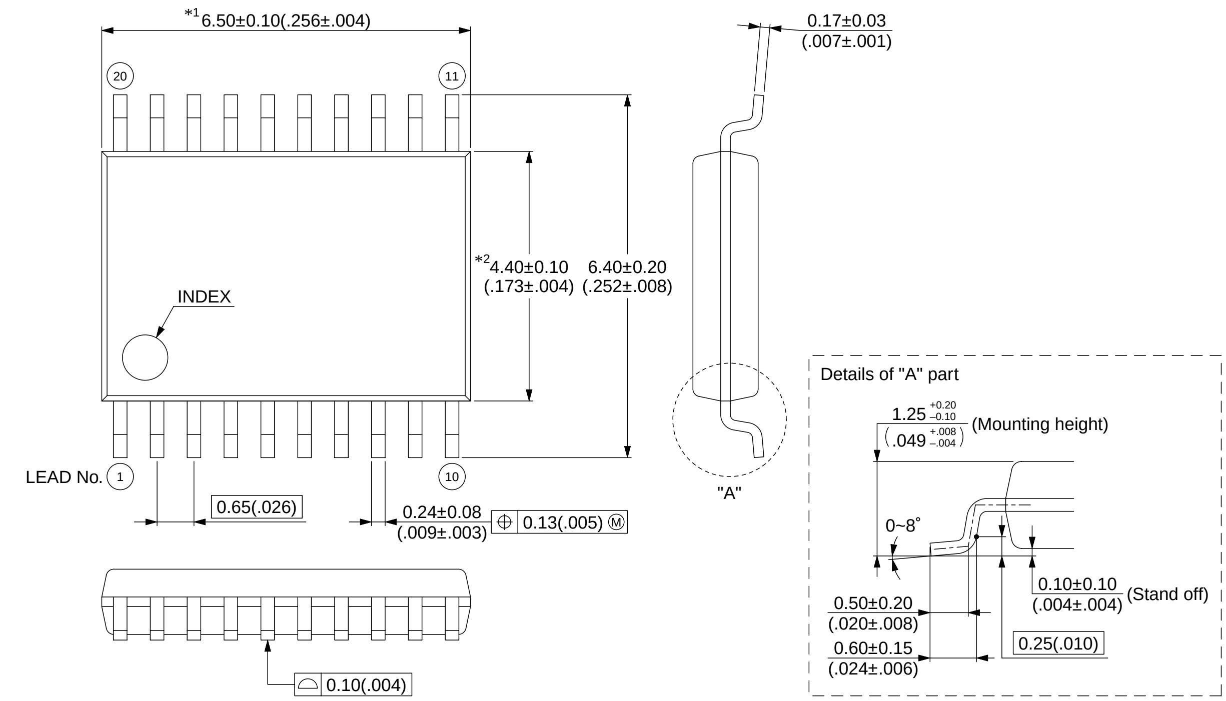
■ ORDERING INFORMATION

Part number	Package	Remarks
MB39F101PFV	20-pin plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

20-pin plastic SSOP
(FPT-20P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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