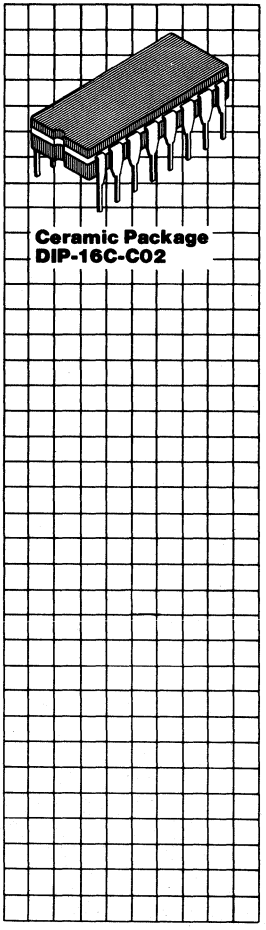
■ MB4316
Driver/Receiver for Disk Head Amp.

Description

The Fujitsu MB4316 is designed for the MB4111/MB4112 Disk Head Amplifier's Driver/Receiver.

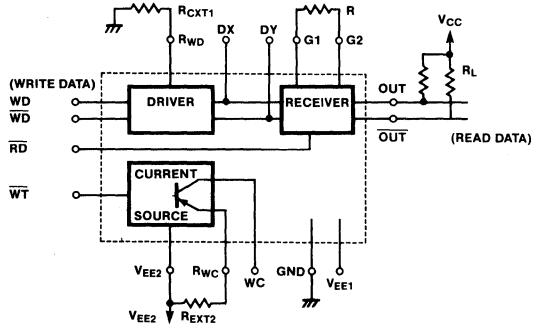
Features

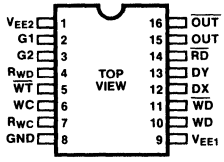
- **Data inputs and Control inputs are CML level inputs.**
- **On-chip Write Current Source which is adjustable by changing an external resister.**



Ceramic Package
DIP-16C-C02

Block Diagram and Pin Assignment





Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{EE1}	−7.0 - 0	V
	V_{EE2}	−15.0 - 0	V
Output Terminal Voltage	V_{CC}	0 - 9.0	V
Input Voltage	V_{IN}	−5.0 - 0	V
Write Current	I_{WG}	0 - 60	mA
Power Dissipation	P_D	580	mW
Operating Temperature	Ta	0 - 70	°C
Storage Temperature	Tstg	−55 - 150	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply voltage	V_{EE1}	−5.2±5%	V
	V_{EE2}	−12.0±5%	V
Output Terminal Voltage	V_{CC}	−6.0±5%	V
External Resistance	R_{EXT1}	700±2%	Ω

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Pin Function Table

Pin No.	Symbol	Functions
1	V_{EE2}	Power Supply (−12 V)
2	G1	Gain of output Amplifier (Receiver) is specified with an External resister between G1 and G2.
3	G2	
4	R_{WD}	This input specifies Data level in write mode.
5	$\overline{WT}$	WC switch. When it is at CML low level, WC is active.
6	WC	Write Current Source Output
7	R_{WC}	Write Current is specified with resister between R_{WC} and V_{EE2} (See Block Diagram). (I_{WC}=5.4V/R_{EXT2})
8	GND	Ground
9	V_{EE1}	Power Supply (−5.2V)
10	WD	Write Data, driven by complementary signal of CML level.
11	$\overline{WD}$	
12	DX	Data Bus
13	DY	
14	$\overline{RD}$	Read/Write mode Switch. When it is at CML low level, read mode is selected, and at high level, write mode is selected.
15	OUT	Output for read data
16	$\overline{OUT}$	

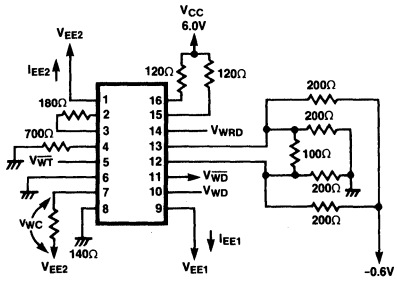
Electrical Characteristics

(V_{EE1} = -5.2V, V_{EE2} = -12.0V, T_A = 25° C)

Parameters	Symbol	Conditions		Measurement Diagram	Min.	Typ.	Max.	Unit
Power Supply Current	I_{EE1}	V_{EE1} = -5.46V, V_{EE2} = -12.6V		1	—	—	65	mA
	I_{EE2R}			1	—	—	15	mA
	I_{EE2W}			1	—	—	10	mA
Input Current	$I_{I\overline{RD}}$	V_{EE1} = -5.46V	$V_{\overline{RD}}$ = -0.81V, $V_{\overline{WT}}$ = -1.71V	1	—	—	0.2	mA
	I_{IWD}		V_{WD} = -0.81V	1	—	—	0.9	mA
	$I_{I\overline{WD}}$	V_{EE2} = -12.6V	$V_{\overline{WD}}$ = -0.81V	1	—	—	0.9	mA
	$I_{I\overline{WT}}$		$V_{\overline{RD}}$ = -1.71V, $V_{\overline{WT}}$ = -0.81V	1	—	—	0.15	mA
Output Voltage	V_{WC}	$V_{\overline{RD}}$ = -0.89V,	$V_{\overline{WT}}$ = -1.75V	1	4.9	5.4	5.9	V
	V_{DXH}	$V_{\overline{RD}}$ = 0.96V, $V_{\overline{WT}}$ = 1.65V	$V_{\overline{WD}}$ = -0.96V	1	-0.59	—	-0.45	V
	V_{DXL}		V_{WD} = -0.96V	1	-0.75	—	-0.61	V
	V_{DYH}			1	-0.59	—	-0.45	V
	V_{DYL}		$V_{\overline{WD}}$ = -0.96V	1	-0.75	—	-0.61	V
DxDy Differential Output Voltage	$\lvert V_{XY}\rvert$	$\lvert V_{DX} - V_{DY}\rvert$		1	160	—	—	mV
Voltage Gain	A_V	V_1 = 100mV_{PP}, f = 5MHz		2	0.95	1.1	1.25	V/V
Band Width	BW			2	30	—	—	MHz
Delay Time	t_{PLH1}	$\overline{WT}$ → RWC		3	—	—	350	ns
	t_{PLH1}			3	—	—	100	ns
	t_{PLH2}	RD → DX, DY		4	—	—	200	ns
	t_{PLH2}			4	—	—	100	ns

Measurement Diagram

1.



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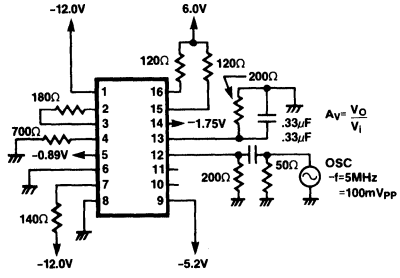

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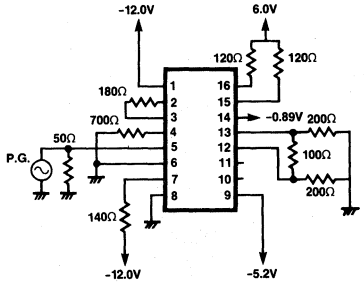

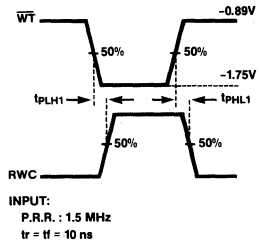

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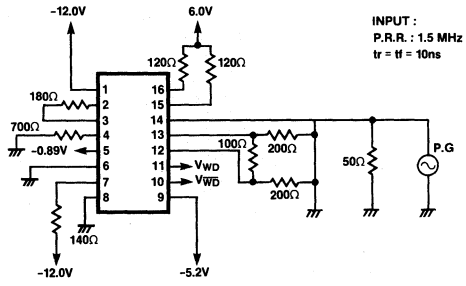

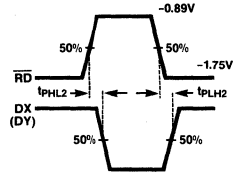

Output	Bias V_{WD}	V_{WD}
DX	−0.89V	-1.75V
DY	−1.75V	-0.89V

Package Dimensions

Dimensions in inches
(millimeters)

16-Lead Ceramic (Cerdip)
Dual In-Line Package
Dip-16C-C02