FUJITSU

ETHERNET ENCODER/DECODER

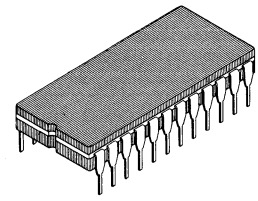
MB 502A

October 1983
Edition 2.0

ETHERNET ENCODER/DECODER

The Fujitsu MB 502A is an Ethernet* Encoder/Decoder designed to meet all the requirements of the Ethernet Blue Book specification and fabricated with high-speed ECL and Schottky TTL technology.

The encoder converts serial binary data into complementary Manchester code. The decoder converts Manchester code into binary data and synchronous clock signals. The decoding method is a digital phase locked loop with dual bandwidth which allows both fast lock-on and a small amount of jitter. Typical acquisition is eight bits or better. A key feature of the decoder design is its capability to recover distorted input signals. The MB 502A is packaged in a 24-pin ceramic standard DIP.

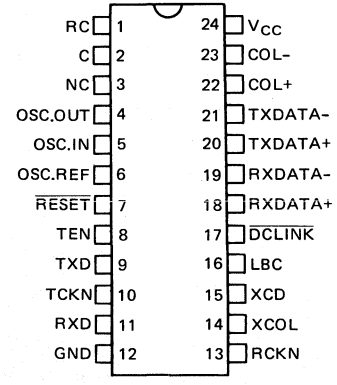


CERAMIC PACKAGE
DIP-24C-C01

FEATURES

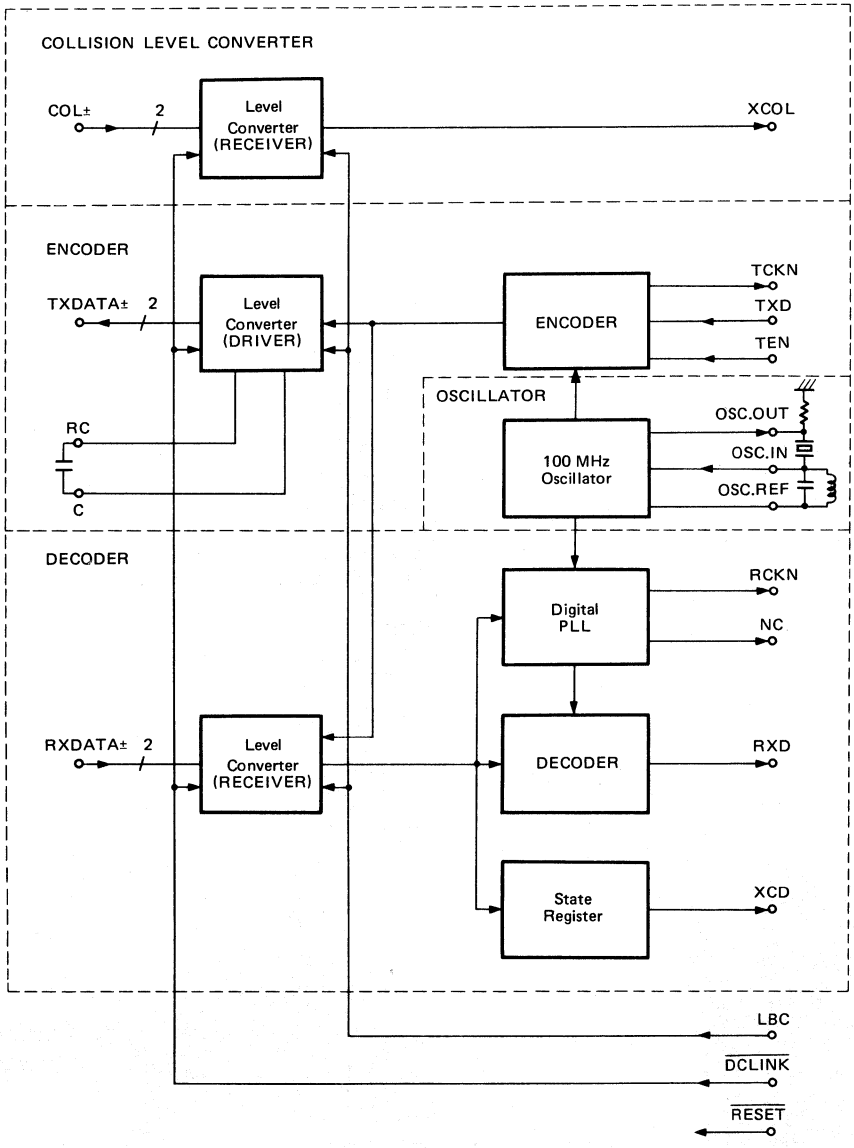
- Full Ethernet compatibility
- Manchester encode and decode
- Level conversion: transceiver level to/from TTL level
- Carrier detection
- Large distortion recovery: ±20 ns
- Dual bandwidth phase locked loop: allows fast acquisition
- Loopback "CONFIDENCE" test feature
- Built-in clock generator
- Small external parts count: all passive external components
- High-speed ECL and Schottky TTL technology
- Single power supply: +5V
- Low power dissipation: 750mW typ.
- 24-pin standard Dual In-line Ceramic Package

PIN ASSIGNMENT



*Ethernet is a trade mark of Xerox Corp. U.S.A.

Fig. 1 BLOCK DIAGRAM



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PIN ASSIGNMENT TABLE

Group	Pin Number	Symbol	Pin Name	I/O	Level	Function
Power Group	12	GND	Power supply	I		Ground
	24	V_{CC}		I		+5V DC power supply
Cable Group	18 19	RXDATA+ RXDATA-	Receive data pair	I I	ECL differential	Interfacing to receive pair of the transceiver cable.
	20 21	TXDATA+ TXDATA-	Transmit data pair	O O	ECL differential	Interfacing to transmit pair of the transceiver cable.
	22 23	COL+ COL-	Collision presence pair	I I	ECL differential	Interfacing to collision presence pair of the transceiver cable.
EDLC Group	8	TEN	Transmit encode enable	I	TTL	Input for encoding and TXDATA± enable.
	9	TXD	Transmit serial data	I	TTL	Input for transmit data to be encoded onto the Ethernet coax.
	10	TCKN	Transmit data clock	O	TTL	Stable 10MHz clock output for transmit bit stream.
	11	RXD	Receive serial data	O	TTL	Output of received and decoded bit stream.
	13	RCKN	Receive data clock	O	TTL	Clock output to strobe RXD.
	14	XCOL	Collision presence	O	TTL	Duplication of the collision presence pair (COL±).
	15	XCD	Receive carrier detect	O	TTL	Carrier detect function of the decoder.
	16	LBC	Loopback command	I	TTL	Input to command the MB502A to operate in loopback mode.
Oscillator Group	4 5 6	OSC. OUT OSC. IN OSC. REF	Oscillator pins	O I O	ECL	Pins for direct connection of discrete oscillator components.
Others	1 2	RC C	Capacitor pins	– –	ECL –	Pins for direct connection of a capacitor.
	3	NC	Non-connection (PLL test)	O	ECL	Output pin for PLL testing purpose only.
	7	$\overline{\text{RESET}}$	FF test	I	TTL	Input pin to initialize flip-flops for testing purpose only.
	17	$\overline{\text{DCLINK}}$	DC/AC coupling select for transceiver pairs	I	TTL	Input to select DC/AC coupling of transceiver cable pairs.

FUNCTIONAL DESCRIPTION

The MB 502A has five major functions; encode, decode, collision, master clock generation and loopback.

ENCODE

The encoder section of the MB 502A is a simple circuit which performs an appropriate exclusive-OR between the transmit clock and transmit data using latches to reduce the skew of TXDATA± outputs. The encoder sends the transmit clock (TCKN) to the Data Link controller. Then an encode enable signal (TEN) and data (TXD) are returned from the Data Link controller.

DECODE

The decoder performs three functions. First, it decodes data using the differential receive inputs (RXDATA+ and RXDATA-) of the transceiver cable. Next is the carrier detect function. The carrier is derived from the receive inputs and passed to the Data Link controller from the XCD output. The last function is the stripping of the first several bits (eight bits maximum) of the packet. This is not a part of the Ethernet Physical Layer specification. The receive clock (RCKN) is actually inhibited for 6 or 7 clock cycles to allow the PLL (phase locked loop) to gain acquisition. This function was designed into the Encoder/Decoder because the EDLC (Ethernet Data Link Controller, MB 8795B) is a byte oriented device, and the function is more appropriately provided in the Encoder/Decoder which is bit oriented.

The decoder PLL has excellent distortion handling capability. It is designed to recover ± 20ns exercised.

COLLISION

The collision detect inputs (COL+ and COL-) are simply converted to a TTL level signal (XCOL). The latching and timing functions for this signal are provided in the EDLC (MB 8795B).

MASTER CLOCK GENERATION

The oscillator generates and supplies a 100MHz master clock signal to the encoder and decoder.
Discrete oscillator components such as a crystal may be directly connected to the provided oscillator pins.
The oscillation frequency must be 100MHz with a tolerance of less than ±0.01% to meet the Ethernet specification because one tenth of the oscillation frequency is the transmit bit rate.

LOOPBACK

A loopback input is provided to allow all encoding and decoding functions to be exercised without using the transceiver cable. During loopback operation, the encoded data is routed internally to the decoder, the transmit outputs are idle, and the receive and collision inputs are ignored.

SIGNAL PIN DESCRIPTION

CABLE GROUP

RXDATA± (receive serial data pair, inputs)

These are the inputs to the decoder. They receive Manchester coded signals which the transceiver encounters on the Ethernet coax.

The input circuit is a differential receiver and can receive voltages of 0 to V_{CC}. The differential receiver has two operation modes; DC coupled operation and AC coupled operation, which are selected by $\overline{DCLINK}$ input.

In DC coupled operation ($\overline{DCLINK}$ is low), the differential threshold is typically 0V. The differential input voltage of more than 0.2V is regarded as high level and the differential input voltage of less than -0.2V is regarded as low level.

In AC coupled operation ($\overline{DCLINK}$ is high), the differential threshold is typically -0.2V. A differential input voltage of more than -0.05V is regarded as high level and a differential input voltage of less than -0.4V is regarded as low level.

The receiver circuit is designed to supply a high level to the decoder when RXDATA+ and RXDATA- are not receiving data but are just short-circuited through a transformer coil or left unconnected. However, when RXDATA± are receiving data, the differential threshold is typically 0V to minimize receiving distortion.

TXDATA± (transmit data pair, outputs)

These are the outputs of the encoder. They transmit Manchester coded signals to the transceiver.

The driver output circuit is an emitter-follower and requires a pull-down resistor (270Ω typ.). It can drive a transceiver cable differential impedance of 78Ω.

The differential transmitter outputs (TXDATA+ and TXDATA-) also have the ability to emulate a transformer drive. This is actually implemented to reduce the current involved in a transformer termination of the transmit outputs in the transceiver which has a DC resistance of zero ohms. After the encoding function stops, the transmitter outputs gradually return to a 0V differential between the two output wires. The returning time is determined by an external capacitor connected between the RC and C pins.

COL± (collision presence pair, inputs)

This pair of signals indicates the presence of a collision generated by the transceiver.

The input circuit is a differential receiver and can receive voltages of 0V to V_{CC}. The differential receiver has two operation modes; DC coupled operation and AC coupled operation, which are selected by $\overline{DCLINK}$ input.

In DC coupled operation ($\overline{DCLINK}$ is low), the differential threshold is typically 0V. A differential input voltage of more than 0.2V is regarded as high level and a differential input voltage of less than -0.2V is regarded as low level.

In AC coupled operation ($\overline{DCLINK}$ is high), the differential threshold is typically -0.2V. A differential input voltage of more than -0.05V is regarded as high

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level and a differential input voltage of less than -0.4V is regarded as low level.
The receiver circuit is designed to supply a high level to the level converter when COL+ and COL- are not receiving data but are just short-circuited through a transformer coil or left unconnected.
Unlike RXDATA±, the differential threshold is set to -0.2V even when COL± are receiving data.

EDLC GROUP

TEN (transmit encode enable, input)
This is an input to the on-chip Manchester encoder and enables TXDATA pair. Input high enables TXDATA pair; input low makes TXDATA pair idle (high).

TXD (transmit serial data, input)
This is an input to the on-chip Manchester encoder and provides data to be encoded.
Serial binary data must be supplied to this input synchronously with the falling edge of TCKN (transmit data clock).
This input is enabled when TEN (transmit encode enable) is high.

TCKN (transmit data clock, output)
10MHz clock output for the transmit serial binary data. This is stable one-tenth of the master clock frequency. See TXD (transmit serial data) description.

RXD (receive serial data, output)
This is an output of the on-chip Manchester decoder and provides decoded data from Ethernet coax to a Data Link controller.
This output is synchronous with the falling edge of RCKN (receive data clock).

RCKN (receive data clock, output)
Clock output to strobe RXD (receive serial data). See RXD (receive serial data) description.
At the beginning of a packet, RCKN is inhibited for 6 or 7 clock cycles to allow the PLL to gain acquisition. And at the end of a packet, RCKN is inhibited for 1 clock cycle.
During idle state, this output generates a 10MHz clock signal.

XCOL (collision presence, output)
This is a TTL duplication of the collision presence pair (COL±). The transceiver connected to Ethernet coax supplies a high level or differential voltage of 0V to COL ± when collision is not seen on the coax. It supplies a 10MHz square wave signal to COL ± when collision is detected. Accordingly, XCOL outputs high level when collision is not seen and outputs a 10MHz square wave signal during collision presence.

XCD (receive carrier detect, output)
This output provides carrier detect function of the Manchester decoder. This signal is used by a Data Link controller receiver as a data acquisition enable signal and by a Data Link controller transmitter as transmition permission information.
Output is low when the Ethernet coax is idle.

LBC (loopback command, input)
High level input to this pin dictates loopback mode operation. During the loopback mode operation,
XCOL output is high level,
TXDATA+ output is high level,
RXDATA± inputs are ignored
and the data supplied to TXD (transmit serial data) when TEN (transmit encode enable) is high is encoded, supplied to the Manchester decoder through the internal route and output from RXD (receive serial data), RCKN (receive data clock) and XCD (receive carrier detect).

OSCILLATOR GROUP

OSC.OUT, OSC.IN AND OSC.REF (oscillator pins)
A 100MHz crystal is to be placed between OSC.IN and OSC.OUT.
An LC tank circuit is to be placed between OSC.IN and OSC.REF to assure start-up in the proper harmonic of the crystal.
OSC.OUT is an emitter-follower output and requires a pull-down resistor (330Ω typ.). A phase adjusting capacitor is to be placed in parallel with the pull-down resistor to make the delay through the oscillator close to 10ns to increase the efficiency of the crystal.

As a design recommendation, connection wires should be as short as possible.

OTHERS

RC and C (capacitor pins)
A capacitor placed between these pins provides the timing for the transformer emulation of the transmit pair.
In AC coupled operation ($\overline{\text{DCLINK}}$ is high), after data transmission, TXDATA- goes high with rise time determined by the time-constant of the internal resistor and the connected capacitor. When a 470pF capacitor is connected, the rise time of TXDATA- is typically 0.8μs (20% to 80%).

Because pin C is connected to V_{CC} on chip, DC voltage must never be supplied to this pin.

$\overline{\text{DCLINK}}$ (DC/AC coupling select for transceiver pair)
This input is to select DC/AC coupling of transceiver cable pairs. Low level selects DC coupling. High level selects AC coupling and makes both TXDATA+ and TXDATA- high during idle state to prevent the transformer from saturation.
See CABLE GROUP description.

This pin must be stuck at high or low level. It may be connected directly to V_{CC} or ground.

$\overline{\text{RESET}}$ (FF testing purpose only)
This input pin is to initialize flip-flops for testing purposes only and must be connected to V_{CC} or stuck at high level in a normal operation.

NC (non-connection)
This output pin is for testing purposes only and must be left open in a normal operation.

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to 7.0	V
TTL Level Input Voltage	V_{ITTL}	-0.3 to 7.0	V
Receiver Input Voltage	V_{IR}	-0.3 to V_{CC} + 0.3	V
Driver Output Voltage	V_{ODV}	V_{CC} (max)	V
Driver Output Current	I_{ODV}	-40.0 to 0	mA
Oscillator Input Voltage	V_{IOSC}	V_{CC}-4 to V_{CC}, and more than -0.3	V
Oscillator Output Current	I_{OOSC}	-20.0 to 0	mA
Operating Temperature	T_{OP}	-25 to 100	°C
Storage Temperature	T_{STG}	-65 to 125	°C

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as destailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value	Operating Temperature
Supply Voltage		V_{CC}	5.0V ± 5%	0°C to +70°C
TTL High Level Output Current		I_{OH}	-0.4 mA to 0 mA	
TTL Low Level Output Current		I_{OL}	0 mA to 8 mA	
Receiver Input Voltage		V_{IR}	0V to V_{CC}	
Driver Terminator		R_{LD}	270Ω	
Differential Load		R_{DLD}	78Ω	
Oscillator Terminator		R_{LOSC}	330Ω and 33pF parallel*	
Crystal for Oscillator		f_{XTAL}	100 MHz ± 0.01%**	
Capacitor placed between C and RC pins		C_{TX}	470pF	
LC Tank Constant	Inductance	L_{OSC}	0.15 μH	
	Capacitance	C_{OSC}	33pF*	

* The values of the oscillator capacitors may have to be tuned for a particular components layout. Both capacitors should be adjusted for maximum voltage at OSC.IN.
However, once the correct values are determined for that layout, any more tuning will not be necessary for each board.
** 5th overtone series resonant.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
			V_{CC} (V)	min.	typ.	max.	
High Level Input Voltage *1	V_{IH}			2.0			V
Low Level Input Voltage *1	V_{IL}					0.8	V
Input Clamp Voltage *1	V_{IC}	I_{IL} = -18mA	4.75	-1.5			V
High Level Output Voltage *2	V_{OH}	I_{OH} = -0.4mA	4.75	2.7			V
Low Level Output Voltage *2	V_{OL}	I_{OL} = 8mA	4.75			0.5	V
High Level Input Current *1	I_{IH}	V_{IH} = 2.7V	5.25			20	μA
Low Level Input Current *1	I_{IL}	V_{IL} = 0.4V	5.25	-100			μA
Output Short Current *2	I_{OS}	V_O = 0V	5.25	-100		-20	mA
High Level Differential Input Voltage *3	V_{IHD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V		0.2			V
Low Level Differential Input Voltage *3	V_{ILD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V				-0.2	V
High Level Differential Input Voltage *4	V_{IHD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V		-0.05			V
Low Level Differential Input Voltage *4	V_{ILD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V				-0.4	V
High Level Differential Input Voltage *5	V_{IHD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V		0.2			V
Low Level Differential Input Voltage *5	V_{ILD}	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V				-0.2	V
High Level Input Current *3	I_{IHR}	V_{IR} = 5.25V, $\overline{DCLINK}$ = 0V	5.25			0.7	mA
Low Level Input Current *3	I_{ILR}	V_{IR} = 0V, $\overline{DCLINK}$ = 0V	5.25	-1.5			mA

Note: 1: Applicable to TTL input pins. (TEN, TXD, LBC, $\overline{DCLINK}$ and $\overline{RESET}$)
2: Applicable to TTL output pins. (TCKN, RXD, RCKN, XCOL and XCD)
3: Applicable to COL± and RXDATA±.
4: Applicable to RXDATA± while XCD output is low (idle state) and COL±.
5: Applicable to RXDATA± while XCD output is high.

DC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
			V_{CC}(V)	min.	typ.	max.	
High Level Output Voltage *1	V_{OHTX}		5.0		4.1		V
Low Level Output Voltage *1	V_{OLTX}		5.0		3.3		V
High Level Differential Output Voltage *1	V_{OHD}	$\frac{V_{O+} - V_{O-}}{\overline{DCLINK} = 0V}$		0.55		1.0	V
Low Level Differential Output Voltage *1	V_{OLD}	$\frac{V_{O+} - V_{O-}}{\overline{DCLINK} = 0V}$		-1.0		-0.55	V
Oscillator Reference Voltage *2	V_{BB}		5.0		3.7		V
High Level Input Current *3	I_{IHO}	V_{IH} = 4.1V	5.0			150	μA
High Level Output Voltage *4	V_{OHO}	OSC.IN is open	5.0		4.15		V
Low Level Output Voltage *4	V_{OLO}	V_{IOSC} = 4.1V	5.0		3.3		V
RC Internal Resistor	R_{RC}	V_{RC} = 0.5V	0.5	25	50	100	kΩ
Power Supply Current	I_{CC}	All signal pins are open.	5.25			220	mA

Note: 1: Applicable to TXDATA±.
These pins are connected to ground through 270Ω resistor. And 78Ω resistor is placed between these pins.
2: Applicable to OSC.REF.
3: Applicable to OSC.IN.
4: Applicable to OSC.OUT.
This pin is connected to ground through a 330Ω resistor.

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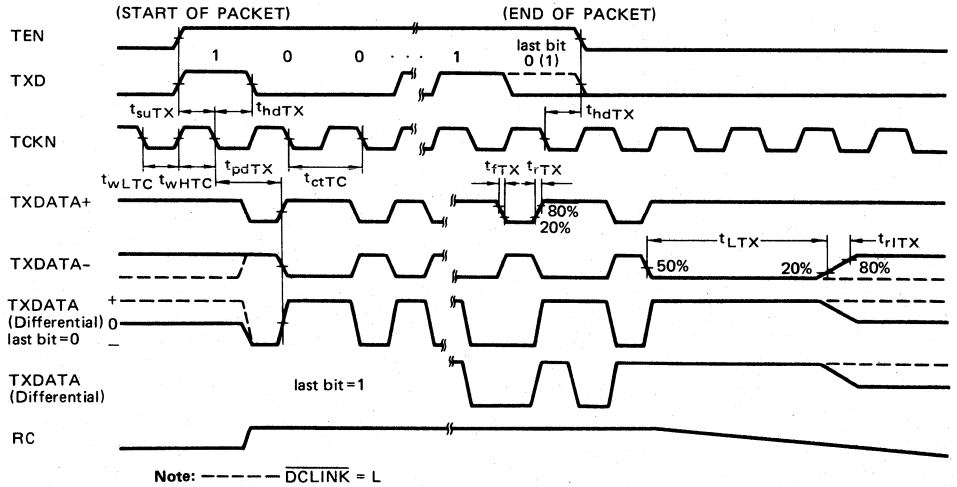
AC CHARACTERISTICS

TRANSMIT TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition	Value				Unit
			Fig.	min.	typ.	max.	
TCKN Cycle Time	t_{ctTC}		2, 3	99.99	100.00	100.01	ns
TCKN Low Time	t_{wLTC}		2, 3	40	50		ns
TCKN High Time	t_{wHTC}		2, 3	40	50		ns
TXDATA± Encode Time	t_{pdTX}		2, 3 5, 6		95		ns
TXDATA± Output Rise Time	t_{rTX}		5, 6		2.0		ns
TADATA± Output Fall Time	t_{fTX}		5, 6		2.0		ns
TXDATA- Low Level Hold Time	t_{LTX}	C_{TX} = 470pF $\overline{DCLINK}$ = V_{CC}	5, 6		3		μs
TXDATA- Idling Rise Time	t_{rITX}	C_{TX} = 470pF (20% ~ 80%) $\overline{DCLINK}$ = V_{CC}	5, 6		0.8		μs
TXD, TEN Setup Time	t_{suTX}		4	20			ns
TXD, TEN Hold Time	t_{hdTX}		4	0			ns

TRANSMIT TIMING DIAGRAM



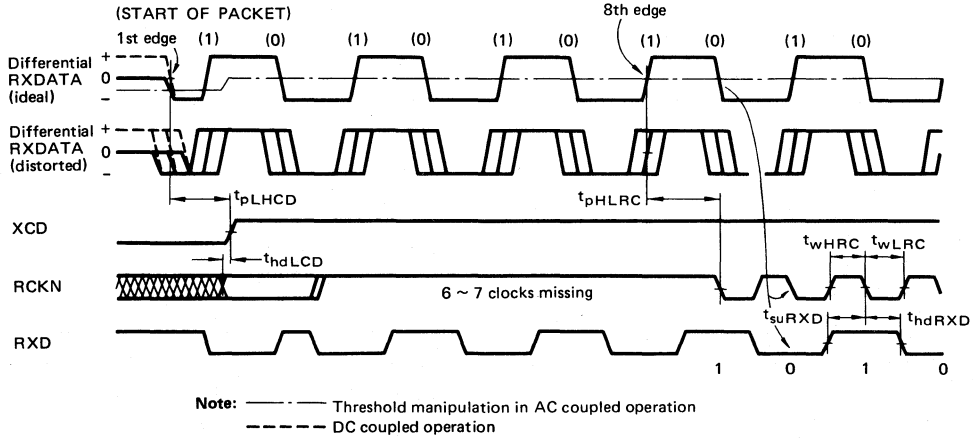
AC CHARACTERISTICS (Cont'd)

RECEIVE TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition	Value				Unit
			Fig.	min.	typ.	max.	
RCKN Cycle Time in Idle	t_{ctRC}		2, 3	99.99	100.00	100.01	ns
RCKN Low Time	t_{wLRC}		2, 3	35	50		ns
RCKN High Time	t_{wHRC}		2, 3	35	50		ns
RCKN Delay Time	t_{pHLRC}		2, 3, 7		120		ns
XCD ON Delay Time	t_{pLHCD}		2, 3, 7		80	110	ns
XCD OFF Delay Time	t_{pHLCD}		2, 3, 7		230		ns
XCD Low Hold Time	t_{hdLCD}		2, 3	0	10		ns
XCD High Hold Time	t_{hdHCD}		2, 3		120		ns
XCD Low Setup Time	t_{suLCD}		2, 3		80		ns
RXD Setup Time	t_{suRXD}		2, 3	20	60		ns
RXD Hold Time	t_{hdRXD}		2, 3	10	20		ns

RECEIVE TIMING DIAGRAM



Note: ——·—— Threshold manipulation in AC coupled operation
– – – – – DC coupled operation

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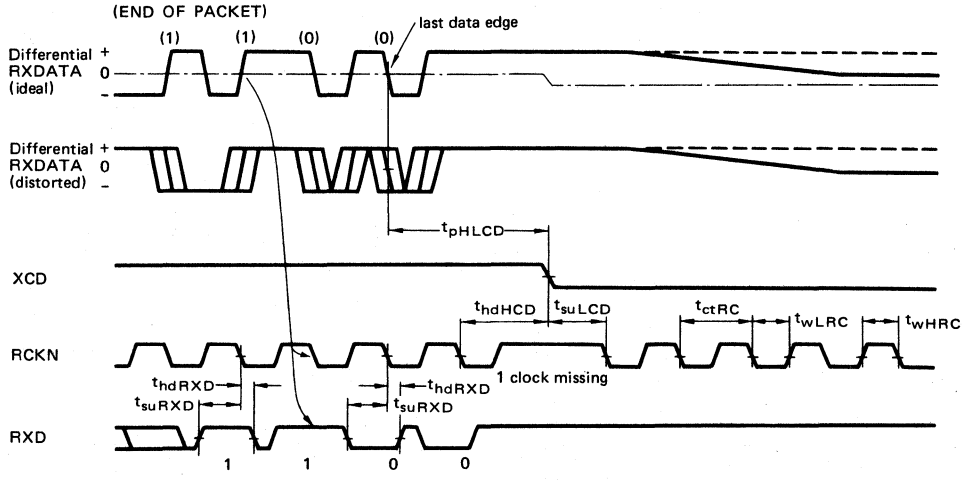
AC CHARACTERISTICS (Cont'd)

RECEIVE TIMING DIAGRAM (Cont'd)



Note: —·— Threshold manipulation in AC coupled operation

— — — — DC coupled operation

AC CHARACTERISTICS (Cont'd)

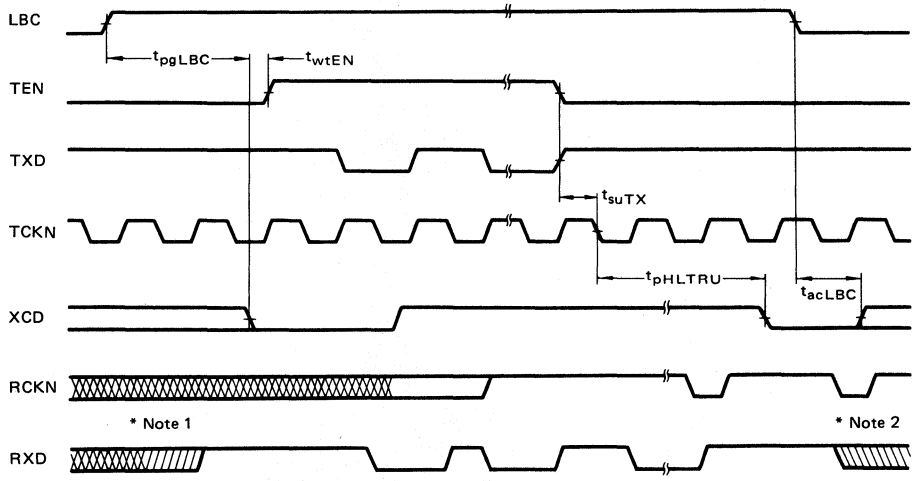
LOOPBACK TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition	Value				Unit
			Fig.	min.	typ.	max.	
LBC Receiving Data Purge Time	t_{pgLBC}		2, 3, 4		230		ns
LBC Receiving Data Accept Time	t_{acLBC}		2, 3, 4		80		ns
DATA Through Time	t_{pHLTRU}		2, 3, 4		280		ns
TEN Wait Time	t_{wtEN}		2, 3, 4	0			ns

In Loopback mode operation, COL± and RXDATA± inputs are ignored, TXDATA+ and XCOL are high level and XCD, RCKN and RXD functions are in the same manner as a normal receive operation.

LOOPBACK TIMING DIAGRAM



Note 1: When RXDATA± are receiving a packet at LBC rising, the received data is not complete.
Note 2: When RXDATA± are receiving a packet at LBC falling, the packet may not be decoded correctly.

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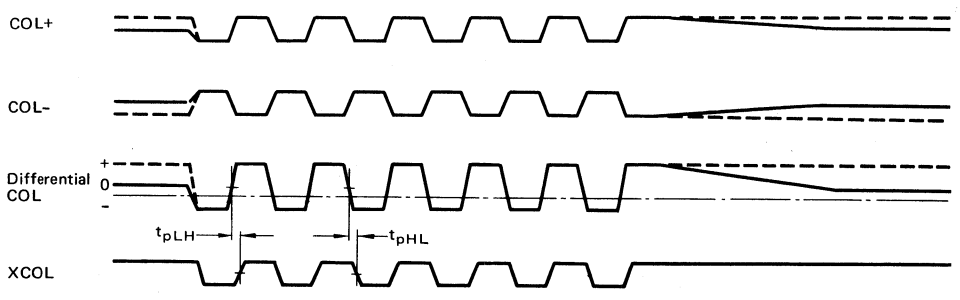
AC CHARACTERISTICS (Cont'd)

COLLISION TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition	Value			Unit
			Fig.	min.	typ.	max.	
COL to XCOL Propagation Delay Time	t_{pLH}	$\overline{DCLINK}$ = 0V	2, 3, 7		9	30	ns
COL to XCOL Propagation Delay Time	t_{pHL}	$\overline{DCLINK}$ = 0V	2, 3, 7		11	30	ns

COLLISION TIMING DIAGRAM



Note: —·— Threshold manipulation in AC coupled operation

– – – – DC coupled operation

AC CHARACTERISTICS (Cont'd)

AC TEST CONDITIONS

Fig. 2 TTL OUTPUT LOAD CIRCUIT

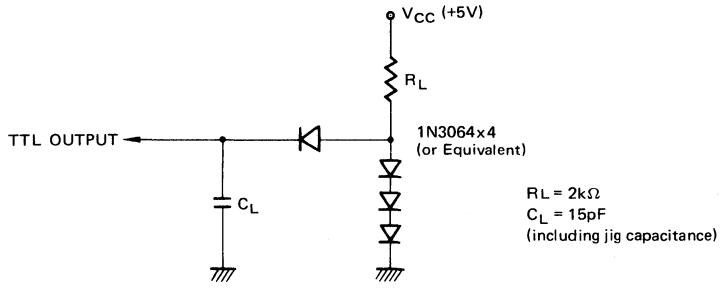
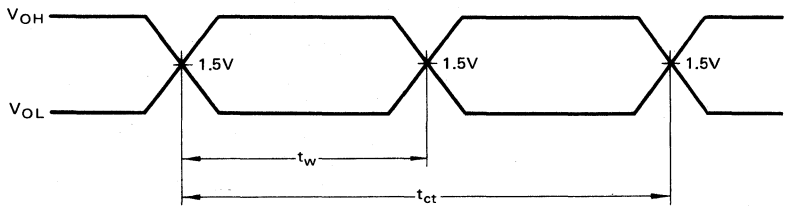
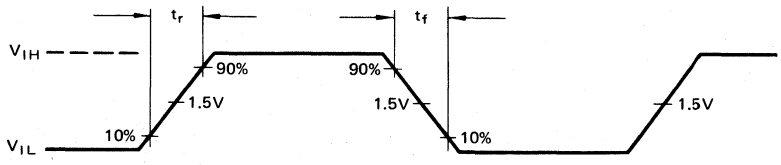


Fig. 3 TTL OUTPUT WAVEFORM



Threshold voltage = 1.5V

Fig. 4 TTL INPUT WAVEFORM



V_{IH} = 3V, V_{IL} = 0V
$t_r = t_f$ = 10ns
Threshold voltage = 1.5V

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AC CHARACTERISTICS (Cont'd)

AC TEST CONDITIONS (Cont'd)

Fig. 5 TXDATA± OUTPUT LOAD CIRCUIT

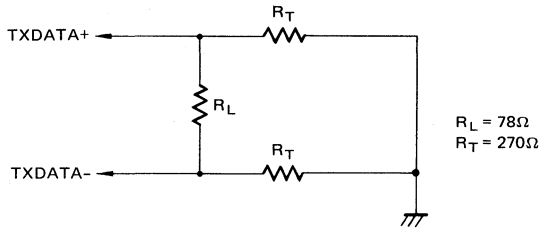


Fig. 6 TXDATA± OUTPUT WAVEFORM

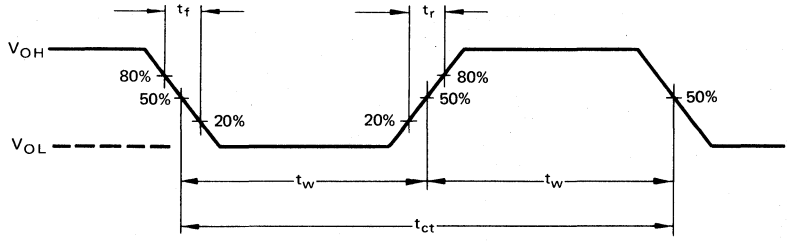
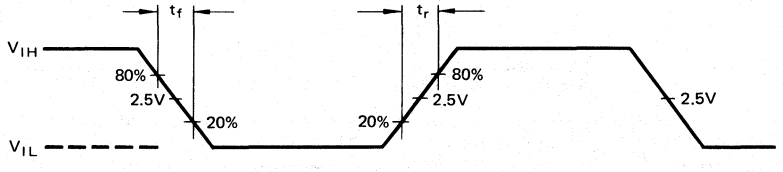


Fig. 7 RXDATA+, COL+ INPUT WAVEFORM



V_{IH} = 3.5V, V_{IL} = 1.5V
t_r = t_f = 2.0ns

RXDATA-, COL- Input voltage = 2.5V (DC)
$\overline{\text{DCLINK}}$ = 0V (DC coupling)

TYPICAL CHARACTERISTICS CURVES

Fig. 8
TXDATA±
Output Voltage vs. Output Current

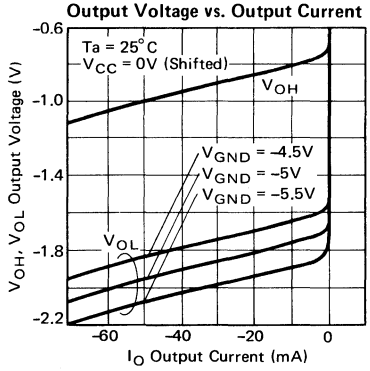


Fig. 9
RXDATA±, COL±
Input Current vs. Input Voltage

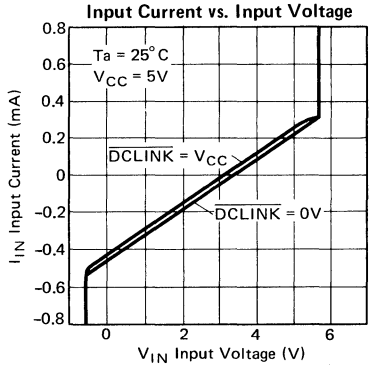


Fig. 10
TTL-OUTPUT
High Level Output Current vs.
High Level Output Voltage

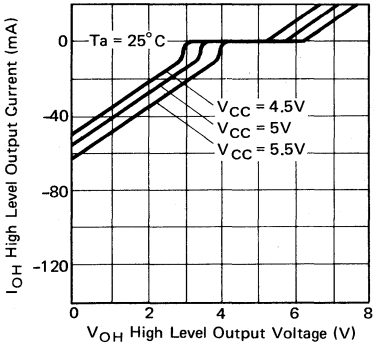


Fig. 11
TTL-OUTPUT
Low Level Output Current vs.
Low Level Output Voltage

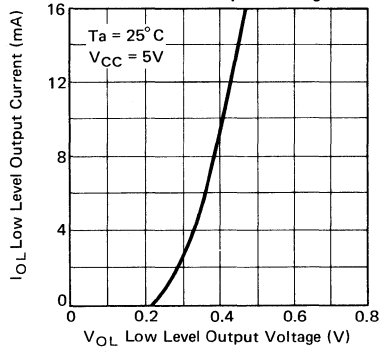


Fig. 12
TTL-INPUT
Input Current vs. Input Voltage

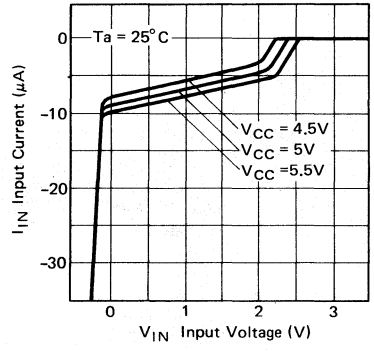
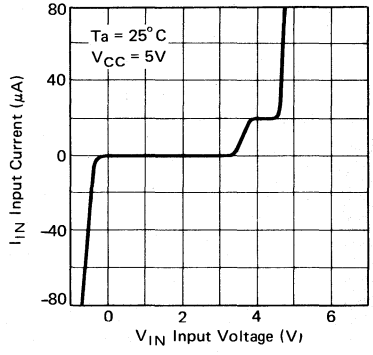


Fig. 13
OSC.IN
Input Current vs. Input Voltage



5

Fig. 14
COL± to XCOL TRANSFER (Receiver Threshold)
Output Voltage vs. Differential Input Voltage

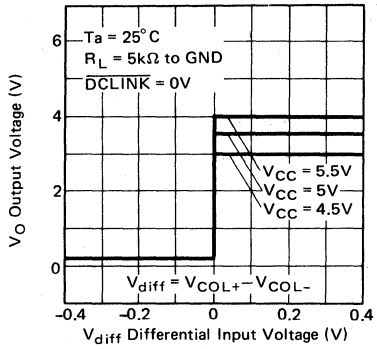


Fig. 15
COL± to XCOL TRANSFER (Receiver Threshold)
Output Voltage vs. Differential Input Voltage

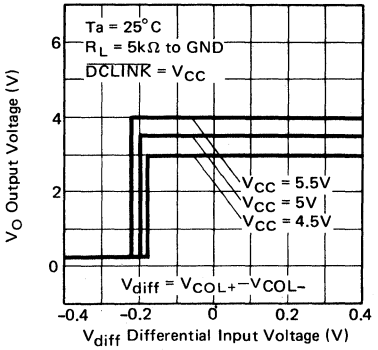


Fig. 16
TTL-INPUT THRESHOLD
TTL Input Threshold vs. Power Supply Voltage

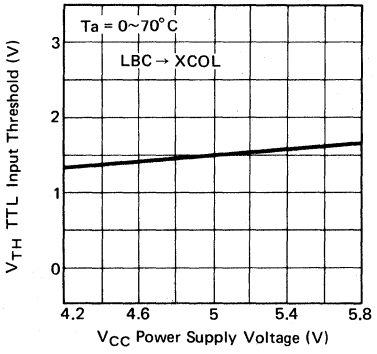


Fig. 17
RC to TXDATA- TRANSFER
Output Voltage vs. RC Input Voltage

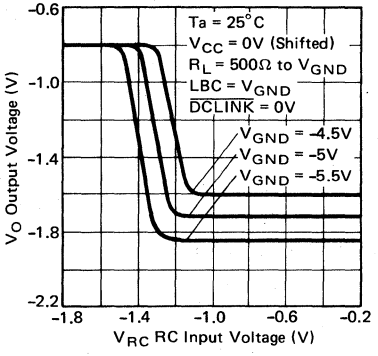


Fig. 18
TXDATA- LOW LEVEL HOLD TIME
TXDATA- Low Level Hold Time
TXDATA- Idling Rise Time vs. RC Capacitance

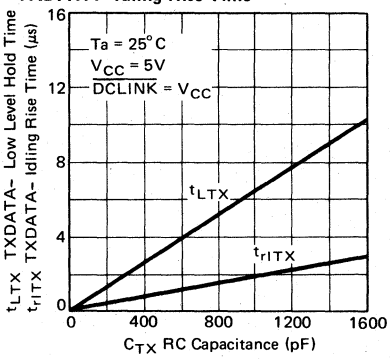
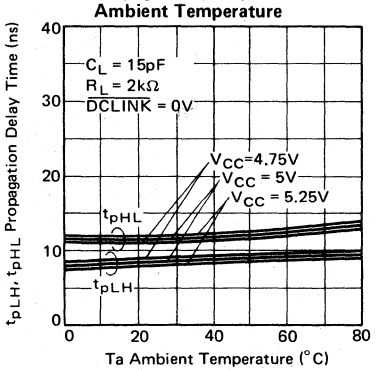
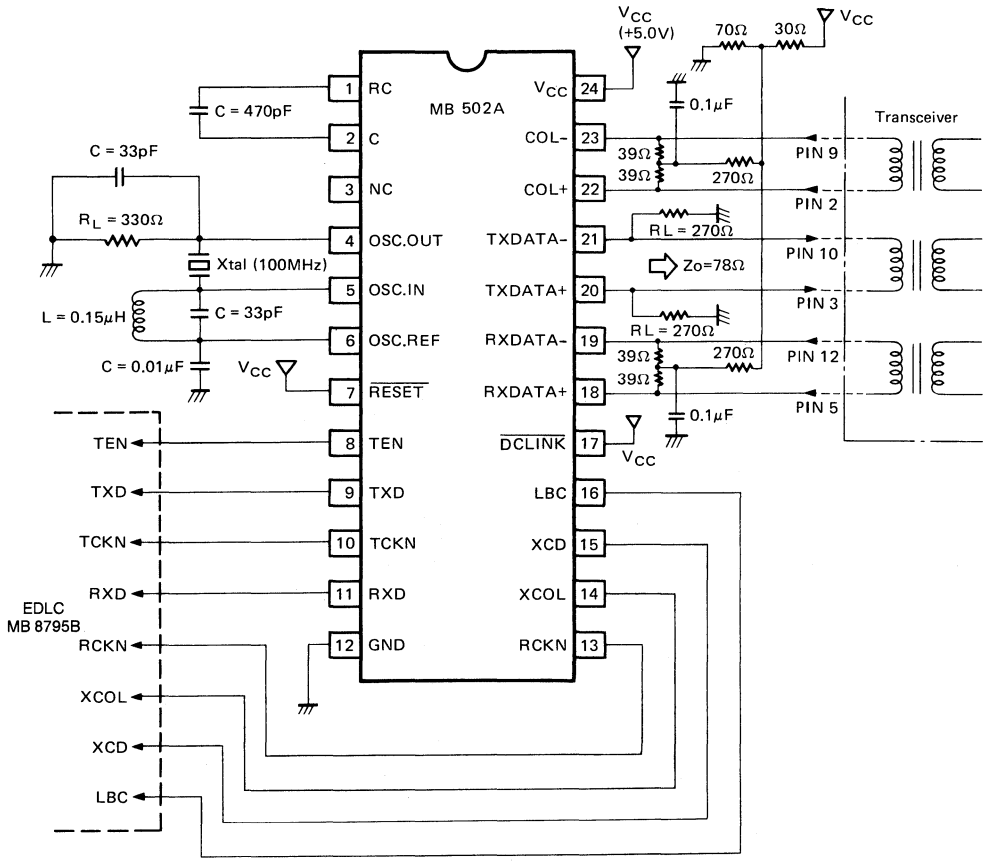


Fig. 19
COL± to XCOL PROPAGATION DELAY TIME
Propagation Delay Time vs.
Ambient Temperature



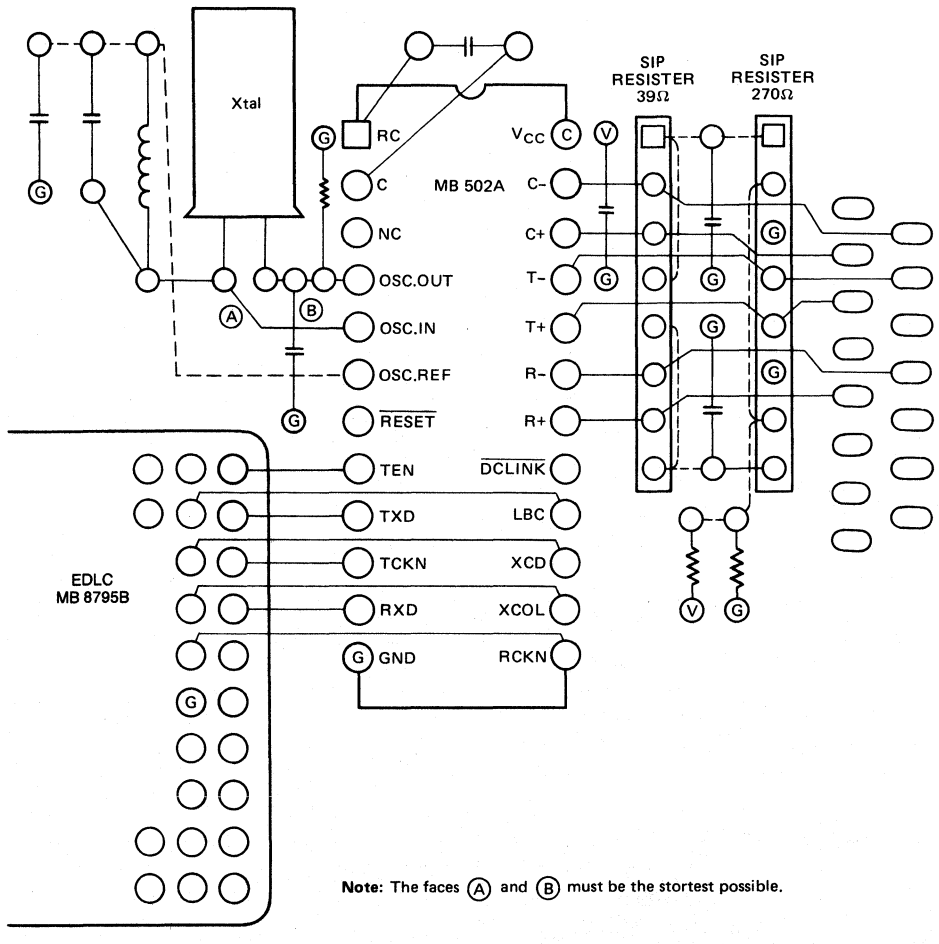
APPLICATION INFORMATION

Fig. 20 TYPICAL APPLICATION CIRCUIT



Note: 39Ω resistors must be balanced less than 1%.

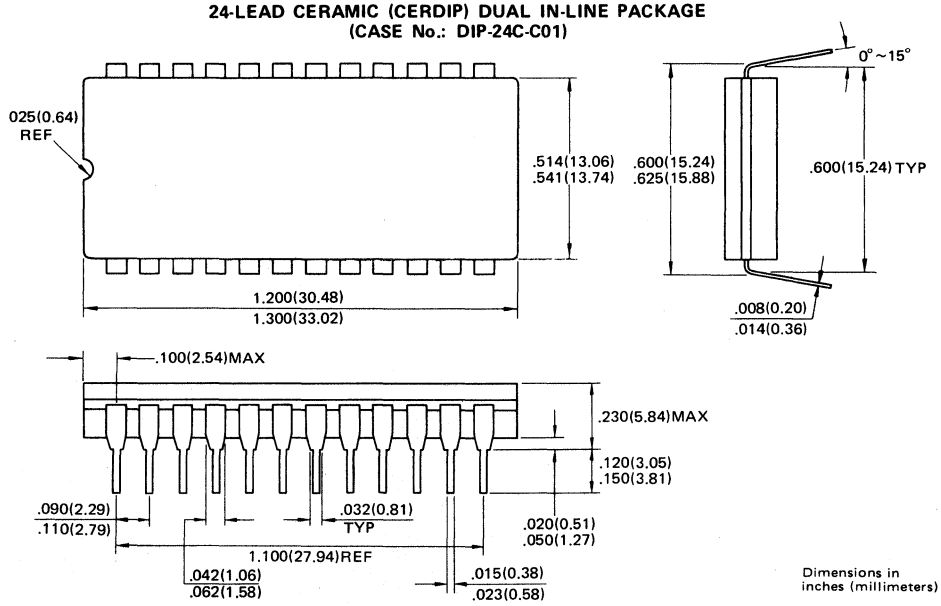
Fig. 21 TYPICAL COMPONENT LAYOUT



Note: The faces (A) and (B) must be the stortest possible.

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



Dimensions in inches (millimeters)

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