Sept. 1995
Edition 3.0b

DATA SHEET

MB510

2.7GHz TWO MODULUS PRESCALER

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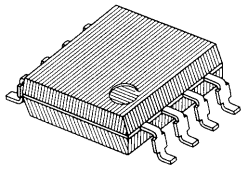
The Fujitsu MB510 is an ultra high speed, two modulus prescaler that forms a Phase Locked Loop (PLL) when combined with a frequency synthesizer such as the Fujitsu MB87001A. It divides the input frequency by the modulus of 128/144 or 256/272, and operates at a low power supply current of 10mA at 5.0V.

Through the use of Fujitsu's Advanced Process Technology, the MB510 achieves extremely small stray capacitance from its internal elements.

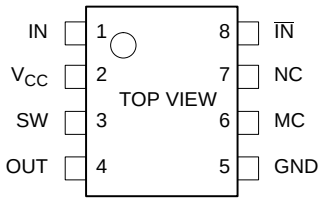


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation: 2.7GHz max.
- Power Dissipation: 50mW typ.
- Pulse Swallow Function: 128/144, 256/272
- Wide Operation Temperature: -40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6V_{p-p} typ.
- Built–in Termination Resistor
- Complete PLL synthesizer circuit with the Fujitsu MB87001A PLL synthesizer IC
- Package
  Standard 8-pin Flat Package (Suffix: –PF)

PIN ASSIGNMENT

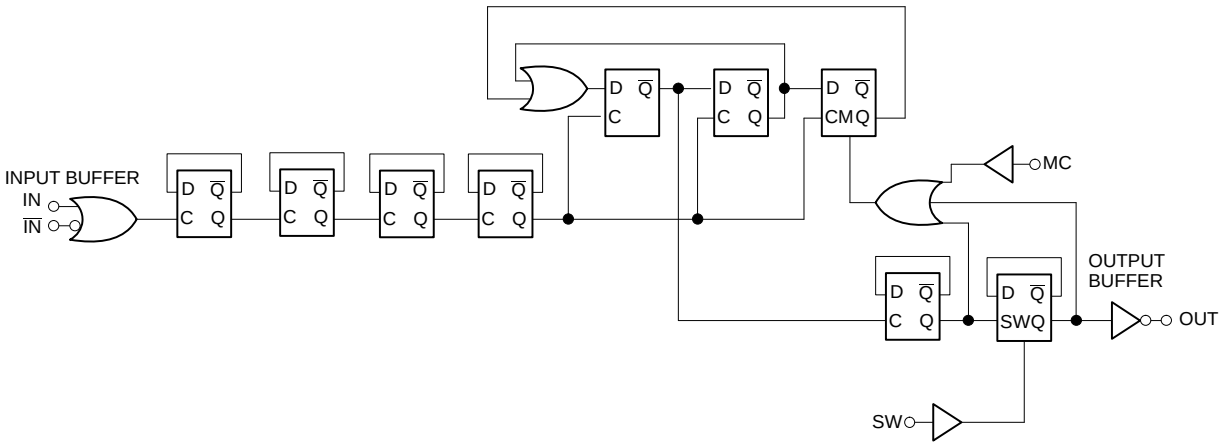


ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



SW	MC	Divide Ratio
H	H	1/128
H	L	1/144
L	H	1/256
L	L	1/272

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC}, L = GND to 0.8V

Figure 1. MB510 Block Diagram

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Curent	I_{CC}			10.0	15.0	mA
Output Amplitude	V_O	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10		2700	MHz
Input Signal Amplitude	P_{IN}	f_{IN} = 10 to 2200MHz	–10		10	dBm
		f_{IN} = 2200 to 2700MHz	–4		10	
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}				0.8	V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input	V_{ILS}		Open			V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	–0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}			16	26	ns

Note: *Design Guarantee

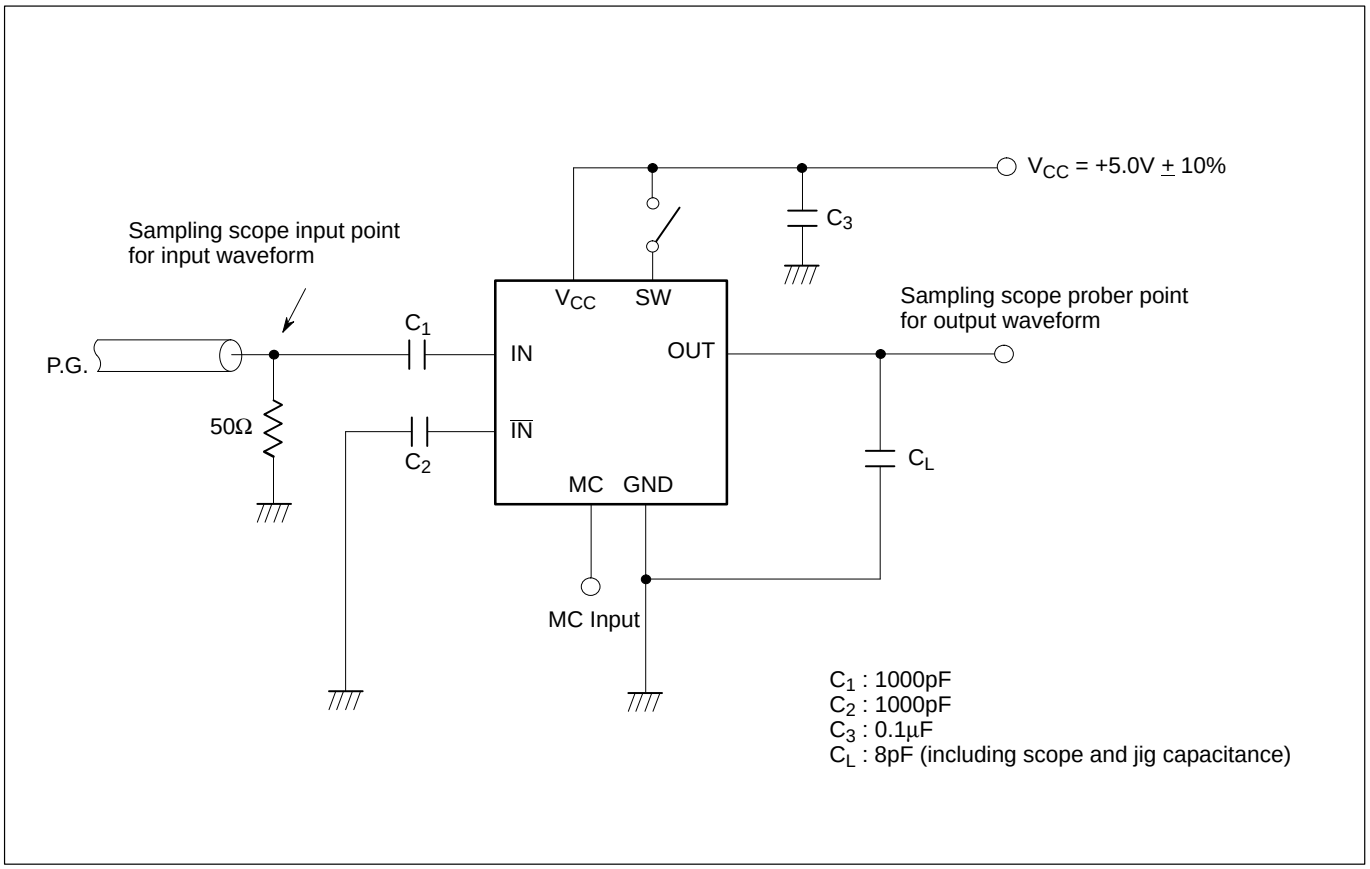


Figure 2. Test Circuit

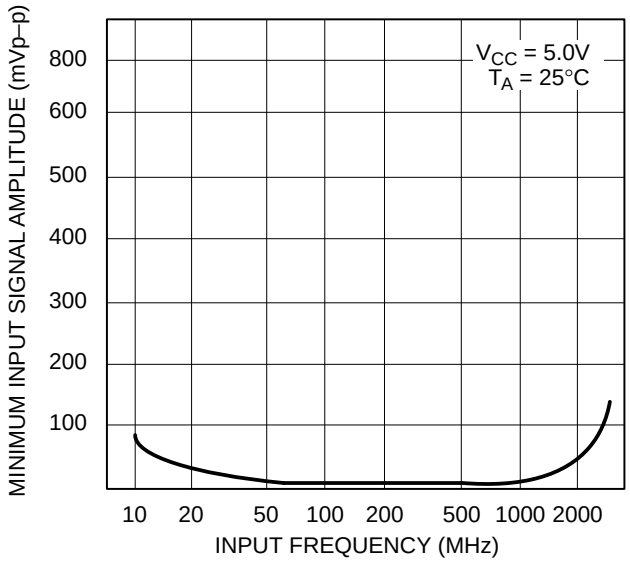
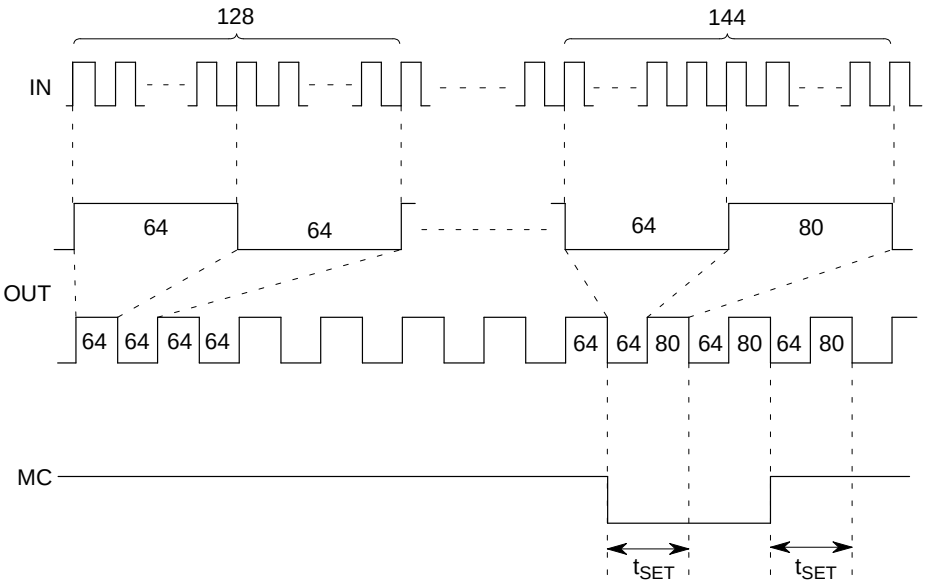


Figure 3. Input Signal Amplitude vs. Input Frequency

TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/144



Note: When divide of 144 is selected, positive pulse is applied by 16 to 80.
The typical set up time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

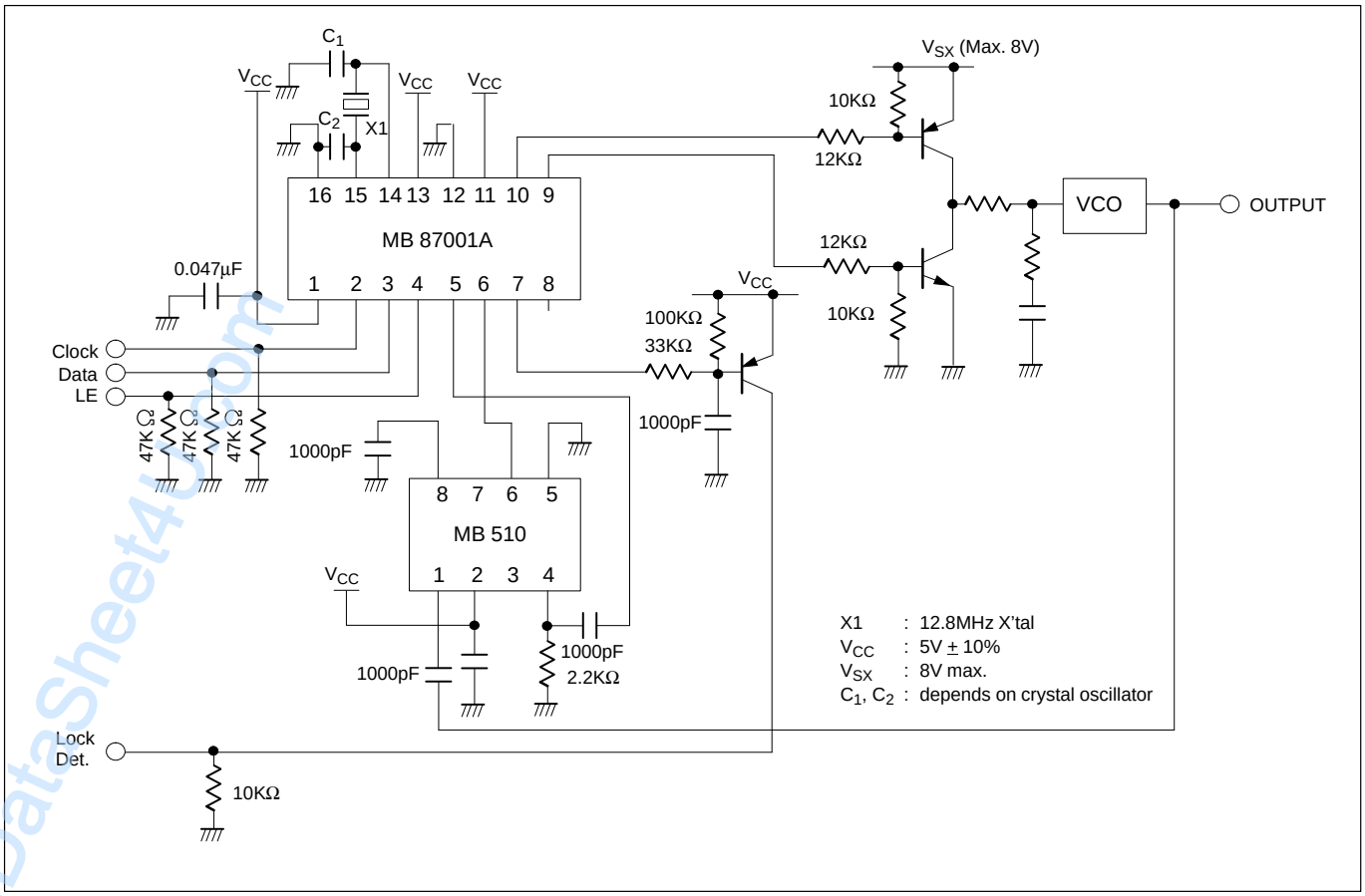
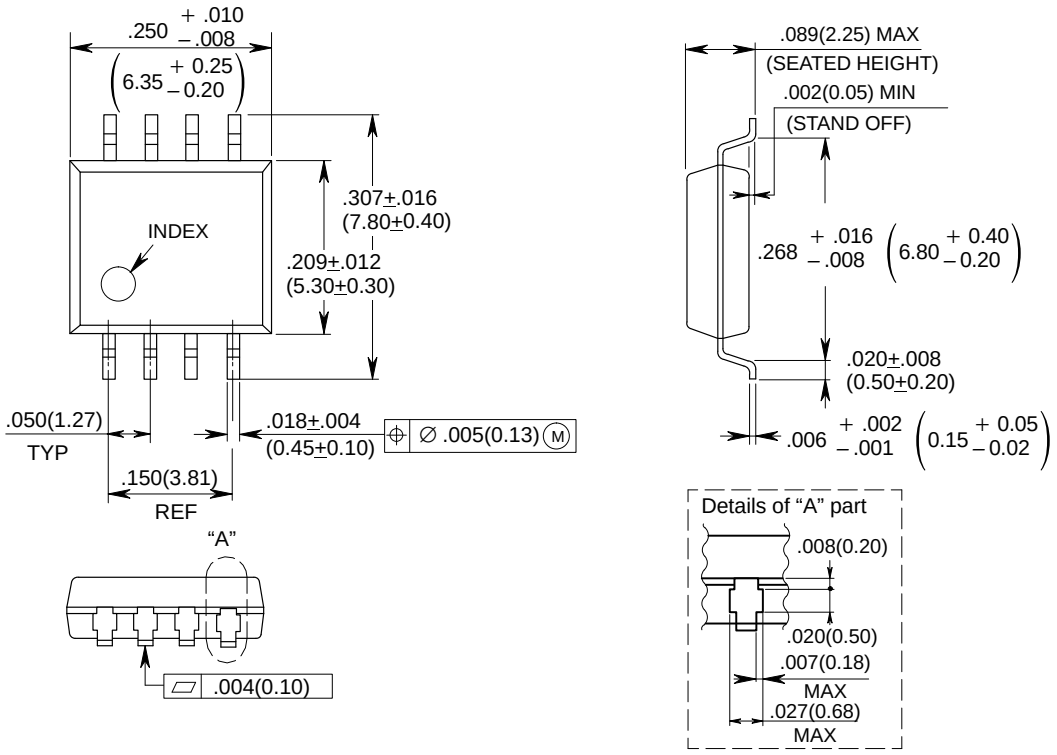


Figure 4. Typical Application Example

PACKAGE DIMENSIONS

(Suffix: –PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No: FPT-08P-M01)



DImensions in
inches (millimeters)