MB7130E
MB7130H

HIGH SPEED SCHOTTKY TTL 8192-BIT PROM

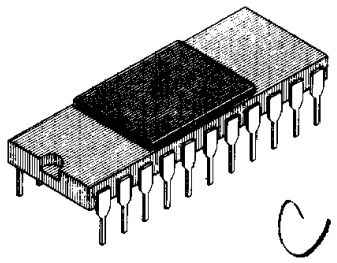
DESCRIPTION

The Fujitsu MB7130 is a high speed Schottky TTL electrically field programmable read only memory organized as 1024 words by 8-bits. With three-state outputs on the MB7130, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon), with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming tests prior to shipment. This results in extremely high programmability.

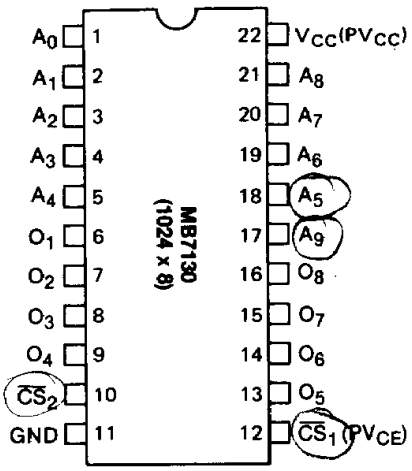


CERAMIC PACKAGE
DIP-22C-F01

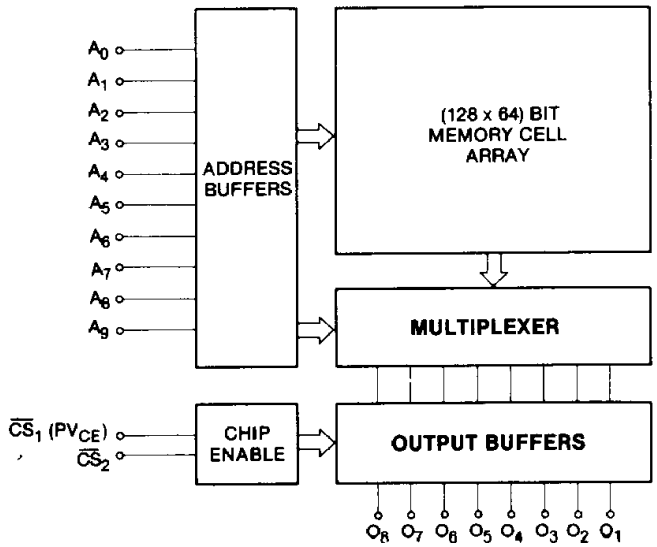
FEATURES

- **Organization: 1024 words by 8-bits, fully decoded**
- **TTL compatible inputs/output**
- **Fast Access Time:**
  MB7130E: 55 ns Max.
  30 ns Typ.
  MB7130H: 45 ns Max.
  30 ns Typ.
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Single +5V supply voltage**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Simplified and lower power programming**
- **Three-state outputs**
- **Two chip enable leads for simplified memory expansion**
- **Standard 22-pin DIP package**

PIN ASSIGNMENT



MB7130 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to $+V_{CC}$	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

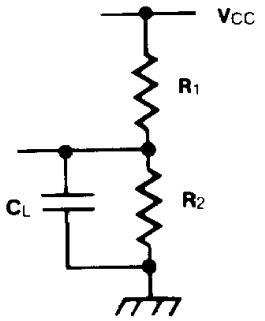
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)	I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)	I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)	I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)	V_{OL}	—	—	0.50	V
Output Leakage Current (V_{OL} = 2.4V, chip disabled from a low)	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.45V, chip disabled from a high)	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)	V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	I_{CC}	—	125	175	mA
Output High Voltage (I_O = −2.4mA)	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	I_{OS}*	15	—	−60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7130E		MB7130H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	30	55	30	45	ns
Output Disable Time	t_{DIS}	—	40	—	30	ns
Output Enable Time	t_{EN}	—	40	—	30	ns



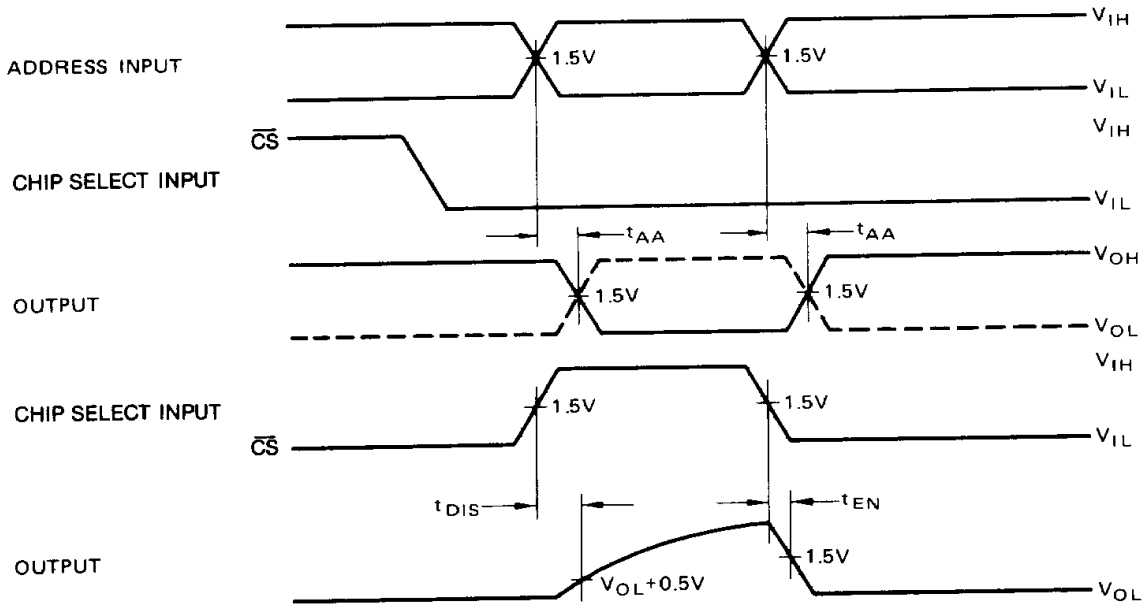
AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude	**0V to 3V**
Rise and Fall Time	**5 ns from 1V to 2V**
Frequency	**1 MHz**

MB7130		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



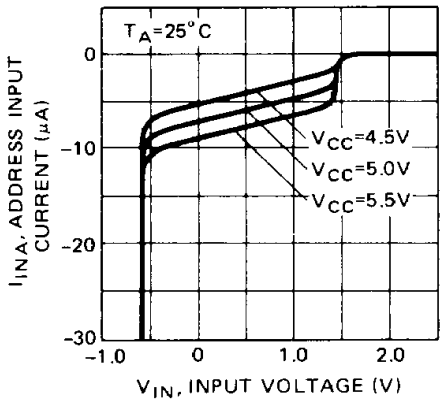
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

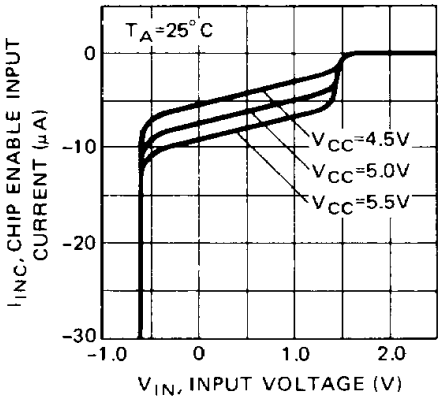
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

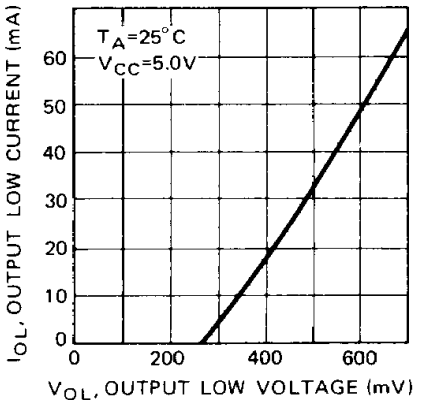
I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



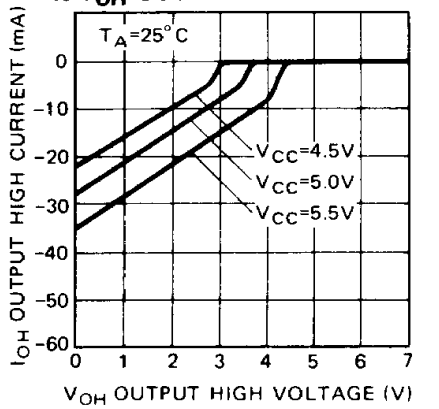
I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



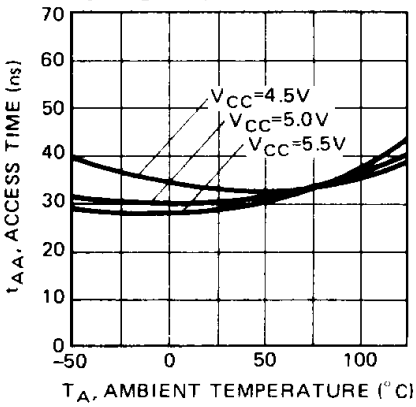
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



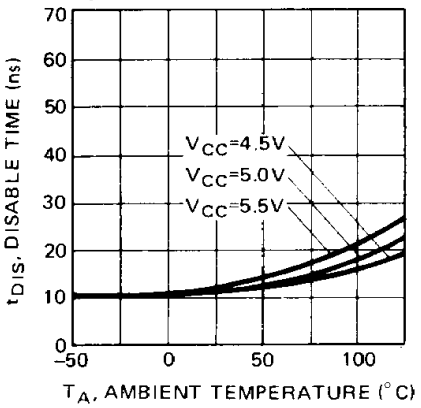
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



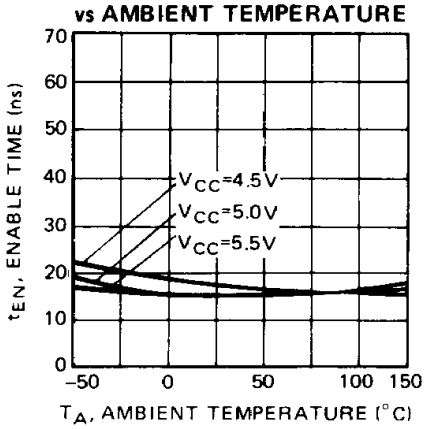
t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE



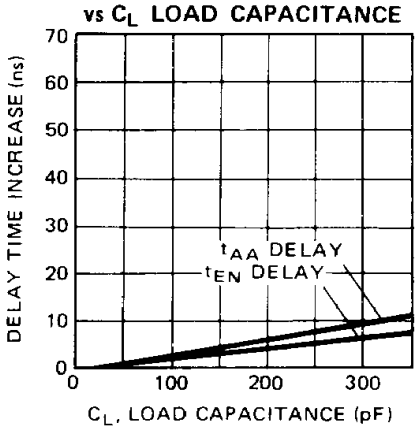
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

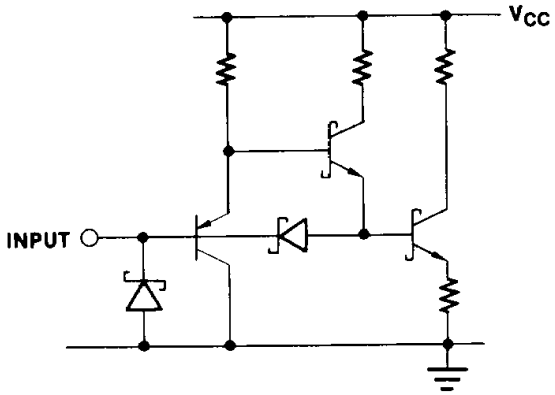
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Enable circuit.

MB7130 INPUT CIRCUIT



MB7130 OUTPUT CIRCUIT