FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB 7133E/H
MB 7134E/H/Y

November 1985
Edition 2.0

SCHOTTKY 16384-BIT DEAP PROM (4096 WORDS X 4 BITS)

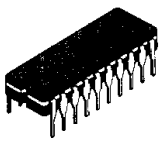
This Fujitsu MB 7133 and MB 7134 are high speed Schottky TTL electrically field programmable read only memories organized as 4096 words by 4 bits. With uncommitted collector output provided on the MB 7133 and three-state outputs on the MB 7134, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic Level "ones" can be programmed by the highly reliable Deap (Diffused Eutectic Aluminum Process) according to simple programming procedures.

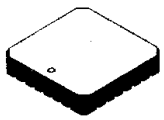
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

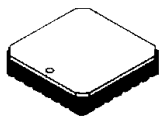
- Single +5V supply voltage.
- 4096 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by Deap (diffused eutectic aluminum process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 35ns typ
  MB 7134Y: 35ns max.
  H : 45ns max.
  E : 55ns max.
- TTL compatible inputs and outputs.
- Open collector (MB 7133)
- 3-state outputs (MB 7134)
- Two chip enables lead for simplified memory expansion.
- Standard 20 pin DIP package (: -CZ)
  Standard 28 pad LCC (: -CV)



CERAMIC PACKAGE
DIP-20C-C03

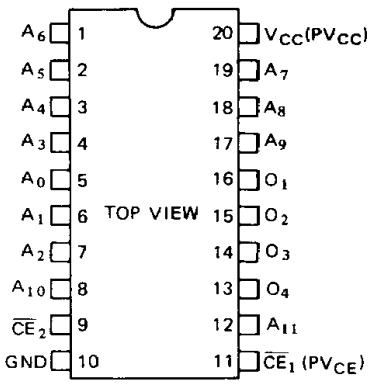


CERAMIC PACKAGE
LCC-28C-A01



CERAMIC PACKAGE
LCC-28C-A02

PIN ASSIGNMENT



LCC PAD CONFIGURATION:
See Page 15 and 16

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	-0.5 to +7.5	V
Input Voltage	V_{IN}	-1.5 to 5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}	V
Output Voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Input Current	I_{IN}	-20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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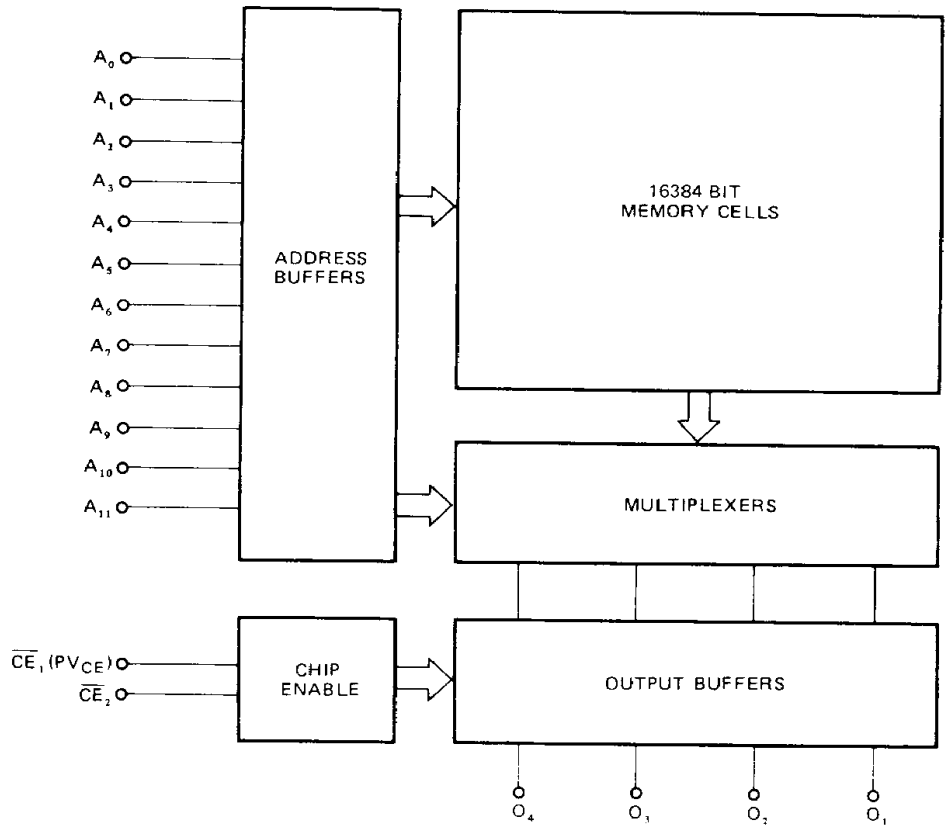
Fig. 1 – MB 7134 BLOCK DIAGRAM



CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7133	I_{OLK}			40	μA
	MB 7134	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB 7134	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		120	170	mA
Output High Voltage (I_O = -2.4mA)	MB 7134	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7134	I_{OS}*	-15		-60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$=0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

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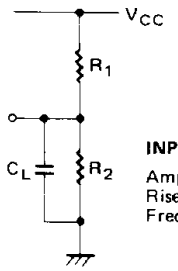
Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

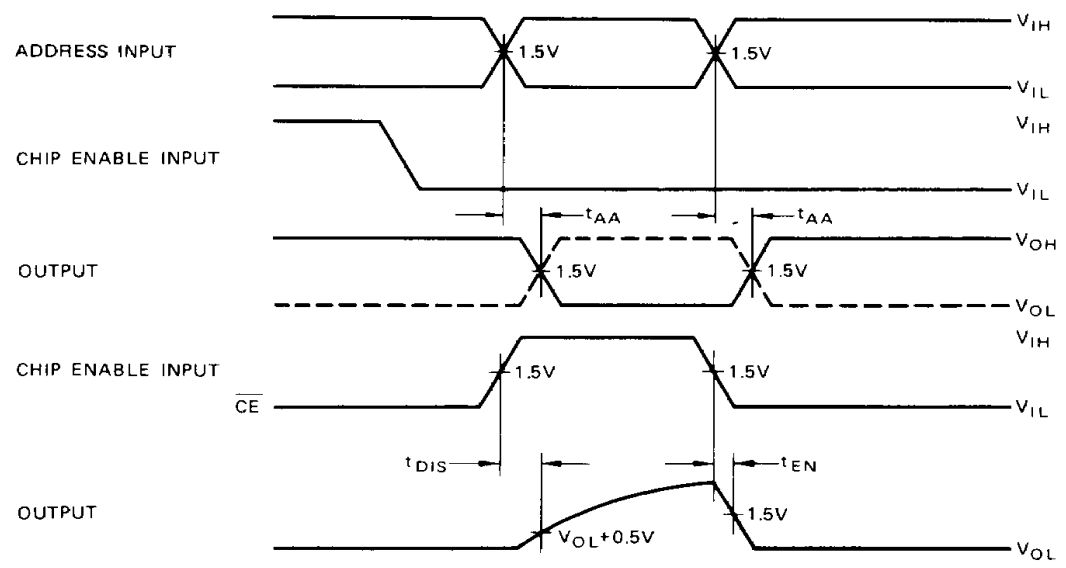
	MB 7133/MB 7134		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		MB 7134Y		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output Disable Time	t_{DIS}		40		40		30	ns
Output Enable Time	t_{EN}		40		40		30	ns

OPERATION TIMING DIAGRAM



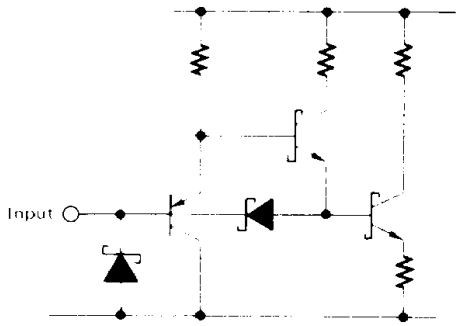
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

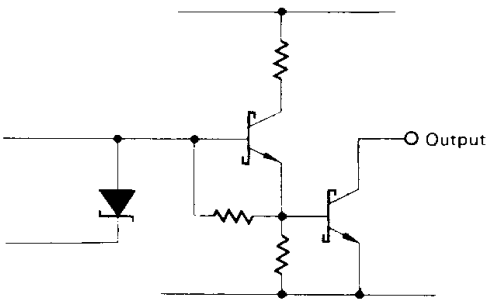
Fig. 3 – MB 7133/MB 7134 INPUT



OPEN COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7134 (3-state) compared to 0mA for the MB 7133 (open-collector)

Fig. 4 – MB 7133 OUTPUT



THREE-STATE OUTPUT

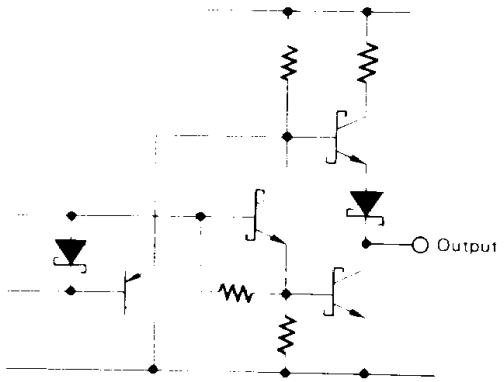
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low

impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7134 OUTPUT



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

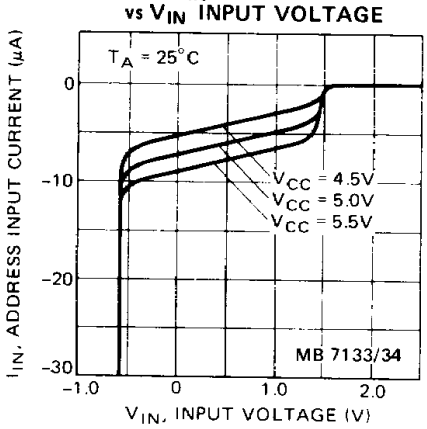


Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

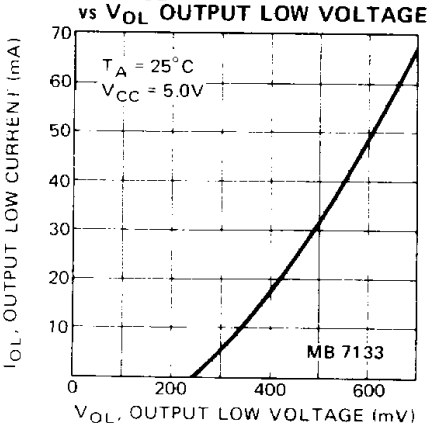


Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

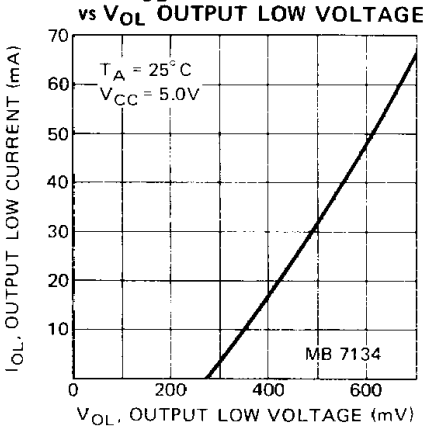


Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

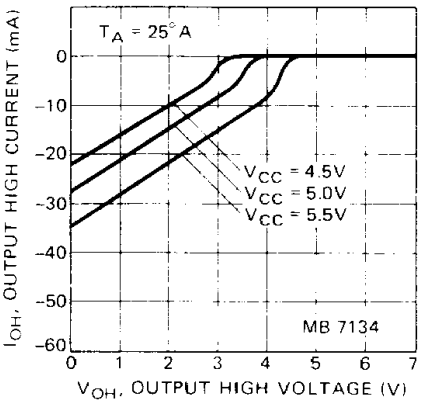


Fig. 10 – t_{AA}, ACCESS TIME vs AMBIENT TEMPERATURE

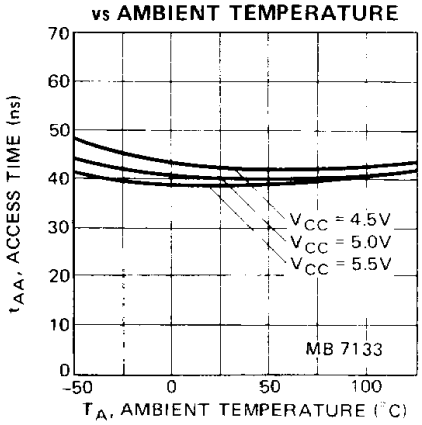


Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

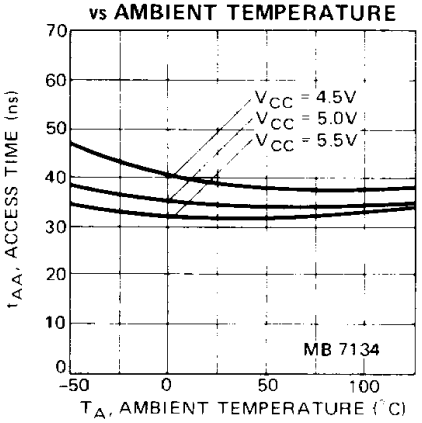


Fig. 12 – t_{DIS}, DISABLE TIME vs AMBIENT TEMPERATURE

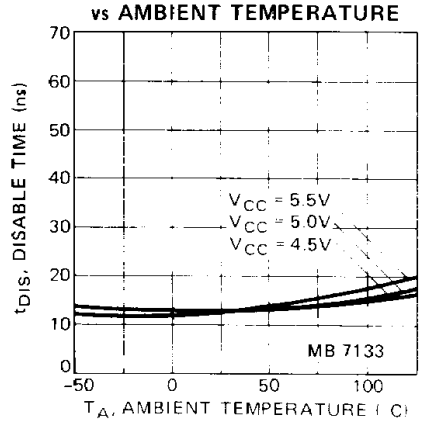


Fig. 13 – t_{DIS}, DISABLE TIME vs AMBIENT TEMPERATURE

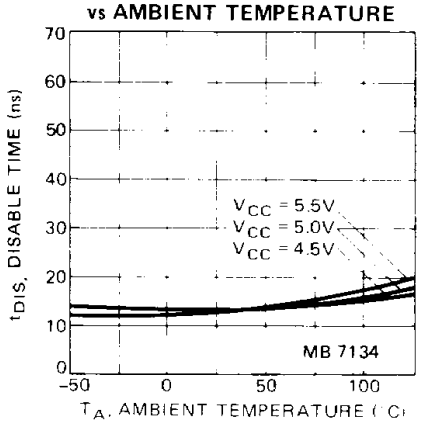


Fig. 14 – t_{EN}, ENABLE TIME vs AMBIENT TEMPERATURE

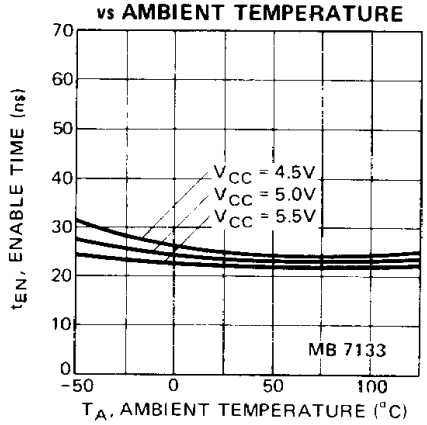


Fig. 15 – t_{EN}, ENABLE TIME vs AMBIENT TEMPERATURE

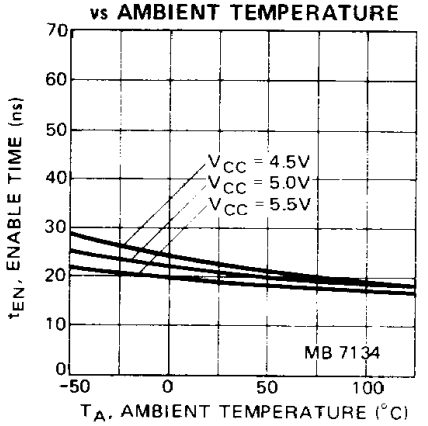


Fig. 16 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

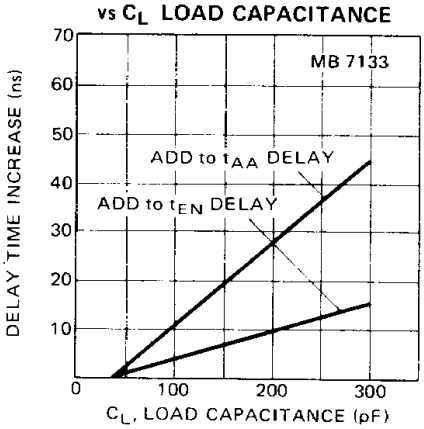
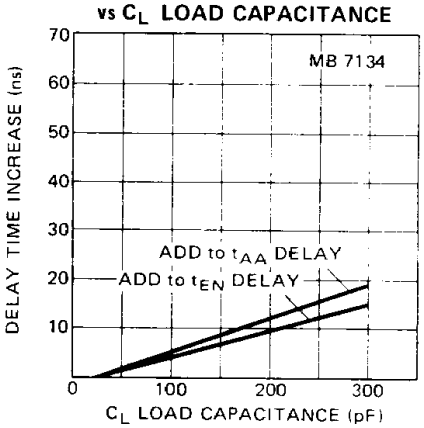


Fig. 17 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

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FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series Schottky PROM is fabricated using Schottky TTL technology, passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP), which is achieved by thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (Deap) technology with fine emitter and pulse programming method which achieve high-speed operation, high-speed programming, high programmability and high reliability.

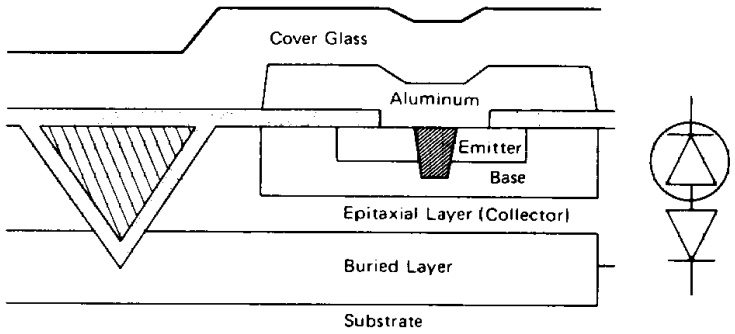
One memory cell is originally structured with a base-open NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of cell diode with relatively low temperature, i.e. Deap technology.

Fast programming time of typically 150μs/bit is achieved with a fine emitter cell which requires less programming energy; the result is negligible thermal stress. This high reliability feature virtually eliminates aluminum migration in the programmed cell. Further, Fujitsu advanced technology allows very high programmability.

SPECIAL FACTORY TESTING

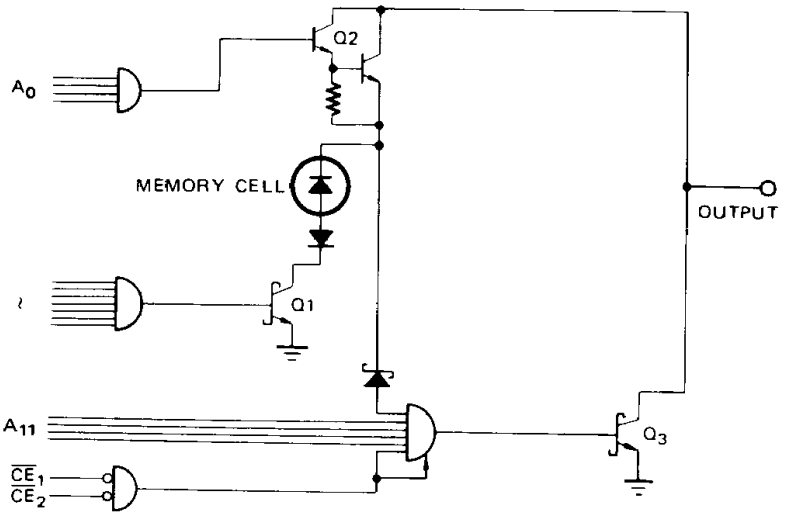
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

Fig. 18 – PROGRAMMED CELL (CROSS SECTION)



▨ Programmed by diffused eutectic aluminum process (DEAP)

Fig. 19 – INTERNAL PROGRAMMING CIRCUIT



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PROGRAMMING INFORMATION (continued)

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using twelve address inputs to turn on transistors Q1 and Q2. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the output voltage indicates that the selected bit is in the logic one state.

To assure that the element is programmed properly, two additional programming pulses are applied immediately after an output voltage indicates conduction in the programmed bit.

One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7V at 25°C ambient temperature.

RELIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS ($T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW} (1)	10	11	12	μs
Programming Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r (3)	–	–	2	μs
Programming Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f (5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP} (6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP} (7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (8)	10	–	–	μs
Programming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

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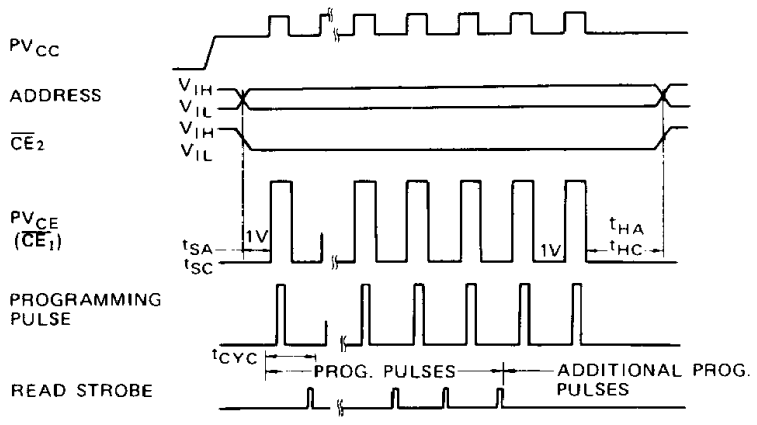
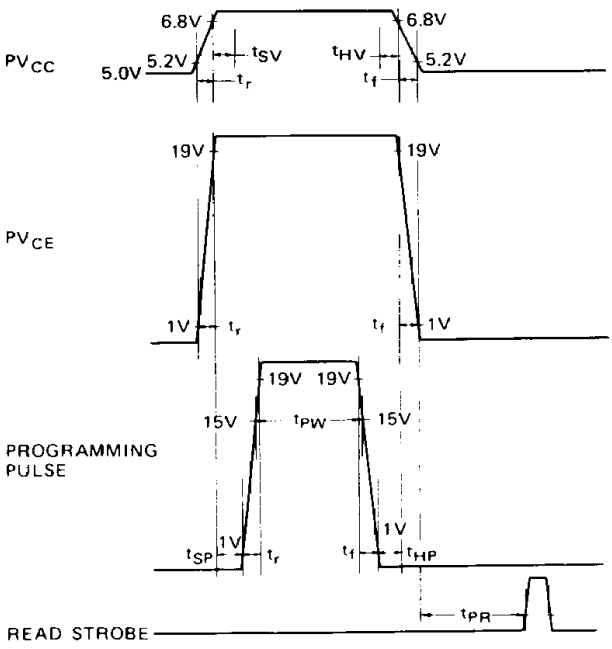
PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

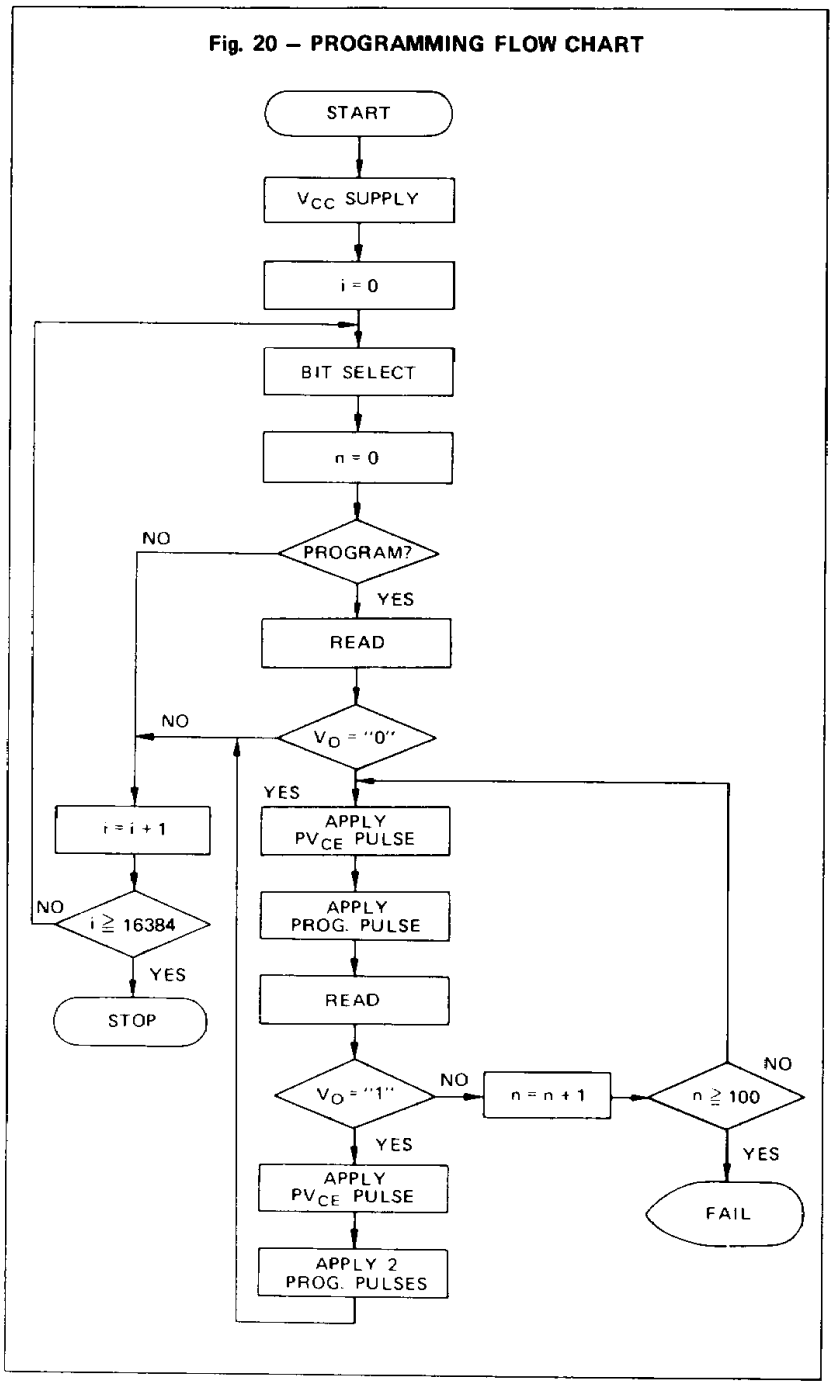


PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

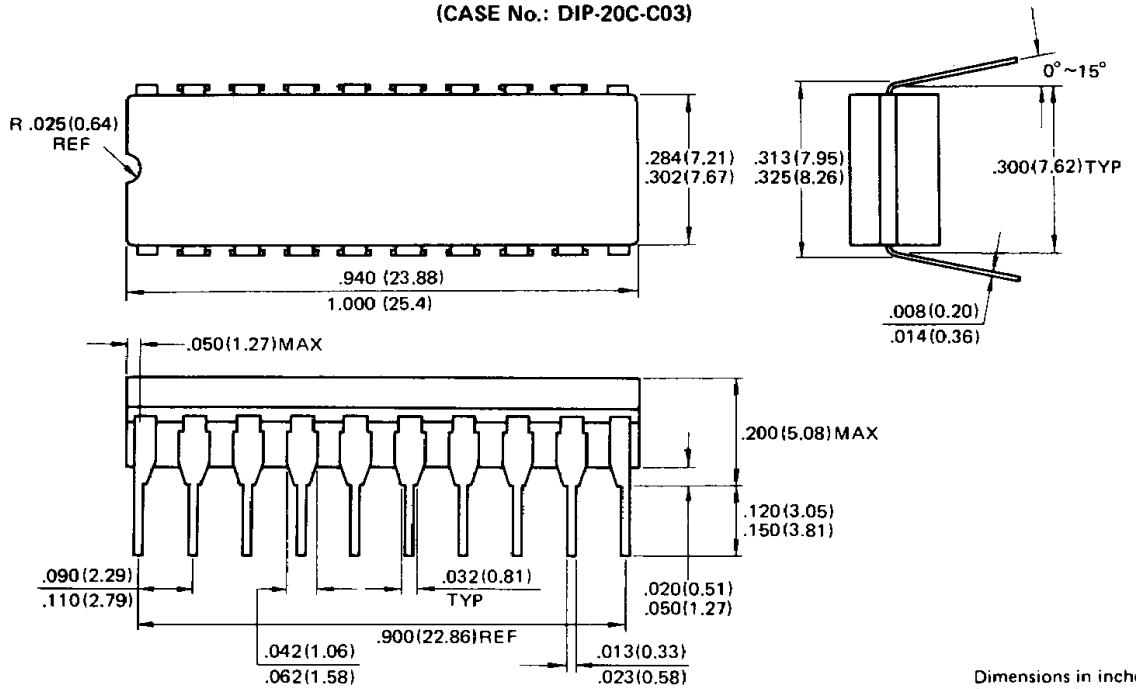
Fig. 20 – PROGRAMMING FLOW CHART



1

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

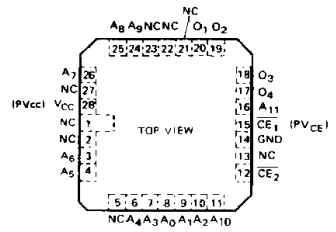


Dimensions in inches
(millimeters)

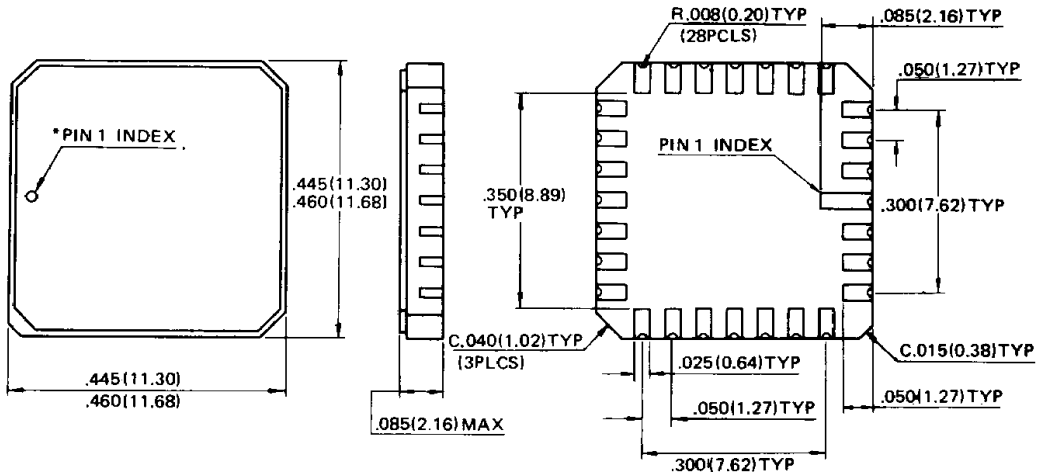
1

PACKAGE DIMENSIONS

PAD CONFIGURATION



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



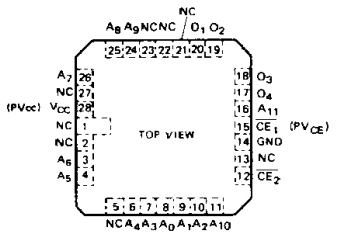
*Shape of Pin 1 index : Subject to change without notice

Dimensions in inches
(millimeters)

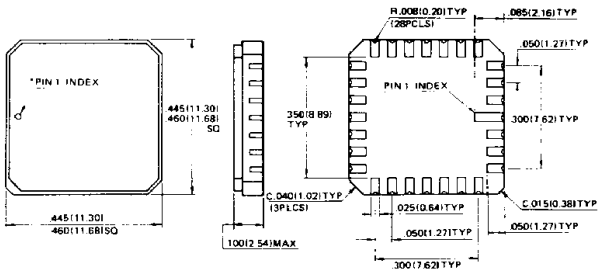
1

PACKAGE DIMENSIONS

PAD CONFIGURATION



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A02)



*Shape of Pin 1 index : Subject to change without notice

Dimensions in inches
(millimeters)