

FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB71A38-25 MB71A38-35

August 1988
Edition 2.0

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SCHOTTKY 16384-BIT DEAP PROM (2048 WORDS X 8 BITS)

The Fujitsu MB71A38 is high speed schottky TTL electrically field programmable read only memory organized as 2048 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed U-FOX (U-groove isolation with thick Field OXide process) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

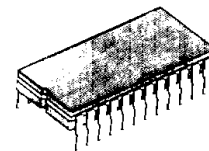
The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

- Single +5V supply voltage.
- 2048 words x 8 bits organization fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time 18ns typ, 25/35 ns max
- TTL compatible inputs and outputs.
- 3 State outputs.
- Three chip enable pins for simplified memory expansion.
- 24-pin Ceramic (Cerdip) DIP (300 & 600 mil)
- 24-pin Plastic DIP (300 & 600mil)

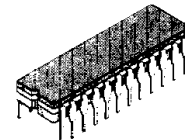
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input Voltage	V_{IN}	-1.5 to 5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Input Current	I_{IN}	-20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+75	mA
Storage Temperature	CERAMIC	T_{stg}	°C
	PLASTIC		
Output Voltage	V_{OUT}	-0.5 to 5.5	V

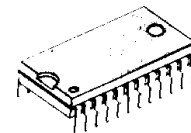
NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



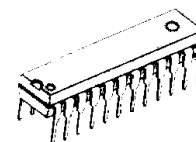
CERAMIC PACKAGE
DIP-24C-C01



CERAMIC PACKAGE
DIP-24C-C04(-SK)

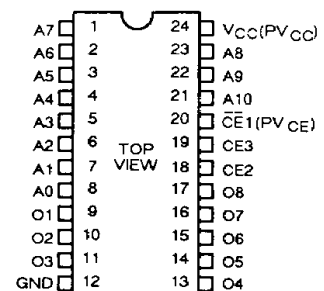


PLASTIC PACKAGE
DIP-24P-M02



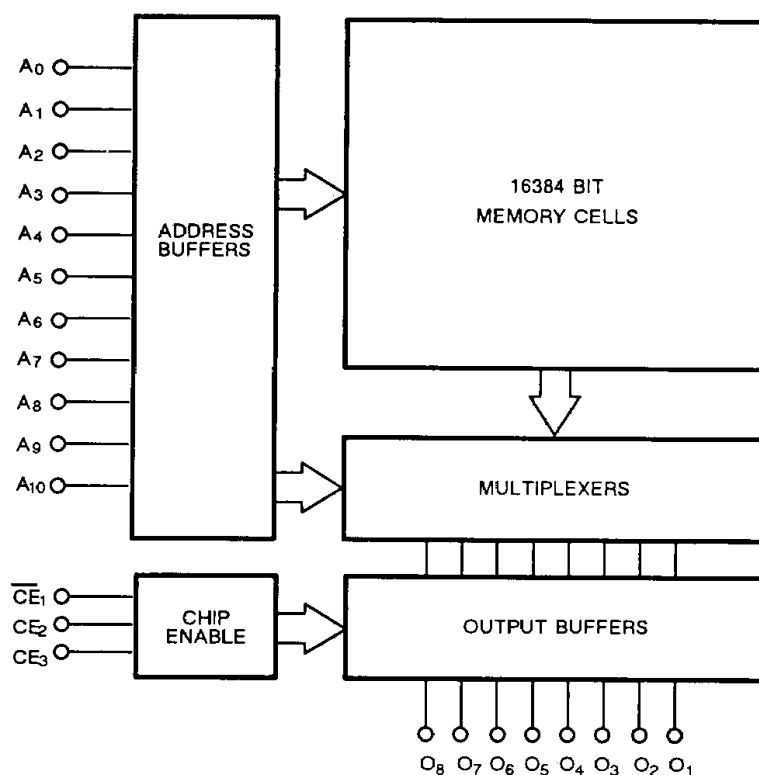
PLASTIC PACKAGE
DIP-24P-M03(-SK)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB71A38 BLOCK DIAGRAM



CAPACITANCE ($f = 1\text{MHz}$, $V_{CC} = +5\text{V}$, $V_{IN} = +2\text{V}$, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

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Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current ($V_{IH} = 5.5V$)	I_R			40	μA
Input Load Current ($V_{IL} = 0.45V$)	I_F			-250	μA
Output Low Voltage	$I_{OL} = 10mA$	V_{OL}		0.45	V
	$I_{OL} = 16mA$			0.50	V
Output Leakage Current ($V_O = 2.4V$, chip disabled)	I_{OIH}			40	μA
Output Leakage Current ($V_O = 0.45V$, chip disabled)	I_{OIL}			-40	μA
Input Clamp Voltage ($I_{IN} = -18mA$)	V_{IC}			-1.2	V
Power Supply Current ($V_{IN} = OPEN$ or GND)	I_{CC}		80**	120	mA
Output High Voltage ($I_O = -2.4mA$)	V_{OH}^*	2.4			V
Output Short Circuit Current ($V_O = GND$)	I_{OS}^*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{CE} = 0.4V$) and the programmed bit is addressed. These characteristics cannot be tested prior to

programming, but are guaranteed by factor testing.

** This value denote conditions at $T_A = 25^\circ C$ and $V_{CC} = +5.0V$

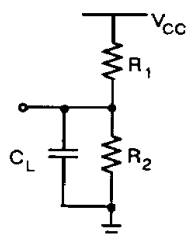


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude 0V to 3V
Rise and Fall Time 5ns from 1V to 2V
Frequency 1MHz

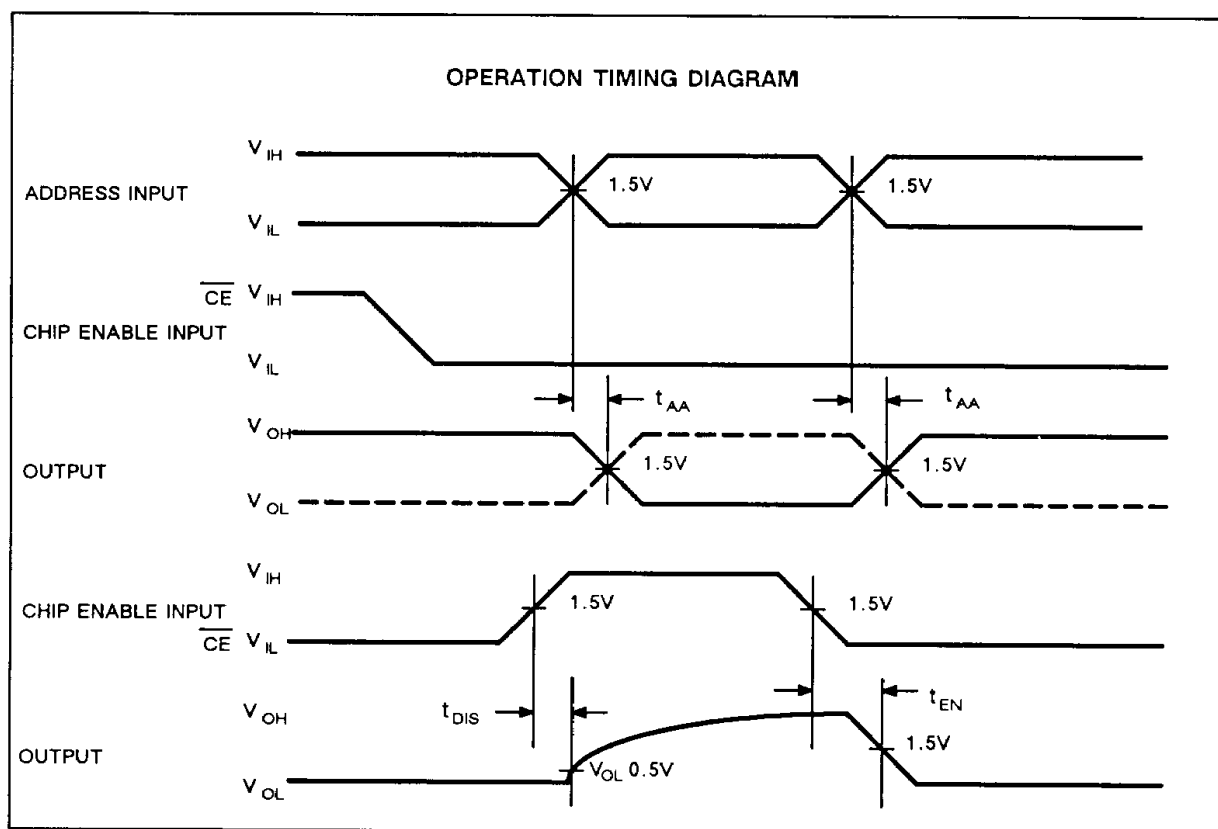
	MB71A38		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF



AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	MB71A38-25		MB71A38-35		Unit
		Typ	Max	Typ	Max	
Address Time (via address input)	t_{AA}	18	25	18	35	ns
Output Disable Time	t_{DIS}	10	20	10	25	ns
Output Enable Time	t_{EN}	12	20	12	25	ns



Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables

are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 3 - MB71A38 INPUT

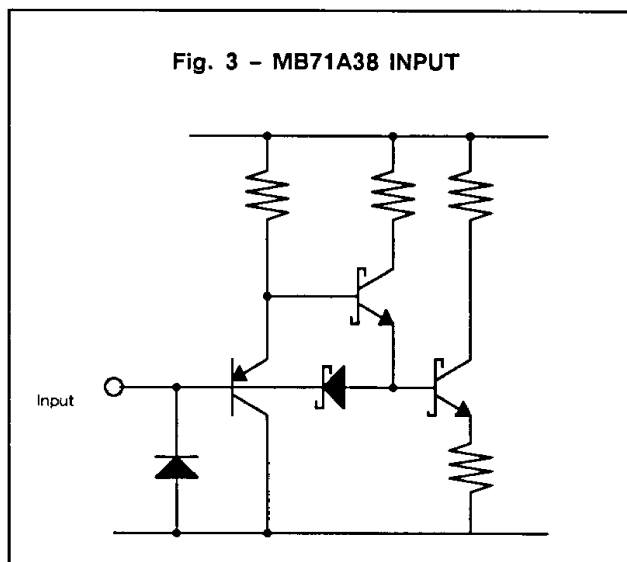
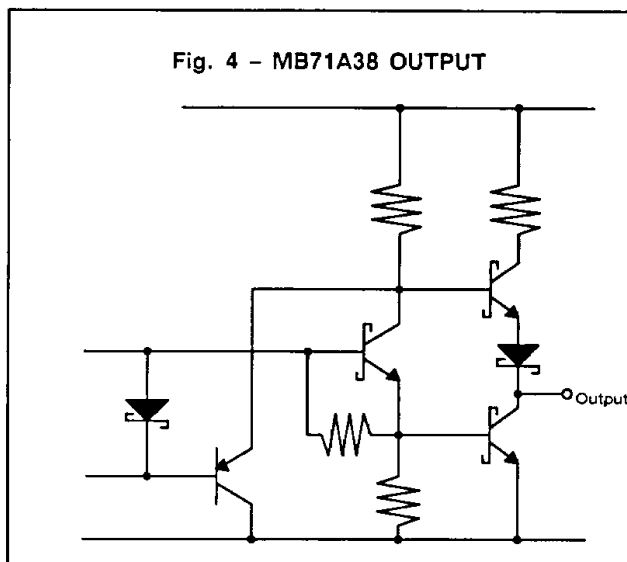


Fig. 4 - MB71A38 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig.5- I_{IN} INPUT CURRENT
VS. V_{IN} INPUT VOLTAGE

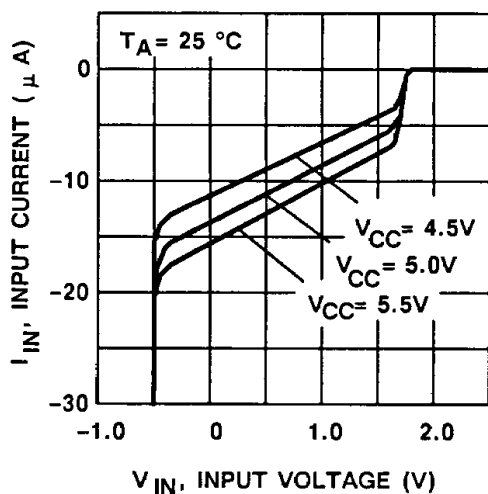


Fig.6- I_{OL} OUTPUT LOW CURRENT
VS. V_{OL} OUTPUT LOW VOLTAGE

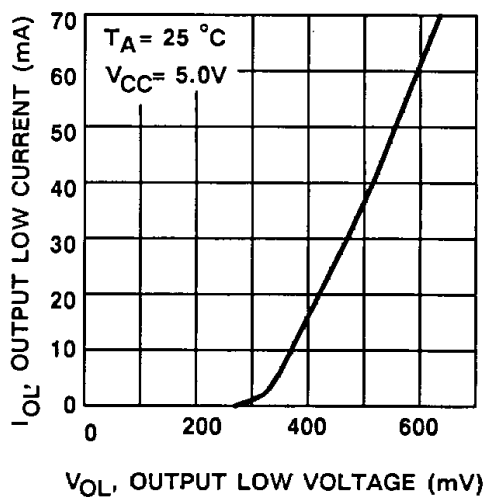


Fig.7- I_{OH} OUTPUT HIGH CURRENT
VS. V_{OH} OUTPUT HIGH VOLTAGE

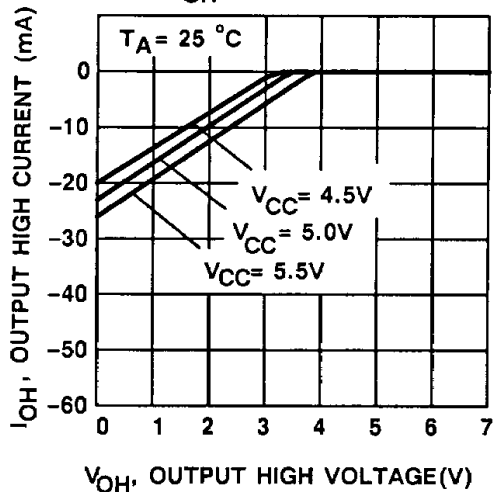
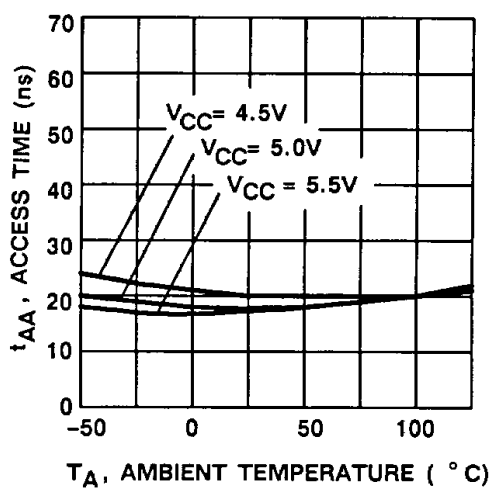


Fig.8- t_{AA} ACCESS TIME
VS. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS CURVES

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Fig.9- t_{DIS} DISABLE TIME
VS. AMBIENT TEMPERATURE

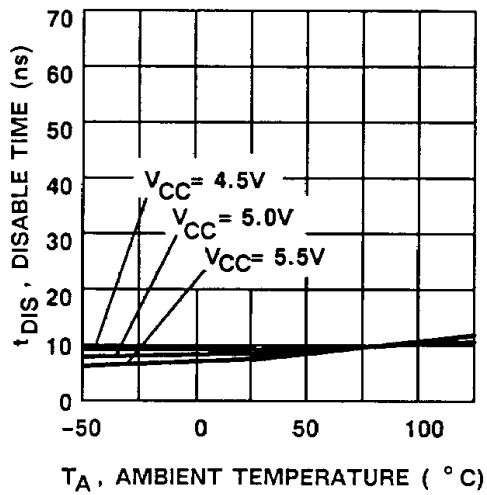


Fig.10- t_{EN} ENABLE TIME
VS. AMBIENT TEMPERATURE

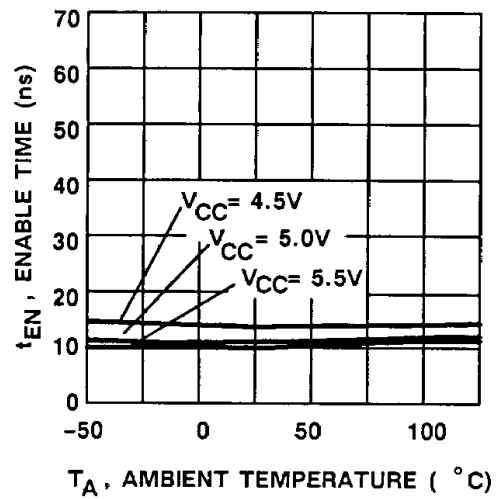
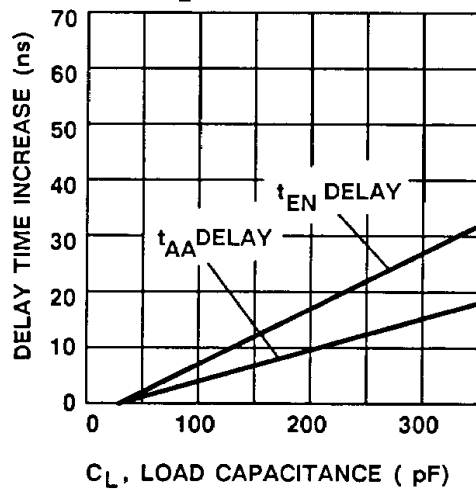


Fig.11-DELAY TIME INCREASE
VS. C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

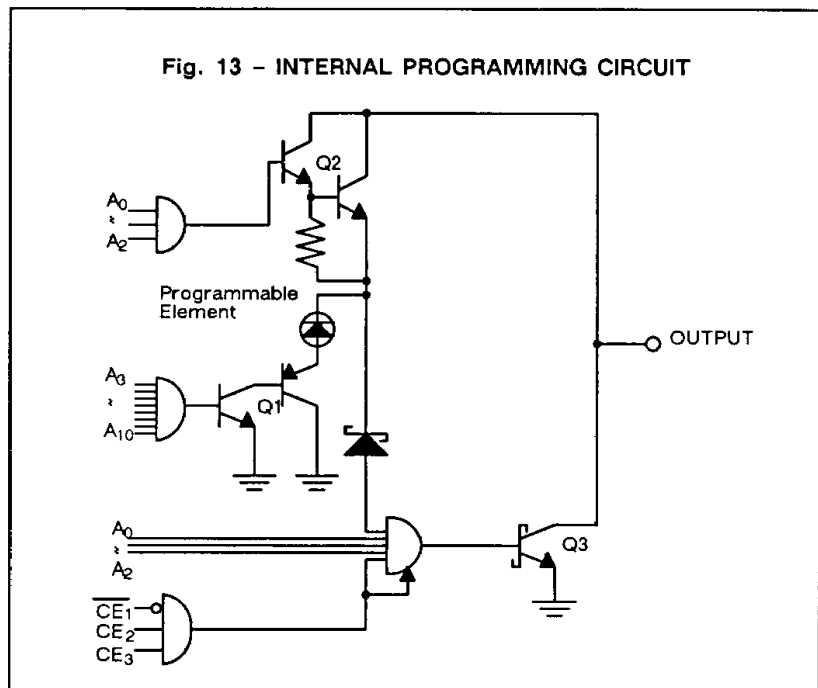
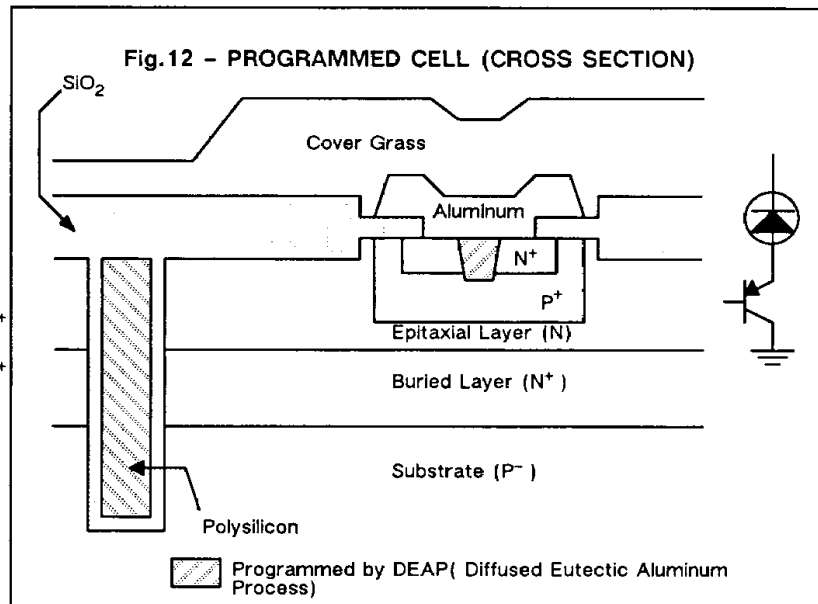
The Fujitsu MB71A00 series is the junction-shorting schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N⁺ and P⁺ diffusion layer, the PNP transistor uses a P⁺ diffusion layer, an N⁺ epitaxial layer, and a P⁻ substrate (Fig. 12).

Each memory cell is divided by passive isolations named U-FOX (U-groove isolation with thick Field OXide process).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.





PROGRAMMING INFORMATION (continued)

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SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 13, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using eleven address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and

transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip

enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at $V_{OH}=2.4V$ and $V_{CC}=7.0V$ at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS ($T_A = 25^\circ C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0		0.8	V
Input High Voltage	V_{IH}	2.0		5.25	V
Power Supply Voltage	PV_{CC} P:	6.7	7.0	7.3	V
	R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}	70		75	mA
PV_{CE} Pulse Voltage	PV_{CE}	20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}	20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}	230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}	1.0	1.5	2.4	V



PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (TA = 25°C)

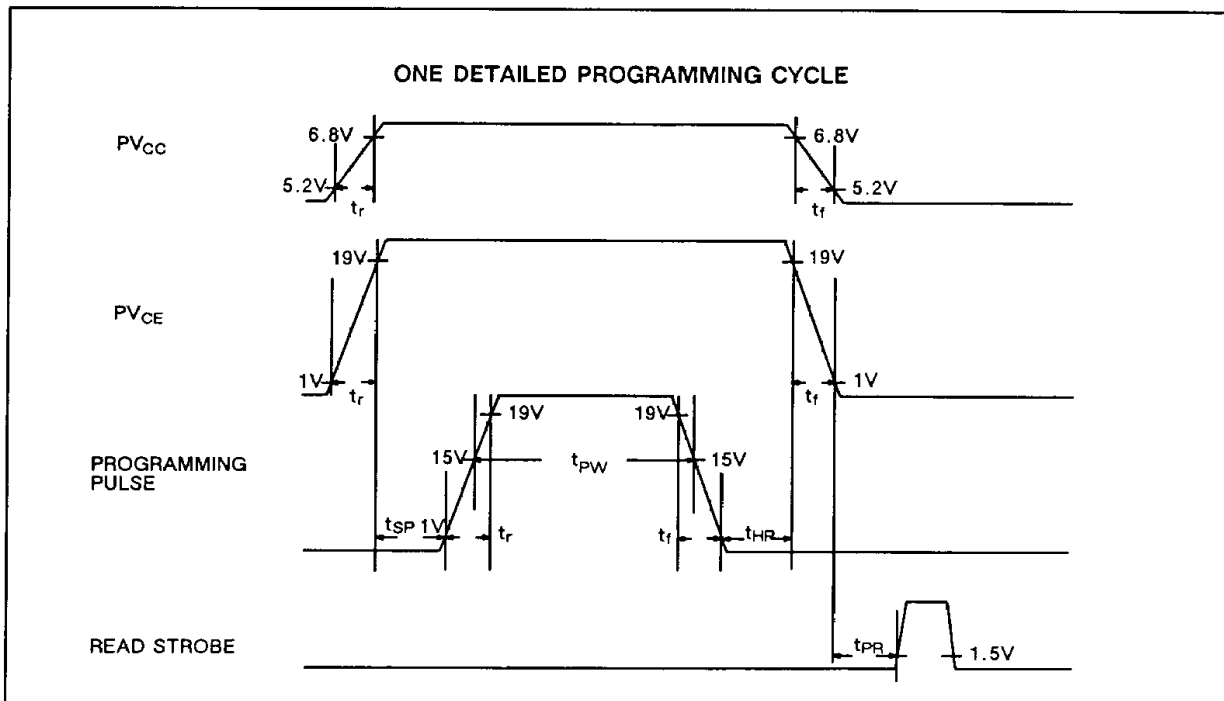
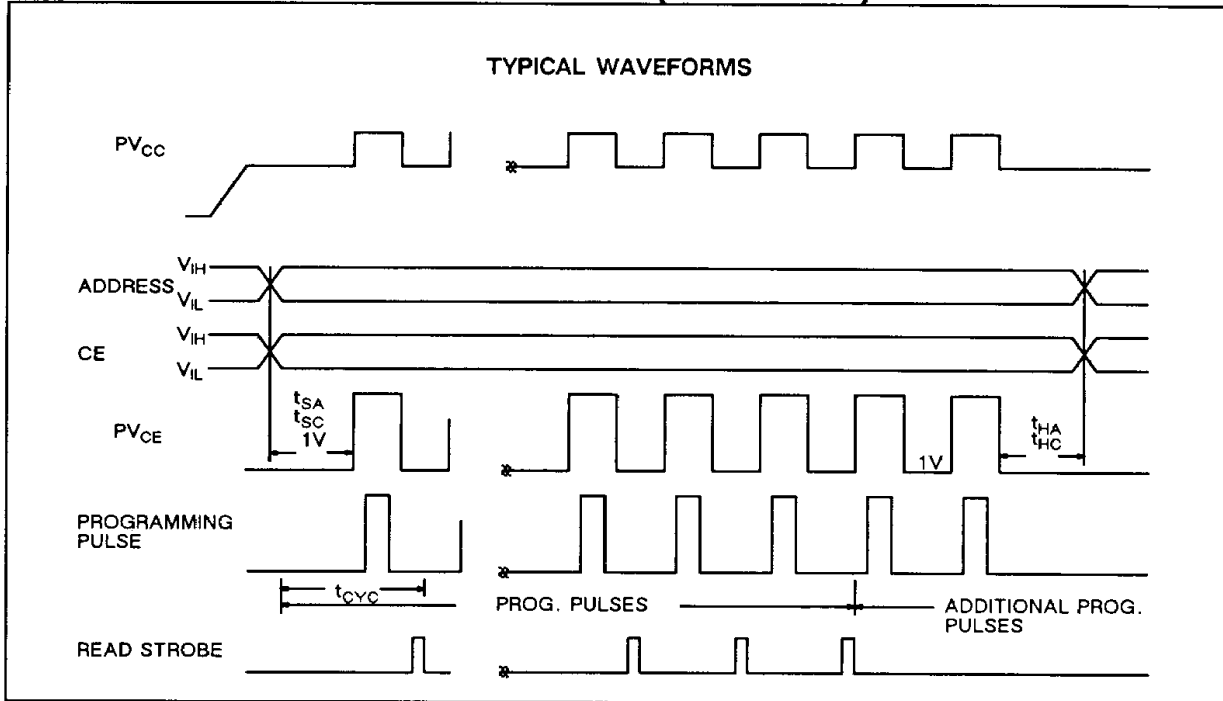
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	$t_{PW}^{(1)}$	10	11	12	μs
Programming Pulse Rise Time	$t_r^{(2)}$	–	–	2	μs
PV _{CE} Pulse Rise Time	$t_r^{(2)}$	–	–	2	μs
PV _{CC} Pulse Rise Time	$t_r^{(3)}$	–	–	2	μs
Programming Pulse Fall Time	$t_f^{(4)}$	–	–	2	μs
PV _{CE} Pulse Fall Time	$t_f^{(4)}$	–	–	2	μs
PV _{CC} Pulse Fall Time	$t_f^{(5)}$	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV _{CE} Set-up Time	$t_{SP}^{(6)}$	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV _{CE} Hold Time	$t_{HP}^{(7)}$	2	–	–	μs
PV _{CE} Pulse Trailing Edge to Read Strobe Time	$t_{PR}^{(8)}$	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	$\mu s/bit$
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 400 Ω load and 15V.
(2) From 1V to 19V (400 Ω load).
(3) From 5.2V to 6.8V (30 Ω load).
(4) From 19V to 1V (400 Ω load).

(5) From 6.8V to 5.2V (30 Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

PROGRAMMING INFORMATION (continued)

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PROGRAMMING INFORMATION (continued)

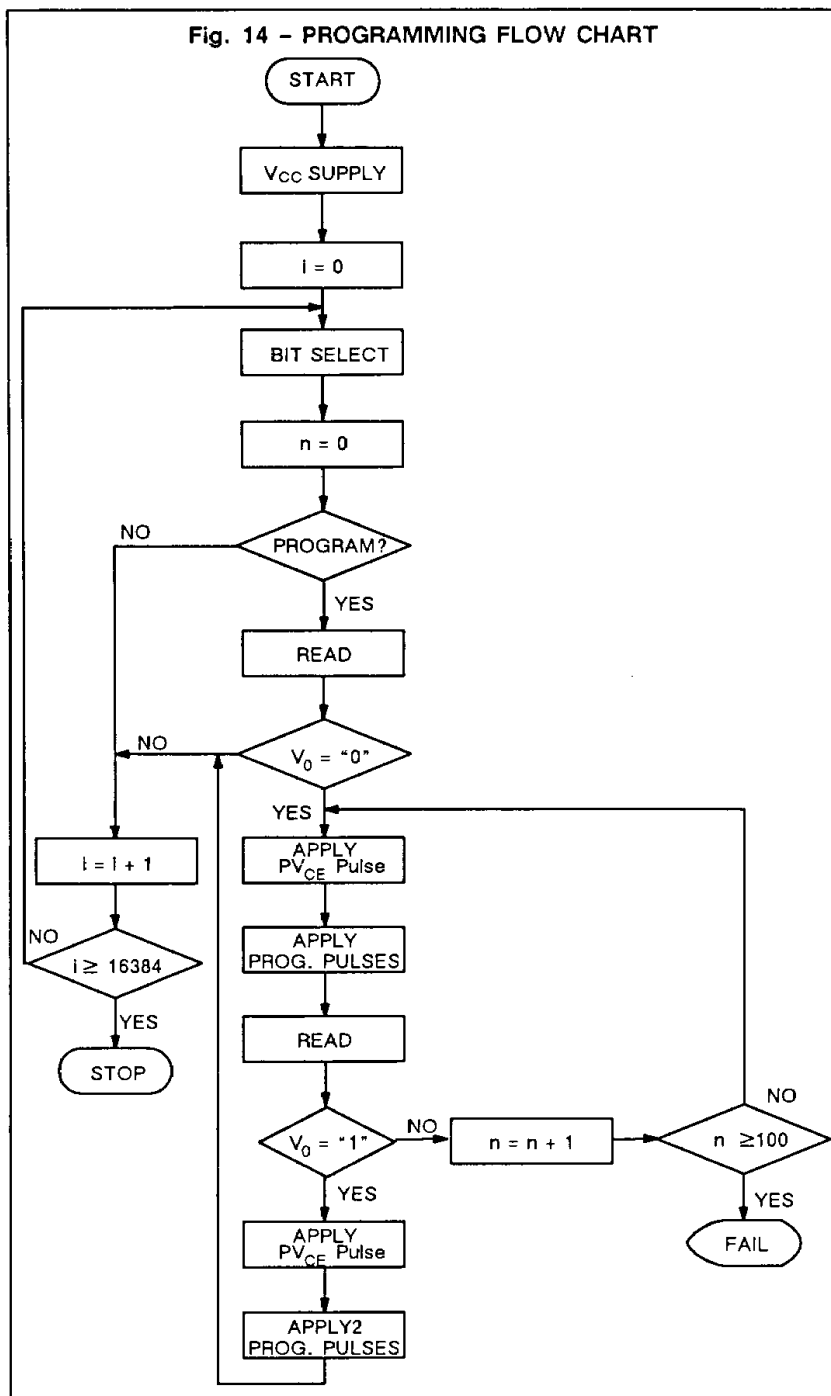
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, $GND = 0V$.
2. Select the desired bit.
3. Read the output to confirm the voltage $V_O = \text{low}$. (In the case of $V_O = \text{high}$, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 62.5mA and duration of t_{PW} (11 μ S) after a delay of t_{SP} (4 μ S).
6. Read the output V_O after a delay of t_{PR} (10 μ S).
 - a) In the case of $V_O = \text{low}$, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50 μ S)
 - b) In the case of $V_O = \text{high}$, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2 μ S).

Note

- 1) Programming must be done bit by bit.
- 2) Ambient temperature during programming must be room temperature. (25°C $\pm$ 2°C)

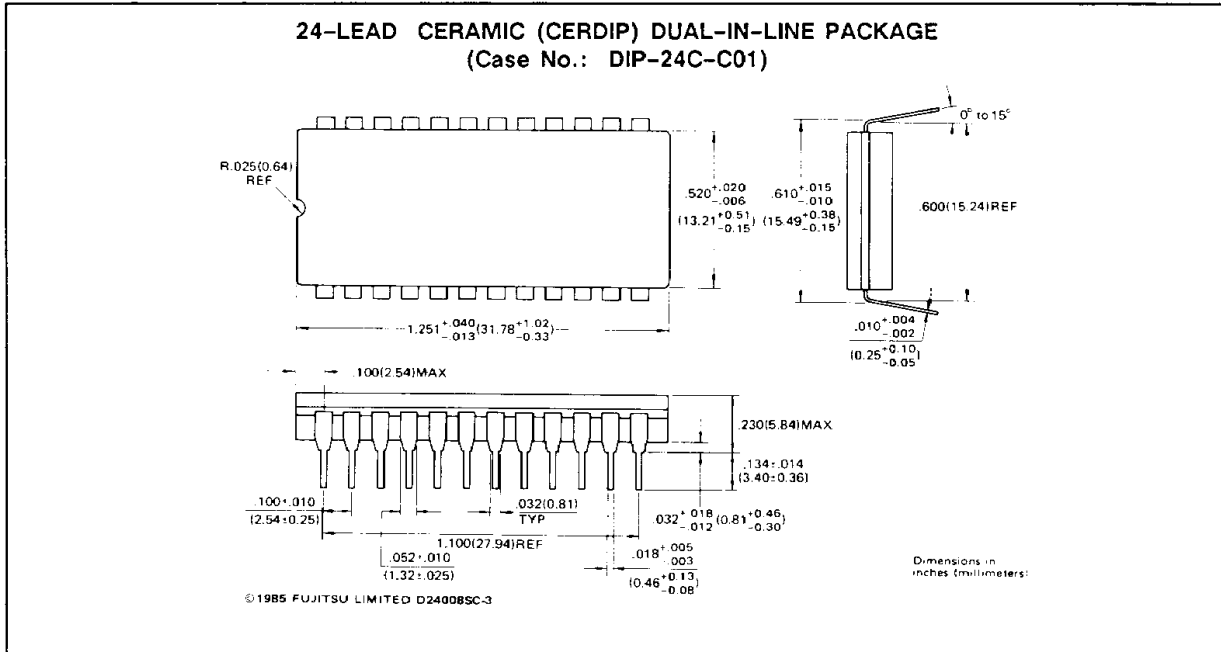
Fig. 14 - PROGRAMMING FLOW CHART



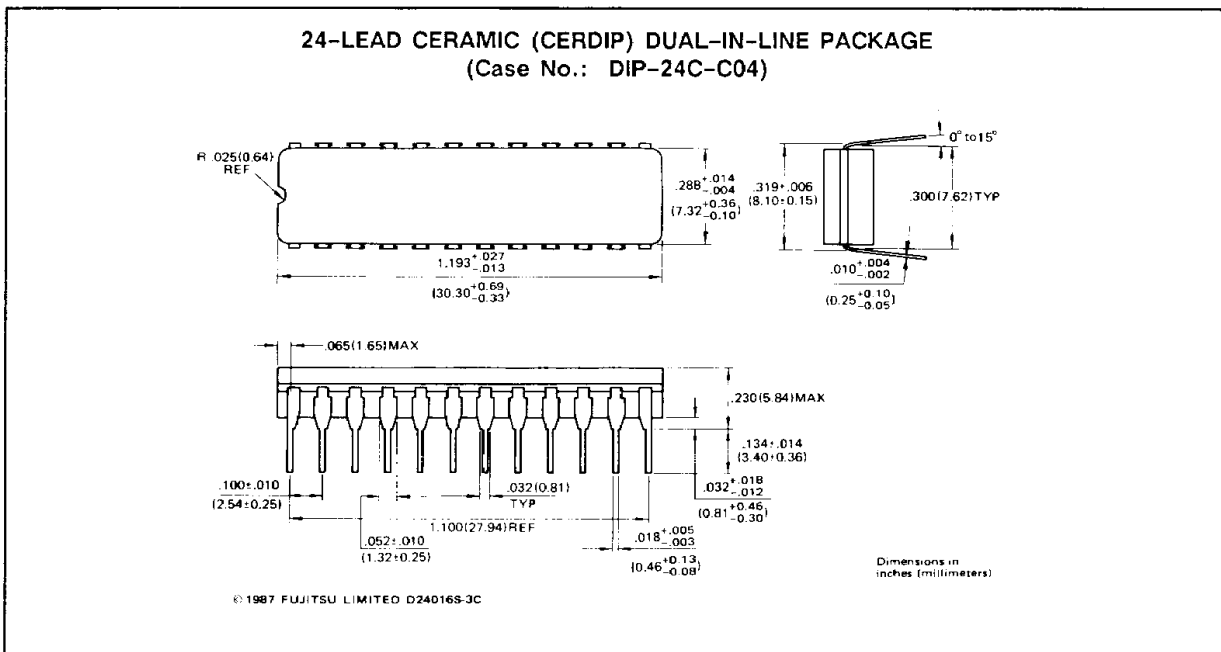
PACKAGE DIMENSIONS

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Standard 24-pin Ceramic DIP (Suffix: -Z)



Standard 24-pin Ceramic DIP (Suffix: -Z)



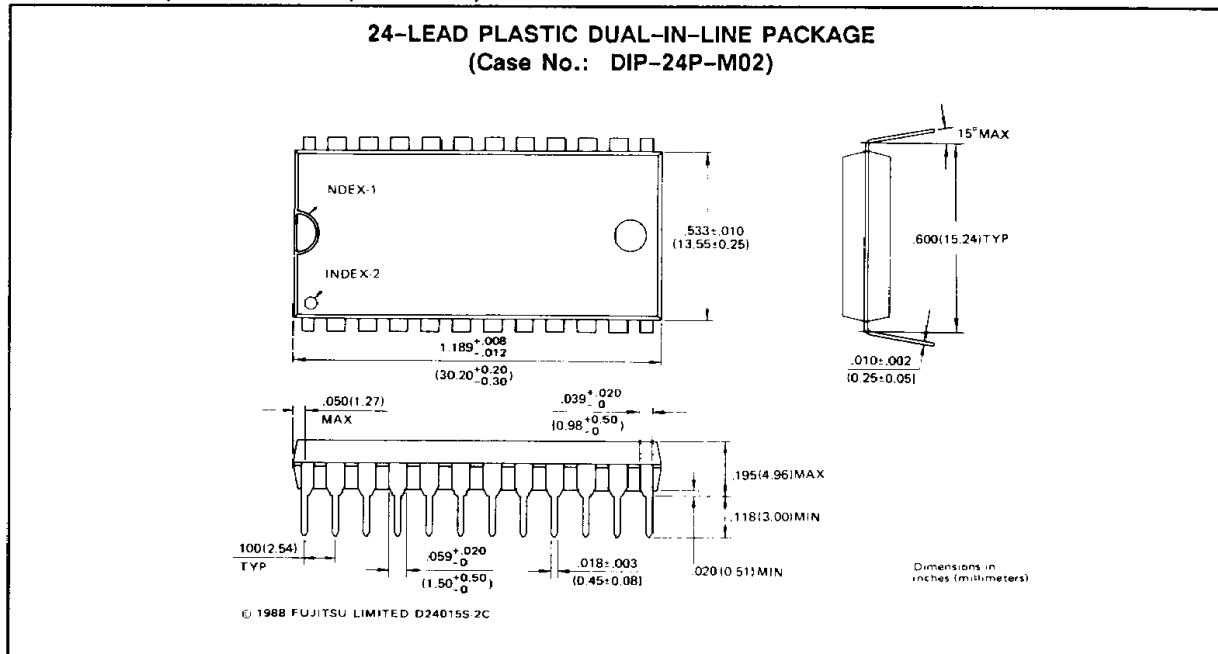


MB71A38-25
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PACKAGE DIMENSIONS

Standard 24-pin Plastic DIP (Suffix: -M)



Standard 24-pin Plastic DIP (Suffix: -M)

