February 1990
Edition 2.0

FUJITSU

DATA SHEET

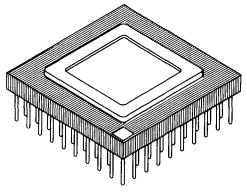
MB81C51-25/-30
CMOS TAG RANDOM ACCESS MEMORY

CMOS Tag Random Access Memory

The Fujitsu MB81C51 is a 512 entry x 4 way or 1024 entry x 2 way tag random access memory (Tag RAM) fabricated with CMOS technology.

The MB81C51 is ideal for use in cache memory systems with other RAMs. This device offers the advantages of compact design and high performance in cache systems for use with 32-bit CPUs.

- Organization: 512 Entry x 4 way or 1024 Entry x 2 way
- Access time: 30 ns max from Address Inputs 18 ns max from Compare Data Inputs
- Power consumption: 1375 mW max.
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- LRU (Least Recently Used) replacement logic
- Purge function (All-purge and partial-purge)
- Internal parity generator/checker
- Standard 64-pin Ceramic Pin Grid Array Package:
  PGA MB81C51-xxCR



PGA-64C-A02
(PIN GRID ARRAY)

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Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.0 to +7	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB81C51 BLOCK DIAGRAM 1

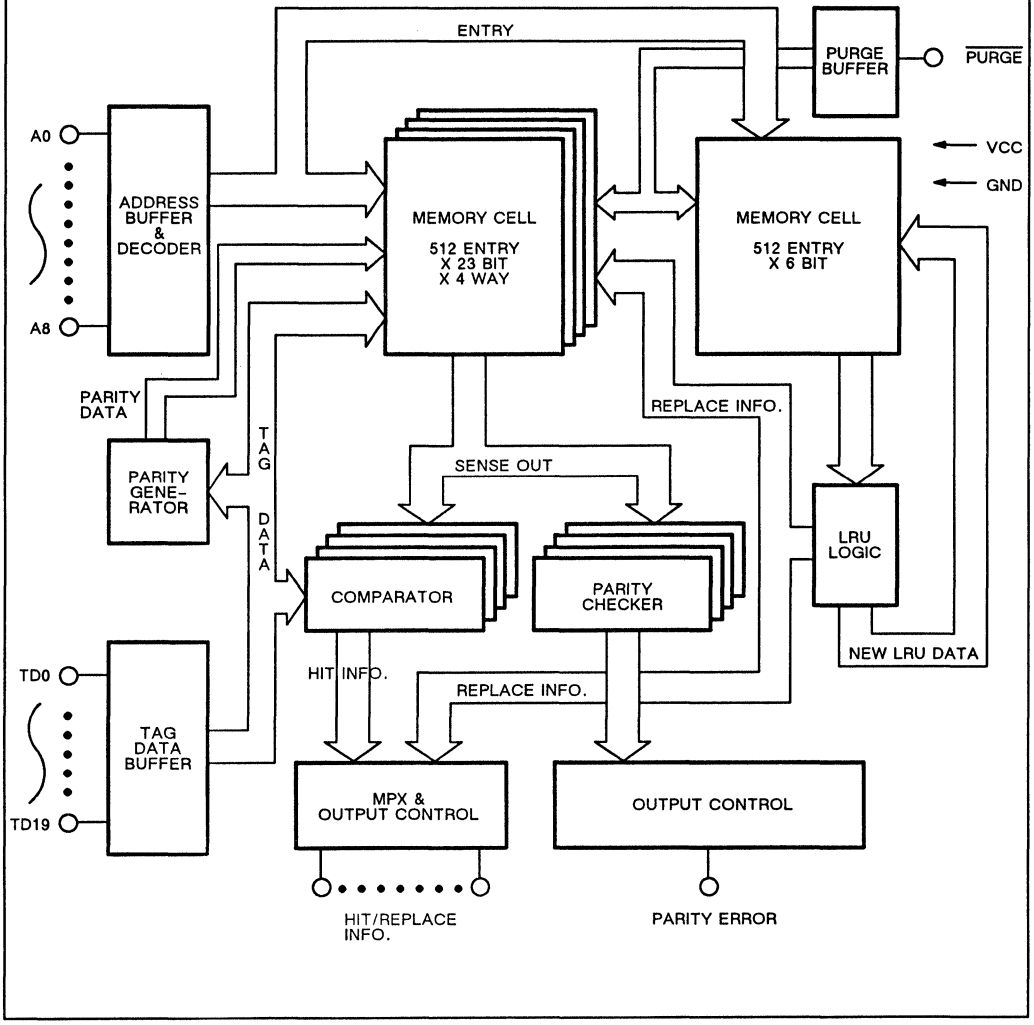
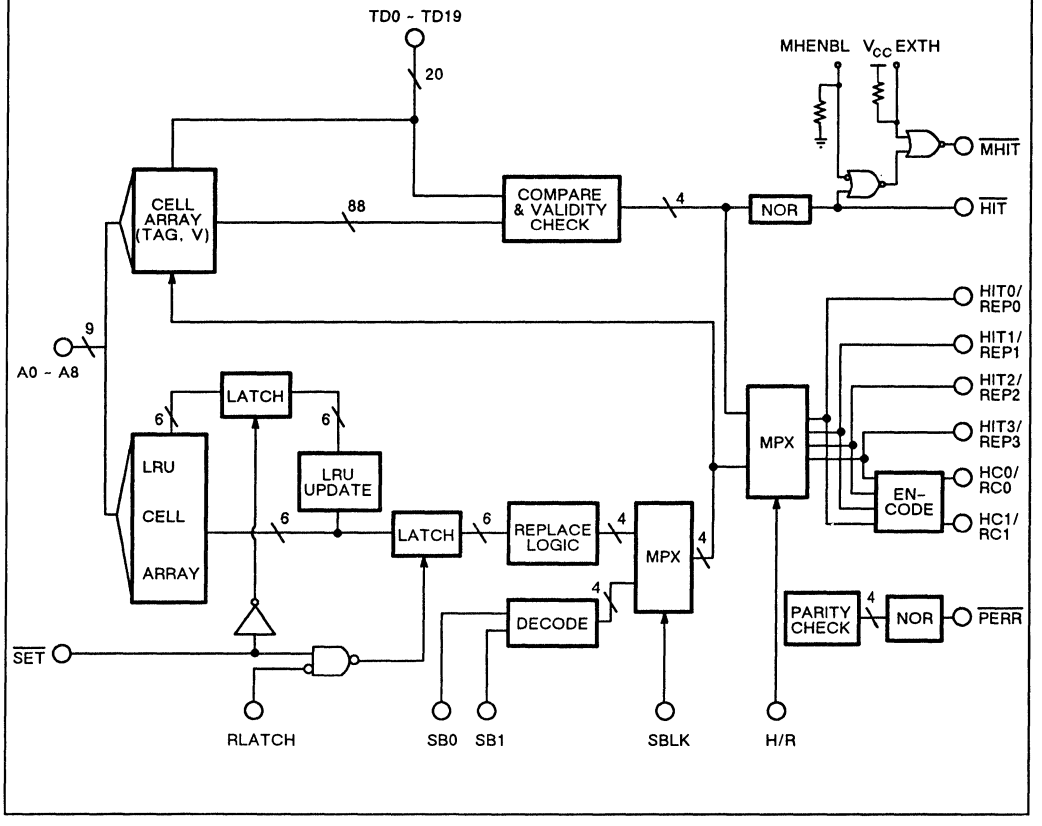


Fig. 2 — MB81C51 BLOCK DIAGRAM 2



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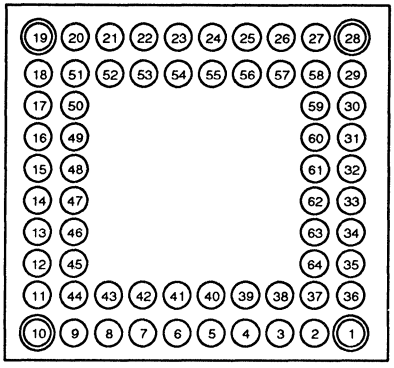
CAPACITANCE (T_A = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		10	pF

PIN ASSIGNMENT

64 PIN PIN GRID ARRAY(PGA-64C-A02)



BOTTOM VIEW

4

PIN FUNCTION

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A4	45	TD6
2	$\overline{\text{MHIT}}$	24	A5	46	TD9
3	HIT0/REP0	25	A7	47	Vcc
4	HIT2/REP2	26	A9	48	TD13
5	HIT3/REP3	27	N.C.	49	TD15
6	TD0	28	N.C.	50	TD17
7	TD2	29	$\overline{\text{PINV}}$	51	TD19
8	EXTH	30	SBLK	52	A0
9	MHENBL	31	SB1	53	A2
10	N.C.	32	$\overline{\text{INH}}$	54	GND
11	TD7	33	$\overline{\text{INVL}}$	55	A6
12	TD8	34	$\overline{\text{SET}}$	56	A8
13	TD10	35	H/R	57	$\overline{\text{PURGE}}$
14	TD11	36	$\overline{\text{HIT}}$	58	MODE
15	TD12	37	HC0/RC0	59	$\overline{\text{VINV}}$
16	TD14	38	HC1/RC1	60	SB0
17	TD16	39	HIT1/REP1	61	Vcc
18	TD18	40	GND	62	$\overline{\text{WRITE}}$
19	N.C.	41	TD1	63	RLATCH
20	N.C.	42	TD3	64	$\overline{\text{PERR}}$
21	A1	43	TD4		
22	A3	44	TD5		

PIN DESCRIPTION

OUTPUTS

$\overline{HIT}$	HIT OUTPUT. "NOR" OF HIT0 TO HIT3
HCn/RCn	CODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 1)
HITn/REPn	UNCODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 3)
$\overline{PERR}$	PARITY ERROR
$\overline{MHIT}$	HIT OUTPUT MODIFIED BY MHENBL AND EXTH

INPUTS

MODE	MODE SELECTION MODE = 1 : 512 Entry x 4 Way MODE = 0 : 1024 Entry x 2 Way
A0–A9	ADDRESS INPUTS (A9 is not used for 4 way)
TD0–19	TAG INFORMATION INPUTS
$\overline{PURGE}$	ALL-PURGE TIMING PULSE
$\overline{INVL}$	PARTIAL-PURGE. V-BIT FORCED TO "0". LRU IS REVERSIVELY UPDATED
SBLK	ENABLE WAY-SELECTION EXTERNALLY AT REPLACEMENT AND INVALIDATION
SB0, SB1	EXTERNAL WAY-ADDRESS INPUTS
$\overline{WRITE}$	WRITE CYCLE SIGNAL
$\overline{SET}$	TIMING PULSE Write : Registrate TAG, V-bit "H", LRU update Read : LRU updated PARTIAL PURGE : LRU reversively update, V-bit "L"
$\overline{INH}$	ALL FUNCTIONS EXCEPT PURGE ARE INHIBITED
H/R	OUTPUT SELECTION H/R = 1 : Hit Information H/R = 0 : Replace Information
RLATCH	LATCH CONTROL FOR REPLACE INFORMATION
$\overline{PINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
$\overline{VINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
MHENBL	ENABLE $\overline{MHIT}$ OUTPUT
EXTH	FORCE $\overline{MHIT}$ OUTPUT TO "L"

FUNCTION TABLE

1) BASIC FUNCTION (Any combination except below are inhibited.)

Input					TAG Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	TAG	P bit	V bit	LRU	Function Mode
L	H	X	X	X	N-CNG	N-CNG	N-CNG	N-CNG	INHIBIT[3]
H	H	H	X	X	N-CNG	N-CNG	N-CNG	N-CNG	TAG READ
H	H	⊓	H	H	N-CNG	N-CNG	N-CNG	N-CNG[1] or UP-D	TAG READ
H	H	⊓	L	H	TD0 to TD19	SET	H	UP-D	TAG WRITE
X	L	H	X	X	UNDEFINED	UNDEFINED	L (All)	INCLZ	ALL PURGE
H	H	⊓	H	L	N-CNG	N-CNG	N-CNG/L[2]	N-CNG[1] or RUP-D	PARTIAL PURGE

X : "H" or "L"
N-CNG : No Change INCLZ : INITIALIZE
UP-D : Up Dated RUP-D : Reversively Updated
1. When SBLK = "L" and no-HIT, then LRU is no change (N-CNG).
2. When SBLK = "L" and no-HIT, then V-Bit is no change (N-CNG).
3. During INHIBIT mode, $\overline{HIT}$ and $\overline{PERR}$ outputs are "H" but the other outputs are "L".

2) OUTPUT PIN FUNCTION

Input		Internal Info.[1, 2]				Output							
Mode	A9	hit0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	$\overline{\text{HIT}}$[3]	Mode
H	X	L	L	L	L	L	L	L	L	L	L	H	
H	X	H	L	L	L	H	L	L	L	L	L	L	4
H	X	L	H	L	L	L	H	L	L	H	L	L	W
H	X	L	L	H	L	L	L	H	L	L	H	L	A
H	X	L	L	L	H	L	L	L	H	H	H	L	Y
L	L	L	X	L	X	L	L	L	L	L	L	H	
L	L	H	X	L	X	H	L	L	L	L	L	L	2
L	L	L	X	H	X	L	L	H	L	L	H	L	W
L	H	X	L	X	L	L	L	L	L	L	L	H	A
L	H	X	H	X	L	L	H	L	L	H	L	L	Y
L	H	X	L	X	H	L	L	L	H	H	H	L	

X: "H" or "L"

1. Internal information, rep0 to rep3 are determined by on-chip LRU logic when SBLK = "L". When SBLK = "H", the internal information are determined by external signal of SB0 & SB1.
2. Correct operation is not guaranteed if 2 ways or more become HIT at the same time.
3. Output of $\overline{\text{HIT}}$ is valid when H/R = "H".

3) PARTIAL PURGE ($\overline{\text{INVL}}$ = "L")

INPUT					INTERNAL INFO.				PURGE BLOCK				$\overline{\text{SET}}$	
					HIT				BLOCK					
MODE	A9	SBLK	SB0	SB1	0	1	2	3	0	1	2	3	LRU	MODE
H	X	L	X	X	L	L	L	L	—	—	—	—	---	
H	X	L	X	X	H	L	L	L	Q	—	—	—	RUP-D	4
H	X	L	X	X	L	H	L	L	—	Q	—	—	RUP-D	
H	X	L	X	X	L	L	H	L	—	—	Q	—	RUP-D	W
H	X	L	X	X	L	L	L	H	—	—	—	Q	RUP-D	A
H	X	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	Y
H	X	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
H	X	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	
H	X	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	
L	L	L	X	X	L	X	L	X	—	—	—	—	---	
L	L	L	X	X	H	X	L	X	Q	—	—	—	RUP-D	
L	L	L	X	X	L	X	H	X	—	—	Q	—	RUP-D	2
L	L	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	
L	L	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	W
L	H	L	X	X	X	L	X	L	—	—	—	—	---	A
L	H	L	X	X	X	H	X	L	—	Q	—	—	RUP-D	Y
L	H	L	X	X	X	L	X	H	—	—	—	Q	RUP-D	
L	H	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
L	H	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	

Note: Correct operation is not guaranteed if 2 ways or more become HIT at the same time.

4) PARITY ERROR & V-BIT[1] (n : 0 to 3)

pen	vn0	vn1	PEn	HIT Info.[2]
L	L	L	L	---
L	L	H	H	HIT
L	H	L	H	HIT
L	H	H	L	HIT
H	L	L	L	---
H	L	H	H	HIT
H	H	L	H	HIT
H	H	H	H	HIT

1. $\overline{\text{PERR}}$ is "NOR" of PE0 to PE3
2. Output information when internal "HIT" is valid.

pen : Internal parity error of way "n"
vn0/vn1 : Duplicate validity bits.
PEn : Determined by the following equation.

$$PEn = (vn0 + vn1) \cdot pen + (vn0 \oplus vn1)$$

BASIC FUNCTIONS

TAG READ

A comparison between the TAG input data (TD0-19) and the contents of the addressed location is performed. If both data are the same, that is "FOUND". Then $\overline{\text{HIT}}$ will be "LOW" and outputs of HCn, HITn indicate hitted "Associative way". In the case of "NOT-FOUND", the TAG RAM will specify the "way", which should be replaced, by using the LRU logic automatically.

The replacement information will be presented at the outputs of RCn and REPn by forcing the H/R input into "LOW". These signals will be latched and used for the data Memory move-in operation.

TAG WRITE

When "NOT-FOUND" is occurred, the TAG-RAM also should be updated. The write operation is performed by $\overline{\text{WRITE}}$ "LOW" and $\overline{\text{SET}}$ pulse input. The TAG data will be written into the proper "way" by the internal LRU logic.

TAG-WRITE mode, V-bit (Validity bit) and the parity are set, and LRU logic is updated.

On the other hand, it will be able to specify the "way" externally by using SBLK, SB0 and SB1 inputs.

ALL PURGE

By asserting $\overline{\text{PURGE}}$ input "LOW", the V-bit are reset and LRU logic is initialized.

In this operation, the contents of each TAG and its parity will not be identified.

PARTIAL PURGE

The partial purge operation is performed by $\overline{\text{INVL}}$ "LOW" and $\overline{\text{SET}}$ pulse input.

The V-bit, which is specified by the address inputs, will be reset, and LRU logic will be reversively updated.

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10	10	µA
Operating Supply Current	D_{OUT} = Open, Cycle = min.	I_{CC}		250	mA
Input Low Voltage		V_{IL}	-0.5*	0.8	V
Input High Voltage		V_{IH}	2.2	6.0	V
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = -4mA	V_{OH}	2.4		V

Note:
*-3.0V min. for pulse width less than 20ns.

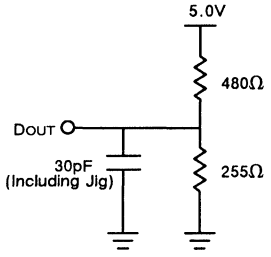
Fig. 3 — AC TEST CONDITION

INPUT PULSE LEVELS : 0.0V to 3.0V

INPUT PULSE RISE AND FALL TIMES : 5ns (Transient time between 0.8V and 2.2V)

TIMING REFERENCE LEVELS : Input : 1.5V
Output : 1.5V

OUTPUT LOAD:



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

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TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H", or "L", $\overline{\text{VINV}}$ = "H" or "L", $\overline{\text{INH}}$ = "H")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	50		50		ns
Address Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{AH}		25		30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}		27		32	ns
TAG Data Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{TH}		18		18	ns
TAG Data Valid to $\overline{\text{MHIT}}$	t_{TMH}		20		20	ns
$\overline{\text{HIT}}$, HCn, HITn Hold Time	t_{HH}	0		0		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
RCn, REPn Hold Time for RLATCH	t_{RH}	0		0		ns
SBLK, SB0, SB1 Setup Time for RCn, REPn	t_{SBR}		25		25	ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns
RCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0		0		ns
H/R to Multiplex output change	t_{HR}		10		12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ output	t_{MMH}		10		12	ns

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", H/R = "L", $\overline{\text{INH}}$ = "H")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	50		50		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Setup Time for PCn, REPn	t_{SBR}		25		25	ns
PCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK Hold Time	t_{SBH}	5		5		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Setup Time for $\overline{\text{SET}}$	t_{IS}	25		25		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Hold Time	t_{IR}	5		5		ns

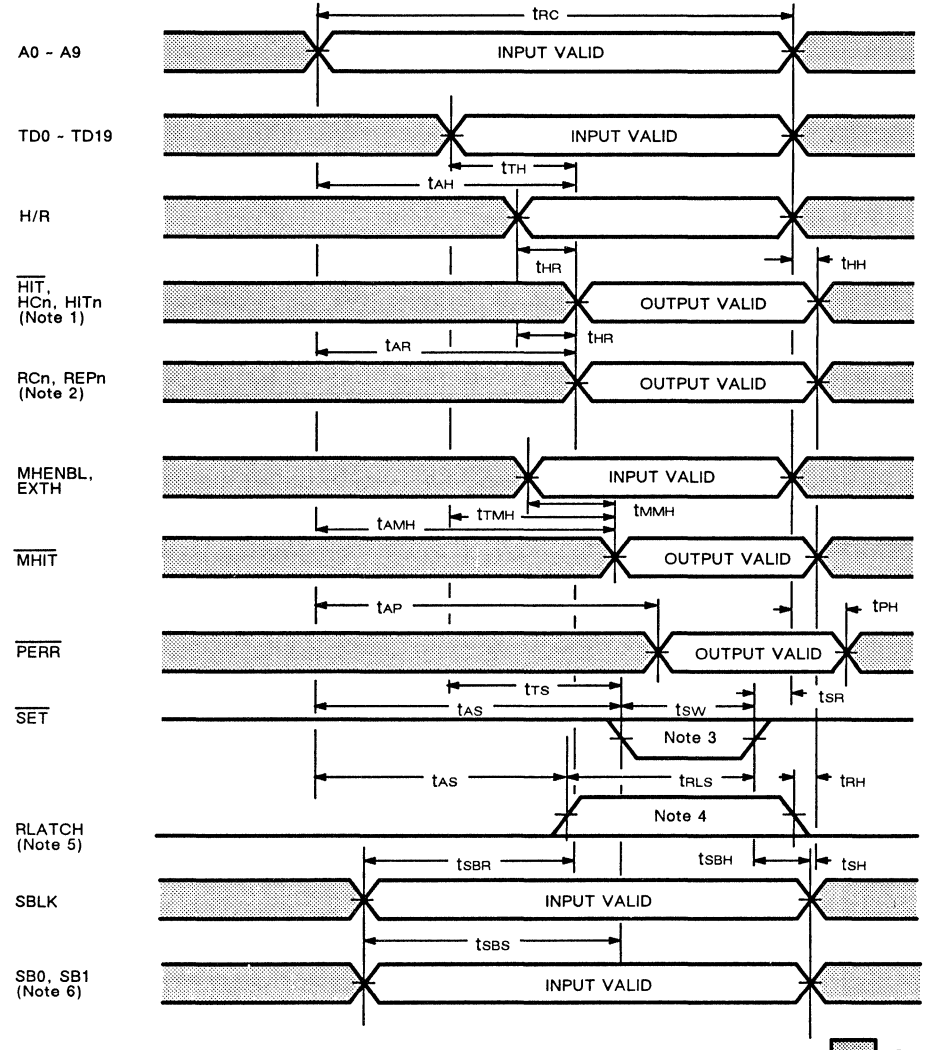
PERTIAL PURGE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$= "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Pertial Purge Cycle	t_{PPC}	50		50		ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns

ALL PURGE ($\overline{\text{SET}}$ = "H", Other control inputs are "H" or "L")

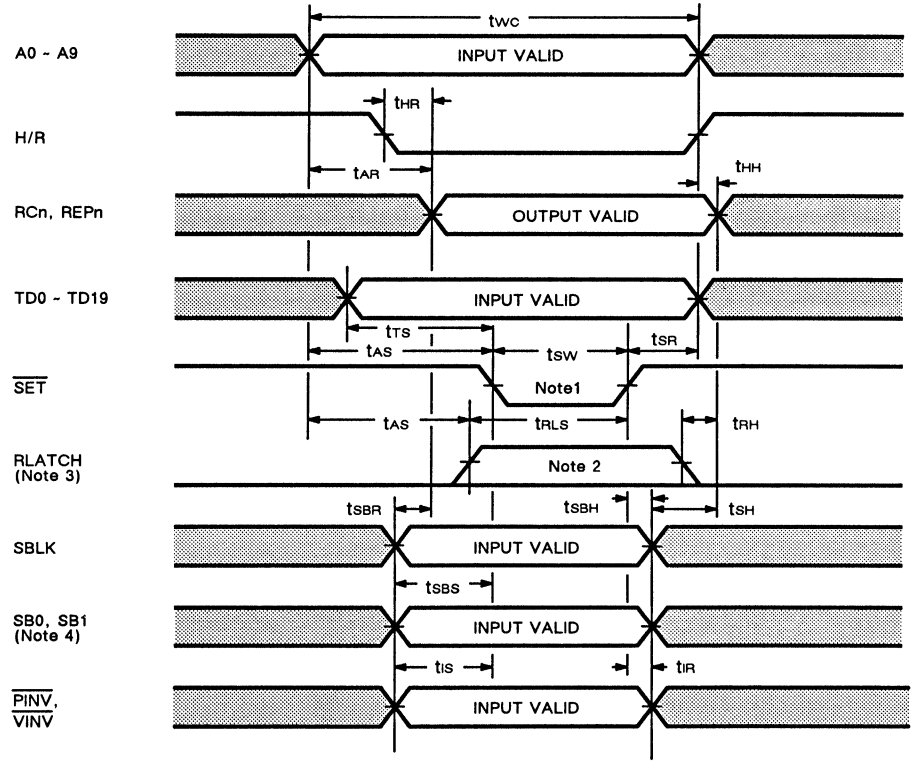
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
All Purge Cycle Time	t_{APC}	100		100		ns
Purge Pulse Width	t_{PPW}	50		50		ns
Purge Recovery Time	t_{PR}	50		50		ns

TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L", INH = "H")



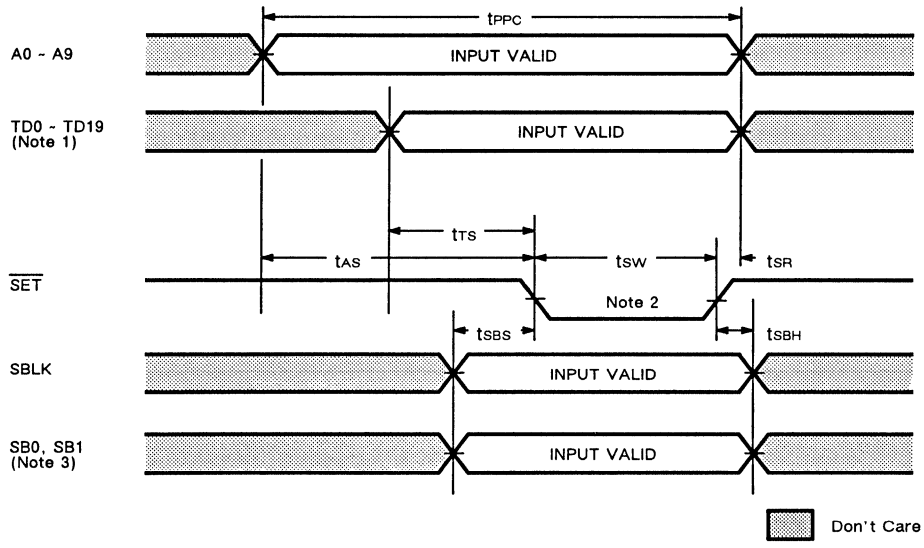
Notes 1: Valid at H/R = "H".
2: Valid at H/R = "L".
3: LRU is updated at $\overline{\text{SET}}$ = "L".
4: Replace latched at RLATCH = "H".
5: Valid at SBLK = "L".
6: Valid at SBLK = "H".

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", $\overline{\text{INH}}$ = "H")



Notes 1. Registrate TAG, V-bit "H", LRU update.
2. Replace latched at $\overline{\text{RLATCH}}$ = "H".
3. Valid at SBLK = "L".
4. Valid at SBLK = "H".

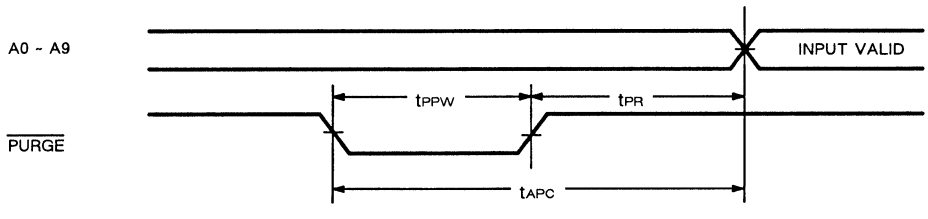
PARTIAL PURGE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")



Notes:

1. Valid at SBLK = "L".
2. LRU is reversively updated, V-bit "L".
3. Valid at SBLK = "H".

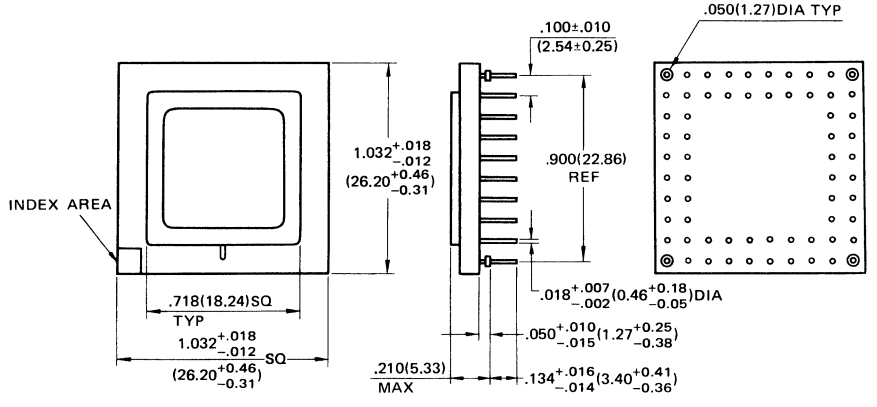
All purge ($\overline{\text{SET}}$ = "H", OTHER CONTROL INPUTS ARE "H" or "L")



PACKAGE DIMENSIONS

(Suffix: -CR)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-64C-A02)



Dimensions in
inches (millimeters)

4