*January 1990*
*Edition 3.0*

FUJITSU

*DATA SHEET*

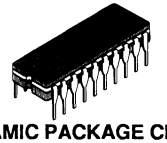
# *MB81C67-35/-45/-55*
# *CMOS 16K-BIT HIGH-SPEED SRAM*

## 16K Words x 1 Bit High-Speed CMOS Static Random Access Memory

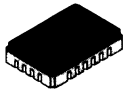
The Fujitsu MB81C67 is a 16,384 words x 1 bit static random access memory fabricated with a CMOS silicon gate process. All pins are TTL compatible and a single +5 V power supply is required.

A chip select ($\overline{CS}$) pin permits the selection of an individual package when outputs are OR-tied, and automatically powers down the device. The MB81C67 offers low power dissipation, low cost, and high performance.

- Organization: 16,384 words x 1 bit
- Static operation: no clocks or refresh required
- Access time: 35 ns max. (MB81C67-35)
  45 ns max. (MB81C67-45)
  55 ns max. (MB81C67-55)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 20-pin Plastic Package:
  DIP MB81C67-xxP
- Standard 20-pad Ceramic Package:
  LCC MB81C67-xxTV
- Standard 20-pin Ceramic Package:
  CERDIP MB81C67-xxZ
- Pin compatible with Fujitsu MB8167A



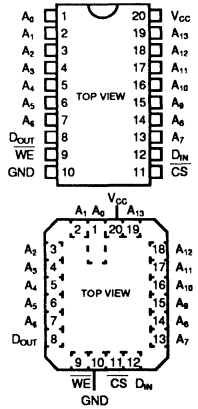
CERAMIC PACKAGE CERDIP
DIP-20C-C03



CERAMIC PACKAGE
LCC-20C-F01

PLASTIC PACKAGE
DIP-20P-M01

**PIN ASSIGNMENT**




## Absolute Maximum Ratings (See Note)

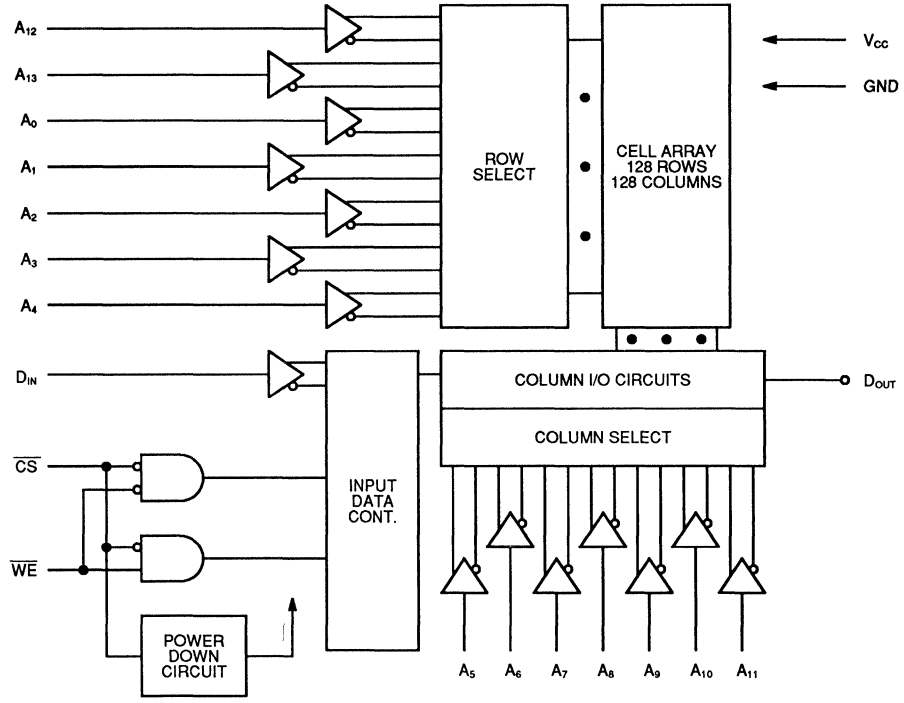
| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage on any pin with respect to GND | | $V_{IN}$ | −3.5 to +7.0 | V |
| Output Voltage on any pin with respect to GND | | $V_{OUT}$ | −0.5 to +7.0 | V |
| Output Current | | $I_{OUT}$ | ±50 | mA |
| Power Dissipation | | $P_D$ | 1.2 | W |
| Temperature Under Bias | | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature Range | Ceramic | $T_{STG}$ | −65 to +150 | °C |
| | Plastic | | −45 to +125 | |

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MB81C67 BLOCK DIAGRAM




TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | MODE | OUTPUT | POWER |
|---|---|---|---|---|
| H | X | NOT SELECTED | HIGH-Z | STANDBY |
| L | L | WRITE | HIGH-Z | ACTIVE |
| L | H | READ | $D_{OUT}$ | ACTIVE |

## CAPACITANCE ($T_A$= 25°C, f = 1MHz)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance ($V_{IN}$=0V) | $C_{IN}$ | | 5 | pF |
| $\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V) | $C_{\overline{CS}}$ | | 7 | pF |
| Output Capacitance ($V_{OUT}$=0V) | $C_{OUT}$ | | 8 | pF |

# RECOMMENDED OPERATING CONDITIONS

**(Referenced to GND)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | –3.0* | | 0.8 | V |
| Input High Voltage | $V_{IL}$ | 2.2 | | 6.0 | V |
| Ambient Temperature | $T_A$ | 0 | | 70 | °C |

*–3.0V Min. for pulse width less than 20ns. ($V_{IL}$ Min=–1.0V at DC level)



# DC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

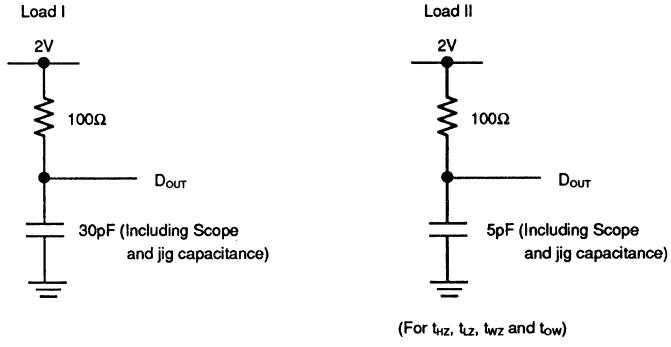
| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | $V_{IN}$=0V to $V_{CC}$ | $I_{LI}$ | –2.0 | | 2.0 | µA |
| Output Leakage Current | $\overline{CS}$=$V_{IH}$, $V_{OUT}$=0V to $V_{CC}$ | $I_{LO}$ | –2.0 | | 2.0 | µA |
| Active Supply Current | $\overline{CS}$=$V_{IL}$, $I_{OUT}$=0mA $V_{IN}$=$V_{IL}$ or $V_{IH}$ | $I_{CC1}$ | | 25 | 40 | mA |
| Operating Supply Current | $\overline{CS}$=$V_{IL}$, $I_{OUT}$=0mA Cycle=Min, $C_L$=0pF | $I_{CC2}$ | | 35 | 60 | mA |
| Standby Supply Current | $\overline{CS}$≥$V_{CC}$–0.2V $V_{IN}$≥$V_{CC}$ –0.2V or $V_{IN}$≤0.2V | $I_{SB1}$ | | 2 | 15 | mA |
| Standby Supply Current | $\overline{CS}$=$V_{IH}$, | $I_{SB2}$ | | 15 | 25 | mA |
| Output Low Voltage | $I_{OL}$=16mA | $V_{OL}$ | | | 0.4 | V |
| Output High Voltage | $I_{OH}$=–4mA | $V_{OH}$ | 2.4 | | | V |

1

### AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels: | 0.6V to 2.4V |
| Input Pulse Rise And Fall Times: | 5ns |
| Timing Measurement Reference Levels: | Input : 1.5V<br>Output : 1.5V |

Output Load: Fig.2




# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

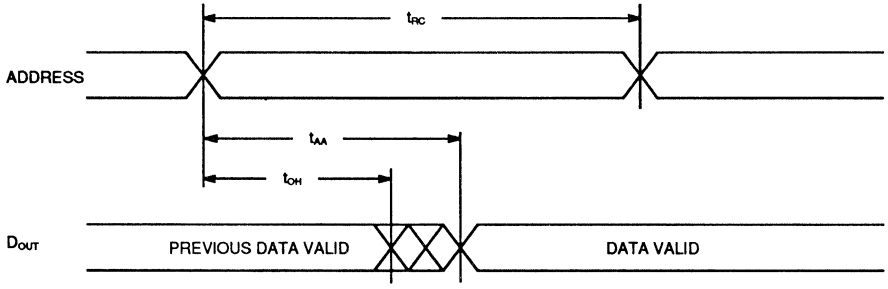
**READ CYCLE *1**

| Parameter | Symbol | MB81C67–35 | | MB81C67–45 | | MB81C67–55 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time *2 | $t_{RC}$ | 35 | | 45 | | 55 | | ns |
| Address Access Time *3 | $t_{AA}$ | | 35 | | 45 | | 55 | ns |
| Chip Select Access Time *4 | $t_{ACS}$ | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | | 5 | | 5 | | ns |
| Chip Selection to Output in Low–Z *5 | $t_{LZ}$ | 5 | | 5 | | 5 | | ns |
| Chip Deselection to Output in High–Z *5 | $t_{HZ}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| Chip Selection to Power Up | $t_{PU}$ | 0 | | 0 | | 0 | | ns |
| Chip Deselection to Power Down | $t_{PD}$ | | 30 | | 40 | | 50 | ns |

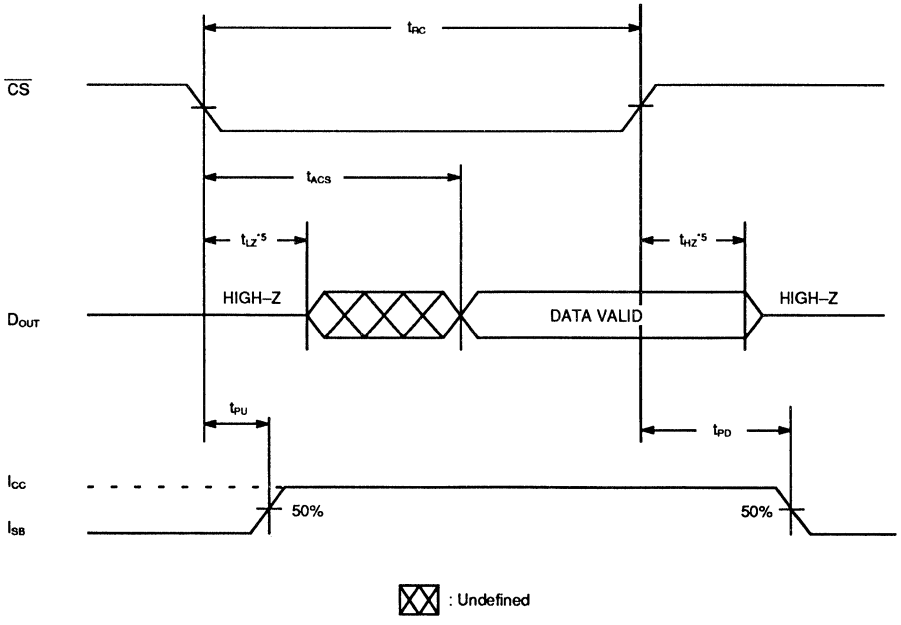
**Note:** *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS}=V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

## READ CYCLE TIMING DIAGRAM *1*2

READ CYCLE : ADDRESS CONTROLLED *3




READ CYCLE : $\overline{CS}$ CONTROLLED *4



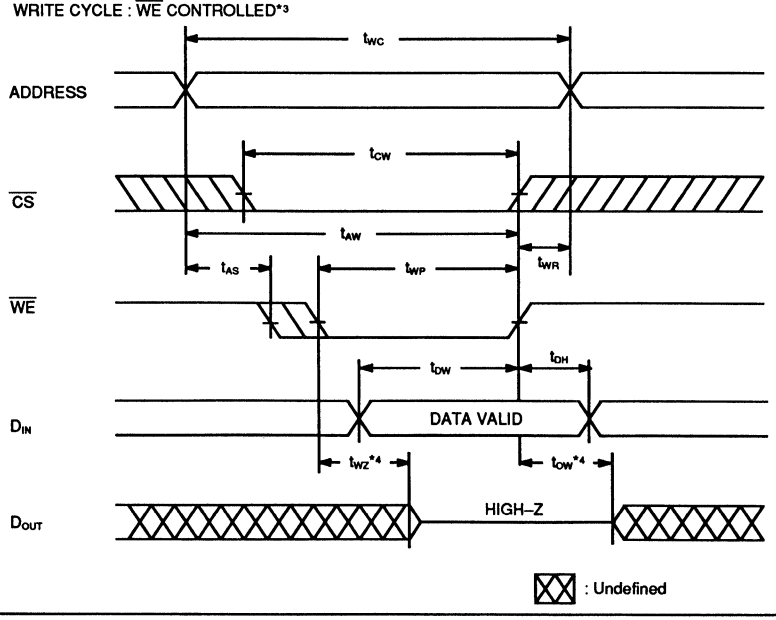

: Undefined

**Note:** *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS}$=$V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

**WRITE CYCLE *1*2**

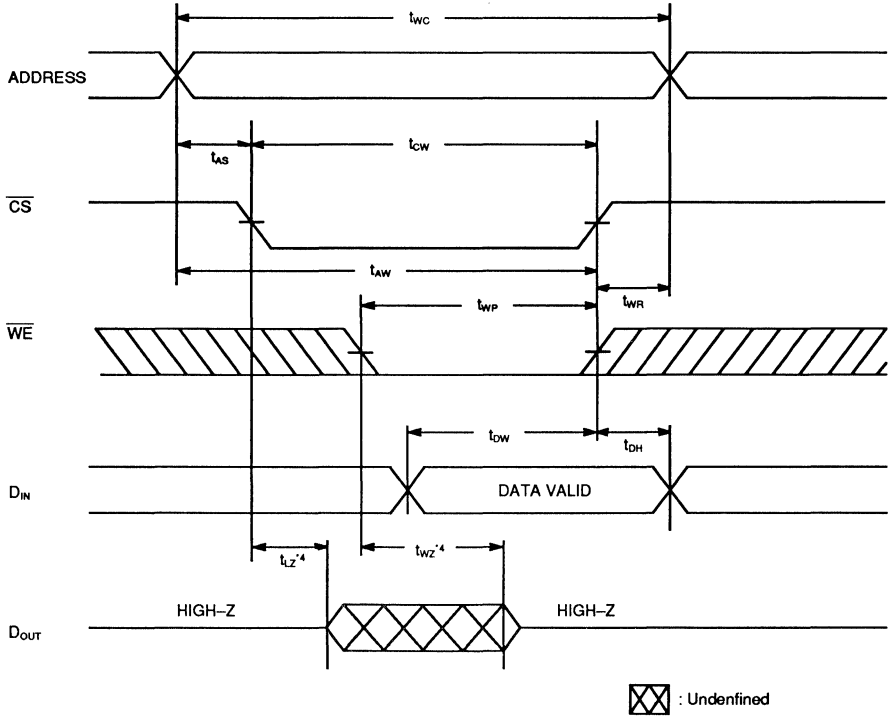
| Parameter | Symbol | MB81C67–35 | | MB81C67–45 | | MB81C67–55 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time *3 | $t_{WC}$ | 35 | | 45 | | 55 | | ns |
| Chip Selection to End of Write | $t_{CW}$ | 30 | | 35 | | 50 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 30 | | 35 | | 50 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | ns |
| Write Pulse Width | $t_{WP}$ | 20 | | 25 | | 30 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 20 | | 20 | | 25 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | ns |
| Write Enable to Output in High–Z *4 | $t_{WZ}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| Output Active from End of Write *4 | $t_{OW}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns |

**WRITE CYCLE TIMING DIAGRAM *1*2**




**Note:** *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transition to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

**WRITE CYCLE TIMING DIAGRAM *1*2**




**Note:** *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transistion.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transistion to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

1

# TYPICAL CHARACTERISTICS CURVES

**Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**

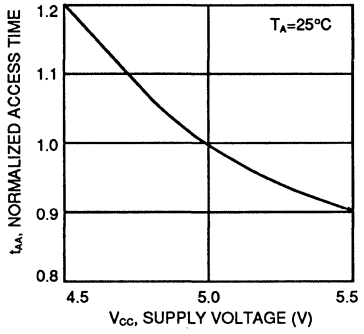



**Fig. 4 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**

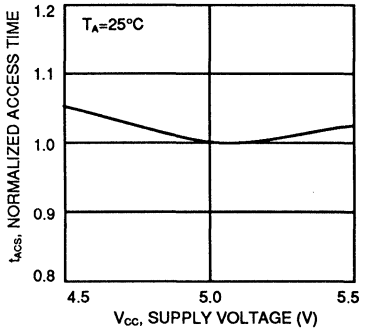



**Fig. 5 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**

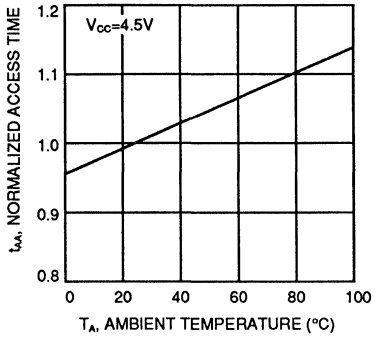



**Fig. 6 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**

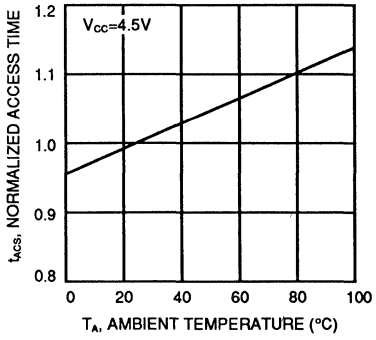



**Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE**

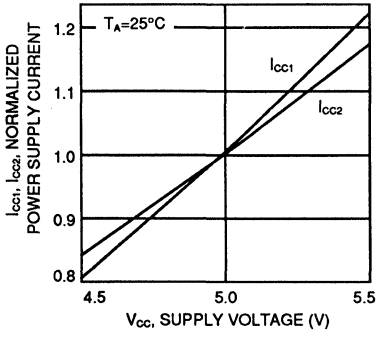



**Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE**

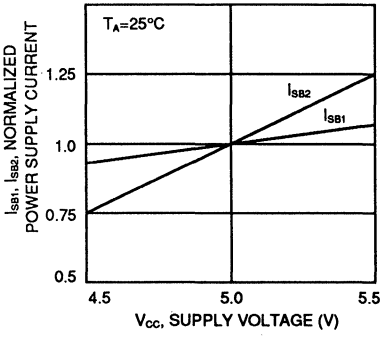


Fig. 9 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

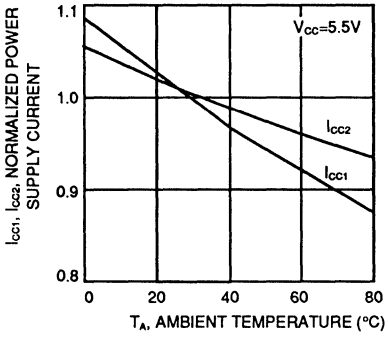



Fig. 10 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

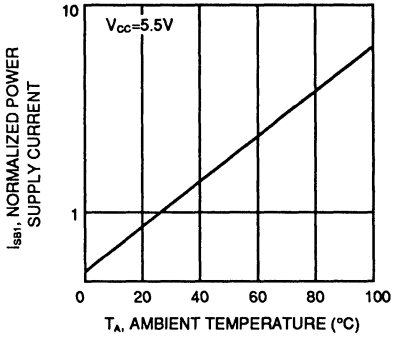



Fig. 11 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

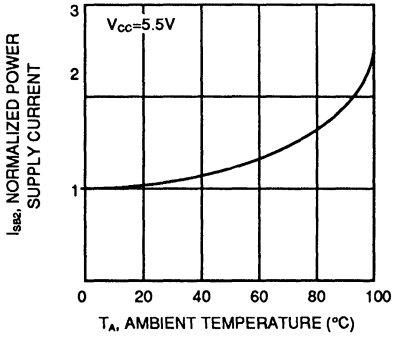



Fig. 12 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

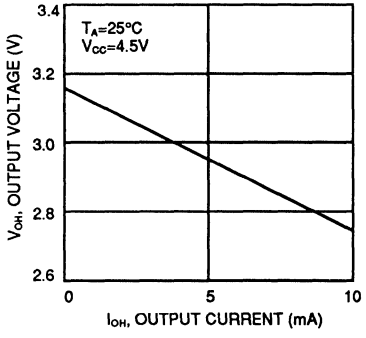



Fig. 13 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

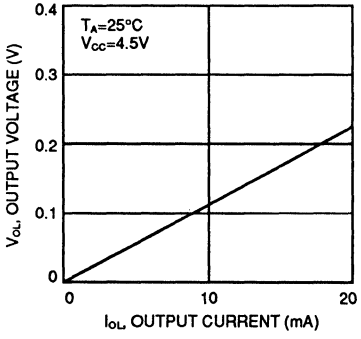
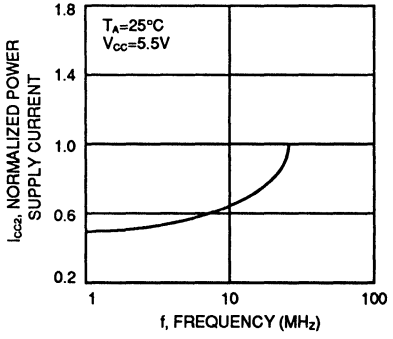



Fig. 14 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY



1

Fig. 15– NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

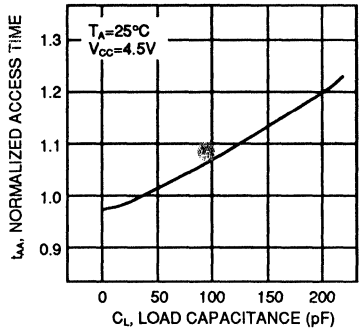
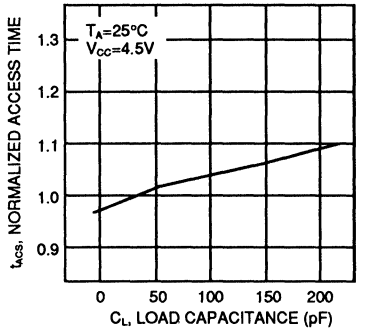


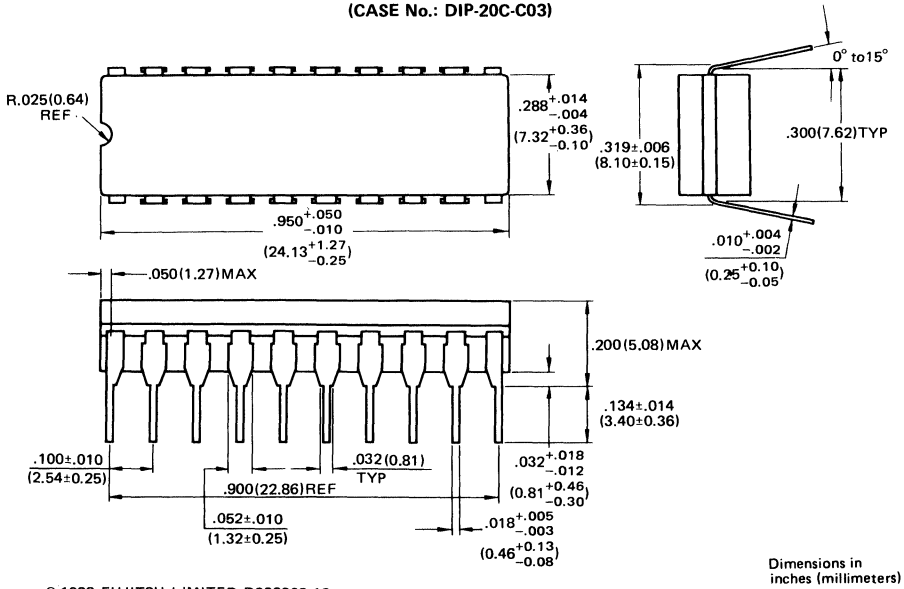

Fig. 16– NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE




# PACKAGE DIMENSIONS

(Suffix: CZ)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

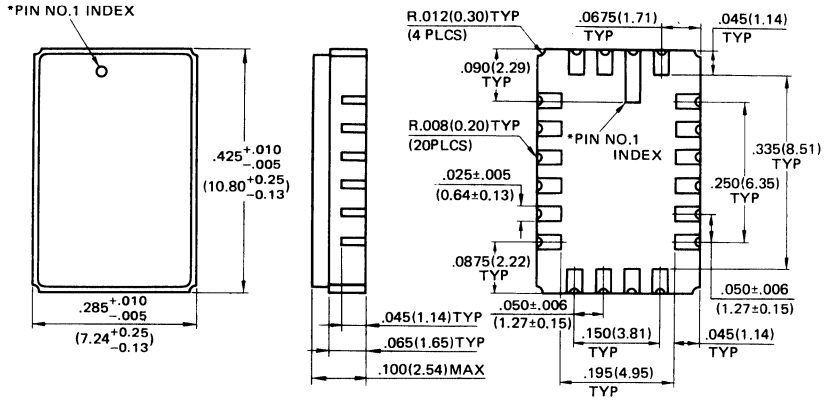



Dimensions in inches (millimeters)

# PACKAGE DIMENSIONS

**(Suffix: TV)**

**20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER**
**(CASE No.: LCC-20C-F01)**




Dimension in
inches (millimeters)

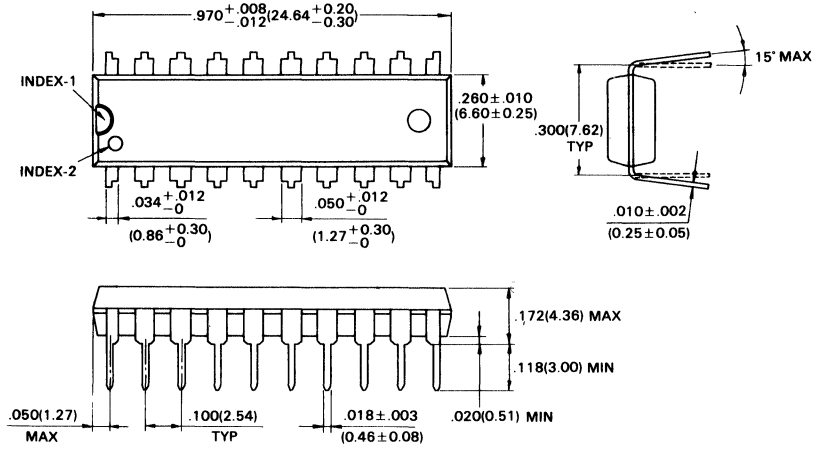
* Shape of PIN NO. 1 INDEX: Subject to change without notice.

# PACKAGE DIMENSIONS

**(Suffix: P)**

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M01)






Dimensions in
inches (millimeters)