April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C69A-25/-30/-35
CMOS 16K-BIT HIGH-SPEED SRAM

1

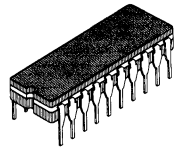
4K Words x 4 Bits Static Random Access Memory with Super High-Speed

The Fujitsu MB81C69A is a 4,096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry. All pins are TTL compatible and a single +5 V power supply is required.

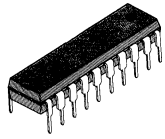
A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design by permiting the selection of an individual package when outputs are OR-tied.

The MB81C69A offers low power dissipation, low cost, and high performance.

- Organization: 4,096 words x 4 bits
- Static operation: no clocks or timing strobe required
- Access time: t_{AA} = 25 ns max, t_{ACS} = 15 ns max. (MB81C69A-25)
  t_{AA} = 30 ns max, t_{ACS} = 18 ns max. (MB81C69A-30)
  t_{AA} = 35 ns max, t_{ACS} = 20 ns max. (MB81C69A-35)
- Low power consumption: 385 mW max. (Active)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion
- Electrostatic protection for all inputs and outputs
- Standard 20-pin Plastic Package:
  DIP MB81C69A-xxP
- Standard 20-pad Ceramic Package:
  LCC MB81C69A-xxTV
- Standard 20-pin Ceramic Package:
  CERDIP MB81C69A-xxZ



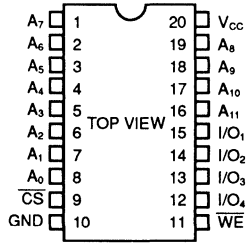
CERAMIC PACKAGE CERDIP
(DIP-20C-C03)



PLASTIC PACKAGE
(DIP-20P-M01)

LCC: See page 11

PIN ASSIGNMENT



LCC: See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{out}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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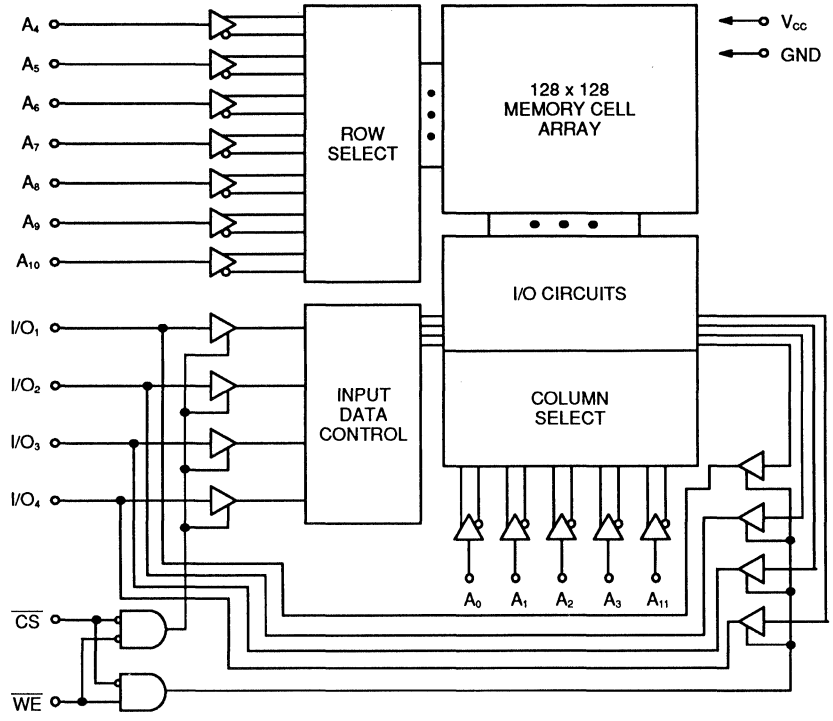
Fig. 1 – MB81C69A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	NOT SELECTED	HIGH-Z
L	L	WRITE	D_{IN}
L	H	READ	D_{OUT}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}	I_{LO}	−10		10	µA
Active Supply Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA V_{IN}=V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$=V_{IL} I_{OUT}=0mA, Cycle=Min	I_{CC2}		40	70	mA
Input Low Voltage		V_{IL}	−2.0*		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V
Output Low Voltage	I_{OL}=8mA	V_{OL}			0.4	V
Output High Voltage	I_{OH}=−4mA	V_{OH}	2.4			V

Note: * −2.0V Min. for pulse width less than 20ns. (V_{IL} Min.=−0.5V at DC level)

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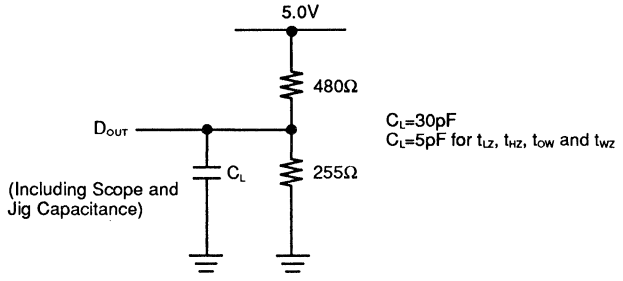
AC TEST CONDITION

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input : 1.5V Output : 1.5V
Output Load:	

Fig. 2



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

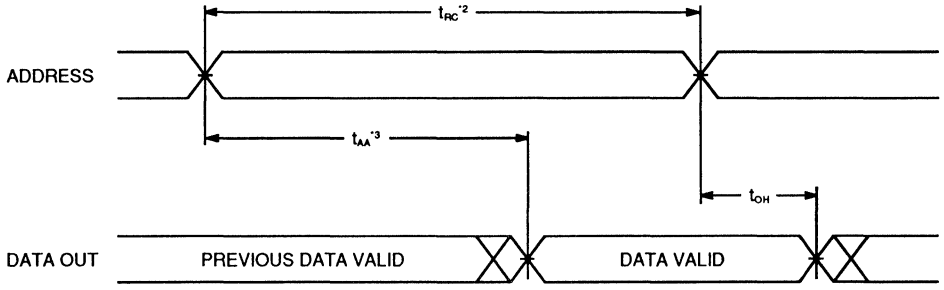
READ CYCLE*1

Parameter	Symbol	MB81C69A-25		MB81C69A-30		MB81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4	t_{ACS}		15		18		20	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*5	t_{LZ}	0		0		0		ns
Chip Deselection to Output in High-Z*5	t_{HZ}		10		13		15	ns

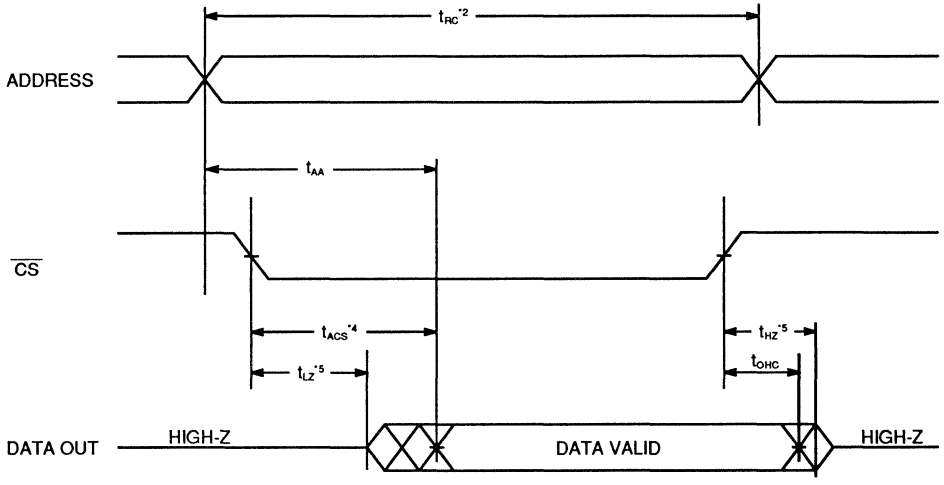
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}=V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state Voltage with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED



READ CYCLE : $\overline{CS}$ CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

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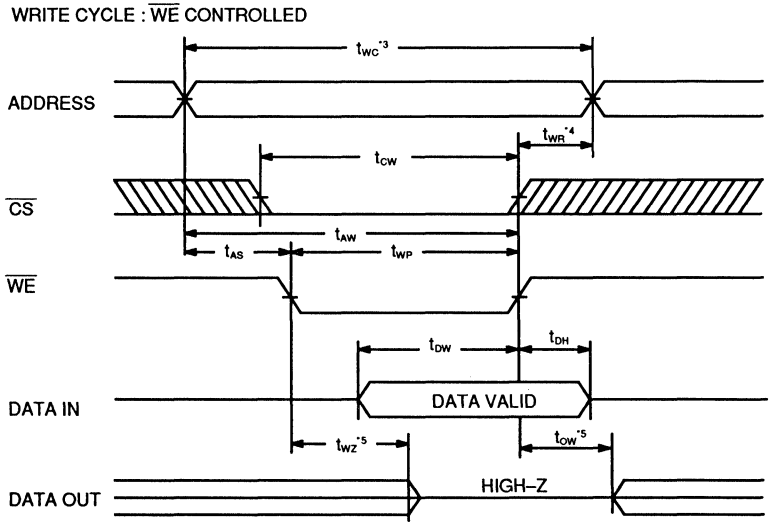
WRITE CYCLE*1 *2

Parameter	Symbol	MB81C69A-25		MB81C69A-30		MB81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time*4	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

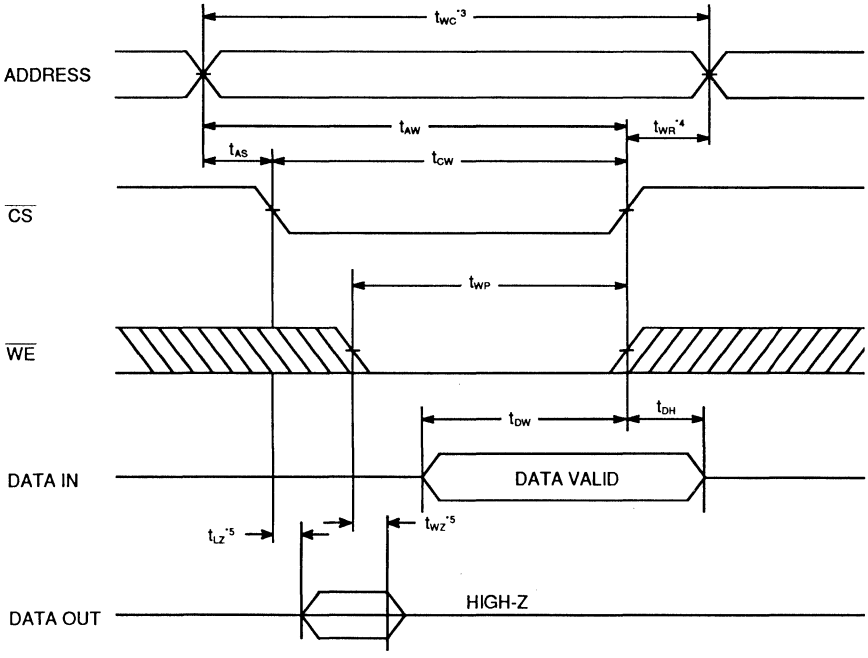
*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is specified at the point of +500mV from steady state voltage with Load II in Fig. 2.

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TYPICAL CHARACTERISTICS CURVES

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

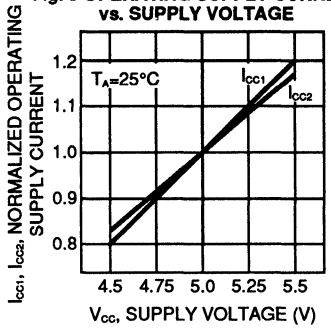


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

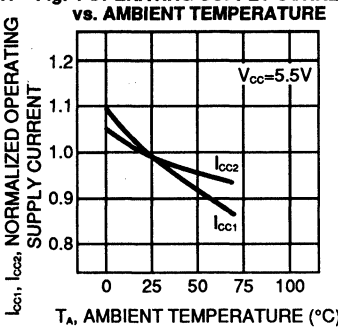


Fig. 5 OPERATING SUPPLY CURRENT vs. FREQUENCY

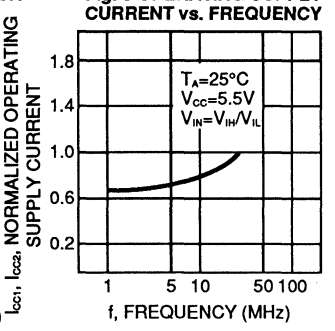


Fig. 6 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

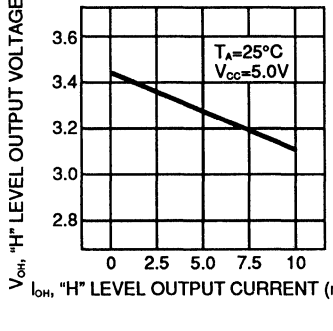


Fig. 7 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

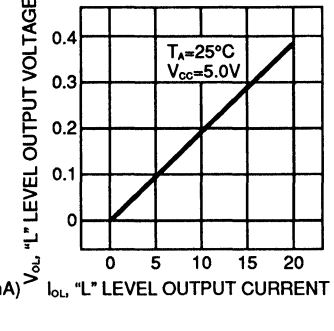


Fig. 8 ACCESS TIME vs. SUPPLY VOLTAGE

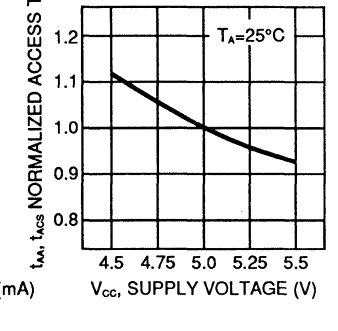


Fig. 9 ACCESS TIME vs. AMBIENT TEMPERATURE

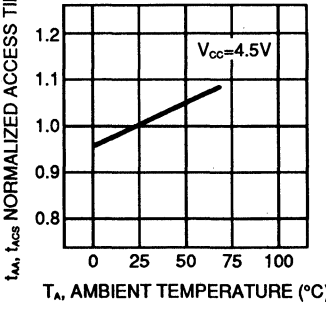
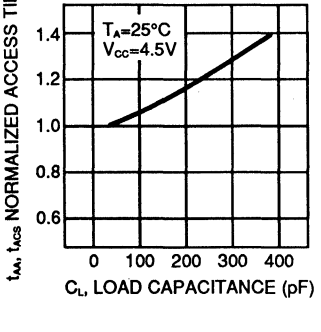


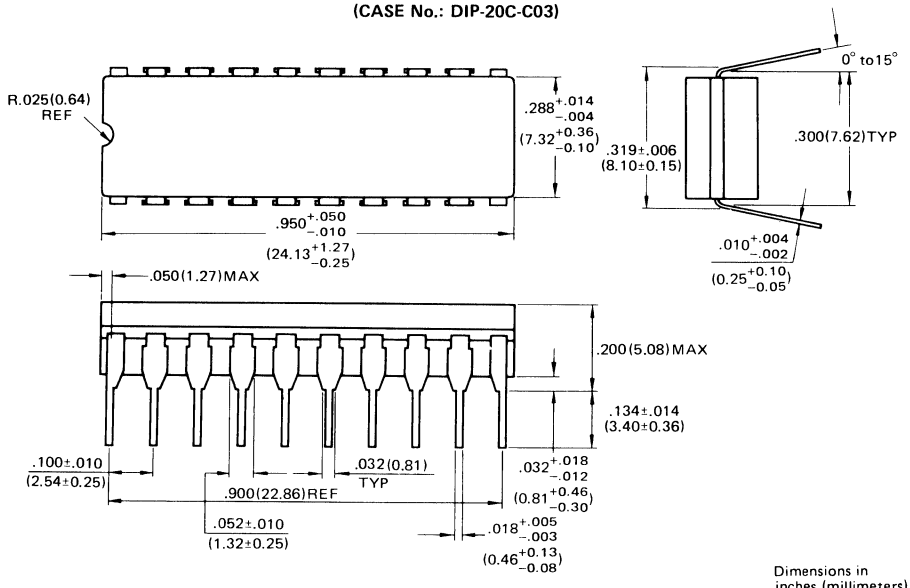
Fig. 10 ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: Z)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in
inches (millimeters)

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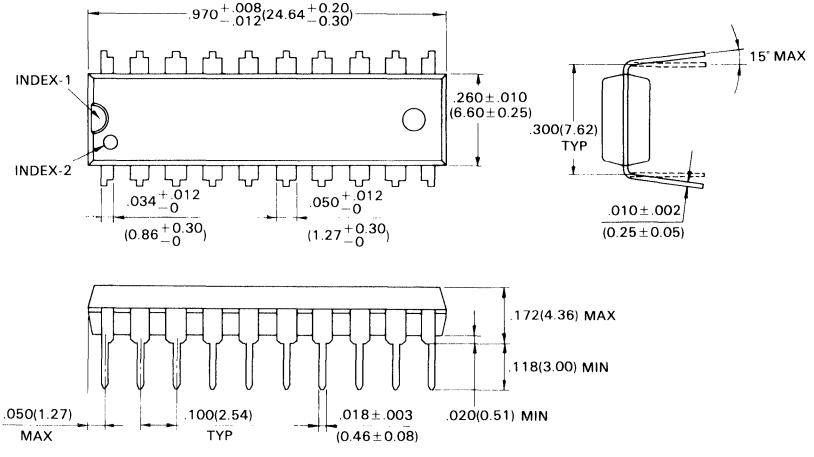
PACKAGE DIMENSIONS (Cont'd)

PLASTIC DIP (Suffix: P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M01)



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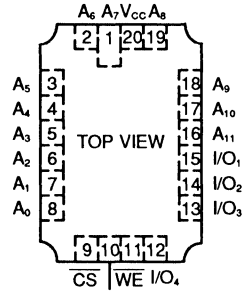
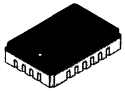
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

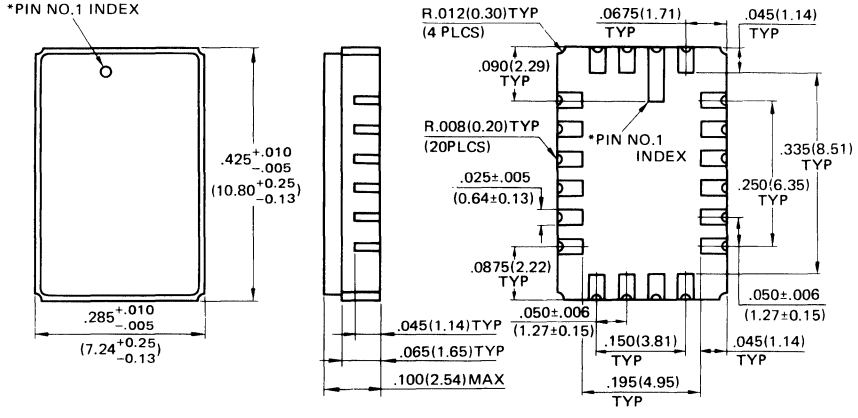
CERAMIC LCC (Suffix: TV)





CERAMIC PACKAGE (LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER (CASE No.: LCC-20C-F01)



Dimension in inches (millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

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