March 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C71A-25/-30/-35
CMOS 64K-BIT HIGH-SPEED SRAM

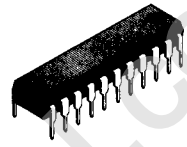
1

64K Words x 1 Bit High-Speed CMOS Static Random Access Memory

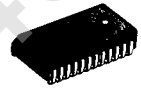
The Fujitsu MB81C71A is a 65,536 words x 1 bit static random access memory fabricated with a CMOS technology. It uses fully static circuitry throughout and, therefore, requires no clocks or refreshes to operate.

The MB81C71A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. It is compatible with TTL logic, and requires a single +5 V supply.

- Organization: 65,536 words x 1 bit
- Static operation: no clocks or refresh required
- Access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB81C71A-25)
  $t_{AA} = t_{ACS}$ = 30 ns max. (MB81C71A-30)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB81C71A-35)
- Single +5 V power supply ±10% tolerance
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 22-pin Plastic Package:
  DIP MB81C71A-xxP
- Standard 24-pin Plastic Package:
  SOJ MB81C71A-xxPJ
- Standard 22-pad Ceramic Package:
  LCC (metal seal) MB81C71A-xxCV



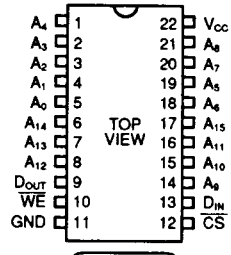
PLASTIC PACKAGE
DIP-22P-M04

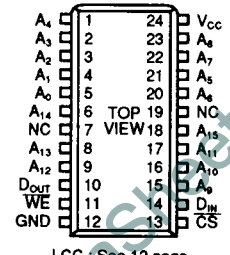


PLASTIC PACKAGE
LCC-24P-M02

LCC : See page 12.

PIN ASSIGNMENT





LCC : See 12 page.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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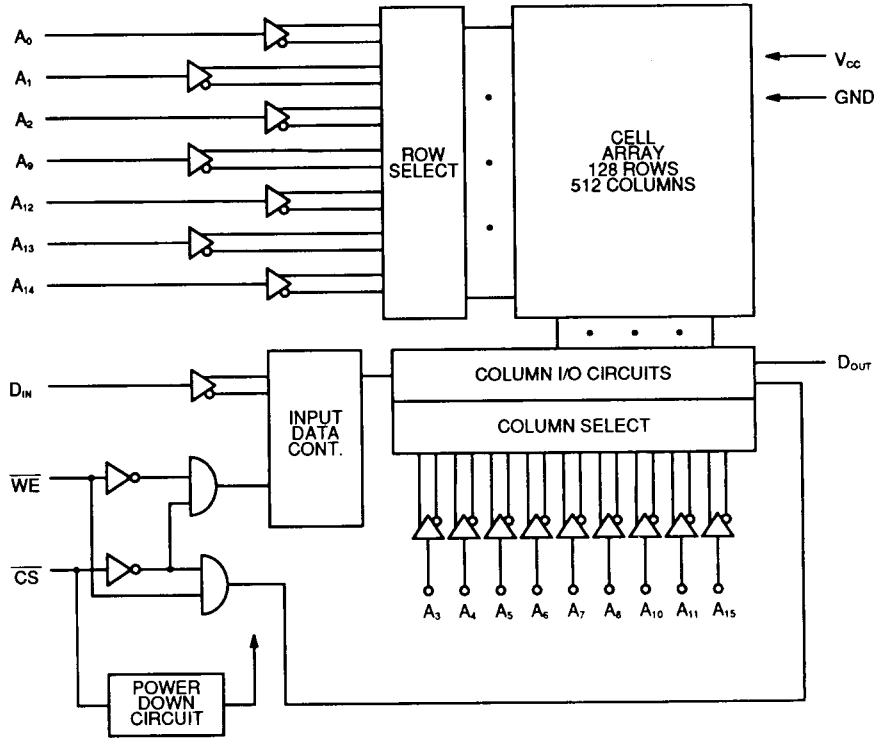
Fig. 1 – MB81C71A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance (V_{IN}=0V)	C_{IN}		7	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current	V_{IN}=0V to V_{CC} V_{CC}=Max.	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, V_{OUT}=0V to 4.5V V_{CC}=Max.	I_{LO}	−10		10	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, V_{CC}=Max. D_{OUT}=Open, Cycle=Min.	I_{CC}		50	80	mA
Standby Current	V_{CC}=Min. to Max. $\overline{CS}$≥V_{CC} −0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC} −0.2V	I_{SB1}		1	10	mA
Standby Current	V_{CC}=Min. to Max. $\overline{CS}$=V_{IH}	I_{SB2}		10	20	mA
Input Low Voltage		V_{IL}	−2.0*		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V
Output Low Voltage	I_{OL}=16mA	V_{OL}			0.45	V
Output High Voltage	I_{OH}=−4mA	V_{OH}	2.4			V
Peak Power on Current**	V_{CC}=0V to V_{CC} Min. $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.	I_{PO}			30	mA

* −2.0V Min, for pulse width less than 20 ns. (V_{IL} Min=−0.5V at DC Level)

** A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

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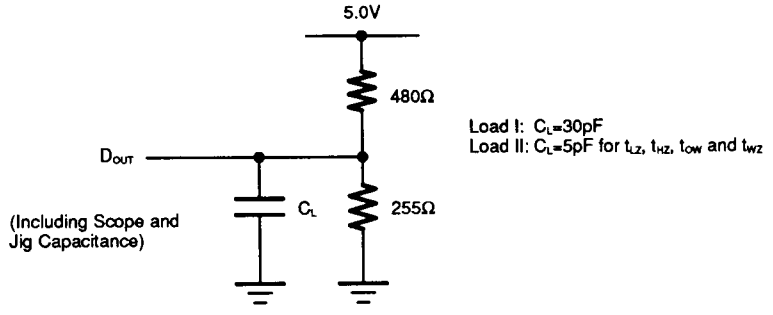
Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise And Fall Times: 5ns
- Timing Measurement Reference Levels: Input : 1.5V, Output : 1.5V
- Output Load:



AC CHARACTERISTICS

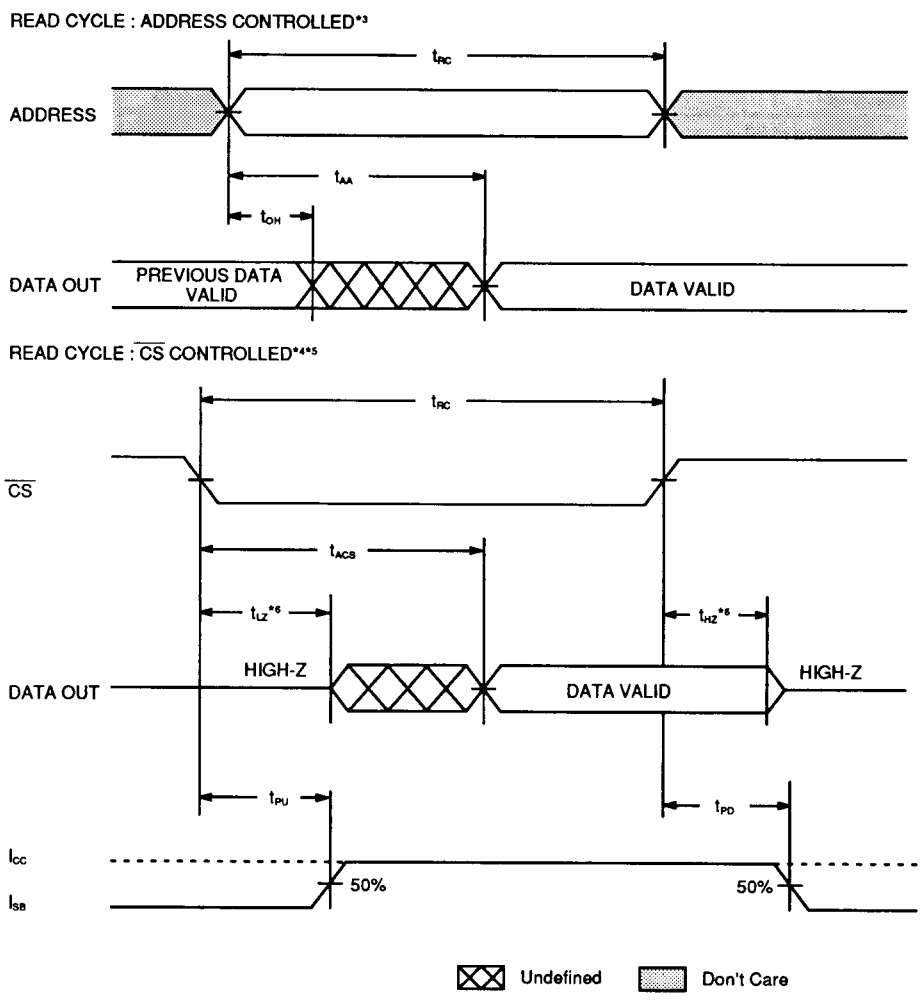
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB81C71A-25		MB81C71A-30		MB81C71A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4*5	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low-Z*6	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*6	t_{HZ}	0	10	0	13	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down time	t_{PD}		20		25		30	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}=V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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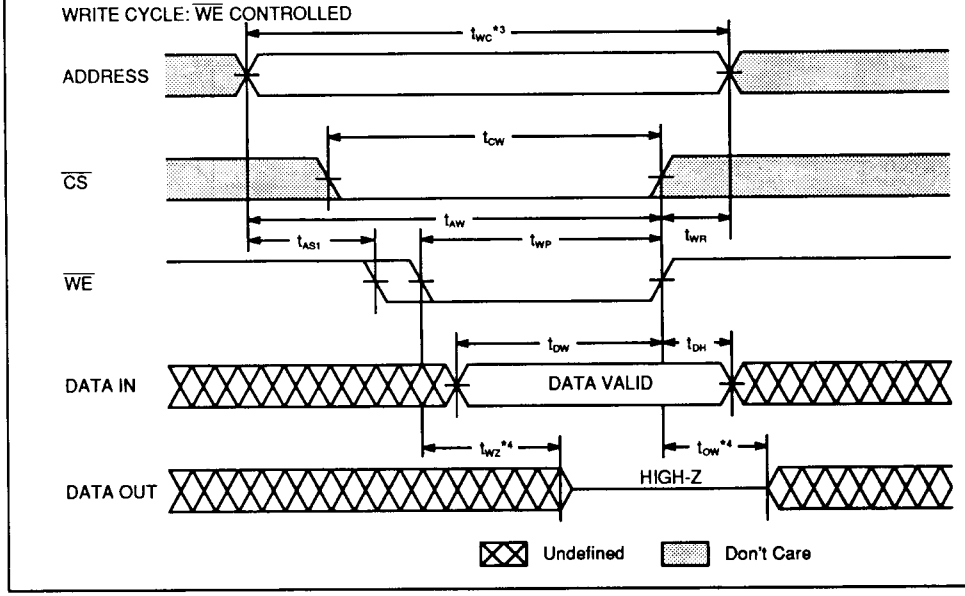
WRITE CYCLE*1*2

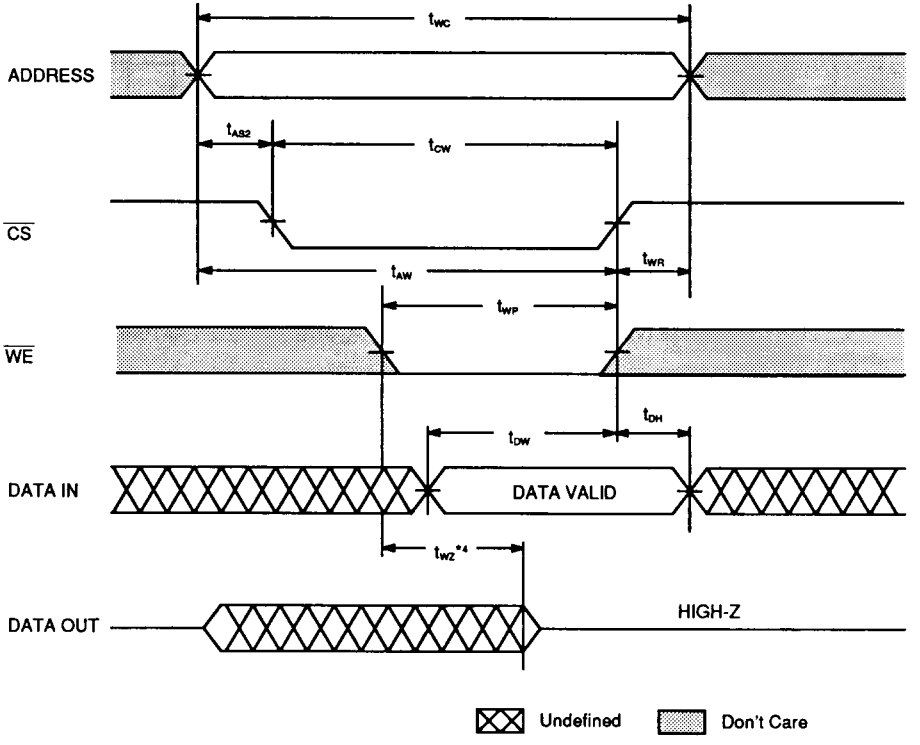
Parameter	Symbol	MB81C71A-25		MB81C71A-30		MB81C71A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS1}	0		0		0		ns
Address Setup Time	t_{AS2}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Valid to End of Write	t_{DW}	15		18		20		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	2		2		2		ns
Write Enable to Output in High-Z*4	t_{WZ}	0	10	0	13	0	15	ns
Output Active from End of Write*4	t_{OW}	0		0		0		ns

WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

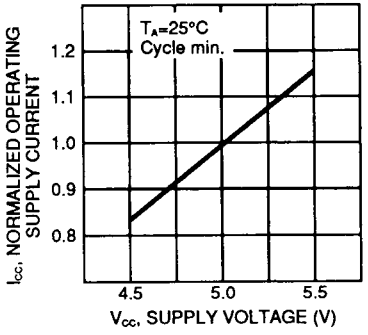


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

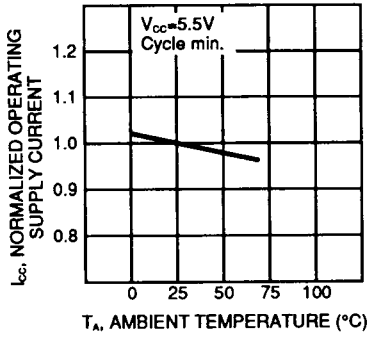


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

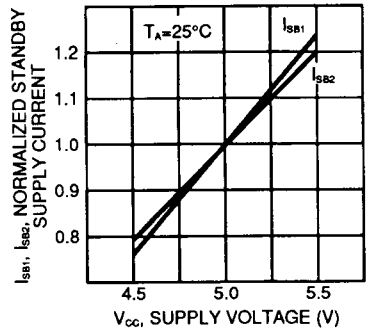


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

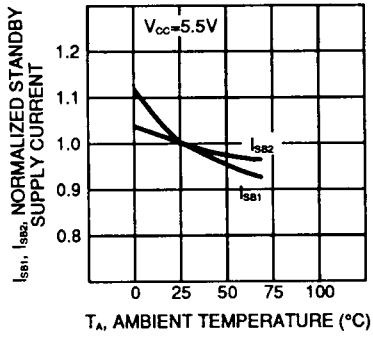
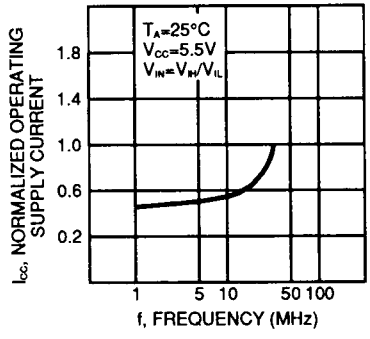


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

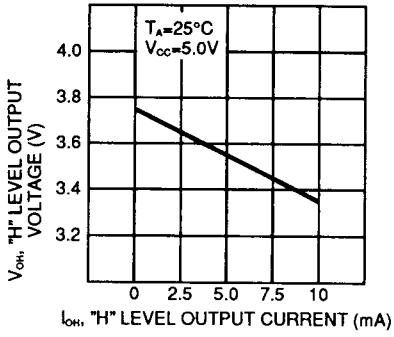


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

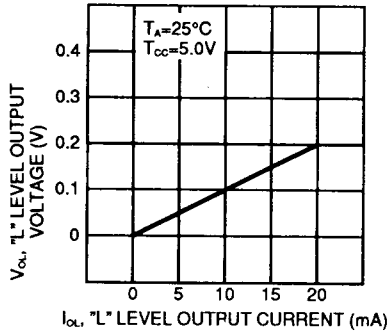


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

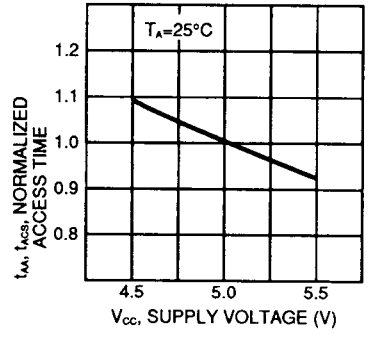


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

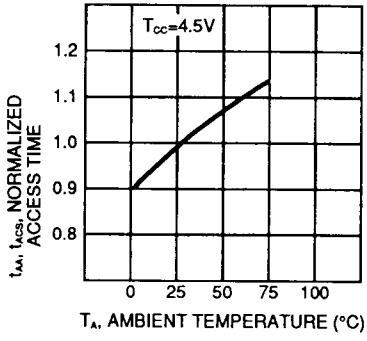
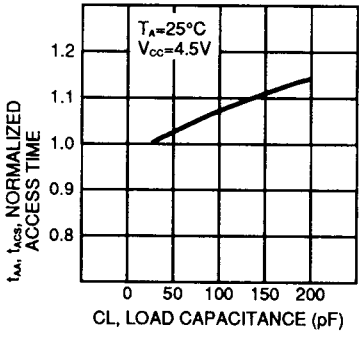


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE

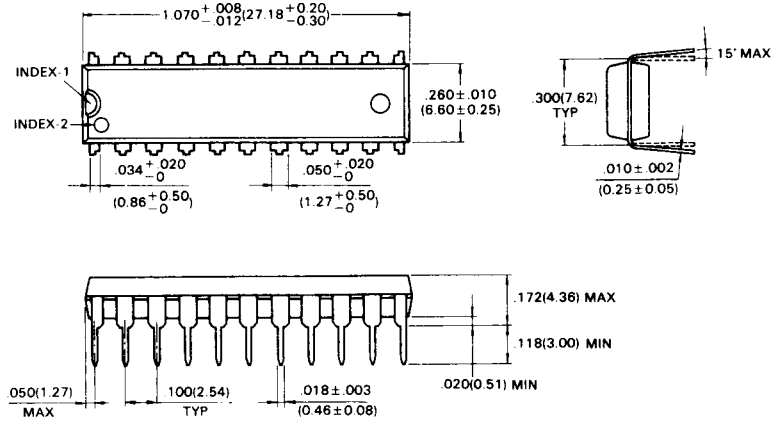


PACKAGE DIMENSIONS

(Suffix: –P)

22-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-22P-M04)

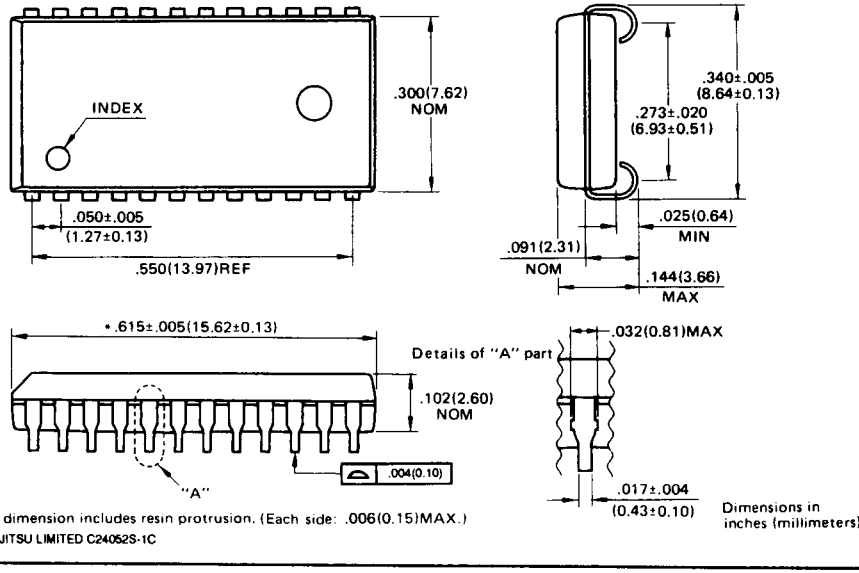


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: –PJ)

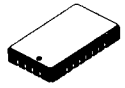
24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



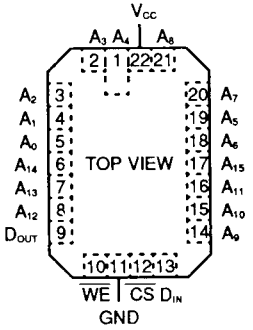
* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

PACKAGE DIMENSIONS

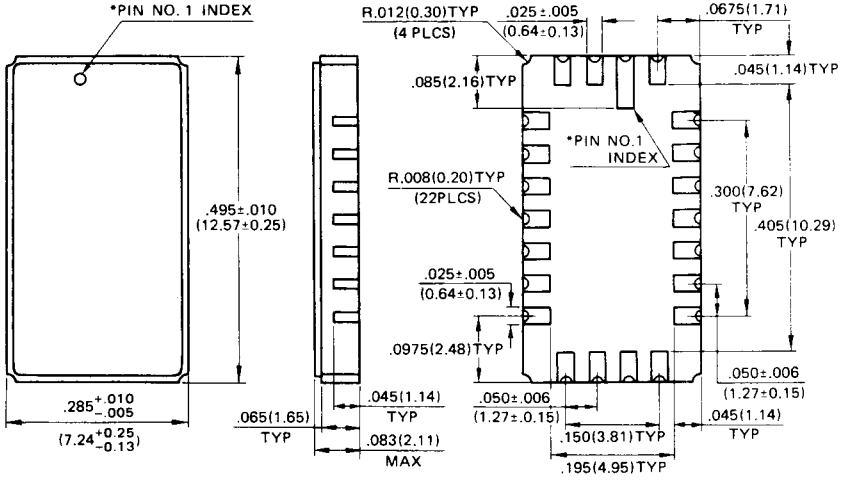
(Suffix: –CV)



CERAMIC PACKAGE
LCC-22C-A01



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)