FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10194-2E

MEMORY

CMOS

1 M × 16 BITS FAST PAGE MODE DYNAMIC RAM

MB81V18160A-60/60L/-70/70L

CMOS 1,048,576 × 16 BITS Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB81V18160A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB81V18160A features a “fast page” mode of operation whereby high-speed random access of up to 1,024 × 16 bits of data within the same row can be selected. The MB81V18160A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V18160A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V18160A is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V18160A are not critical and all inputs are LVTTL compatible.

■ PRODUCT LINE & FEATURES

Parameter			MB81V18160A			
			-60	-60L	-70	-70L
$\overline{\text{RAS}}$ Access Time			60 ns max.		70 ns max.	
Randam Cycle Time			110 ns min.		130 ns min.	
Address Access Time			30 ns max.		35 ns max.	
$\overline{\text{CAS}}$ Access Time			15 ns max.		17 ns max.	
Fast Page Mode Cycle Time			40 ns min.		45 ns min.	
Low Power Dissipation	Operating Current		648 mW max.		612 mW max.	
	Standby Current	LVTTL Level	3.6 mW max.	3.6 mW max.	3.6 mW max.	3.6 mW max.
		CMOS Level	1.8 mW max.	0.54 mW max.	1.8 mW max.	0.54 mW max.

- 1,048,576 words × 16 bits organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 1,024 refresh cycles every 16.4 ms
- Self refresh function
- Standard and low power versions
- Early write or $\overline{\text{OE}}$ controlled write capability
- $\overline{\text{RAS}}$-only, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

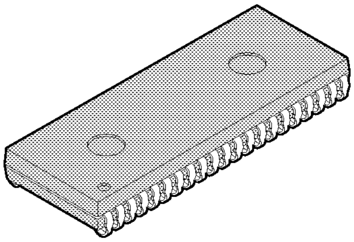
■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +4.6	V
Voltage of V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	±50	mA
Operating Temperature	T_{OPE}	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

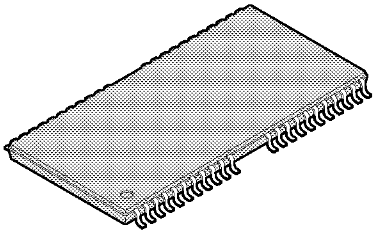
■ PACKAGE

Plastic SOJ Packaage



(LCC-42P-M01)

Plastic TSOP Package

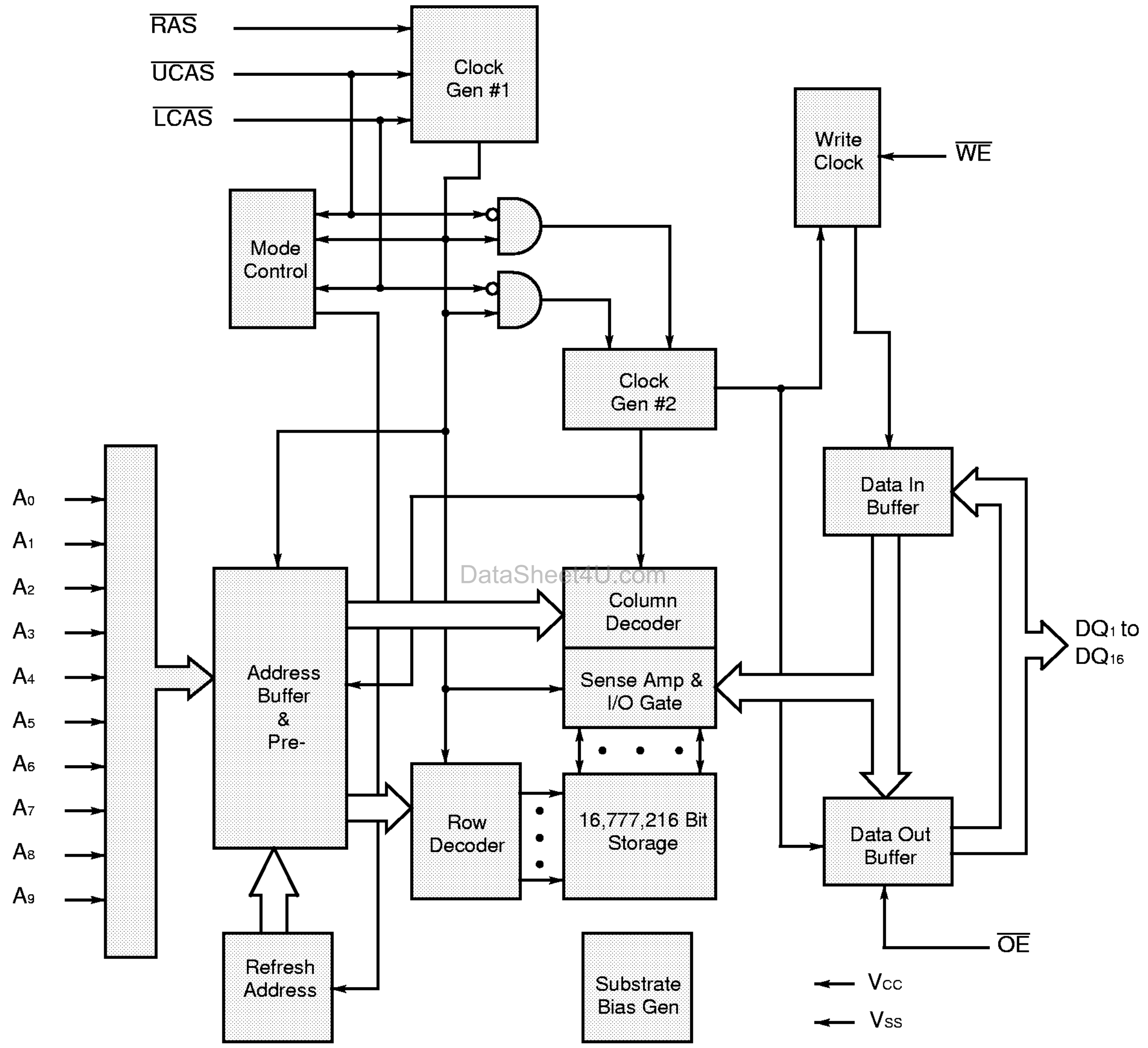


(FPT-50P-M06)
(Normal Bend)

Package and Ordering Information

- 42-pin plastic (400 mil) SOJ,order as MB81V18160A-××PJ
- 50-pin plastic (400 mil) TSOP-II with normal bend leads,order as MB81V18160A-××PFTN and MB81V18160A-××LPFTN (Low Power)

Fig. 1 – MB81V18160A DYNAMIC RAM - BLOCK DIAGRAM



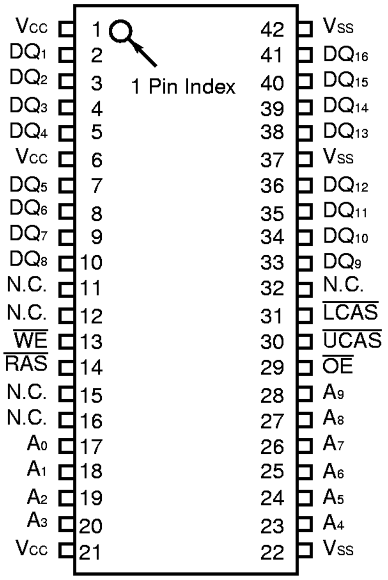
■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	5	pF
Input/Output Capacitance, DQ_1 to DQ_{16}	C_{DQ}	7	pF

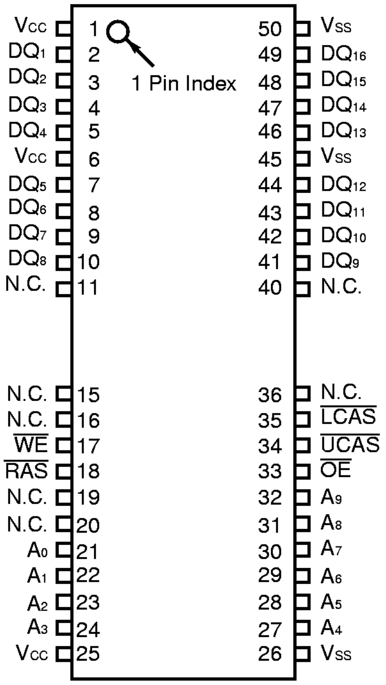
■ PIN ASSIGNMENTS AND DESCRIPTIONS

42-Pin SOJ
(TOP VIEW)
<LCC-42P-M01>



Designator	Function
A_0 to A_9	Address inputs row: A_0 to A_9 column: A_0 to A_9
$\overline{RAS}$	Row address strobe
$\overline{LCAS}$	Lower column address strobe
$\overline{UCAS}$	Upper column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_1 to DQ_{16}	Data Input/Output
V_{CC}	+3.3 volt power supply
V_{SS}	Circuit ground
N.C.	No connection

50-Pin TSOP
(TOP VIEW)
<Normal Bend: FPT-50P-M06>



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Spply Voltage	*1	V_{CC}	3.0	3.3	3.6	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	*1	V_{IH}	2.0	—	V_{CC} + 0.3 V	V	
Input Low Voltage, all inputs*	*1	V_{IL}	–0.3	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A_0 to A_9) are available, the column and row inputs are separately strobed by $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and $\overline{\text{RAS}}$ as shown in Figure 1. First, ten row address bits are input on pins A_0-through-A_9 and latched with the row address strobe ($\overline{\text{RAS}}$) then, ten column address bits are input and latched with the column address strobe ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$). Both row and column addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{\text{WE}}$. When $\overline{\text{WE}}$ is active Low, a write cycle is initiated; when $\overline{\text{WE}}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways-an early write cycle, an $\overline{\text{OE}}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{\text{WE}}$ or $\overline{\text{LCAS}}/\overline{\text{UCAS}}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ_1 to DQ_8 is strobed by $\overline{\text{LCAS}}$ and DQ_9 to DQ_{16} is strobed by $\overline{\text{UCAS}}$ and the setup/hold times are referenced to each $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ because $\overline{\text{WE}}$ goes Low before $\overline{\text{LCAS}}/\overline{\text{UCAS}}$. In a delayed write or a read-modify-write cycle, $\overline{\text{WE}}$ goes Low after $\overline{\text{LCAS}}/\overline{\text{UCAS}}$; thus, input data is strobed by $\overline{\text{WE}}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied.
t_{CAC} : from the falling edge of $\overline{\text{LCAS}}$ (for DQ_1 to DQ_8) $\overline{\text{UCAS}}$ (for DQ_9 to DQ_{16}) when t_{RCD} is greater than t_{RCD} (max).
t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).
t_{OEA} : from the falling edge of $\overline{\text{OE}}$ when $\overline{\text{OE}}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}, and t_{RCD} (max) is satisfied.

The data remains valid until either $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ or $\overline{\text{OE}}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{\text{RAS}}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024 × 16 bits can be accessed and, when multiple MB81V18160As are used, $\overline{\text{CAS}}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes		Symbol	Conditions	Value				Unit
					Min.	Typ.	Max.		
							Std power	Low power	
Output High Voltage	*1		V_{OH}	I_{OH} = –2.0 mA	2.4	—	—	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = +2.0 mA	—	—	0.4	0.4	
Input Leakage Current (Any Input)			$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}; 3.0 V ≤ V_{CC} ≤ 3.6 V; V_{SS} = 0 V; All other pins not under test = 0 V	–10	—	10	10	µA
Output Leakage Current			$I_{DO(L)}$	0 V ≤ V_{OUT} ≤ V_{CC}; Data out disabled	–10	—	10	10	
Operating Current (Average Power Supply Current)	*2	MB81V18160A -60/60L	I_{CC1}	$\overline{\text{RAS}}$ & $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ cycling; t_{RC} = min	—	—	180	180	mA
		MB81V18160A -70/70L					170	170	
Standby Current (Power Supply Current)	*2	LVTTL Level	I_{CC2}	$\overline{\text{RAS}}$ = $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ = V_{IH}	—	—	1.0	1.0	mA
		CMOS Level		$\overline{\text{RAS}}$ = $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ ≥ V_{CC} –0.2 V			500	150	µA
Refresh Current#1 (Average Power Supply Current)	*2	MB81V18160A -60/60L	I_{CC3}	$\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ = V_{IH}, $\overline{\text{RAS}}$ cycling; t_{RC} = min	—	—	180	180	mA
		MB81V18160A -70/70L					170	170	
Fast Page Mode Current	*2	MB81V18160A -60/60L	I_{CC4}	$\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ cycling; t_{PC} = min	—	—	100	100	mA
		MB81V18160A -70/70L					90	90	
Refresh Current#2 (Average Power Supply Current)	*2	MB81V18160A -60/60L	I_{CC5}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$; t_{RC} = min	—	—	170	170	mA
		MB81V18160A -70/70L					160	160	
Battery Back Up Current (Average Power Supply Current)	*2	MB81V18160A -60/-70	I_{CC6}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$; t_{RC} = 16 µs t_{RAS} = min to 300 ns V_{IH} ≥ V_{CC}–0.2 V, V_{IL} ≤ 0.2 V	—	—	2000	—	µA
		MB81V18160A -60L/70L		$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$; t_{RC} = 32 µs t_{RAS} = min to 300 ns V_{IH} ≥ V_{CC}–0.2 V, V_{IL} ≤ 0.2 V	—	—	—	300	
Refresh Current#3 (Average Power Supply Current)		MB81V18160A -60/60L	I_{CC9}	$\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$ = V_{IL} Self refresh;	—	—	1000	250	µA
		MB81V18160A -70/70L							

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V18160A-60/60L		MB81V18160A-70/70L		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std power	t_{REF}	—	16.4	—	16.4	ms
		Low power		—	128	—	128	
2	Random Read/Write Cycle Time		t_{RC}	110	—	130	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	174	—	ns
4	Access Time from $\overline{RAS}$	*6,9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*7,9	t_{CAC}	—	15	—	17	ns
6	Column Address Access Time	*8,9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	*10	t_{OFF}	—	15	—	17	ns
10	Transition Time		t_{T}	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	17	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*11,12	t_{RCD}	20	45	20	53	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	17	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	*19	t_{CPN}	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	ns
23	Column Address Hold Time from $\overline{RAS}$		t_{AR}	35	—	35	—	ns
24	$\overline{RAS}$ to Column Address Delay Time	*13	t_{RAD}	15	30	15	35	ns
25	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
26	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
27	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{RAS}$	*14	t_{RRH}	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{CAS}$	*14	t_{RCH}	0	—	0	—	ns
30	Write Command Set Up Time	*15,20	t_{WCS}	0	—	0	—	ns
31	Write Command Hold Time		t_{WCH}	15	—	15	—	ns
32	Write Hold Time from $\overline{RAS}$		t_{WCR}	35	—	35	—	ns
33	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	ns
34	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	17	—	ns
35	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	17	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB81V18160A-60/60L		MB81V18160A-70/70L		Unit
				Min.	Max.	Min.	Max.	
36	DIN Set Up Time		t_{DS}	0	—	0	—	ns
37	DIN Hold Time		t_{DH}	15	—	15	—	ns
38	Data Hold Time from $\overline{\text{RAS}}$		t_{DHR}	35	—	35	—	ns
39	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t_{RWD}	80	—	92	—	ns
40	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t_{CWD}	35	—	39	—	ns
41	Column Address to $\overline{\text{WE}}$ Delay Time	*20	t_{AWD}	50	—	57	—	ns
42	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)		t_{RPC}	5	—	5	—	ns
43	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh		t_{CSR}	0	—	0	—	ns
44	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh		t_{CHR}	10	—	12	—	ns
45	Access time from $\overline{\text{OE}}$	*9	t_{OEA}	—	15	—	17	ns
46	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	*10	t_{OEZ}	—	15	—	17	ns
47	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
48	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	*16	t_{OEH}	5	—	5	—	ns
49	$\overline{\text{OE}}$ to Data In Delay Time		t_{OED}	15	—	17	—	ns
50	$\overline{\text{CAS}}$ to Data In Delay Time		t_{CDD}	15	—	17	—	ns
51	DIN to $\overline{\text{CAS}}$ Delay Time	*17	t_{DZC}	0	—	0	—	ns
52	DIN to $\overline{\text{OE}}$ Delay Time	*17	t_{DZO}	0	—	0	—	ns
60	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width		t_{RASP}	—	100000	—	100000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	89	—	ns
63	Access Time from $\overline{\text{CAS}}$ Precharge	*9,18	t_{CPA}	—	35	—	40	ns
64	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time		t_{CP}	10	—	10	—	ns
65	Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t_{RHCP}	35	—	40	—	ns
66	Fast Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	*20	t_{CPWD}	55	—	62	—	ns

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
I_{CC1}, I_{CC3} I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$.
I_{CC2} is specified during $\overline{RAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
I_{CC6} is measured on condition that all address signals are fixed steady state.

*3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*4. AC characteristics assume $t_T = 5$ ns.

*5. Input voltage levels are 0 V and 3.0 V, and input reference levels are V_{IH} (min) and V_{IL} (max) for measuring timing of input signals. Also, the transition time (t_T) is measured between V_{IH} (min) and V_{IL} (max).
The output reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.

*6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig.2 and 3.

*7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*9. Measured with a load equivalent to one TTL load and 100 pF.

*10. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.

*11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. t_{RCD} (min) $= t_{RAH}$ (min) $+ 2t_T + t_{ASC}$ (min).

*13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*16. Assumes that $t_{WCS} < t_{WCS}$ (min).

*17. Either t_{DZC} or t_{DZO} must be satisfied.

*18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$ and $\overline{LCAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

*19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*20. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high-impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.

Fig. 2 – t_{RAC} vs. t_{RCD}

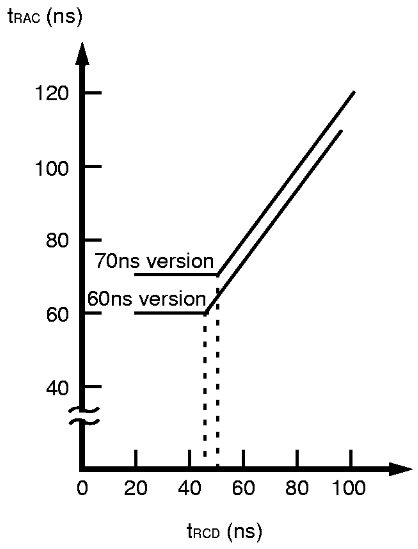


Fig. 3 – t_{RAC} vs. t_{RAD}

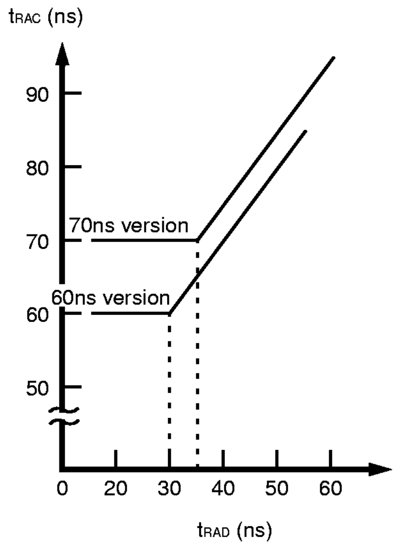
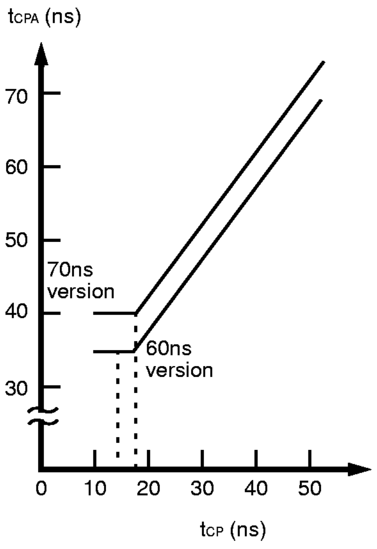


Fig. 4 – t_{CPA} vs. t_{CP}

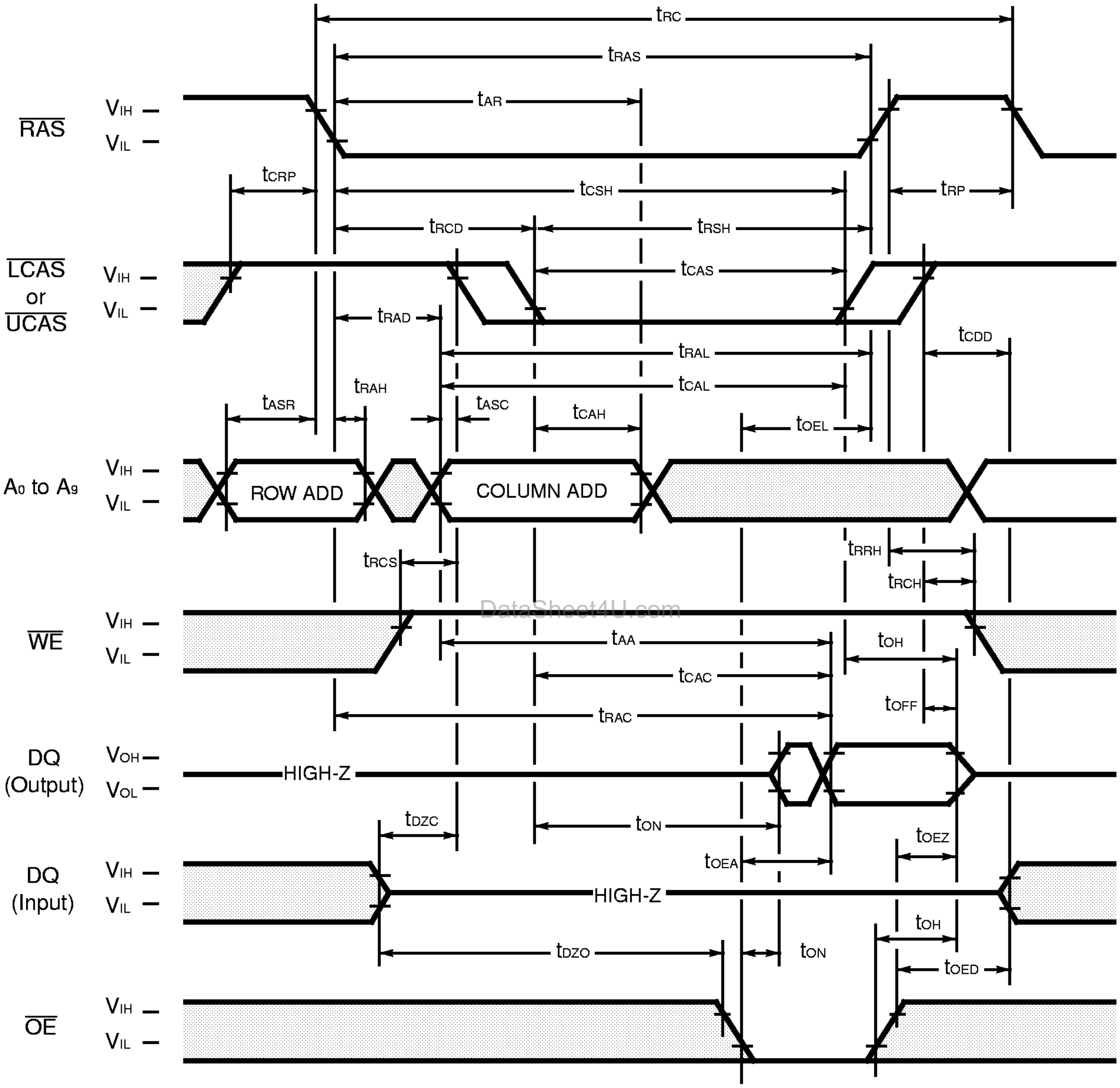


■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	DQ_1 to DQ_8		DQ_9 to DQ_{16}			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	H	X	X	Valid	—	—	High-Z	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	L	X	X	—	—	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L H L	H L L	H→L	L	—	—	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept

X: "H" or "L"
*: It is impossible in Fast Page Mode.

Fig. 5 – READ CYCLE



▨ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

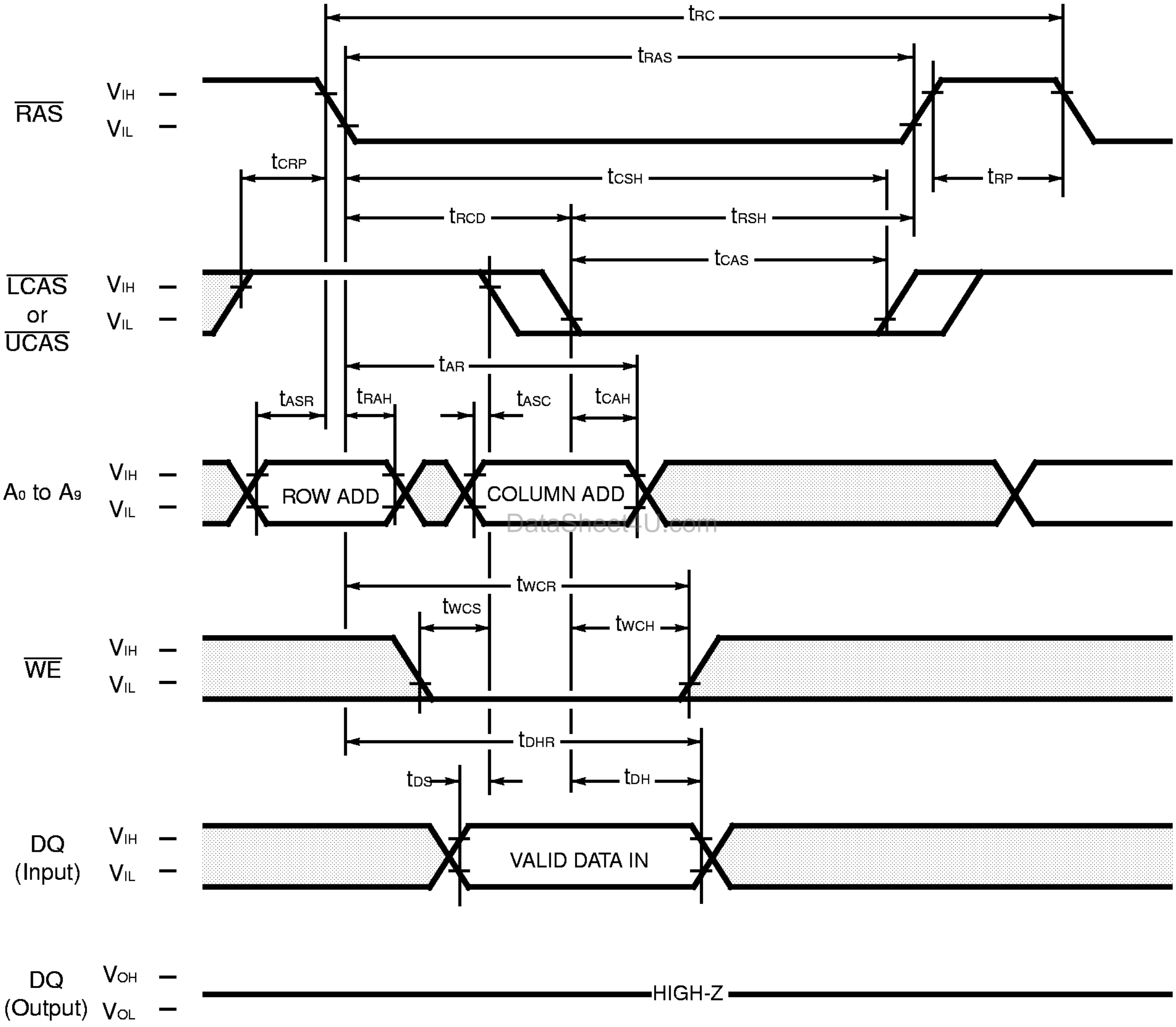
DESCRIPTION

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. $\overline{LCAS}$ controls the input/output data on DQ_1 to DQ_8 pins, $\overline{UCAS}$ controls one on DQ_8 to DQ_{16} pins. The access time is determined by $\overline{RAS}$(t_{RAC}), $\overline{LCAS}$/$\overline{UCAS}$(t_{CAC}), $\overline{OE}$(t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}$(max), access time = t_{CAC}.
If $t_{RAD} > t_{RAD}$(max), access time = t_{AA}.
If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}(whichever occurs later), access time = t_{OEA}.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = “H” or “L”)

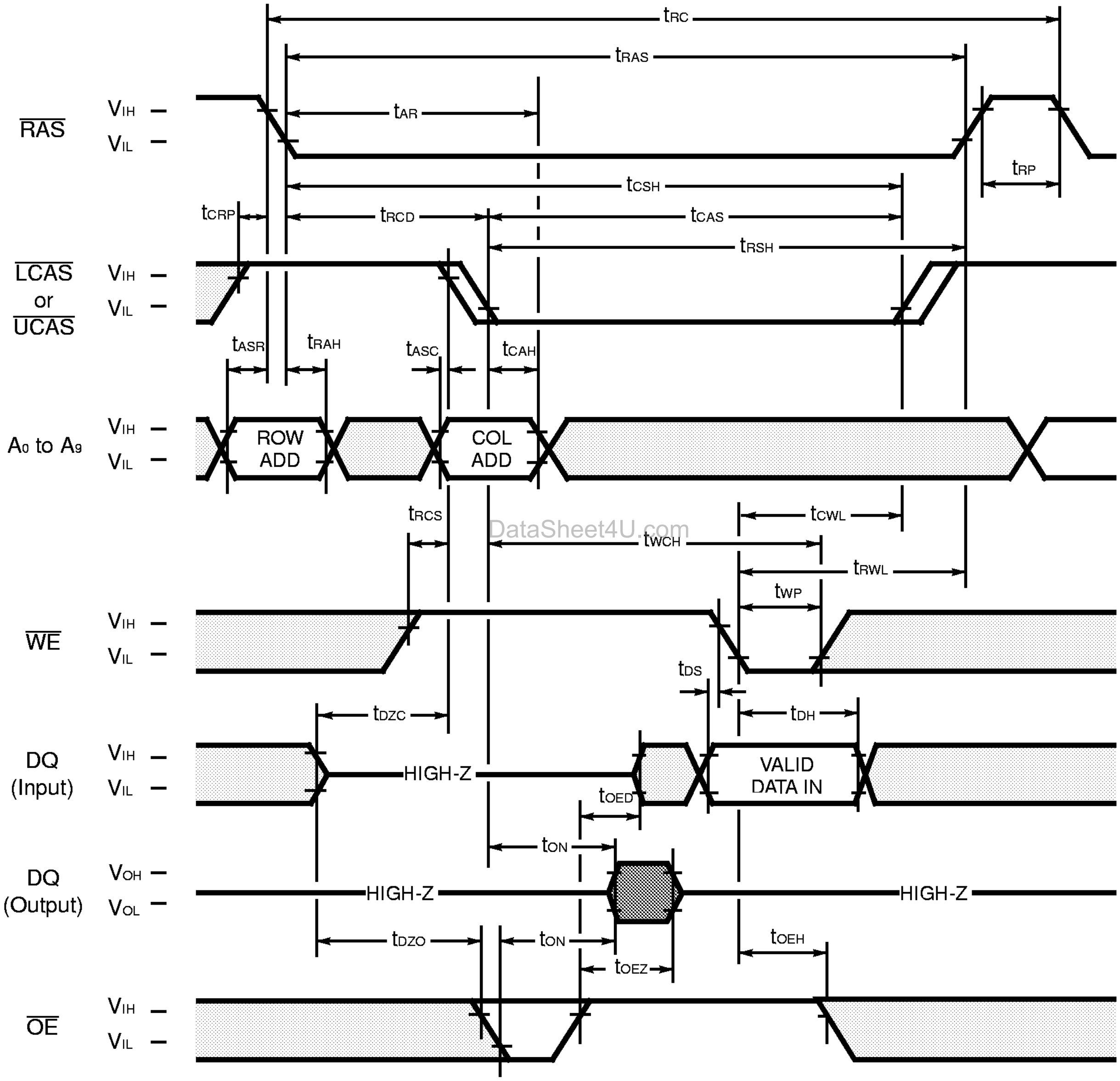


▨ “H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an “H” or “L” signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

Fig. 7 – DELAYED WRITE CYCLE



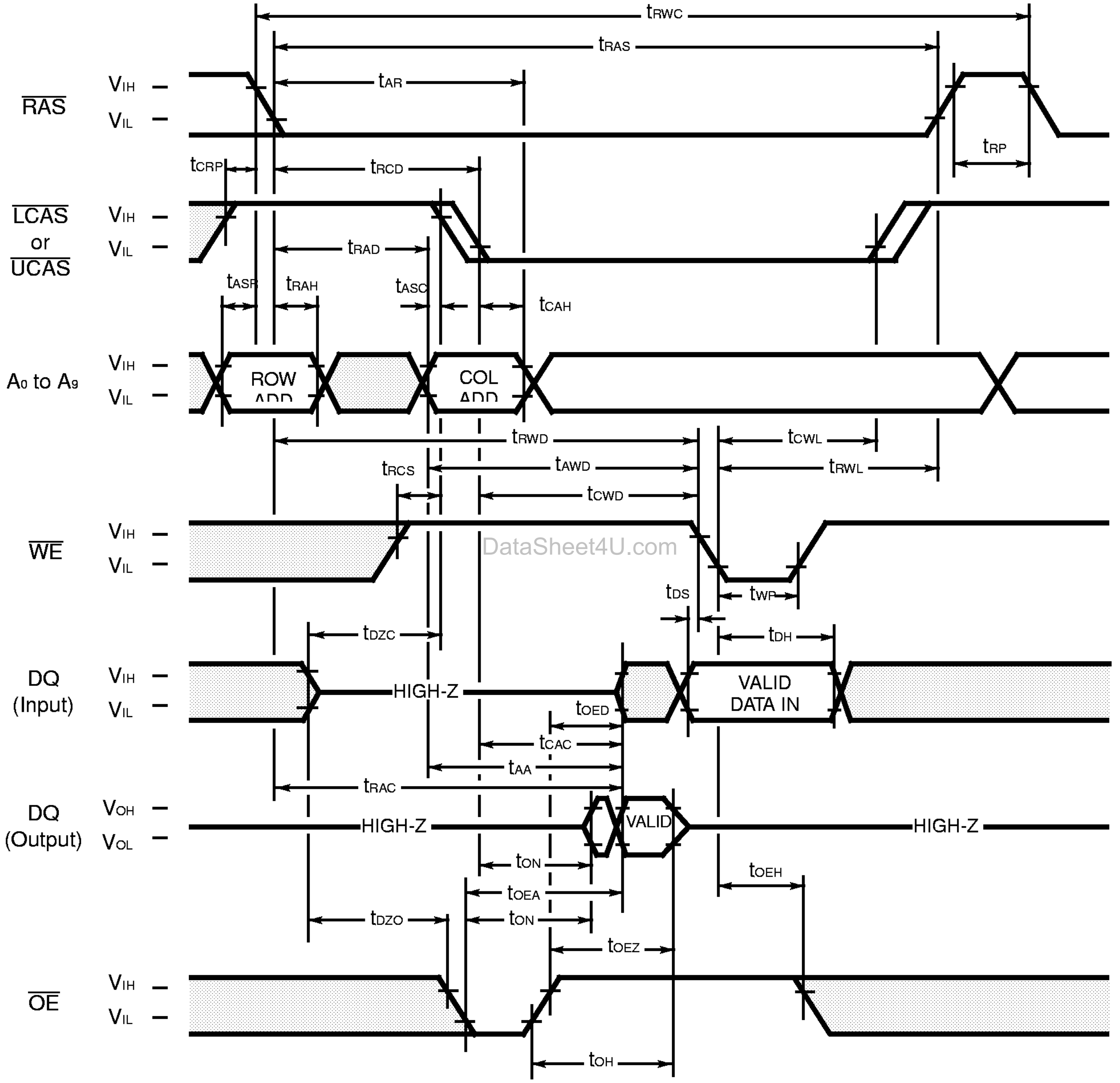
▨ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

▩ Invalid Data

DESCRIPTION

In the delayed write cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{\text{WE}}$ and written into memory. The Output Enable ($\overline{\text{OE}}$) signal must be changed from Low to High before $\overline{\text{WE}}$ goes Low ($t_{OED} + t_{T} + t_{DS}$).

Fig. 8 – READ-MODIFY-WRITE-CYCLE

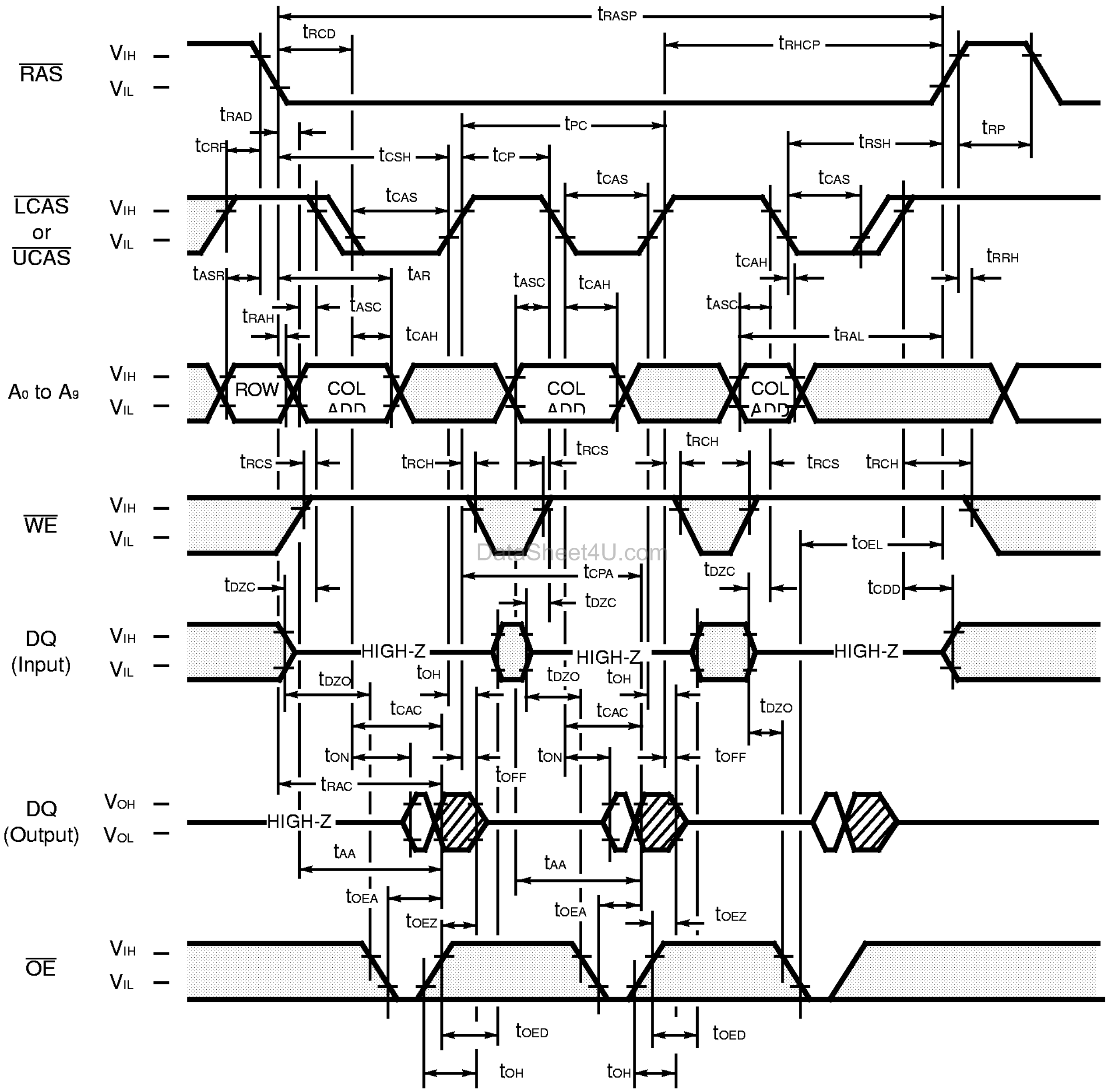


▨ “H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 9 – FAST PAGE MODE READ CYCLE



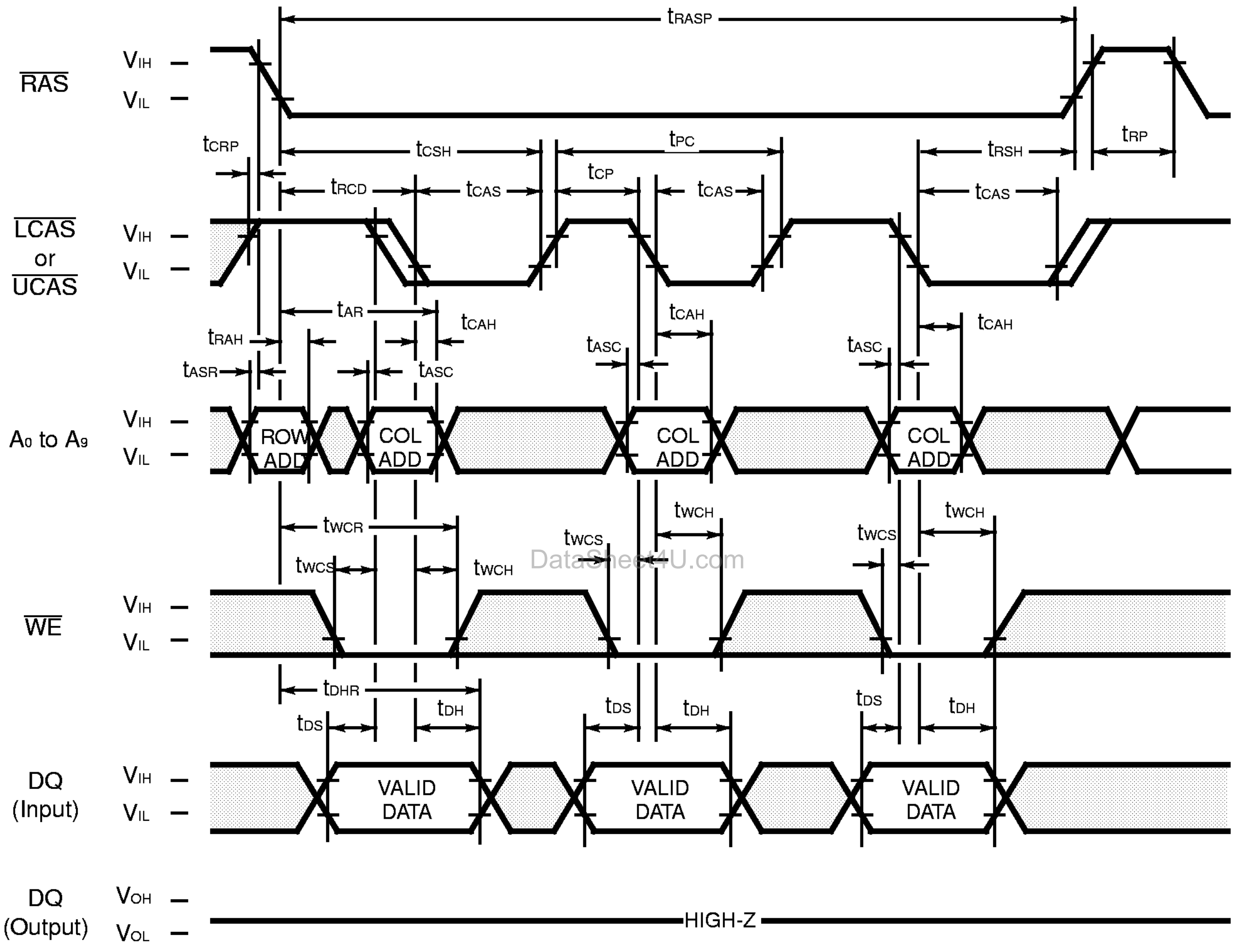
▒ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

▨ Valid Data

DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the lastest in occuring.

Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE ($\overline{OE}$ = “H” or “L”)

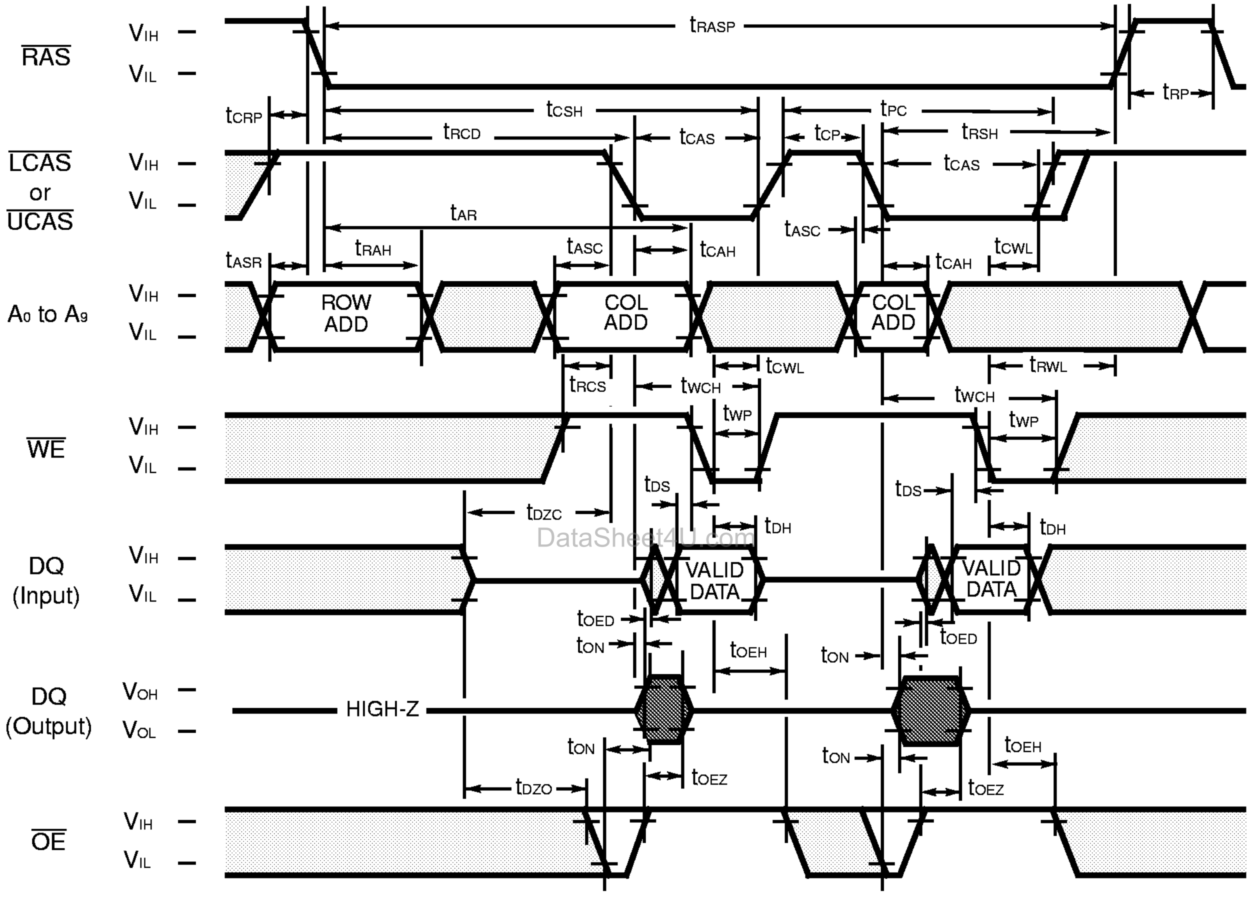


▨ “H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

DESCRIPTION

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ_1 to DQ_8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ_9 to DQ_{16} is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the fast page mode early write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

Fig. 11 – FAST PAGE MODE DELAYED WRITE CYCLE



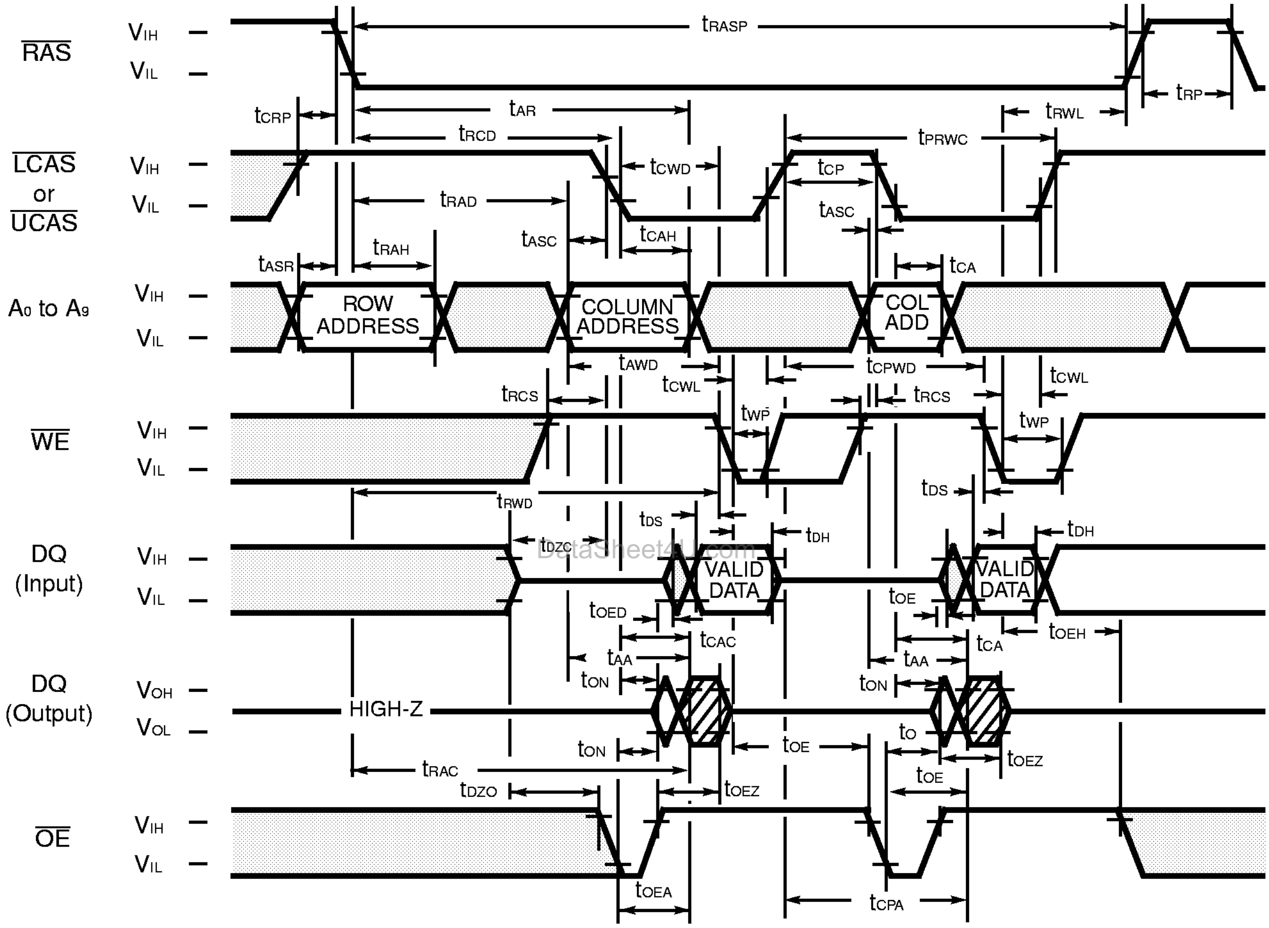
▨ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

■ Invalid Data

DESCRIPTION

The fast page mode delayed write cycle is executed in the same manner as the fast page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE



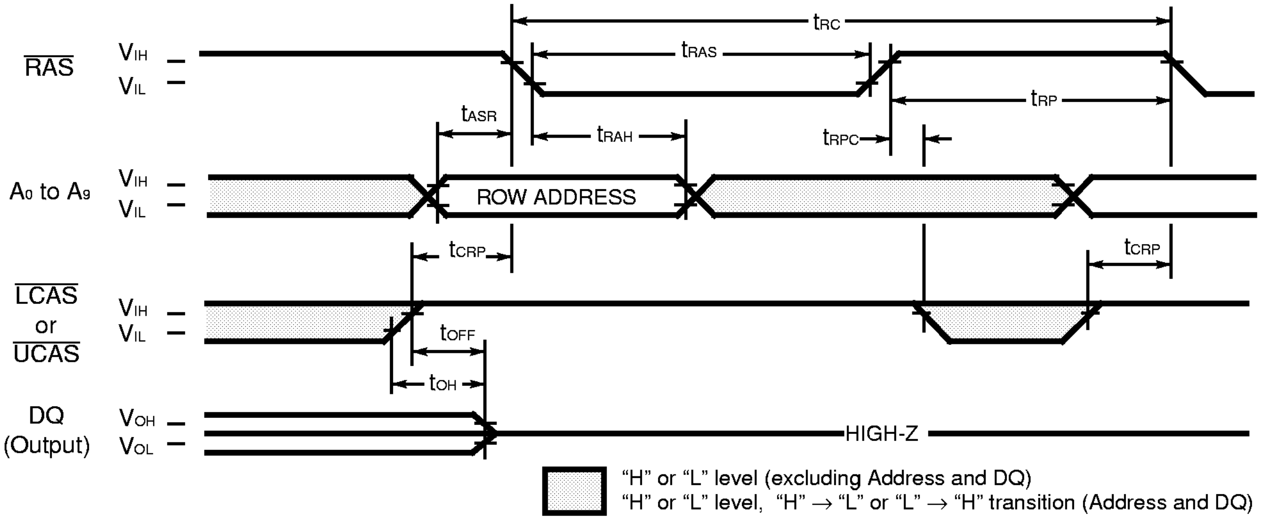
▨ “H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

▨ Valid Data

DESCRIPTION

During the fast page mode of operation, the read-modify-write cycle can be executed by switching WE from High to Low after input data appears at the DQ pins during a normal cycle.

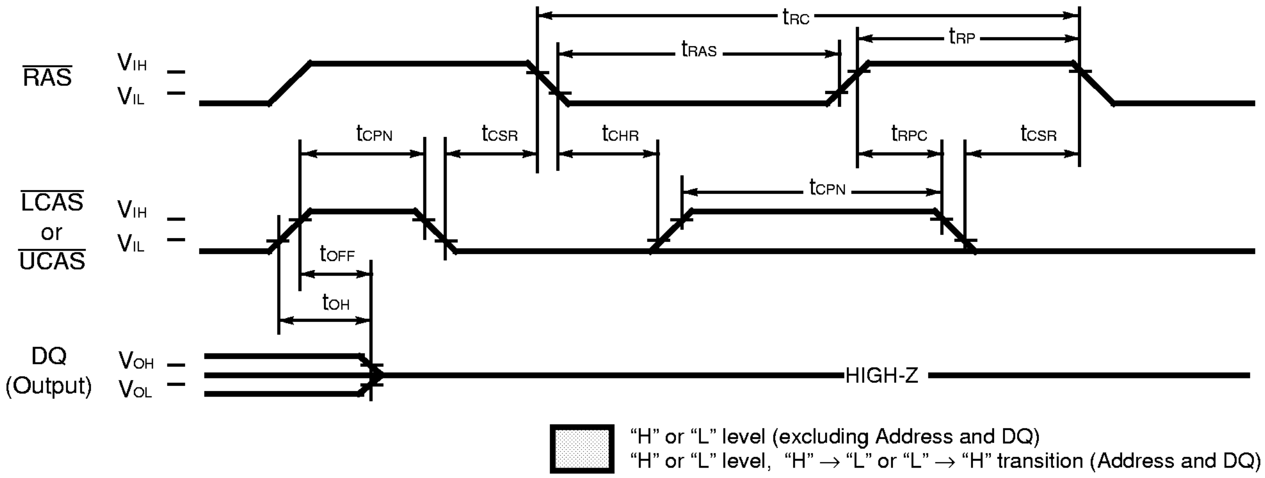
Fig. 13 – $\overline{\text{RAS}}$-ONLY REFRESH ($\overline{\text{WE}}$ = $\overline{\text{OE}}$ = “H” or “L”)



DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, and hidden refresh. $\overline{\text{RAS}}$-only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$-only refresh, DQ pins are kept in a high-impedance state.

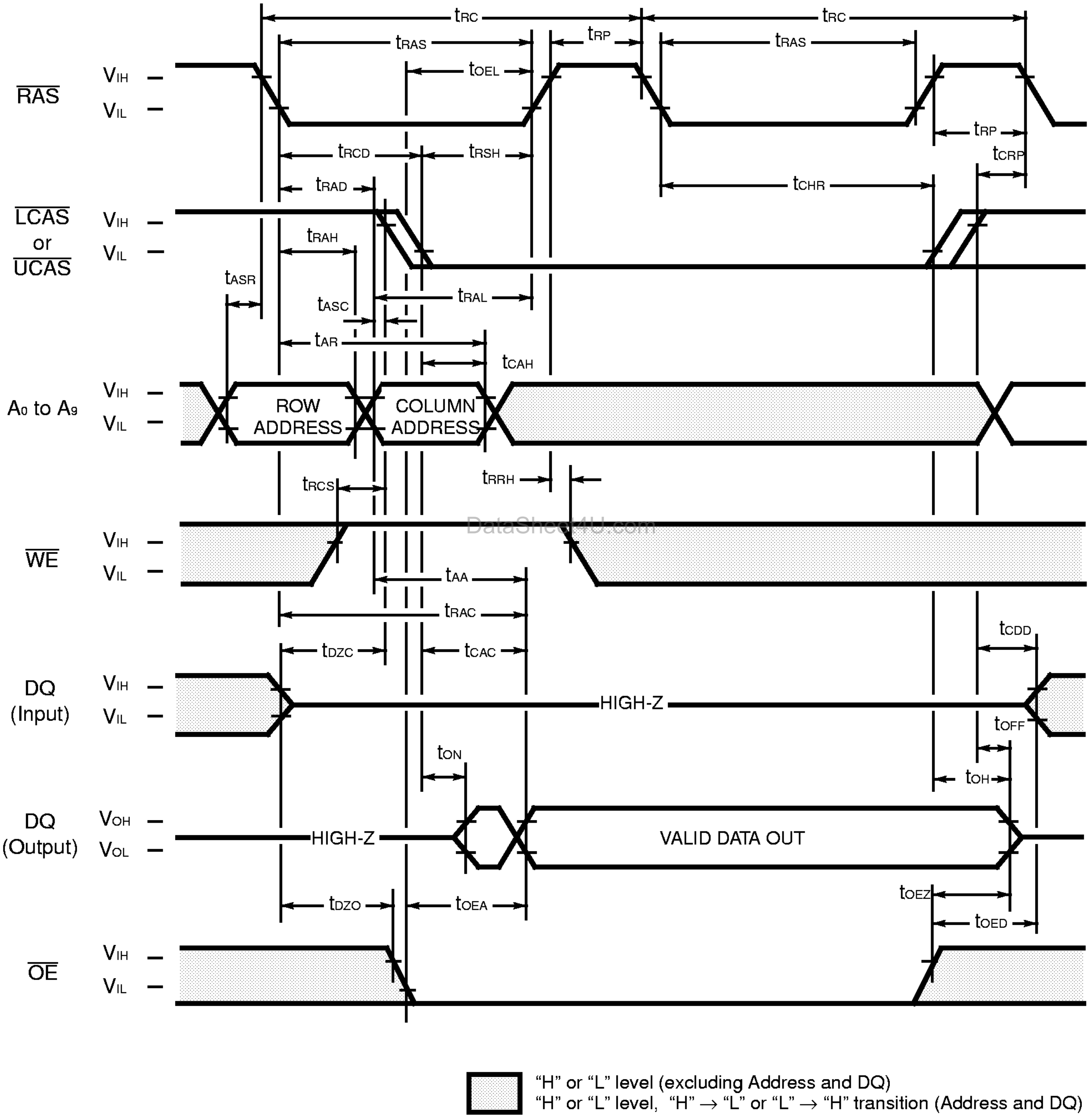
Fig. 14 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = “H” or “L”)



DESCRIPTION

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ is held Low for the specified setup time (tCSR) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

Fig. 15 – HIDDEN REFRESH CYCLE

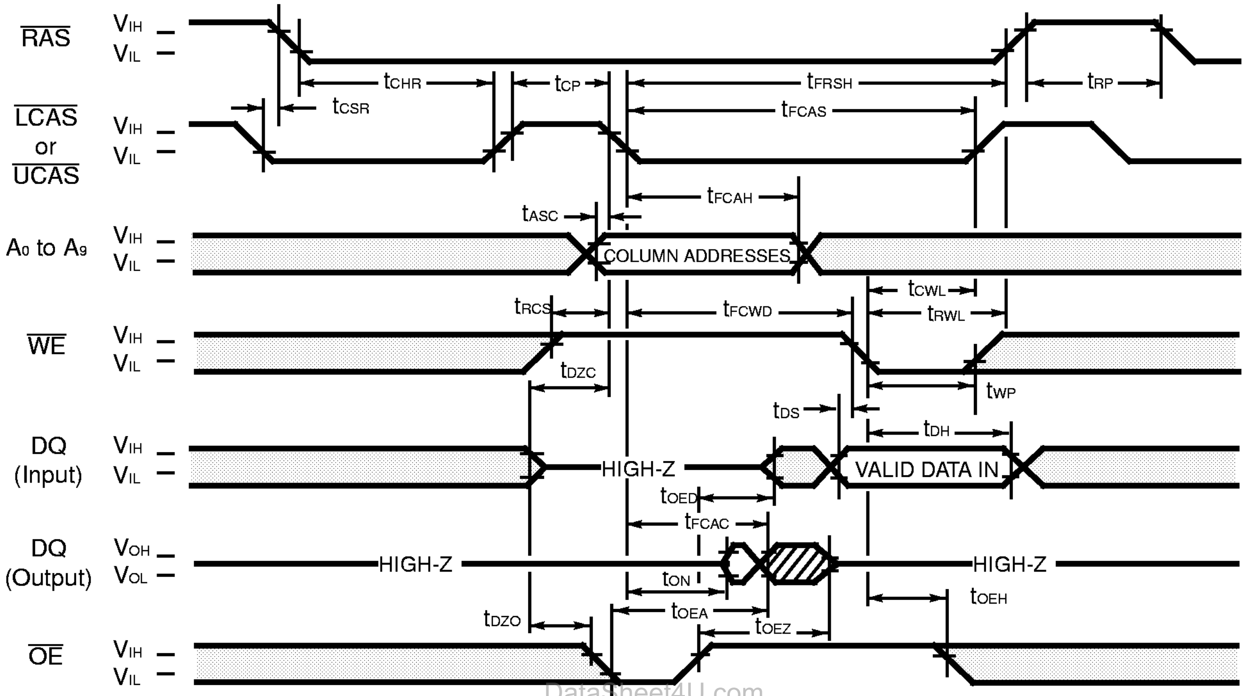


▨ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability..

Fig. 16 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



▨ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

▨ Valid Data

DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the function of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_9 are defined by the on-chip refresh counter
Column Addresses: Bits A_0 through A_9 are defined by latching levels on A_0 to A_9 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows;

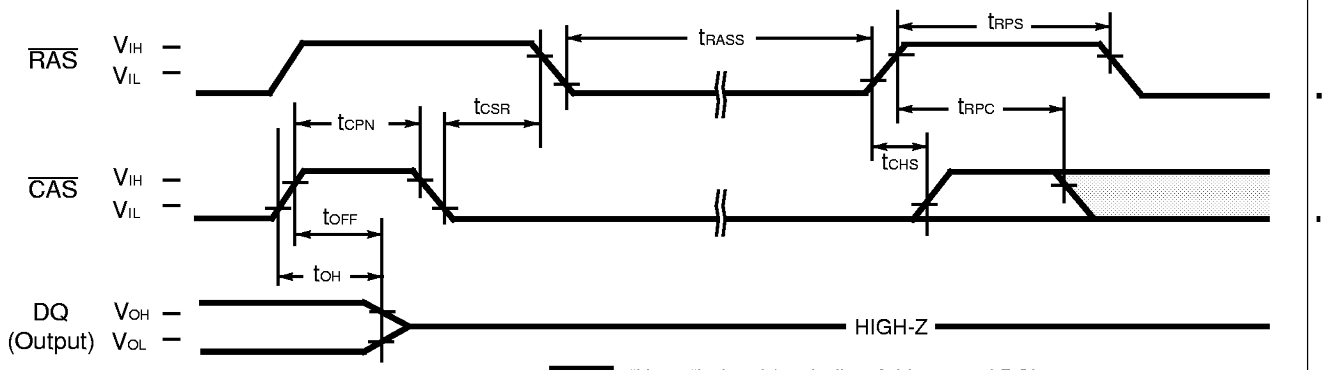
1) Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$-only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1,024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1,024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1,024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V18160A-60/60L		MB81V18160A-70/70L		Unit
			Min.	Max.	Min.	Max.	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	50	—	55	ns
91	Column Address Hold Time	t_{FCAH}	35	—	35	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	70	—	77	—	ns
93	$\overline{\text{CAS}}$ Pulse Width	t_{FCAS}	90	—	99	—	ns
94	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	90	—	99	—	ns

Note: Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle only.

Fig. 17 – SELF REFRESH CYCLE (A_0 to A_9 = $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = “H” or “L”)



▨ “H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V18160A-60/60L		MB81V18160A-70/70L		Unit
			Min.	Max.	Min.	Max.	
100	$\overline{\text{RAS}}$ Pulse Width	t_{RASS}	100	—	100	—	µs
101	$\overline{\text{RAS}}$ Precharge Time	t_{RPS}	110	—	125	—	ns
102	$\overline{\text{CAS}}$ Hold Time	t_{CHS}	–50	—	–50	—	ns

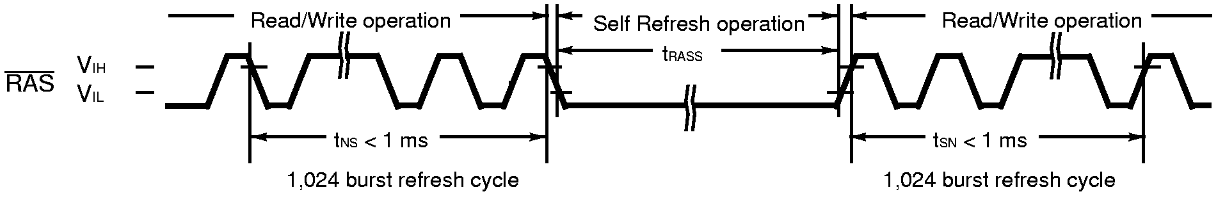
Note: Assumes Self Refresh cycle only.

DESCRIPTION

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self Refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator.
If $\overline{\text{CAS}}$ goes to “L” before $\overline{\text{RAS}}$ goes to “L” (CBR) and the condition of $\overline{\text{CAS}}$ “L” and $\overline{\text{RAS}}$ “L” is kept for term of t_{RASS} (more than 100 µs), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during $\overline{\text{RAS}}$=L” and ”$\overline{\text{CAS}}$=L”.
Exit from self refresh cycle is performed by toggling $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to “H” with specified t_{CHS} min. In this time, $\overline{\text{RAS}}$ must be kept “H” with specified t_{RPS} min.
Using self refresh mode, data can be retained without external $\overline{\text{CAS}}$ signal during system is in standby.

Restriction for Self Refresh operation ;
For Self Refresh operation, the notice below must be considered.

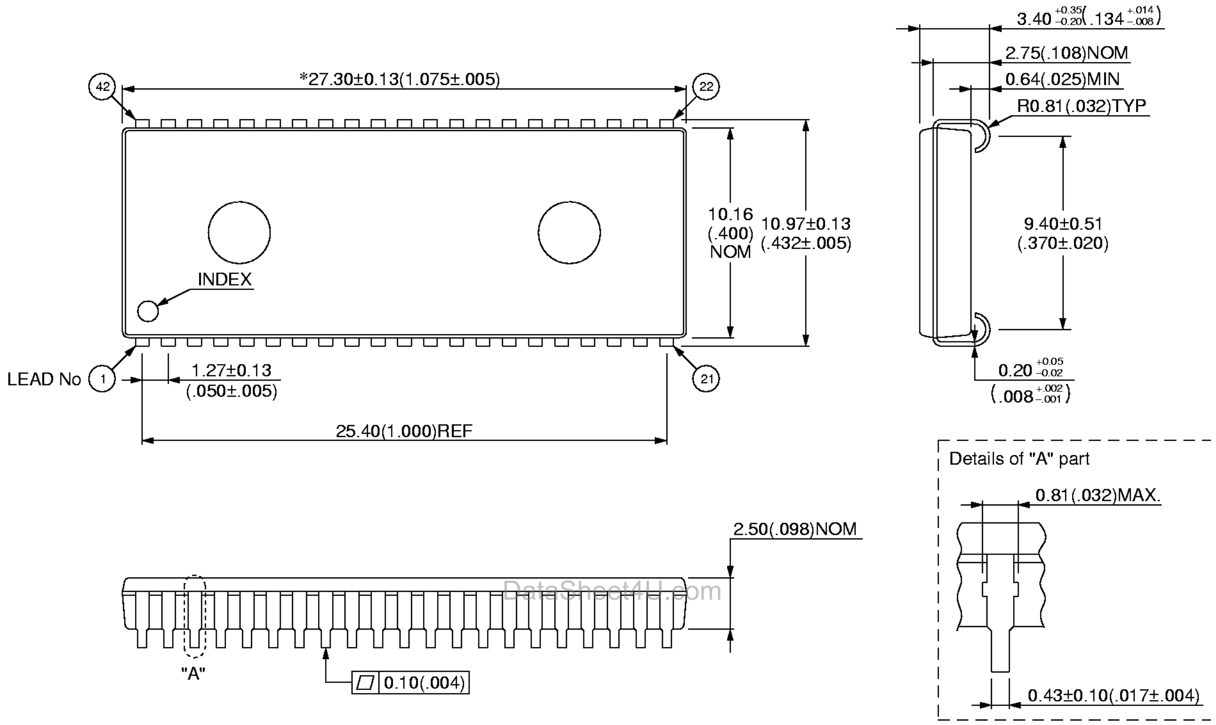
1) In the case that distributed CBR refresh are operated between read/write cycles
   Self Refresh cycles can be executed without special rule if 1,024 cycles of distributed CBR refresh are executed within t_{REF} max.
2) In the case that burst CBR refresh or distributed/burst $\overline{\text{RAS}}$-only refresh are operated between read/write cycles
   1,024 times of burst CBR refresh or 1,024 times of burst $\overline{\text{RAS}}$ only refresh must be executed before and after Self Refresh cycles.



* Read/write operation can be performed non refresh time within t_{NS} or t_{SN}.

■ PACKAGE DIMENSIONS

42-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-42P-M01)

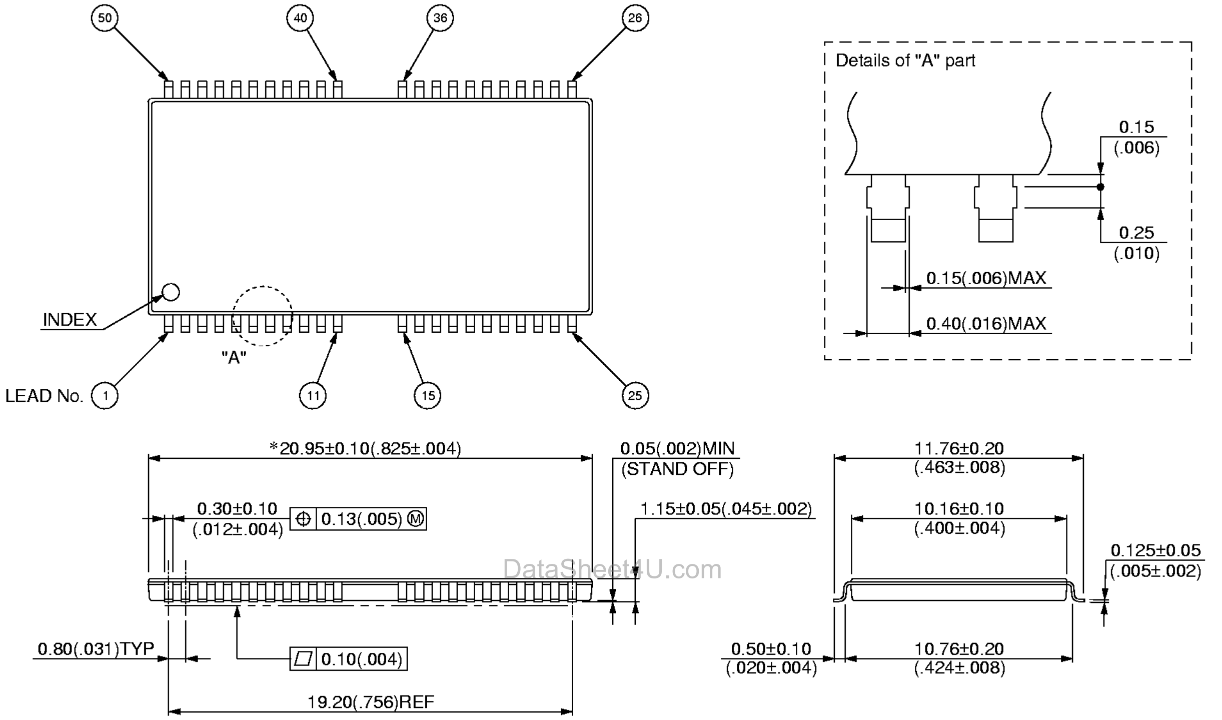


*: This dimension exclude resin protrusion. (Each side: 0.15 (.006) MAX.)

Dimensions in mm (inches)

■ PACKAGE DIMENSIONS

50-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-50P-M06)



*: This dimension exclude resin protrusion. (Each side: 0.15 (.006) MAX.)

Dimensions in mm (inches)