www.DataSheet4U.com

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB8299-25/-35
CMOS 288K-BIT HIGH-SPEED BiCMOS SRAM

32K Words x 9 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB8299 is a high-speed static random access memory organized as 32,768 words x 9 bits and fabricated with CMOS technology. To obtain a smaller chip size, the cells use NMOS transistors and resistors. The MB8299 is housed in 300 mil plastic DIP and SOJ packages, and a 450 mil SOP package. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

The MB8299 offers low power dissipation, low cost, and high performance.

- Organization: 32,768 words x 9 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB8299-25)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB8299-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  27.5 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8299-xxPSK
  SOJ (300 mil) MB8299-xxPJ
  SOP (450 mil) MB8299-xxPF

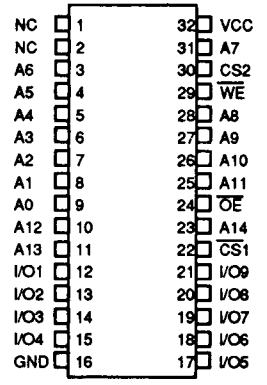
ADVANCE INFORMATION

Plastic Package
(DIP-32P-M02)

Plastic Package
(LCC-32P-M04)

Plastic Package
(FPT-32P-M02)

Pin Assignment
(TOP VIEW)



Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

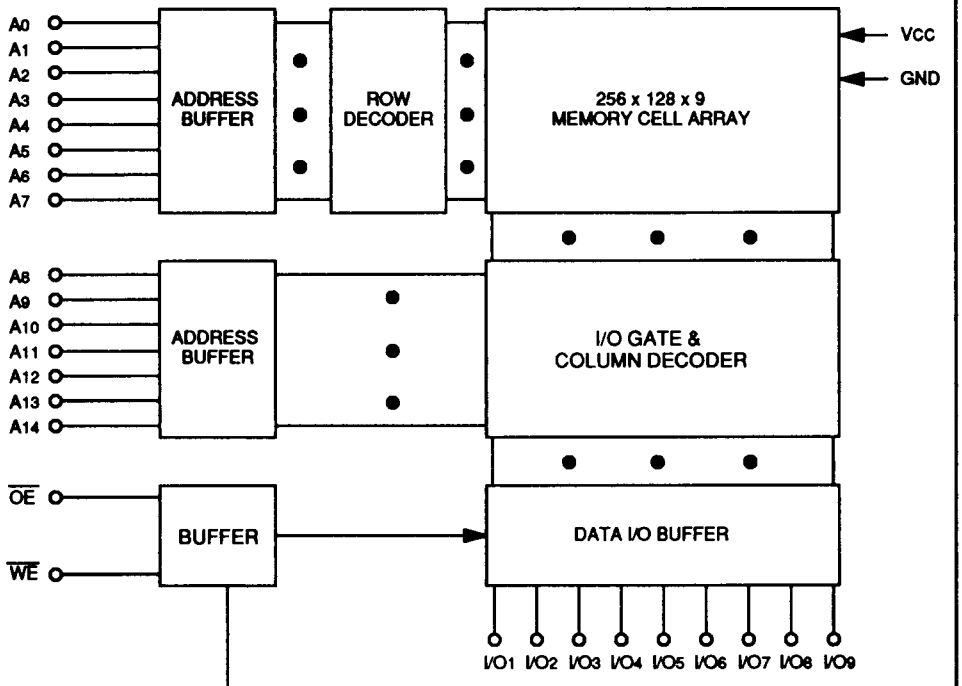
Copyright © 1990 by FUJITSU LIMITED and Fujitsu Microelectronics, Inc.

www.DataSheet4U.com

www.DataSheet4U.com

1

Fig. 1 – MB8299 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	STANDBY	ISB	HIGH-Z
L	L	X	X	DESELECT	ICC	HIGH-Z
L	H	H	H	DOUT DESABLE	ICC	HIGH-Z
L	H	H	L	READ	ICC	DOUT
L	H	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS1}$, CS2 $\overline{OE}$, $\overline{WE}$)	VIN = 0V	CI1			8	pF
Input Capacitance (Other Input)	VIN = 0V	CI2			7	pF
I/O Capacitance	VI/O = 0V	CI/O			8	pF

www.DataSheet4U.com

www.DataSheet4U.com

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

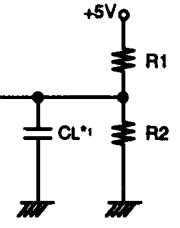
Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		ISB1	$\overline{CS1} \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		5	mA
		ISB2	$VIN \leq 0.2V$ $\overline{CS1} = VIH$		25	mA
Operating Supply Current	25ns	ICC	IOUT = 0mA, $\overline{CS1} = VIL$ Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		ILI	VIN = 0V to VCC, VCC = Max.	–5	5	µA
Output Leakage Current		ILI/O	$\overline{CS1} = VIH$ or $CS2 = VIL$ or $\overline{WE} = VIL$ or $\overline{OE} = VIH$, VI/O = 0V to VCC	–5	5	µA
Input Low Voltage		VIL		–2.0*1	0.8	V
Input High Voltage		VIH		2.2	6.0	V
Output High Voltage		VOH	IOH = –4mA	2.4		V
Output Low Voltage		VOL	IOL = 8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20% of cycle time. (VIL min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
  Output :VOL=0.8V, VOH=2.2V

- Output Load:



*1 Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480kΩ	255Ω	30pF	except tLZ1, tLZ2, tHZ1, tHZ2, tWZ, tOW, tOLZ and tOHZ
Load II	480kΩ	255Ω	5pF	tLZ1, tLZ2, tHZ1, tHZ2, tWZ, tOW, tOLZ and tOHZ

www.DataSheet4U.com

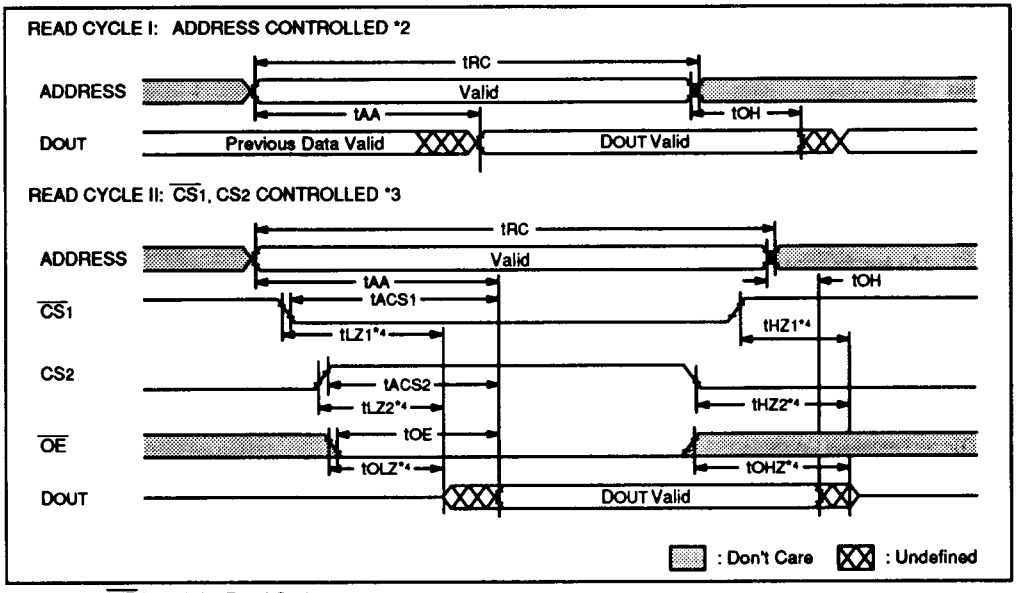
www.DataSheet4U.com

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8299-25		MB8299-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
$\overline{CS1}$ Access Time *3	tACS1		25		35	ns
CS2 Access Time *3	tACS2		14		15	ns
$\overline{OE}$ Access Time	tOE		12		14	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from $\overline{CS1}$ *4	tLZ1	5		8		ns
Output Low-Z from CS2 *4	tLZ2	2		3		ns
Output Low-Z from $\overline{OE}$ *4	tOLZ	2		3		ns
Output High-Z from $\overline{CS1}$ *4	tHZ1	1	15	1	15	ns
Output High-Z from CS2 *4	tHZ2	1	15	1	15	ns
Output High-Z from $\overline{OE}$ *4	tOHZ	1	15	1	15	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS1}$ = VIL, CS2 = VIH and $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS1}$ transition low, CS2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

www.DataSheet4U.com

www.DataSheet4U.com

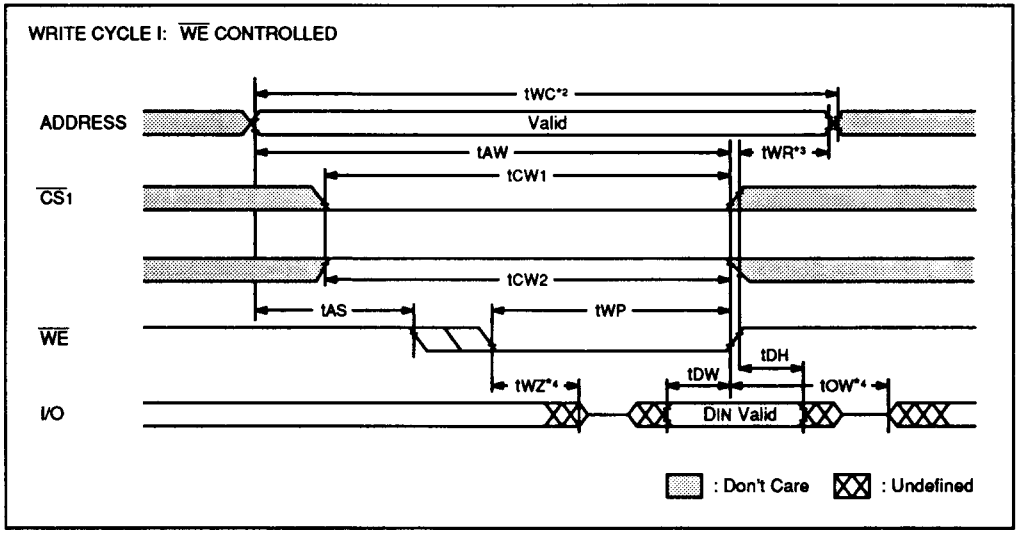
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1

Parameter	Symbol	MB8299-25		MB8299-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	tWC	25		35		ns
Address Valid to End of Write	tAW	18		28		ns
$\overline{CS1}$ to End of Write	tCW1	16		26		ns
CS2 to End of Write	tCW2	13		20		ns
Data Setup Time	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	15		20		ns
Write Recovery Time*3	tWR	0		0		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from $\overline{WE}$*4	tOW	0		0		ns
Output High-Z from $\overline{WE}$*4	tWZ	0	8	0	14	ns

WRITE CYCLE TIMING DIAGRAM *1



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

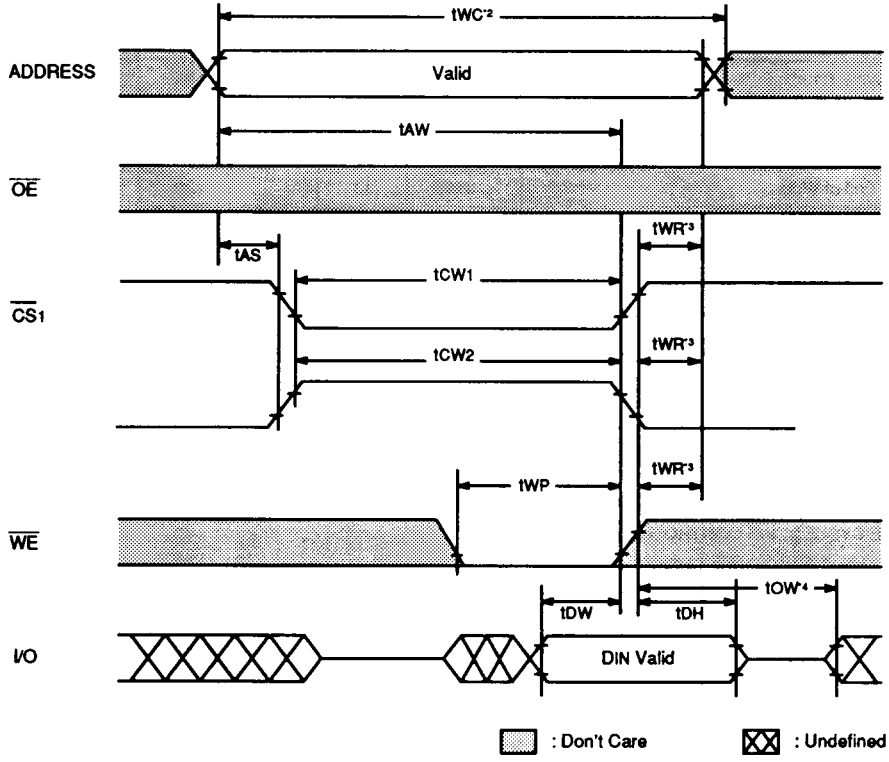
www.DataSheet4U.com

www.DataSheet4U.com

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE No. II: $\overline{CS}_1$, CS_2 CONTROLLED



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

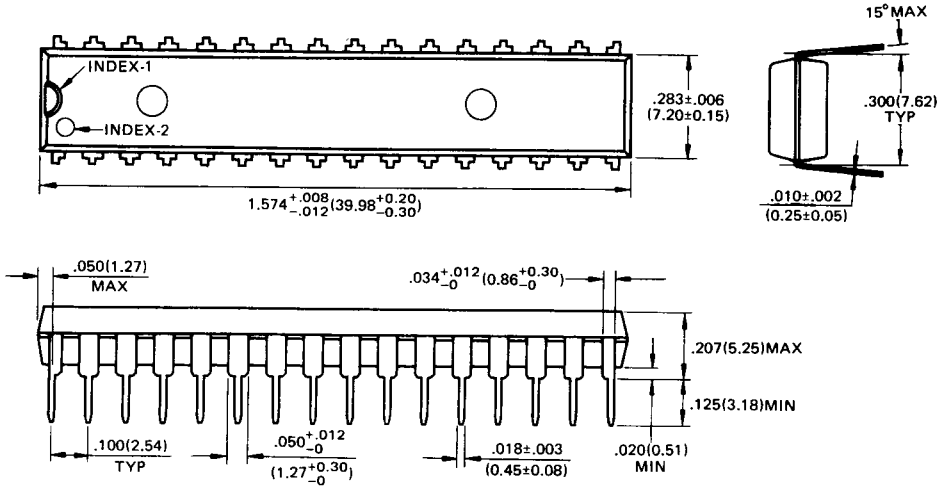
www.DataSheet4U.com

www.DataSheet4U.com

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in
inches (millimeters)

© 1988 FUJITSU LIMITED D32009S-1C

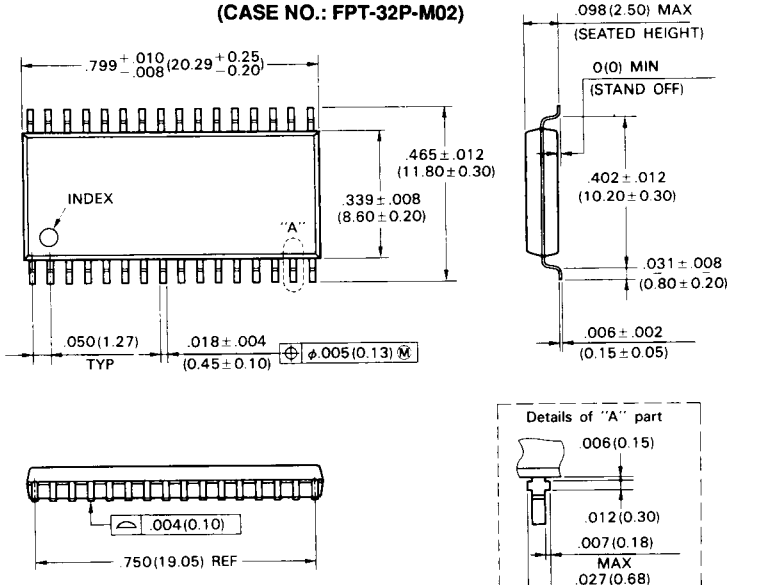
www.DataSheet4U.com

www.DataSheet4U.com

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PF)

32-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-32P-M02)



©1990 FUJITSU LIMITED F32004S-2C

Dimensions in
inches (millimeters)

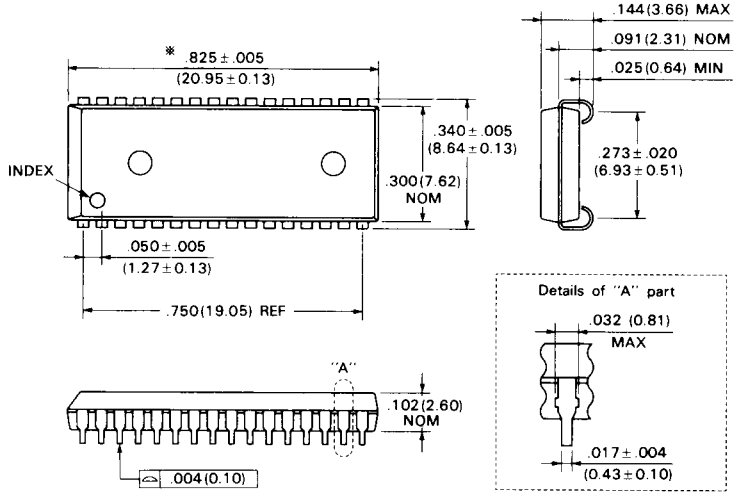
www.DataSheet4U.com

www.DataSheet4U.com

PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PJ)

32-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-32P-M04)



* : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

©1990 FUJITSU LIMITED C32024S-1C

Dimensions in
inches (millimeters)

1

www.DataSheet4U.com