FUJITSU

=== DATA SHEET ===

MB82B001-25/-35
1M-BIT HIGH-SPEED BiCMOS SRAM

1M Words x 1 Bit High-Speed BiCMOS Static Random Access Memory

The Fujitsu MB82B001 is a 1,048,576 words x 1 bit static random access memory fabricated with a BiCMOS process technology. For lower power dissipation and higher speed, peripheral circuits are fabricated with BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors.

The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.
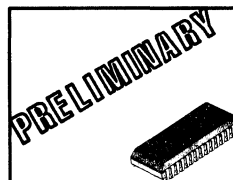
The MB82B001 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 1,048,576 words x 1 bit
- Static operation: no clock or refresh required
- Access time: 25 ns max. (MB82B001-25)
                       35 ns max. (MB82B001-35)
- Single +5 V power supply ±10% tolerance
                       120 mA max.   (Active operation)
                       5 mA max.   (Standby, CMOS level)
                       25 mA max.   (Standby, TTL level)
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- 28-pin Plastic Package:
         SOJ   (400 mil)   MB82B001-xxPJ
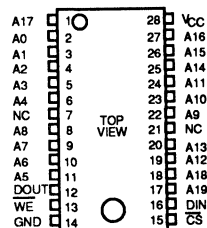
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	–3.5 to +7.0	V
Output Voltage on any pin with respect to GND	V_{OUT}	–0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

PLASTIC PACKAGE
LCC–28P–M05

PIN ASSIGNMENT

```
           TOP VIEW
A17  1 O        28  VCC
A0   2         27  A16
A1   3         26  A15
A2   4         25  A14
A3   5         24  A11
A4   6         23  A10
NC   7         22  A9
A8   8         21  NC
A7   9         20  A13
A6  10         19  A12
A5  11         18  A18
DOUT 12        17  A19
WE  13         16  DIN
GND 14         15  CS
```

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB82B001 BLOCK DIAGRAM

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	D_{OUT}	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE $(T_A = 25°C, f = 1 \text{ MHz})$

Parameter	Symbol	Typ	Max	Unit
Input Capacitance ($V_{IN} = 0$ V)	C_{IN}		6	pF
$\overline{CS}$ Capacitance ($V\overline{CS} = 0$ V)	$C\overline{CS}$		7	pF
Output Capacitance ($V_{OUT} = 0$ V)	C_{OUT}		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A9	Address Input	$\overline{WE}$	Write Enable
D_{IN}	Data Input	Vcc	Power Supply($\pm$10%)
$\overline{D_{OUT}}$	Data Output	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

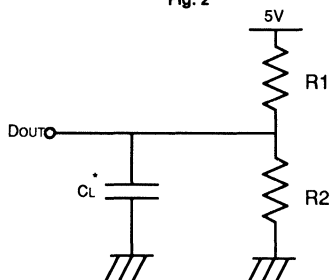| Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to Vcc Vcc = Max.	I_{LI}	−1		1	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to Vcc Vcc = Max.	I_{LO}	−1		1	μA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA Vcc = Max., V_{IN} = V_{IL} or V_{IH}	I_{CC1}		50	80	mA
	Vcc = Max., $\overline{CS}$ = V_{IL} Cycle = Min., I_{OUT} = 0mA	I_{CC2}		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ $\geq$ Vcc −0.2V V_{IN} $\geq$ Vcc − 0.2V or V_{IN} $\leq$ 0.2V	I_{SB1}		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}		10	25	
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = −4 mA	V_{OH}	2.4			V
Peak Power on Current [*1]	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or V_{IH} Min.	I_{PO}			50	mA
Input Low Voltage		V_{IL}	−0.5 [*2]		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V

*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 −3.0 V Min. for pulse width less than 20 ns.

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V

- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)

- Timing Reference Levels: Input: $V_{IL} = 0.8$, $V_{IH} = 2.2$ V
  Output: $V_{OL} = 0.8$, $V_{OH} = 2.2$ V

- Output Load: **Fig. 2**

*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	tRC	25		35		ns
Address Access Time *3	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	5		5		ns
Chip Selection to Output in Low-Z *5 *6	tLZ	5		5		ns
Chip Deselection to Output in High-Z *5 *6	tHZ	2	15	2	15	ns
Chip Selection to Power Up time	tPU	0		0		ns
Chip Deselection to Power Down	tPD		20		30	ns

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
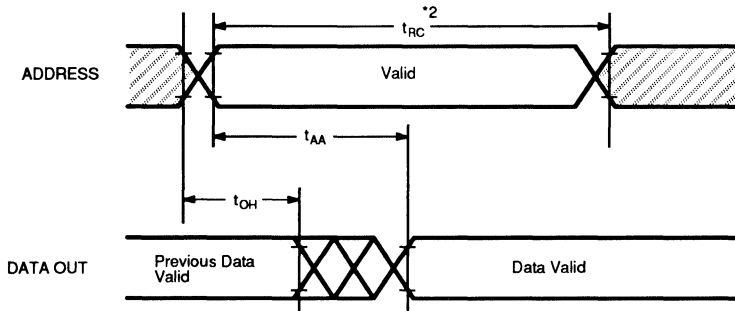*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
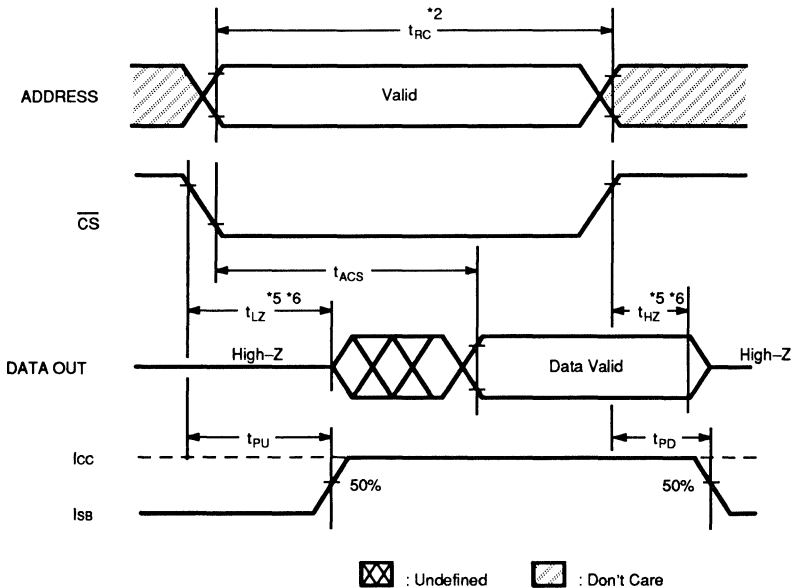*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3

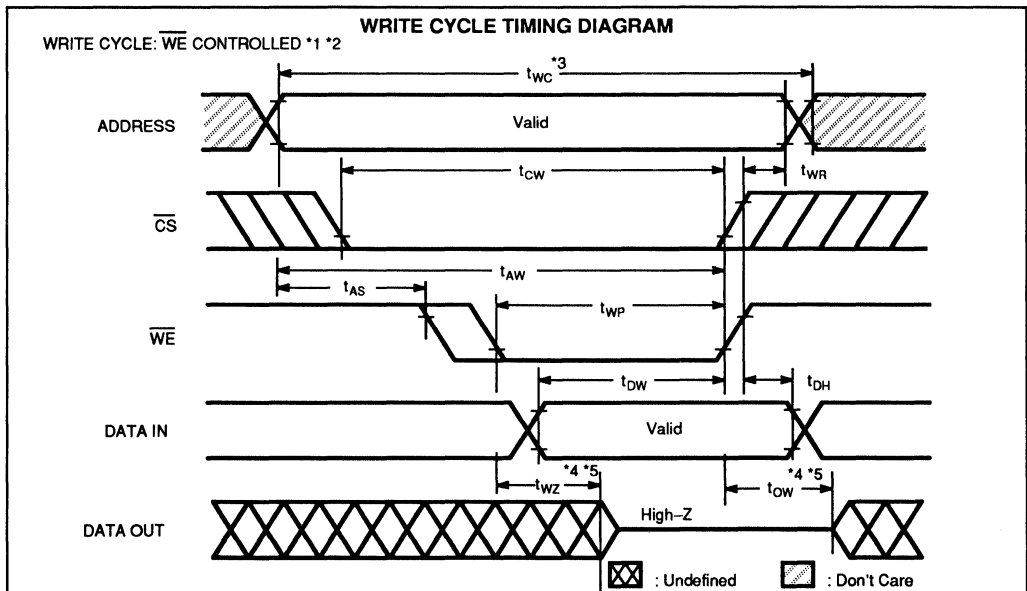READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4

XX : Undefined   ▨ : Don't Care

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

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AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	tWC	25		35		ns
Chip Selection to End of Write	tCW	16		26		ns
Address Valid to End of Write	tAW	18		28		ns
Address Setup Time	tAS	0		0		ns
Write Pulse Width	tWP	15		20		ns
Data Valid to End of Write	tDW	10		15		ns
Write Recovery Time	tWR	0		0		ns
Data Hold Time	tDH	0		0		ns
Write Enable to Output in High-Z *4 *5	tWZ	0	10	0	15	ns
Output Active from End of Write *4 *5	tOW	0		0		ns

2

WRITE CYCLE TIMING DIAGRAM
WRITE CYCLE: $\overline{\text{WE}}$ CONTROLLED *1 *2

*1 $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
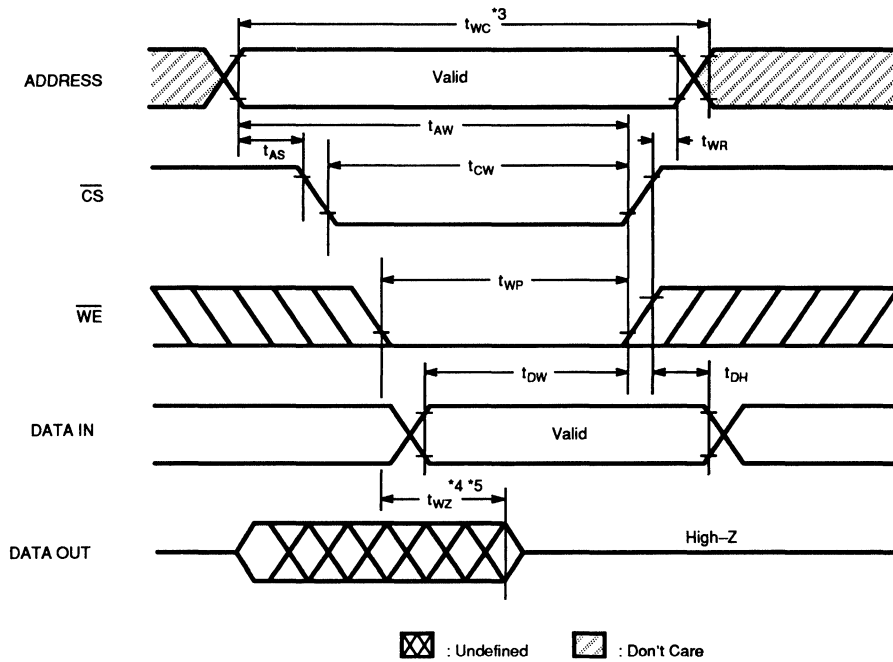*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

ADDRESS

$\overline{CS}$

$\overline{WE}$

DATA IN

DATA OUT

t_{WC} *3
Valid
t_{AW}
t_{AS}
t_{CW}
t_{WR}
t_{WP}
t_{DW}
t_{DH}
Valid
*4 *5
t_{WZ}
High–Z

⬛⬛ : Undefined   ▨ : Don't Care

*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
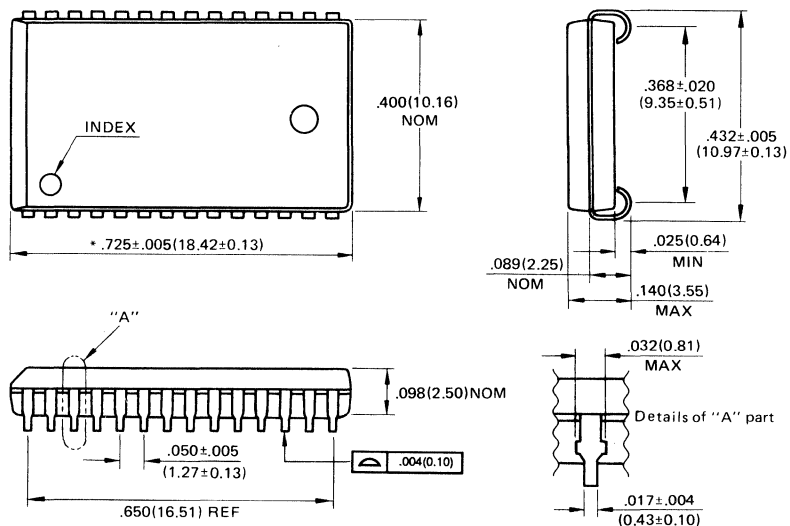*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

2

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)

INDEX

.400(10.16)
NOM

* .725±.005(18.42±0.13)

.368±.020
(9.35±0.51)

.432±.005
(10.97±0.13)

.089(2.25)
NOM

.025(0.64)
MIN

.140(3.55)
MAX

"A"

.098(2.50)NOM

.050±.005
(1.27±0.13)

.004(0.10)

.650(16.51) REF

.032(0.81)
MAX

Details of "A" part

.017±.004
(0.43±0.10)

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* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)