September 1990
Edition 2.0

FUJITSU

DATA SHEET

MB82B005-25/-35
1M-BIT HIGH-SPEED BiCMOS SRAM

256K Words x 4 Bits High-Speed BiCMOS Static Random Access Memory

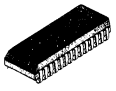
The Fujitsu MB82B005 is a 262,144 words x 4 bits static random access memory fabricated with a BiCMOS process technology. For lower power dissipation and higher speed, peripheral circuits use BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors.

The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required. The MB82B005 is housed in a 400 mil plastic small outline J-lead (SOJ) package.

The MB82B005 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

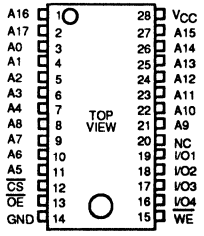
- Organization: 262,144 words x 4 bit
- Static operation: no clock or refresh required
- Access time: 25 ns max. (MB82B005-25)
  35 ns max. (MB82B005-35)
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. (Standby, CMOS level)
  25 mA max. (Standby, TTL level)
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- 28-pin Plastic Package:
  SOJ (400 mil) MB82B005-xxPJ

PRELIMINARY



PLASTIC PACKAGE
LCC–28P–M05

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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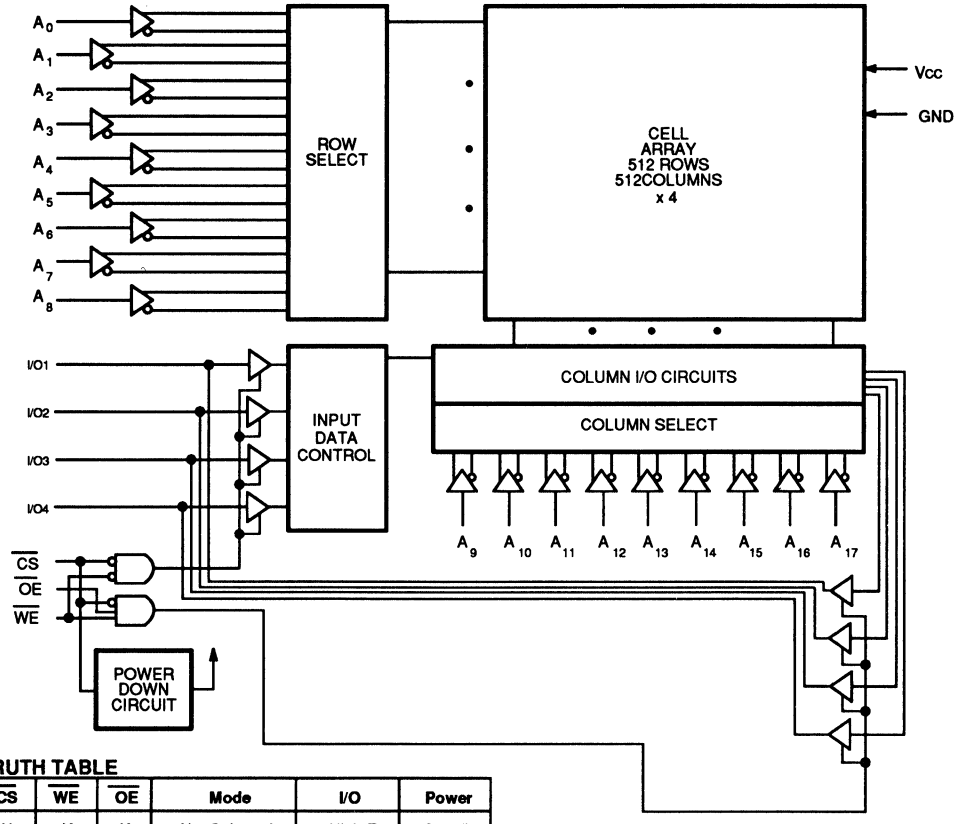
Fig. 1 – MB82B005 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Desable	High-Z	Active
L	L	X	Writte	DIN	Active
L	H	L	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O4	Data Input/Output	Vcc	Power Supply(±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to Vcc Vcc = Max.	ILI	–1		1	µA
Output Leakage Current	$\overline{CS}$ = VIH, or $\overline{OE}$=VIH VOUT = 0V to Vcc Vcc = Max.	ILO	–1		1	µA
Active Supply Current	$\overline{CS}$ = VIL, IOUT = 0mA Vcc = Max., VIN = VIL or VIH	ICC1		50	80	mA
	Vcc = Max., $\overline{CS}$ = VIL Cycle = Min., IOUT = 0mA	ICC2		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ ≥ Vcc –0.2V VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V	ISB1		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = VIH	ISB2		10	25	
Output Low Voltage	IOL = 8 mA	VOL			0.4	V
Output High Voltage	IOH = –4 mA	VOH	2.4			V
Peak Power on Current *1	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or VIH Min.	IPO			50	mA
Input Low Voltage		VIL	–0.5 *2		0.8	V
Input High Voltage		VIH	2.2		6.0	V

*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

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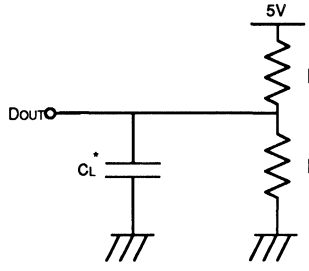
AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ

*Including Scope and Jig capacitance

AC CHARACTERISTICS

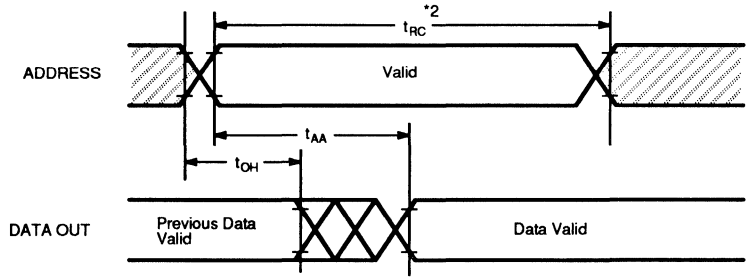
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	t_{RC}	25		35		ns
Address Access Time *3	t_{AA}		25		35	ns
Chip Select Access Time *4	t_{ACS}		25		35	ns
Output Enable Access Time	t_{OE}		10		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *5 *6	t_{CLZ}	5		5		ns
Chip Selection to Output in High-Z *5 *6	t_{CHZ}	2	15	2	15	ns
Output Enable to Output in Low-Z *5 *6	t_{OLZ}	0		0		ns
Output Enable to Output in High-Z *5 *6	t_{OHZ}	0	15	0	15	ns
Chip Selection to Power Up time	t_{PU}	0		0		ns
Chip Deselection to Power Down	t_{PD}		20		30	ns

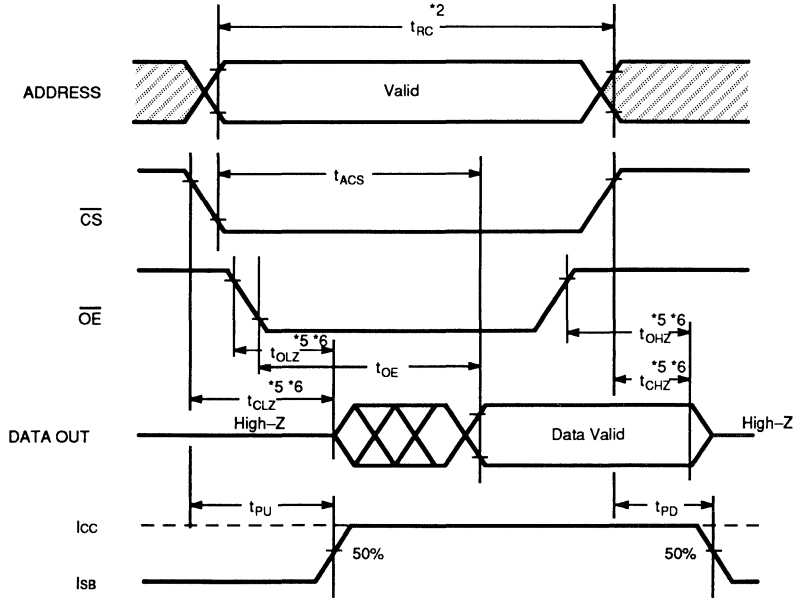
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL} $\overline{OE}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



: Undefined : Don't Care

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL, $\overline{OE}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

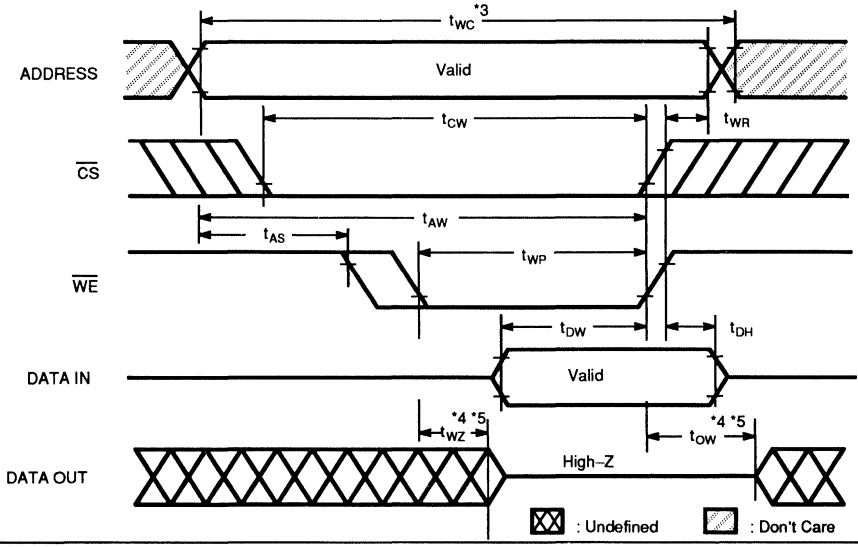
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	8		12		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	8	0	14	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

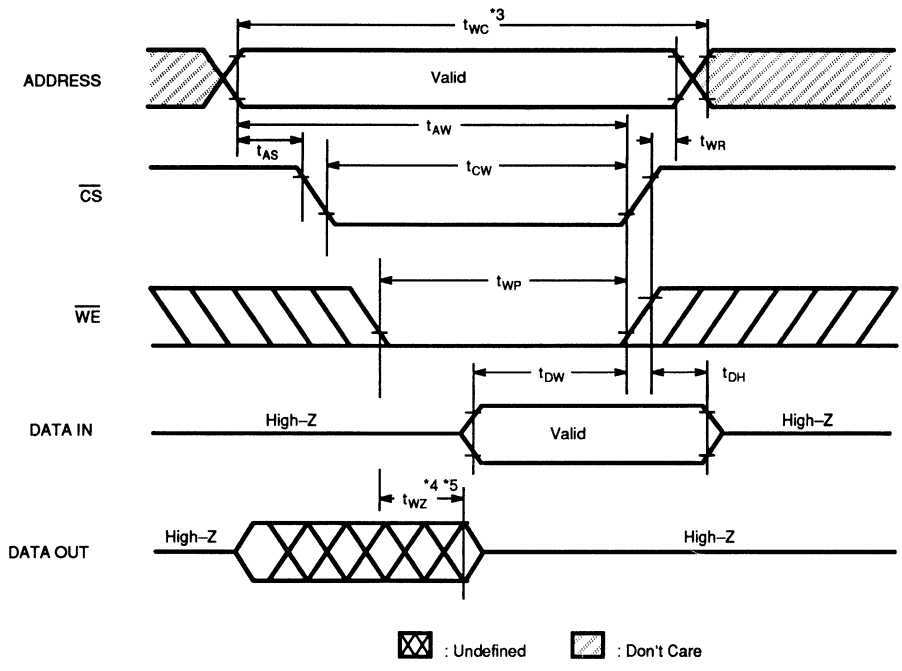
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

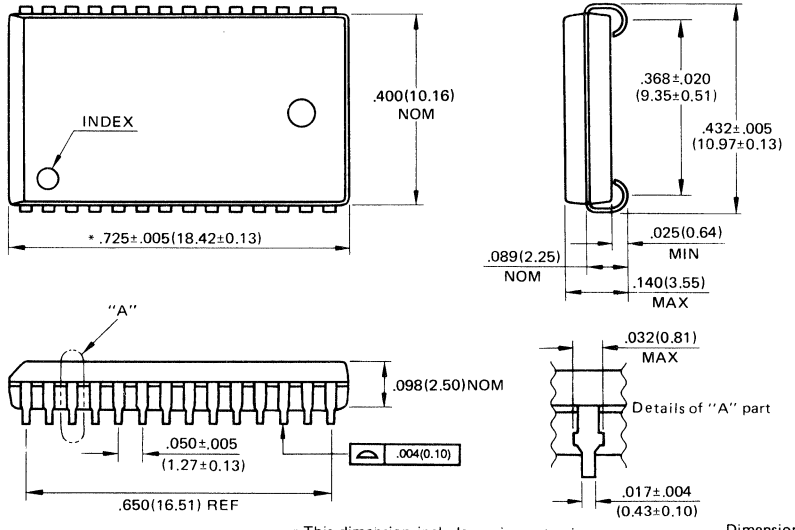
WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)



* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)