

# MB82B78-15/-20

## 64K-BIT HIGH-SPEED BiCMOS SRAM

### 8K Words x 8 Bits High-Speed Static Random Access Memory

The Fujitsu MB82B78 is a static random access memory organized as 8,192 words x 8 bits and fabricated with CMOS silicon gate process. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B78 is housed in 300 mil plastic DIP and SOJ packages, and a 450 mil plastic SOP package. The memory uses asynchronous circuitry and requires +5 V power supply. All pins are TTL compatible.

The MB82B78 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

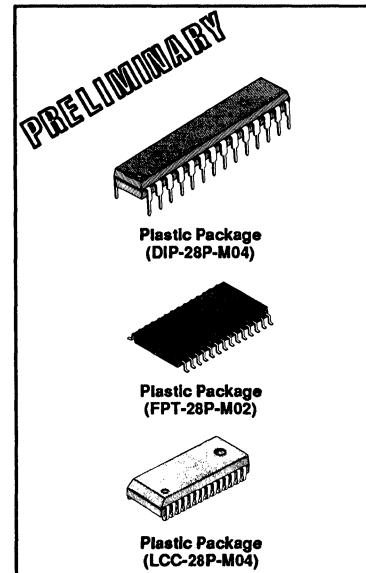
- Organization: 8,192 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time:
  - $t_{AA} = t_{ACSI} = 15$  ns max.,  $t_{ACS2} = t_{OE} = 8$  ns max (MB82B78-15)
  - $t_{AA} = t_{ACSI} = 20$  ns max.,  $t_{ACS2} = t_{OE} = 10$  ns max (MB82B78-20)
- Single 5 V power supply  $\pm 10\%$  tolerance with low current drain:
  - 120 mA max. (Operating)
  - 30 mA max. (TTL Standby)
  - 15 mA max. (CMOS Standby)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Three-state outputs
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:

Skinny DIP (300 mil)	MB82B78-xxPSK
SOP (450 mil)	MB82B78-xxPF
SOJ (300 mil)	MB82B78-xxPJ

### Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.5 to +7	V
Input Voltage on any pin with respect to GND	$V_{IN}$	-3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	$V_{IO}$	-0.5 to +7	V
Output Current	$I_{OUT}$	$\pm 20$	mA
Power Dissipation	$P_D$	1.0	W
Temperature Under Bias	$T_{BIAS}$	-10 to +85	$^{\circ}$ C
Storage Temperature Range	$T_{STG}$	-45 to +125	$^{\circ}$ C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

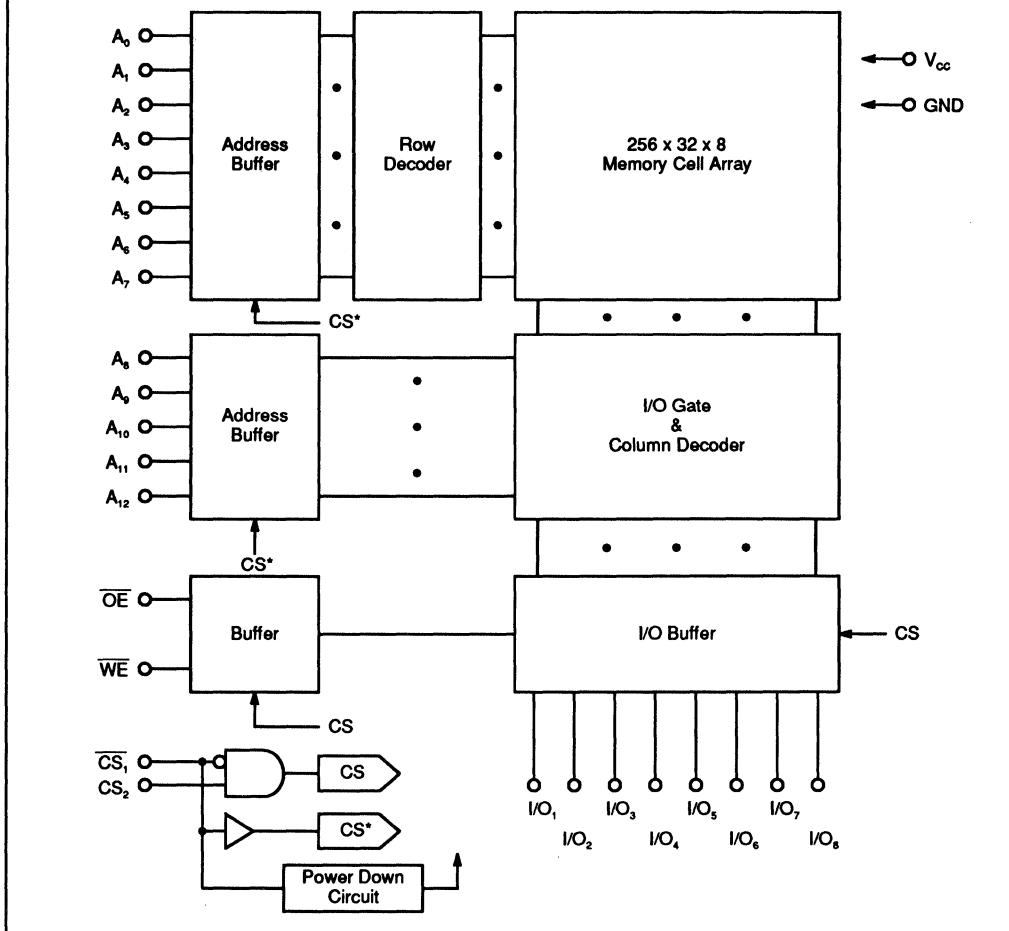


Pin Assignment  
(TOP VIEW)

NC	<input type="checkbox"/>	1	28	<input type="checkbox"/> $V_{CC}$
$A_4$	<input type="checkbox"/>	2	27	<input type="checkbox"/> $WE$
$A_5$	<input type="checkbox"/>	3	26	<input type="checkbox"/> $CS_2$
$A_6$	<input type="checkbox"/>	4	25	<input type="checkbox"/> $A_2$
$A_7$	<input type="checkbox"/>	5	24	<input type="checkbox"/> $A_1$
$A_8$	<input type="checkbox"/>	6	23	<input type="checkbox"/> $A_0$
$A_9$	<input type="checkbox"/>	7	22	<input type="checkbox"/> $OE$
$A_{10}$	<input type="checkbox"/>	8	21	<input type="checkbox"/> $A_3$
$A_{11}$	<input type="checkbox"/>	9	20	<input type="checkbox"/> $CS_1$
$A_{12}$	<input type="checkbox"/>	10	19	<input type="checkbox"/> $I/O_6$
$I/O_1$	<input type="checkbox"/>	11	18	<input type="checkbox"/> $I/O_7$
$I/O_2$	<input type="checkbox"/>	12	17	<input type="checkbox"/> $I/O_6$
$I/O_3$	<input type="checkbox"/>	13	16	<input type="checkbox"/> $I/O_5$
GND	<input type="checkbox"/>	14	15	<input type="checkbox"/> $I/O_4$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB82B78 BLOCK DIAGRAM



## CAPACITANCE ( $T_a = 25^\circ C$ , $f = 1MHz$ )

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ( $V_{IO}=0V$ )	$C_{IO}$			8	pF
Input Capacitance ( $V_{IN}=0V$ )	$C_{IN}$			7	pF

## PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A <sub>0</sub> to A <sub>12</sub>	Address input.	OE	Output Enable.
I/O <sub>1</sub> to I/O <sub>8</sub>	Data input/output.	WE	Write Enable.
CS <sub>1</sub>	Chip Select 1.	V <sub>cc</sub>	Power Supply (+5V ±10%)
CS <sub>2</sub>	Chip Select 2.	GND	Ground.

## TRUTH TABLE

CS <sub>1</sub>	CS <sub>2</sub>	WE	OE	Mode	I/O Pin	Power Supply Current
H	X	X	X	Standby	High-Z	Standby
L	L	X	X	Not selected	High-Z	Active
L	H	H	H	Dout disable	High-Z	Active
L	H	H	L	Read	Data out	Active
L	H	L	X	Write	Data in	Active

Legend: H=High level, L=Low level, X=Don't care

## RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	V
Ambient Temperature	T <sub>A</sub> *	0		70	°C

\* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

## DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	$V_{IN}$ =GND to $V_{CC}$ $V_{CC}$ =max.	$I_U$	-10	10	$\mu A$
Output Leakage Current	$V_{IO}$ =GND to $V_{CC}$ $CS_1=V_{IH}$ or $CS_2=V_{IL}$ or $WE=V_{IL}$ or $OE=V_{IH}$	$I_{IO}$	-10	10	$\mu A$
Operating Supply Current	$CS_1=V_{IL}$ , I/O=Open Cycle=min.	$I_{CC}$		120	mA
Standby Supply Current	$V_{CC}$ =min. to max. $CS_1=V_{CC}-0.2V$ , $V_{IN}\leq 0.2V$ or $V_{IH}\geq V_{CC}-0.2V$	$I_{SB1}$		15	mA
Standby Supply Current	$CS_1=V_{IH}$ $V_{IN}=V_{IH}$ or $V_{IL}$	$I_{SB2}$		30	mA
Input High Voltage		$V_{IH}$	2.2	6.0	V
Input Low Voltage		$V_{IL}$	-0.5 <sup>*1</sup>	0.8	V
Output High Voltage	$I_{OH}=4mA$	$V_{OH}$	2.4		V
Output Low Voltage	$I_{OL}=8mA$	$V_{OL}$		0.4	V
Peak Power-on Current *2	$V_{CC}$ =GND to 4.5V $CS_1$ =Lower of $V_{CC}$ or $V_{IH}$ min.	$I_{PO}$		50	mA

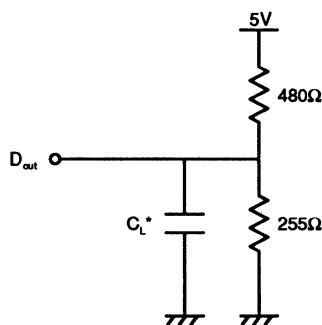
Note: \*1 -2.0V min. for pulse width less than 8ns.

\*2 The  $CS_1$  input should be connected to  $V_{CC}$  to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Output Load

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input:  $V_{IL}=0.8V$ ,  $V_{IH}=2.2V$   
Output:  $V_{OL}=0.8V$ ,  $V_{OH}=2.2V$



	$C_L$	Parameters Measured
Load I	30pF	except $t_{LZ}$ , $t_{HZ}$ , $t_{OW}$ , $t_{OLZ}$ and $t_{OHZ}$
Load II	5pF	$t_{LZ}$ , $t_{HZ}$ , $t_{OW}$ , $t_{OLZ}$ and $t_{OHZ}$

\*Including Scope and jig Capacitance.

## AC CHARACTERISTICS

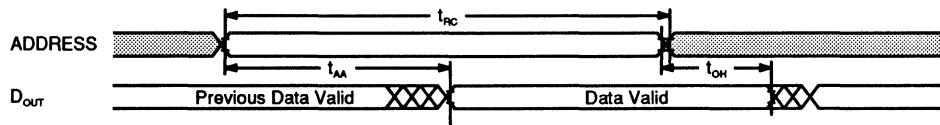
(Recommended operating conditions unless otherwise noted.)

### READ CYCLE \*1

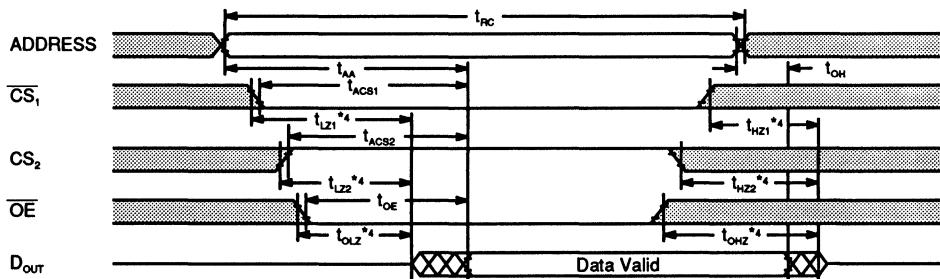
Parameter	Symbol	MB82B78-15		MB82B78-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	15		20		ns
Address Access Time *2	$t_{AA}$		15		20	ns
$\overline{CS}_1$ Access Time *3	$t_{ACS1}$		15		20	ns
$CS_2$ Access Time	$t_{ACS2}$		8		10	ns
$OE$ Access Time	$t_{OE}$		8		10	ns
Output Hold from Address Change	$t_{OH}$	3		3		ns
Output Low-Z from $\overline{CS}_1$ *4	$t_{LZ1}$	3		3		ns
Output Low-Z from $CS_2$ *4	$t_{LZ2}$	2		2		ns
Output Low-Z from $OE$ *4	$t_{OLZ}$	2		2		ns
Output High-Z from $CS_1$ *4	$t_{HZ1}$		8		10	ns
Output High-Z from $CS_2$ *4	$t_{HZ2}$		8		10	ns
Output High-Z from $OE$ *4	$t_{OHZ}$		8		10	ns

### READ CYCLE TIMING DIAGRAM \*1

#### READ CYCLE I: ADDRESS CONTROLLED \*2\*3



#### READ CYCLE II: $\overline{CS}_1$ , $CS_2$ CONTROLLED \*4



: Don't Care    : Undefined

Note: \*1  $WE$  is high for Read cycle.

\*2 Device is continuously selected,  $CS_1=OE=V_{IL}$ ,  $CS_2=V_{IH}$ .

\*3 Address valid prior to or coincident with  $\overline{CS}_1$  and  $CS_2$  transition low and high, respectively.

\*4 Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage with specified Load II in Fig. 2.

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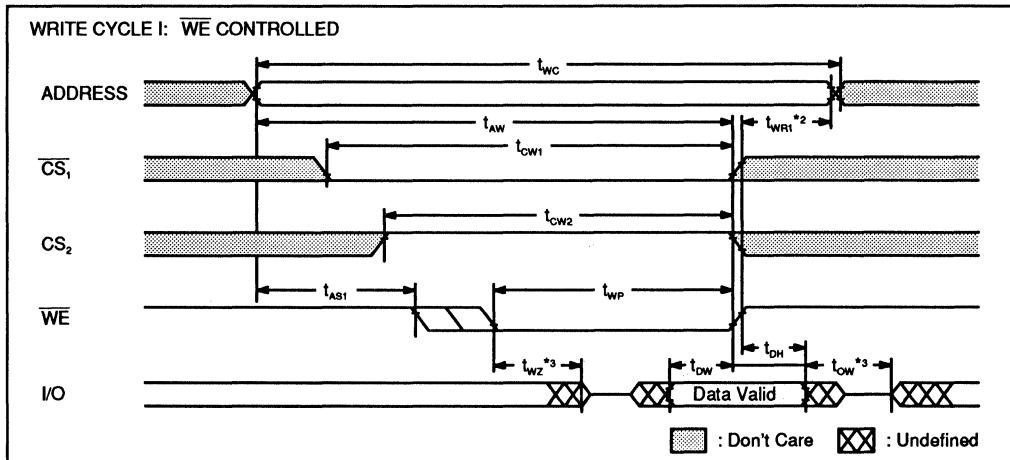
**MB82B78-20**

**2**

### WRITE CYCLE \*1

Parameter	Symbol	MB82B78-15		MB82B78-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	$t_{WC}$	15		20		ns
Address Valid to End of Write	$t_{AW}$	10		15		ns
$\overline{CS}_1$ to End of Write	$t_{CWI}$	10		15		ns
$\overline{CS}_2$ to End of Write	$t_{CW2}$	6		8		ns
Data Setup Time	$t_{DW}$	7		10		ns
Data Hold Time	$t_{DH}$	3		3		ns
Write Pulse Width	$t_{WP}$	8		10		ns
Write Recovery Time *2	$\overline{CS}_1, \overline{WE}$	$t_{WR1}$	3	3		ns
	$CS_2$	$t_{WR2}$	5	5		ns
Address Setup Time	$\overline{CS}_1, \overline{WE}$	$t_{AS1}$	0	0		ns
	$CS_2$	$t_{AS2}$	2	2		ns
Output Low-Z from $\overline{WE}$ *3	$t_{OW}$	0		0		ns
Output High-Z from $\overline{WE}$ *3	$t_{WZ}$			8	10	ns

### WRITE CYCLE TIMING DIAGRAM \*1

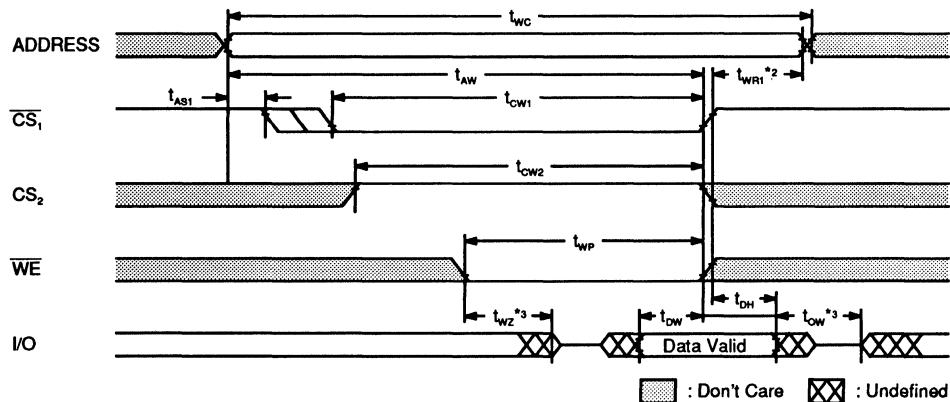


**Note:** \*1 If  $\overline{CS}_1$ ,  $\overline{OE}$  and  $CS_2$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

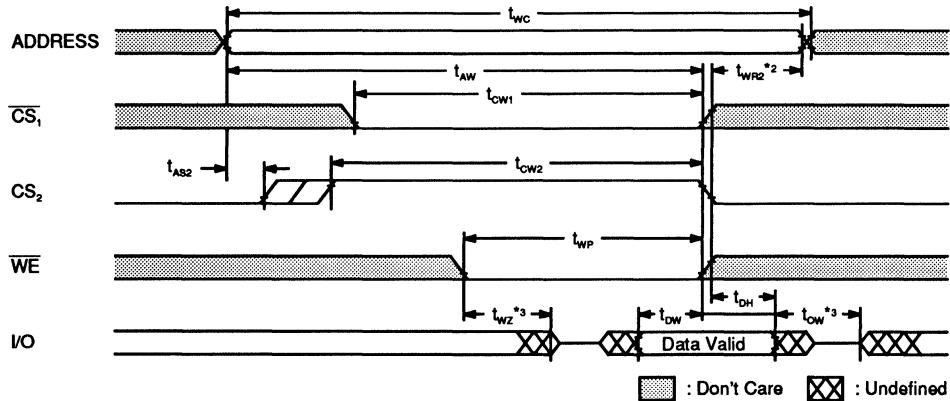
\*2  $t_{WR}$  is defined from the end point of WRITE Mode.

\*3 Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage with specified Load II in Fig. 2.

**WRITE CYCLE II:  $\overline{CS_1}$  CONTROLLED**



**WRITE CYCLE III:  $\overline{CS_2}$  CONTROLLED**



**Note:** \*1 If  $CS_1$ ,  $OE$  and  $CS_2$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

\*2  $t_{WR}$  is defined from the end point of WRITE Mode.

\*3 Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage with specified Load II in Fig. 2.

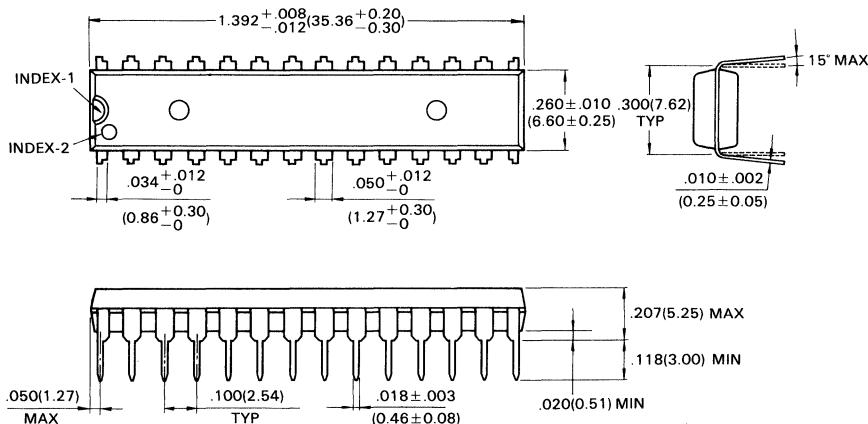
**MB82B78-15**

**MB82B78-20**

## **PACKAGE DIMENSIONS**

**PLASTIC DIP (Suffix: P-SK)**

### **28-LEAD PLASTIC DUAL-IN-LINE PACKAGE (CASE No.: DIP-28P-M04)**



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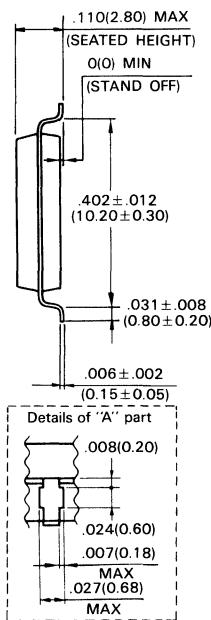
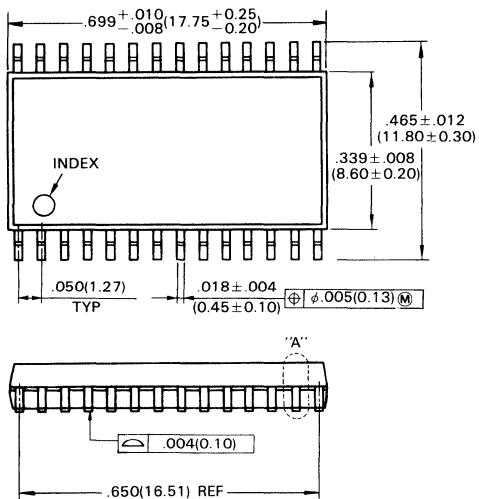
Dimensions in  
inches (millimeters)

**PACKAGE DIMENSIONS (Continued)**

Plastic FPT (Suffix: PF)

**2**

**28-LEAD PLASTIC FLAT PACKAGE  
(CASE NO.: FPT-28P-M02)**



Dimensions in  
inches (millimeters)

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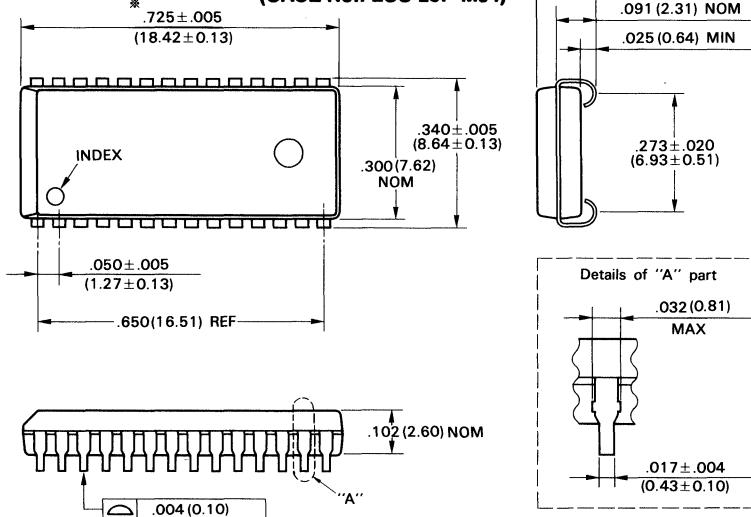
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## PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PJ)

2

### 28-LEAD PLASTIC LEADED CHIP CARRIER (CASE No.: LCC-28P-M04)



\* : This dimension includes resin protrusion. (Each side : .006 (0.15) MAX)

Dimensions in  
inches (millimeters)

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