July 1990
Edition 1.0

FUJITSU

DATA SHEET

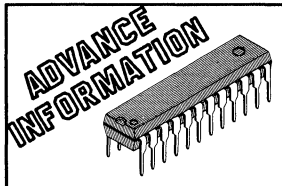
# MB82B84-15/-20
# CMOS 256K-BIT HIGH-SPEED BiCMOS SRAM

## 64K Words x 4 Bits BiCMOS High-Speed Static Random Access Memory with Automatic Power Down

The Fujitsu MB82B84 is a 65,536 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. For lower power dissipation and higher speed, peripheral circuits use BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors. The MB82B84 is housed in 300 mil plastic DIP and small outline J-lead (SOJ) packages. The memory uses asynchronous circuitry and requires a +5 V power supply. All pins are TTL compatible.

The MB82B84 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

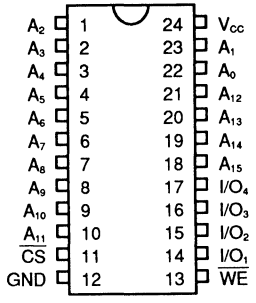
- Organization: 65,536 words x 4 bits
- Access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B84-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B84-20)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Static operation: no clock required
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. (Standby, CMOS level)
  25 mA max. (Standby, TTL level)
- Standard 24-pin Plastic Package:
  Skinny DIP (300 mil) MB82B84-xxPSK
  SOJ MB82B84-xxPJ
- Pin compatible with MB81C84A




PLASTIC PACKAGE
DIP-24P-M03

PLASTIC PACKAGE
LCC-24P-M02

**PIN ASSIGNMENT**
(TOP VIEW)




(DIP & SOJ Package)

## Absolute Maximum Ratings (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage on any pin with respect to GND | $V_{IN}$ | −3.5 to +7.0 | V |
| Output Voltage on any I/O pin with respect to GND | $V_{I/O}$ | −0.5 to +7.0 | V |
| Output Current | $I_{OUT}$ | ±20 | mA |
| Power Dissipation | $P_D$ | 1.0 | W |
| Temperature Under Bias | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature Range | $T_{STG}$ | −40 to +125 | °C |

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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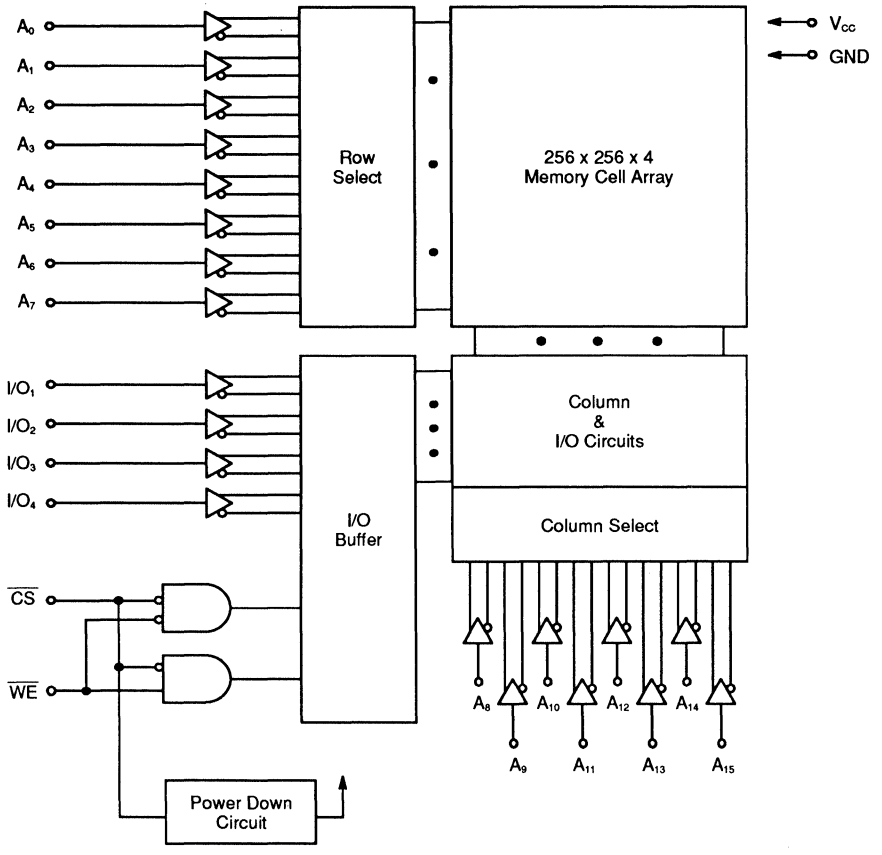
Fig. 1 – MB82B84 BLOCK DIAGRAM




## CAPACITANCE ($T_a$= 25° C, f = 1MHz)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| I/O Capacitance ($V_{I/O}$=0V) | $C_{I/O}$ | | | 8 | pF |
| Input Capacitance (V/CS=0V) | C/CS | | | 8 | pF |
| Input Capacitance ($V_{IN}$=0V) | $C_{IN}$ | | | 6 | pF |

# PIN DESCRIPTION

| Symbol | Pin name | Symbol | Pin name |
|---|---|---|---|
| $A_0$ to $A_{15}$ | Address input | $\overline{WE}$ | Write Enable |
| $I/O_1$ to $I/O_4$ | Data input/output | $V_{CC}$ | Power Supply (+5V ±10%) |
| $\overline{CS}$ | Chip Select 1 | GND | Ground |

# TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | Mode | I/O pin | Power Supply Current |
|---|---|---|---|---|
| H | X | Standby | High-Z | Standby |
| L | L | Write | $D_{IN}$ | Active |
| L | H | Read | $D_{OUT}$ | Active |

**Legend:** H=High level, L=Low level, X=Don't care

# RECOMMENDED OPERATING CONDITIONS

**(Referenced to GND)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ambient Temperature | $T_A$* | 0 | | 70 | °C |

* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

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# DC CHARACTERISTICS

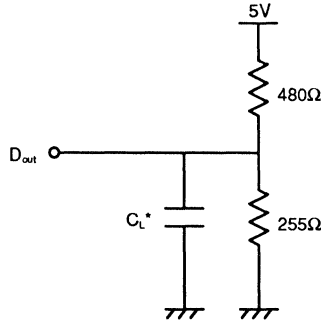
**(Recommended operating conditions otherwise noted.)**

| Parameter | Test Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current | $V_{IN}$=GND to $V_{CC}$<br>$V_{CC}$=max. | $I_{LI}$ | –10 | 10 | µA |
| Output Leakage Current | $V_{I/O}$=GND to $V_{CC}$<br>$\overline{CS}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$ | $I_{LI/O}$ | –10 | 10 | µA |
| Operating Supply Current | $\overline{CS}$=$V_{IL}$, I/O=Open<br>Cycle=min. | $I_{CC}$ | | 120 | mA |
| Standby Supply Current | $V_{CC}$=min. to max.<br>$\overline{CS}$=$V_{CC}$–0.2V, $V_{IN}$≤0.2V or<br>$V_{IN}$≥$V_{CC}$–0.2V | $I_{SB1}$ | | 15 | mA |
| Standby Supply Current | $\overline{CS}$=$V_{IH}$<br>$V_{CC}$=min. to max. | $I_{SB2}$ | | 25 | mA |
| Input High Voltage | | $V_{IH}$ | 2.2 | 6.0 | V |
| Input Low Voltage | | $V_{IL}$ | –0.5*1 | 0.8 | V |
| Output High Voltage | $I_{OH}$=–4mA | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage | $I_{OL}$=8mA | $V_{OL}$ | | 0.4 | V |
| Peak Power-on Current *2 | $V_{CC}$=GND to 4.5V<br>$\overline{CS}$=Lower of $V_{CC}$ or $V_{IH}$ min. | $I_{PO}$ | | 50 | mA |

**Note:** *1 –2.0V min. for pulse width less than 8ns.
*2 The $\overline{CS}$ input should be connected to $V_{CC}$ to keep the device deselected.

**Fig. 2 – AC TEST CONDITIONS**

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: $V_{IL}$=0.8V, $V_{IH}$=2.2V
  Output: $V_{OL}$=0.8V, $V_{OH}$=2.2V
- Output Load




*Including Scope and jig capacitance

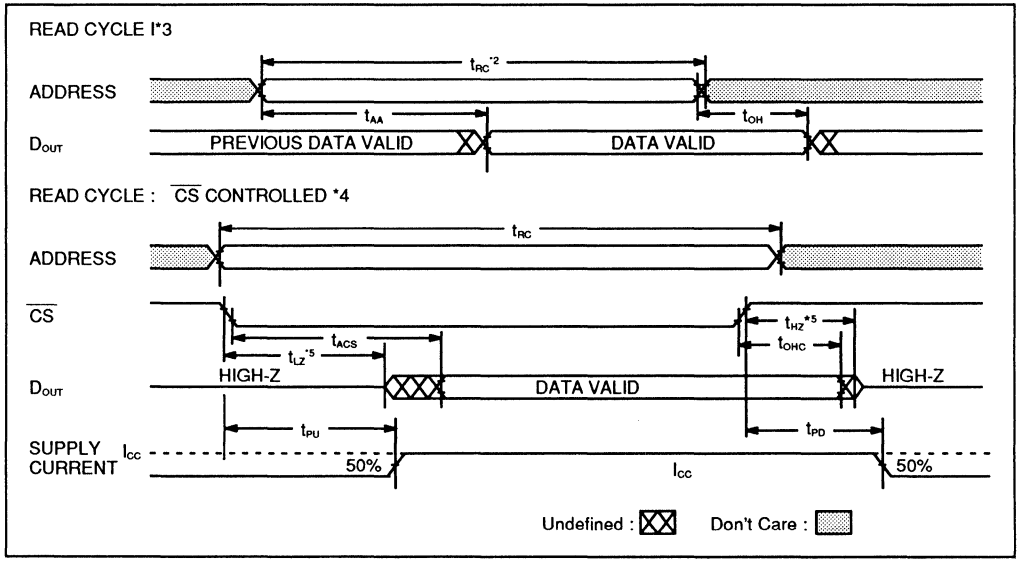
| | $C_L$ | Parameters measured |
|---|---|---|
| Load I | 30pF | except $t_{LZ}$, $t_{HZ}$, $t_{OW}$ and $t_{WZ}$ |
| Load II | 5pF | $t_{LZ}$, $t_{HZ}$, $t_{OW}$ and $t_{WZ}$ |

# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**
**READ CYCLE**

| Parameter | Symbol | MB82B84-15 | | MB82B84-20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 15 | | 20 | | ns |
| Address Access Time | $t_{AA}$ | | 15 | | 20 | ns |
| $\overline{CS}$ Access Time | $t_{ACS}$ | | 15 | | 20 | ns |
| Output Hold from Address Change | $t_{OH}$ | 0 | | 0 | | ns |
| Output Low-Z from $\overline{CS}$ | $t_{LZ}$ | 3 | | 3 | | ns |
| Output High-Z from $\overline{CS}$ | $t_{HZ}$ | | 8 | | 8 | ns |
| Power Up from $\overline{CS}$ | $t_{PU}$ | 0 | | 0 | | ns |
| Power Down from $\overline{CS}$ | $t_{PD}$ | | 15 | | 20 | ns |

**READ CYCLE TIMING DIAGRAM *1**




**Note:** *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS}$=$V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

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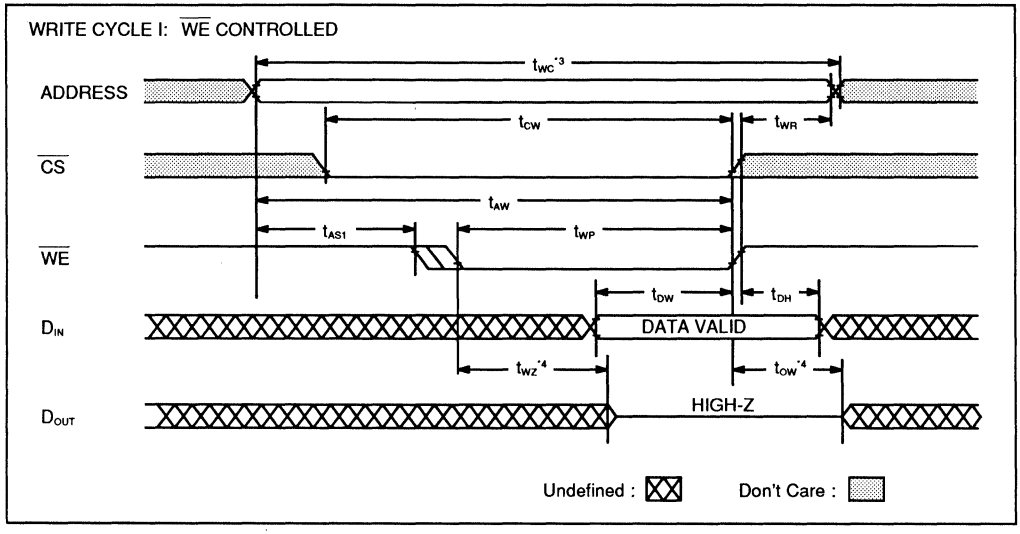
## WRITE CYCLE

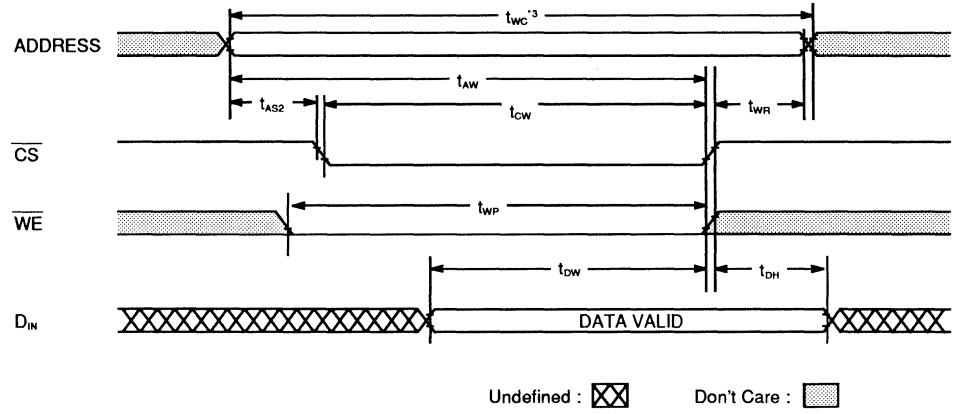
| Parameter | Symbol | MB82B84-15 | | MB82B84-20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 15 | | 20 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 11 | | 15 | | ns |
| $\overline{CS}$ to End of Write | $t_{CW}$ | 11 | | 15 | | ns |
| Data Setup Time | $t_{DW}$ | 4 | | 8 | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns |
| Write Pulse Width | $t_{WP}$ | 11 | | 15 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns |
| Output Low-Z from $\overline{WE}$ | $t_{OW}$ | 0 | | 0 | | ns |
| Output High-Z from $\overline{WE}$ | $t_{WZ}$ | | 6 | | 10 | ns |

## WRITE CYCLE TIMING DIAGRAM *1




**Note:** *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2




**Note:** *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

# PACKAGE DIMENSIONS

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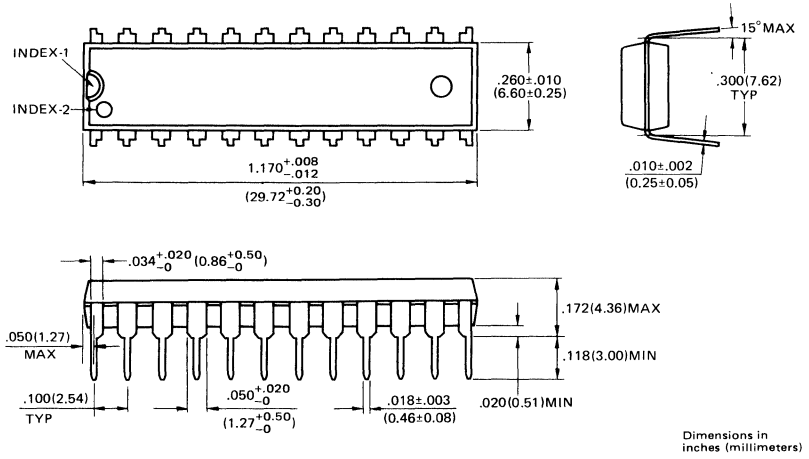
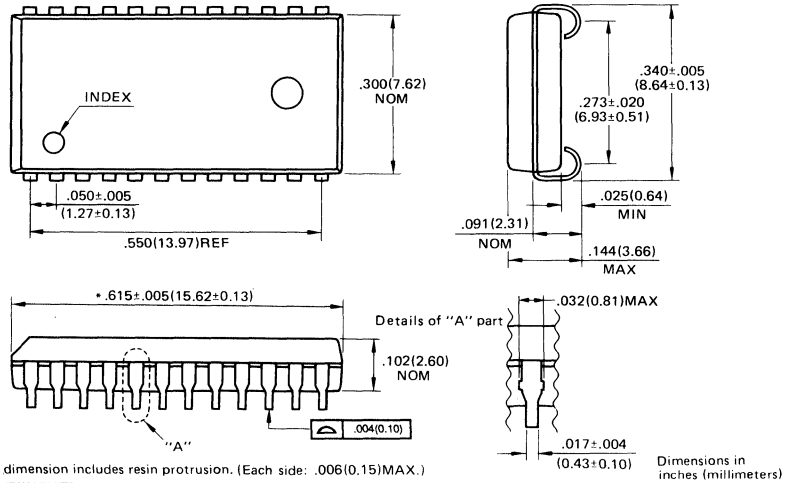
## 24-LEAD PLASTIC DUAL-IN LINE PACKAGE
## (CASE No.: DIP-24P-M03)




Dimensions in inches (millimeters)



## 24-LEAD PLASTIC LEADED CHIP CARRIER
## (CASE No.: LCC-24P-M02)




* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)