FUJITSU

==== DATA SHEET ====

MB82B85-15/-20
256K-BIT HIGH-SPEED BiCMOS SRAM

64K Words x 4 Bits BiCMOS High-Speed Static Random Access Memory With Automatic Power Down

The Fujitsu MB82B85 is a static random access memory organized as 65,536 words by 4 bits and fabricated with a CMOS silicon gate process. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B85 is housed in 300 mil plastic DIP and small outline J-lead (SOJ) packages. The memory uses asynchronous circuitry and requires +5 V power supply. All pins are TTL compatible

The MB82B85 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.
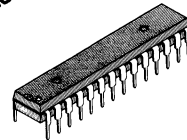
- Organization: 65,536 words x 4 bits
- Access time: $t_{AA} = t_{ACS}$ = 15 ns max. (MB82B85-15)
  $t_{AA} = t_{ACS}$ = 20 ns max. (MB82B85-20)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Static operation: no clock required
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max.   (Active operation)
  15 mA max.   CMOS Standby)
  25 mA max.   (TTL Standby)
- Standard 28-pin Plastic Packages:
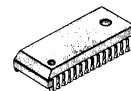 Skinny DIP   MB82B85-xxPSK
  SOJ   MB82B85-xxPJ

ADVANCE INFORMATION

Plastic Package (DIP-28P-M04)

Plastic Package (LCC-28P-M04)

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	$V_{I/O}$	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Assignment (TOP VIEW)

NC	1	28	V_{CC}
A_{15}	2	27	A_{14}
A_8	3	26	A_{13}
A_7	4	25	A_9
A_6	5	24	A_{10}
A_5	6	23	A_{11}
A_4	7	22	A_{12}
A_3	8	21	NC
A_2	9	20	NC
A_1	10	19	I/O_1
A_0	11	18	I/O_2
$\overline{CS}$	12	17	I/O_3
$\overline{OE}$	13	16	I/O_4
GND	14	15	$\overline{WE}$

(DIP & SOJ Package)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB82B85 BLOCK DIAGRAM
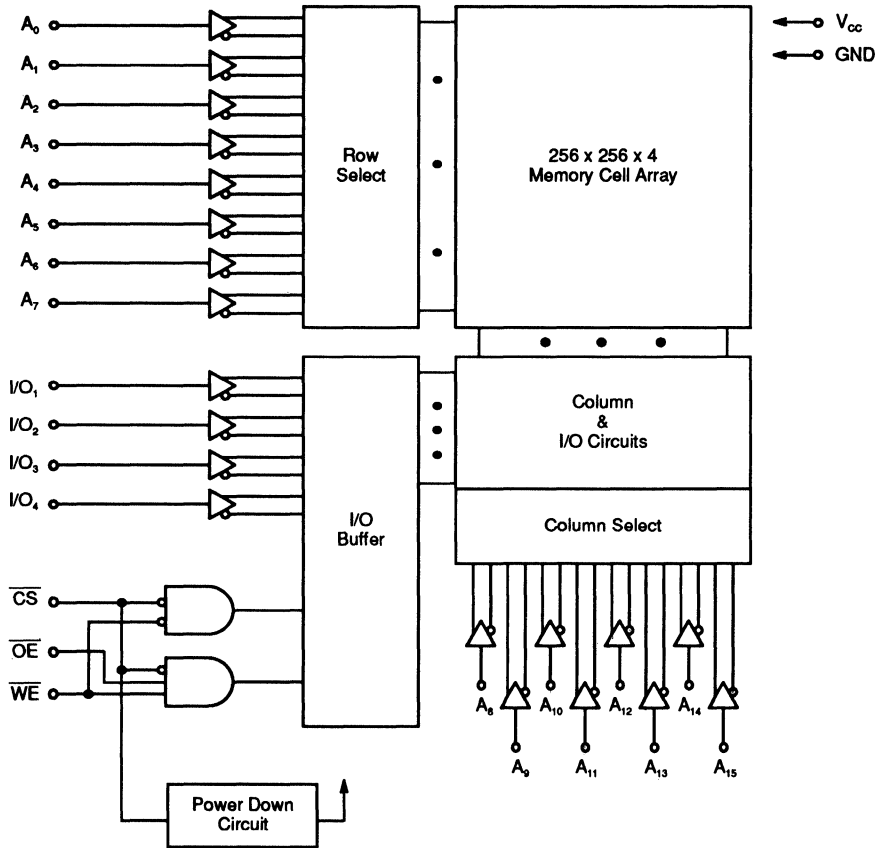
CAPACITANCE (T$_a$= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (V$_{I/O}$=0V)	C$_{I/O}$			8	pF
Input Capacitance (V$_{\overline{CS}}$=0V)	C$_{\overline{CS}}$			8	pF
Input Capacitance (V$_{IN}$=0V)	C$_{IN}$			6	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{15}	Address input	$\overline{WE}$	Write Enable
I/O_1 to I/O_4	Data input/output	V_{cc}	Power Supply (+5V ±10%)
$\overline{CS}$	Chip Select	GND	Ground
$\overline{OE}$	Output Enable		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	Power Supply Current
H	X	X	Standby	High–Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	H	Output Desable	High–Z	Active
L	H	L	Read	D_{OUT}	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Ambient Temperature	T_A*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.
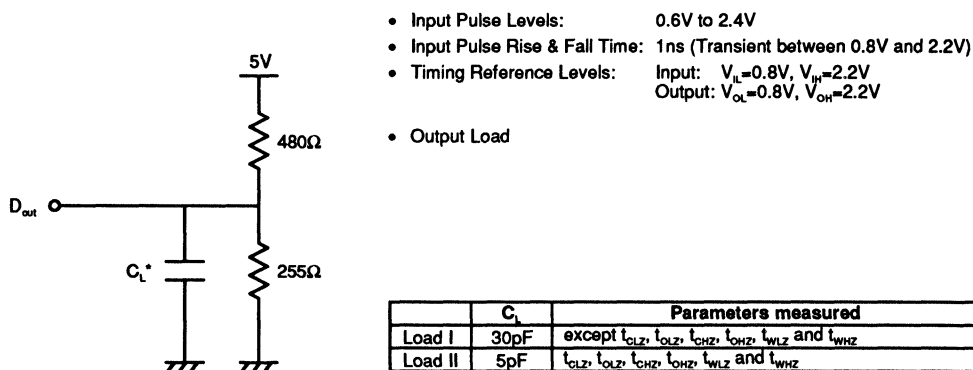
DC CHARACTERISTICS
(Recommended operating conditions otherwise noted.)

2

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=max.	I_{LI}	−10	10	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}	I_{LIO}	−10	10	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=min. to max. $\overline{CS}$=V_{CC}−0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}−0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS}$=V_{IH} V_{CC}=min. to max.	I_{SB2}		25	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	−0.5*1	0.8	V
Output High Voltage	I_{OH}=−4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS}$=Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 −2.0V min. for pulse width less than 8ns.

*2 The $\overline{CS}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
Output: V_{OL}=0.8V, V_{OH}=2.2V

- Output Load

5V

480Ω

D_{out}

C_L*

255Ω

|	C_L	Parameters measured
Load I	30pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

*Including Scope and jig capacitance

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B85-15		MB82B85-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time	t_{AA}		15		20	ns
$\overline{CS}$ Access Time	t_{ACS}		15		20	ns
$\overline{OE}$ Access Time	t_{OE}		8		10	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Low-Z from $\overline{CS}$	t_{CLZ}	3		3		ns
Output Low-Z from $\overline{OE}$	t_{OLZ}	3		3		ns
Output High-Z from $\overline{CS}$	t_{CHZ}		8		8	ns
Output High-Z from $\overline{OE}$	t_{OHZ}		8		8	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		15		20	ns

READ CYCLE TIMING DIAGRAM *1
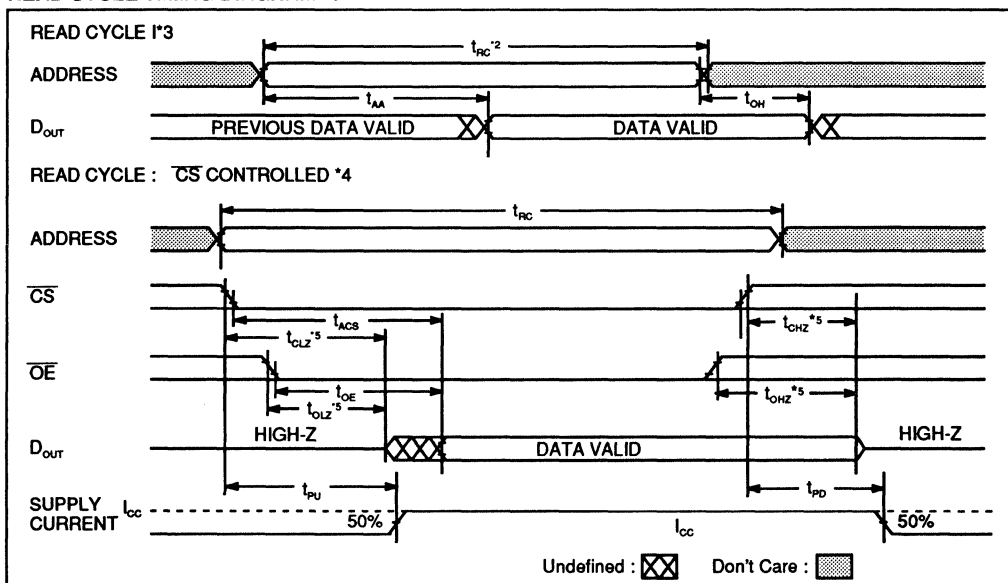
Note:
- *1 $\overline{WE}$ is high for Read cycle.
- *2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
- *3 Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
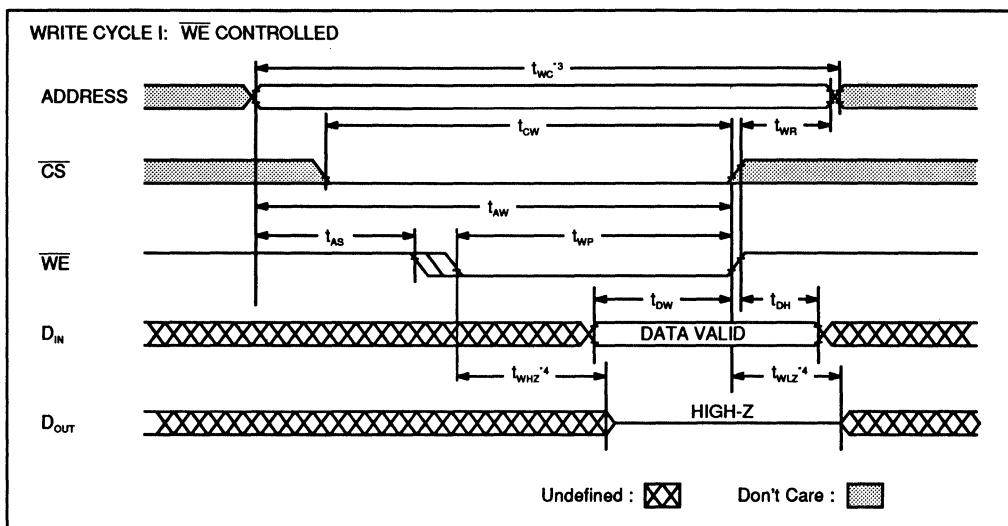- *4 Address valid prior to or coincident with $\overline{CS}$ transition low.
- *5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE

Parameter	Symbol	MB82B85-15		MB82B85-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		ns
Address Valid to End of Write	t_{AW}	11		15		ns
$\overline{CS}$ to End of Write	t_{CW}	11		15		ns
Data Setup Time	t_{DW}	4		8		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	11		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$	t_{WLZ}	0		0		ns
Output High-Z from $\overline{WE}$	t_{WHZ}		6		10	ns

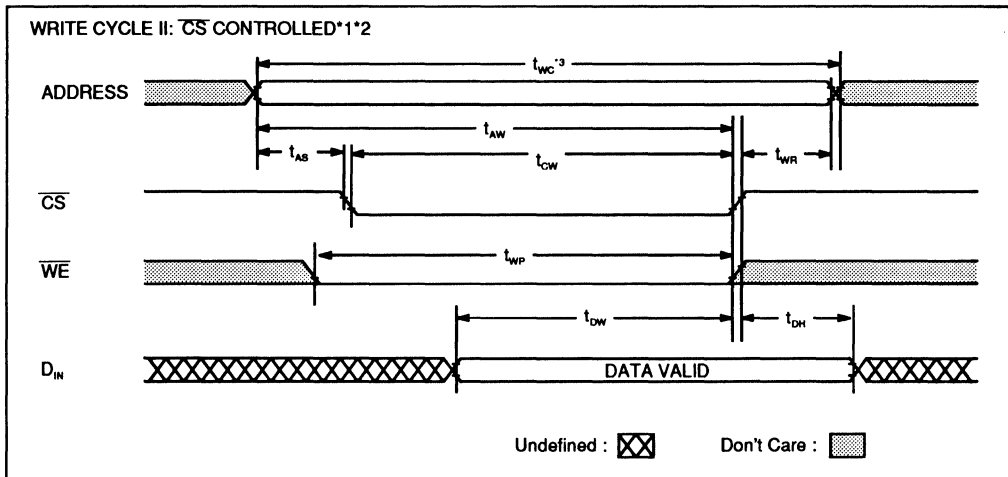### WRITE CYCLE TIMING DIAGRAM *1

Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load II in Fig. 2.
*5 If $\overline{CS}$, $\overline{OE}$ are in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2

Undefined : ▨▨   Don't Care : ▨

Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load II in Fig. 2.
*5 If $\overline{CS}$, $\overline{OE}$ are in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
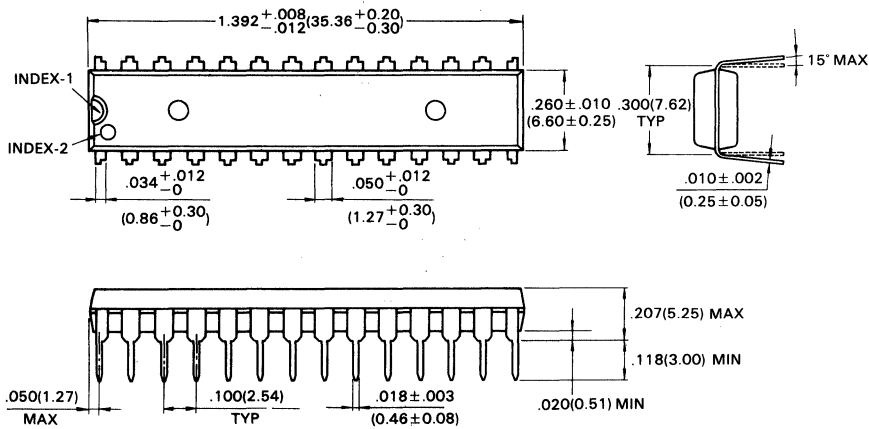
PACKAGE DIMENSIONS

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

INDEX-1

INDEX-2

$1.392^{+.008}_{-.012}(35.36^{+0.20}_{-0.30})$

$.260\pm.010$ $.300(7.62)$
(6.60 ± 0.25) TYP

$15°$ MAX

$.034^{+.012}_{-0}$
$(0.86^{+0.30}_{-0})$

$.050^{+.012}_{-0}$
$(1.27^{+0.30}_{-0})$

$.010\pm.002$
(0.25 ± 0.05)

$.207(5.25)$ MAX

$.118(3.00)$ MIN

$.050(1.27)$
MAX

$.100(2.54)$
TYP

$.018\pm.003$
(0.46 ± 0.08)

$.020(0.51)$ MIN

© 1988 FUJITSU LIMITED D28018S–2C

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-28P-M04)

※
.725±.005
(18.42±0.13)

INDEX

.340±.005
(8.64±0.13)

.300(7.62)
NOM

.050±.005
(1.27±0.13)

.650(16.51) REF

.004(0.10)

"A"

.102(2.60) NOM

.144(3.66) MAX

.091(2.31) NOM

.025(0.64) MIN

.273±.020
(6.93±0.51)

Details of "A" part

.032(0.81)
MAX

.017±.004
(0.43±0.10)

※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

© 1989 FUJITSU LIMITED C28054S-1C